SINK/SOURCE DDR TERMINATION REGULATOR

Check for Samples: TPS51200-Q1

FEATURES

- **Qualified for Automotive Applications**
- **Input Voltage: Supports 2.5-V Rail and 3.3-V Rail**
- **VLDOIN Voltage Range: 1.1 V to 3.5 V**
- **Sink/Source Termination Regulator Includes Droop Compensation**
- **Requires Minimum Output Capacitance of 20-µF (typically 3 × 10-µF MLCCs) for Memory Termination Applications (DDR)**
- **PGOOD to Monitor Output Regulation**
- **EN Input**
- **REFIN Input Allows for Flexible Input Tracking Either Directly or Through Resistor Divider**
- **Remote Sensing (VOSNS)**
- **±10-mA Buffered Reference (REFOUT)**
- **Built-in Soft Start, UVLO and OCL**
- **Thermal Shutdown**
- **Meets DDR, DDR2 JEDEC Specifications; Supports DDR3 and Low-Power DDR3/DDR4 VTT Applications**
- **SON-10 PowerPAD™ Package**

APPLICATIONS

- **Memory Termination Regulator for DDR, DDR2, DDR3, and Low Power DDR3/DDR4**
- **Notebook/Desktop/Server**
- **Telecom/Datacom, GSM Base Station, LCD-TV/PDP-TV, Copier/Printer, Set-Top Box**

DESCRIPTION

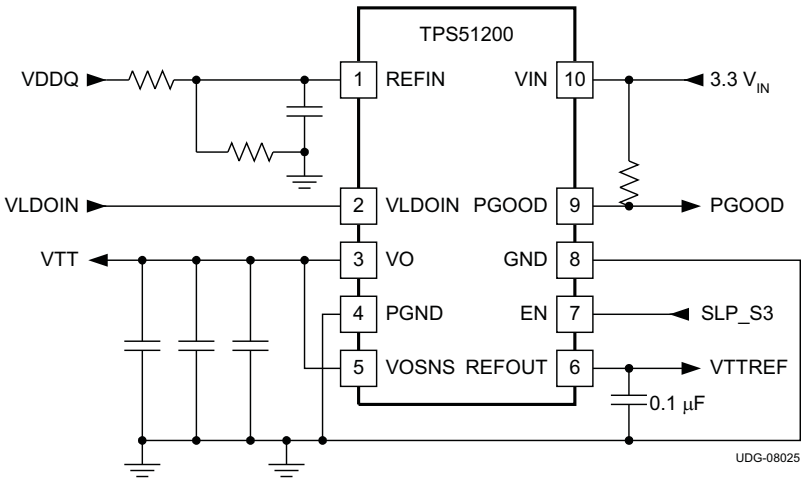
The TPS51200 is a sink/source Double Data Rate (DDR) termination regulator specifically designed for low input voltage, low-cost, low-noise systems where space is a key consideration.

The TPS51200 maintains a fast transient response and only requires a minimum output capacitance of 20 µF. The TPS51200 supports a remote sensing function and all power requirements for DDR, DDR2, DDR3, and Low Power DDR3/DDR4 VTT bus termination.

In addition, the TPS51200 provides an open-drain PGOOD signal to monitor the output regulation and an EN signal that can be used to discharge VTT during S3 (suspend to RAM) for DDR applications.

The TPS51200 is available in the thermally-efficient SON-10 PowerPAD package, and is rated both Green and Pb-free. It is specified from -40°C to 125°C.

STANDARD DDR APPLICATION



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)(2)

T_A	PACKAGE		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	SON – DRC	Reel of 3000	TPS51200QDRCRQ1	PSNQ

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

		VALUE	UNIT
Input voltage range(2)	VIN, VLDOIN, VOSNS, REFIN	–0.3 to 3.6	V
	EN	–0.3 to 6.5	
	PGND to GND	–0.3 to 0.3	
Output voltage range(2)	VO, REFOUT	–0.3 to 3.6	V
	PGOOD	–0.3 to 6.5	
T_J	Operating junction temperature	150	°C
T_{stg}	Storage temperature	–55 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal unless otherwise noted.

DISSIPATION RATINGS TABLE(1)

PACKAGE	T_A = 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 85°C POWER RATING
10-Pin SON (DRC)	1.92 W	19 mW/°C	0.79 W

(1) PowerPAD size: 3.0 × 1.9 mm, 4 standard thermal vias. Based on the above environment, junction to thermal pad resistance θ_{JP} is 10.24°C/W. Junction to ambient thermal resistance θ_{JA} is 52.06°C/W.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS51200-Q1 DRC (10 PINS)	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	51.6	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	60.8	
θ_{JB}	Junction-to-board thermal resistance	27.0	
ψ_{JT}	Junction-to-top characterization parameter	2.6	
ψ_{JB}	Junction-to-board characterization parameter	27.2	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	11.1	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		MIN	MAX	UNIT
Supply voltage	VIN	2.375	3.500	V
Voltage range	EN, VLDOIN, VOSNS	–0.1	3.5	
	REFIN	0.5	1.8	
	VO, PGOOD	–0.1	3.5	
	REFOUT	–0.1	1.8	
	PGND	–0.1	0.1	
Operating free-air temperature, T_A		–40	125	°C

ELECTRICAL CHARACTERISTICS

Over recommended free-air temperature range, V_{VIN} = 3.3 V,V_{VLDOIN} = 1.8 V, V_{REFIN} = 0.9 V, V_{VOSNS} = 0.9 V, V_{EN} = V_{VIN}, C_{OUT} = 3 × 10 µF and circuit shown in STANDARD DDR APPLICATION (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{IN}	Supply current	T_A = 25 °C, V_{EN} = 3.3 V, No Load		0.7	1	mA
$I_{IN(SDN)}$	Shutdown current	T_A = 25 °C, V_{EN} = 0 V, V_{REFIN} = 0, No Load		65	80	µA
		T_A = 25 °C, V_{EN} = 0 V, V_{REFIN} > 0.4 V, No Load		200	400	
I_{LDOIN}	Supply current ofVLDOIN	T_A = 25 °C, V_{EN} = 3.3 V, No Load		1	50	µA
$I_{LDOIN(SDN)}$	Shutdown current of VLDOIN	T_A = 25 °C, V_{EN} = 0 V, No Load		0.1	50	µA
INPUT CURRENT						
I_{REFIN}	Input current, REFIN	V_{EN} = 3.3 V			1	µA
VO OUTPUT						
V_{VOSNS}	Output DC voltage, VO	V_{REFOUT} = 1.25 V (DDR1), I_O = 0 A		1.25		V
			–15		15	mV
		V_{REFOUT} = 0.9 V (DDR2), I_O = 0 A		0.9		V
			–15		15	mV
		V_{LDOIN} = 1.5 V, V_{REFOUT} = 0.75 V (DDR3), I_O = 0 A		0.75		V
			–15		15	mV
V_{VOTOL}	Output voltage tolerance to REFOUT	–2A < I_{VO} < 2A	–25		25	mV
I_{VOSRCL}	VO source vurrent Limit	With reference to REFOUT, V_{OSNS} = 90% × V_{REFOUT}	3		4.5	A
I_{VOSNCL}	VO sink current Limit	With reference to REFOUT, V_{OSNS} = 110% × V_{REFOUT}	3.5		5.5	A
I_{DSCHRG}	Discharge current, VO	V_{REFIN} = 0 V, V_{VO} = 0.3 V, V_{EN} = 0 V, T_A = 25°C		18	25	Ω
POWERGOOD COMPARATOR						
$V_{TH(PG)}$	VO PGOOD threshold	PGOOD window lower threshold with respect to REFOUT	–23.5%	–20%	–17.5%	
		PGOOD window upper threshold with respect to REFOUT	17.5%	20%	23.5%	
		PGOOD hysteresis		5%		
$T_{PGSTUPDLY}$	PGOOD startup delay	Startup rising edge, VOSNS within 15% of REFOUT		2		ms
$V_{PGOODLOW}$	Output low voltage	I_{SINK} = 4 mA			0.4	V
$T_{PBADDLY}$	PGOOD bad delay	VOSNS is outside of the ±20% PGOOD window		10		µs
$I_{PGOODLK}$	Leakage current(1)	V_{OSNS} = V_{REFIN} (PGOOD high impedance), PGOOD = V_{IN} + 0.2 V			1	µA
REFIN AND REFOUT						
V_{REFIN}	REFIN voltage range		0.5		1.8	V
$V_{REFINUVLO}$	REFIN undervoltage lockout	REFIN rising	360	390	420	mV
$V_{REFINUVHYS}$	REFIN undervoltage lockout hysteresis			20		mV
V_{REFOUT}	REFOUT voltage			REFIN		V
$V_{REFOUTTOL}$	REFOUT voltage tolerance to V_{REFIN}	–10 mA < I_{REFOUT} < 10 mA, V_{REFIN} = 1.25 V	–15		15	mV
		–10 mA < I_{REFOUT} < 10 mA, V_{VREFIN} = 0.9 V	–15		15	
		–10 mA < I_{REFOUT} < 10 mA, V_{REFIN} = 0.75V	–15		15	
		–10 mA < I_{REFOUT} < 10 mA, V_{REFIN} = 0.6 V	–15		15	
$I_{REFOUTSRCL}$	REFOUT source current limit	V_{REFOUT} = 0 V	10	40		mA
$I_{REFOUTSNCL}$	REFOUT sink current limit	V_{REFOUT} = 0 V	10	40		mA

(1) Ensured by design. Not production tested.

ELECTRICAL CHARACTERISTICS (continued)

Over recommended free-air temperature range, V_{VIN} = 3.3 V,V_{VLDOIN} = 1.8 V, V_{REFIN} = 0.9 V, V_{VOSNS} = 0.9 V, V_{EN} = V_{VIN}, C_{OUT} = 3 × 10 µF and circuit shown in STANDARD DDR APPLICATION (unless otherwise noted)

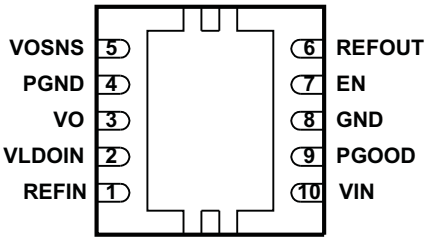
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
UVLO / EN LOGIC THRESHOLD						
$V_{VINUVVIN}$	UVLO threshold	Wake up, T_A = 25°C	2.2	2.3	2.375	V
		Hysteresis		50		mV
V_{ENIH}	High-level input voltage	Enable	1.7			V
V_{ENIL}	Low-level input voltage	Enable			0.3	
V_{ENYST}	Hysteresis voltage	Enable		0.5		
I_{ENLEAK}	Logic input leakage current	EN, T_A = 25°C	–1		1	µA
THERMAL SHUTDOWN						
T_{SON}	Thermal shutdown threshold(2)	Shutdown temperature		150		°C
		Hysteresis		25		

(2) Ensured by design. Not production tested.

DEVICE INFORMATION

DRC PACKAGE
(BOTTOM VIEW)

TPS51200
(Bottom View)

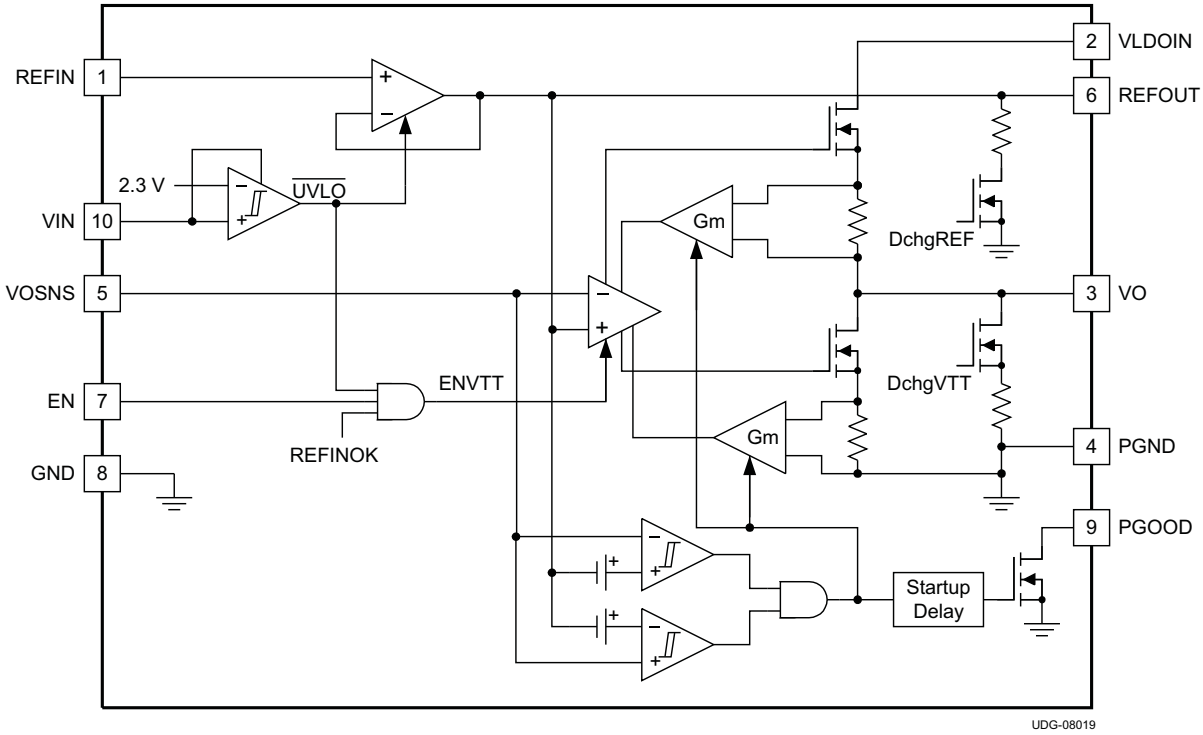


TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
EN	7	I	For DDR VTT application, connect EN to SLP_S3. For any other application(s), use EN as the ON/OFF function.
GND	8	–	Ground.Signal ground. Connect to negative terminal of the output capacitor.
PGND (1)	4	–	Power ground output for the LDO
PGOOD	9	O	PGOOD output. Indicates regulation.
REFIN	1	I	Reference input
REFOUT	6	O	Reference output. Connect to GND through 0.1-µF ceramic capacitor.
VIN	10	I	2.5-V or 3.3-V power supply A ceramic decoupling capacitor with a value between 1-µF and 4.7-µF is required.
VLDOIN	2	I	Supply voltage for the LDO
VO	3	O	Power output for the LDO
VOSNS	5	I	Voltage sense output for the LDO. Connect to positive terminal of the output capacitor or the load.

(1) PowerPAD™ connection. See Figure 9 in the THERMAL DESIGN section for additional information.

FUNCTIONAL BLOCK DIAGRAM



DETAILED DESCRIPTION

VO SINK/SOURCE REGULATOR

The TPS51200 is a sink/source tracking termination regulator specifically designed for low input voltage, low-cost, and low external component count systems where space is a key application parameter. The TPS51200 integrates a high-performance, low-dropout (LDO) linear regulator that is capable of both sourcing and sinking current. The LDO regulator employs a fast feedback loop so that small ceramic capacitors can be used to support the fast load transient response. To achieve tight regulation with minimum effect of trace resistance, a remote sensing terminal, VOSNS, should be connected to the positive terminal of the output capacitor(s) as a separate trace from the high current path from VO.

REFERENCE INPUT (REFIN)

The output voltage, VO, is regulated to REFOUT. When REFIN is configured for standard DDR termination applications, REFIN can be set by an external equivalent ratio voltage divider connected to the memory supply bus (VDDQ). The TPS51200 supports REFIN voltage from 0.5 V to 1.8 V, making it versatile and ideal for many types of low-power LDO applications.

REFERENCE OUTPUT (REFOUT)

When it is configured for DDR termination applications, REFOUT generates the DDR VTT reference voltage for the memory application. It is capable of supporting both a sourcing and sinking load of 10 mA. REFOUT becomes active when REFIN voltage rises to 0.390 V and VIN is above the UVLO threshold. When REFOUT is less than 0.375 V, it is disabled and subsequently discharges to GND through an internal 10-kΩ MOSFET. REFOUT is independent of the EN pin state.

SOFT-START

The soft-start function of the VO pin is achieved via a current clamp. The current clamp allows the output capacitors to be charged with low and constant current, providing a linear ramp-up of the output voltage. When VO is outside of the powergood window, the current clamp level is one-half of the full overcurrent limit (OCL) level. When VO rises or falls within the PGOOD window, the current clamp level switches to the full OCL level. The soft-start function is completely symmetrical; it works not only from GND to the REFOUT voltage, but also from VLDOIN to the REFOUT voltage.

EN CONTROL (EN)

When EN is driven high, the TPS51200 VO regulator begins normal operation. When EN is driven low, VO is discharges to GND through an internal 18-Ω MOSFET. REFOUT remains on when EN is driven low.

POWERGOOD FUNCTION (PGOOD)

The TPS51200 provides an open-drain PGOOD output that goes high when the VO output is within ±20% of REFOUT. PGOOD de-asserts within 10 µs after the output exceeds the size of the powergood window. During initial VO startup, PGOOD asserts high 2 ms (typ) after the VO enters power good window. Because PGOOD is an open-drain output, a 100-kΩ, pull-up resistor between PGOOD and a stable active supply voltage rail is required.

VO CURRENT PROTECTION

The LDO has a constant overcurrent limit (OCL). Note that the OCL level reduces by one-half when the output voltage is not within the powergood window. This reduction is a non-latch protection.

VIN UVLO PROTECTION

For VIN undervoltage lockout (UVLO) protection, the TPS51200 monitors VIN voltage. When the VIN voltage is lower than the UVLO threshold voltage, both the VO and REFOUT regulators are powered off. This shutdown is a non-latch protection.

THERMAL SHUTDOWN

The TPS51200 monitors the its junction temperature. If the device junction temperature exceeds its threshold value, (typically 150°C), the VO and REFOUT regulators are both shut off, discharged by the internal discharge MOSFETs. This shutdown is a non-latch protection.

APPLICATION INFORMATION

VIN CAPACITOR

Add a ceramic capacitor, with a value between 1.0-µF and 4.7-µF, placed close to the VIN pin, to stabilize the bias supply (2.5- V rail or 3.3- V rail) from any parasitic impedance from the supply.

VLDO INPUT CAPACITOR

Depending on the trace impedance between the VLDOIN bulk power supply to the device, a transient increase of source current is supplied mostly by the charge from the VLDOIN input capacitor. Use a 10-µF (or greater) ceramic capacitor to supply this transient charge. Provide more input capacitance as more output capacitance is used at VO. In general, use one-half of the C_{OUT} value for input.

OUTPUT CAPACITOR

For stable operation, the total capacitance of the VO output terminal must be greater than 20 µF. Attach three, 10-µF ceramic capacitors in parallel to minimize the effect of equivalent series resistance (ESR) and equivalent series inductance (ESL). If the ESR is greater than 2 mΩ, insert an R-C filter between the output and the VOSNS input to achieve loop stability. The R-C filter time constant should be almost the same as or slightly lower than the time constant of the output capacitor and its ESR.

Low VIN Applications

TPS51200 can be used in an application system where either a 2.5-V rail or a 3.3-V rail is available. If only a 5-V rail is available, TPS51100 can be used instead. The TPS51200 minimum input voltage requirement is 2.375 V. If a 2.5-V rail is used, ensure that the absolute minimum voltage (both DC and transient) at the device pin is be 2.375 V or greater. The voltage tolerance for a 2.5-V rail input is between –5% and 5% accuracy, or better.

S3 and Pseudo-S5 Support

The TPS51200 provides S3 support by an EN function. The EN pin could be connected to an SLP_S3 signal in the end application. Both REFOUT and VO are on when EN = high (S0 state). REFOUT is maintained while VO is turned off and discharged via an internal discharge MOSFET when EN = low (S3 state). When EN = low and the REFIN voltage is less than 0.390 V, TPS51200 enters pseudo-S5 state. Both VO and REFOUT outputs are turned off and discharged to GND through internal MOSFETs when pseudo-S5 support is engaged (S4/S5 state). Figure 1 shows a typical startup and shutdown timing diagram for an application that uses S3 and pseudo-S5 support.

Tracking Startup and Shutdown

The TPS51200 also supports tracking startup and shutdown when EN is tied directly to the system bus and not used to turn on or turn off the device. During tracking startup, VO follows REFOUT once REFIN voltage is greater than 0.39 V. REFIN follows the rise of VDDQ rail via a voltage divider. The typical soft-start time for the VDDQ rail is approximately 3 ms, however it may vary depending on the system configuration. The SS time of the VO output no longer depends on the OCL setting, but it is a function of the SS time of the VDDQ rail. PGOOD is asserted 2 ms after VO is within ±20% of REFOUT. During tracking shutdown, VO falls following REFOUT until REFOUT reaches 0.37 V. Once REFOUT falls below 0.37 V, the internal discharge MOSFETs are turned on and quickly discharge both REFOUT and VO to GND. PGOOD is deasserted once VO is beyond the ±20% range of REFOUT. Figure 2 shows the typical timing diagram for an application that uses tracking startup and shutdown.

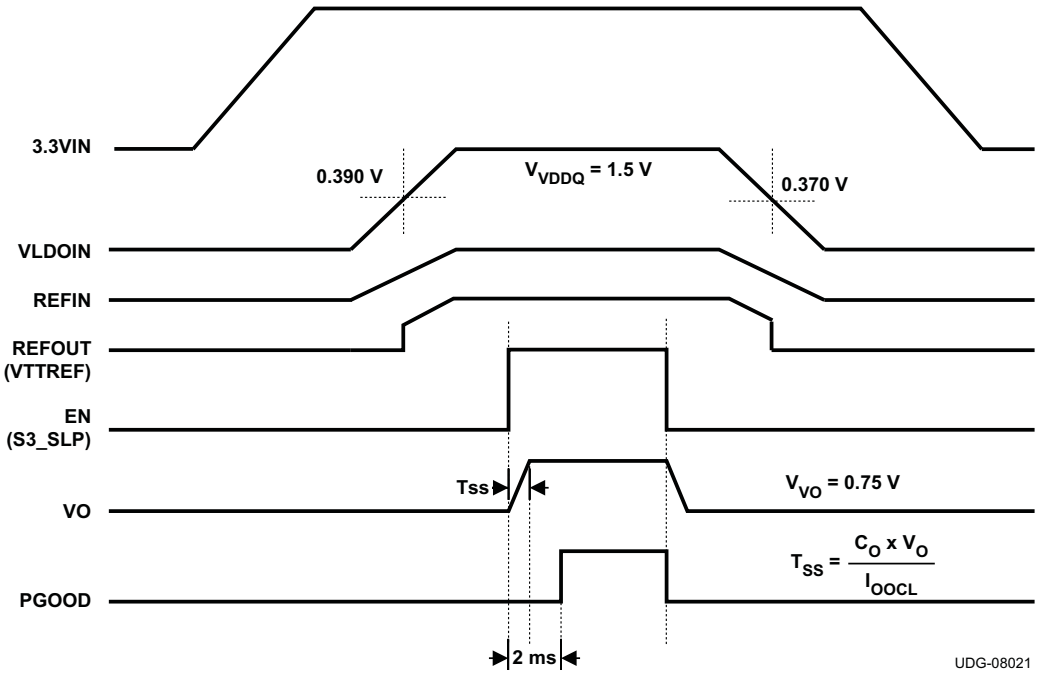


Figure 1. Typical Timing Diagram for S3 and pseudo-S5 Support

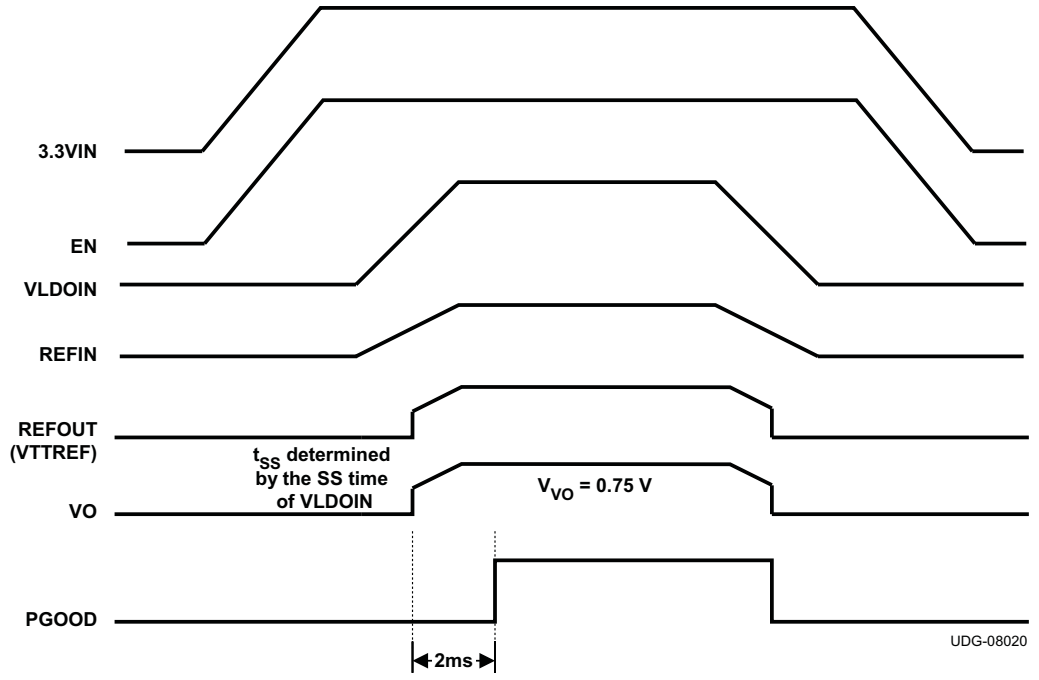


Figure 2. Typical Timing Diagram of Tracking Startup and Shutdown

Output Tolerance Consideration for VTT DIMM Applications

The TPS51200 is specifically designed to power up the memory termination rail (as shown in Figure 3). The DDR memory termination structure determines the main characteristics of the VTT rail, which is to be able to sink and source current while maintaining acceptable VTT tolerance. See Figure 4 for typical characteristics for a single memory cell.

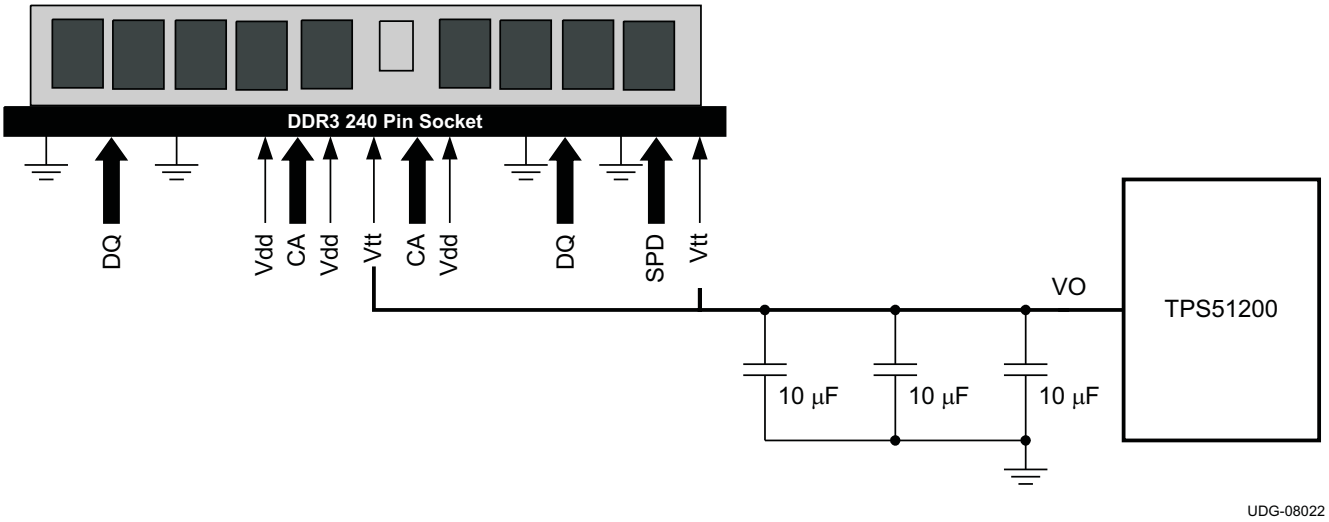


Figure 3. Typical Application Diagram for DDR3 VTT DIMM using TPS51200

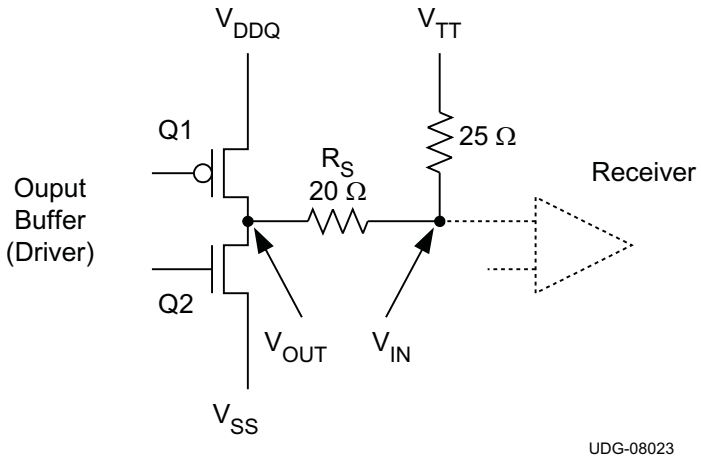


Figure 4. DDR Physical Signal System Bi-Directional SSTL Signaling

In Figure 4, when Q1 is on and Q2 is off:

- Current flows from VDDQ via the termination resistor to VTT
- VTT sinks current

In Figure 4, when Q2 is on and Q1 is off:

- Current flows from VTT via the termination resistor to GND
- VTT sources current

Because VTT accuracy has a direct impact on the memory signal integrity, it is imperative to understand the tolerance requirement on VTT. Based on JEDEC VTT specifications for DDR and DDR2 (JEDEC standard: DDR JESD8-9B May 2002; DDR2 JESD8-15A Sept 2003).

VTTREF – 40 mV < VTT < VTTREF + 40 mV, for both dc and ac conditions

The specification itself indicates that VTT must keep track of VTTREF for proper signal conditioning.

The TPS51200 ensures the regulator output voltage to be:

VTTREF –25 mV < VTT < VTTREF + 25mV, for both DC and AC conditions and –2 A < I_{VTT} < 2 A

The regulator output voltage is measured at the regulator side, not the load side. The tolerance is applicable to DDR, DDR2, DDR3 and Low Power DDR3/DDR4 applications (see Table 1 for detailed information). To meet the stability requirement, a minimum output capacitance of 20 µF is needed. Considering the actual tolerance on the MLCC capacitors, three 10-µF ceramic capacitors are sufficient to meet the above requirement.

Table 1. DDR, DDR2, DDR3 and LP DDR3 Termination Technology and Their Differences

	DDR	DDR2	DR3	Low Power DDR3
FSB Data Rates	200, 266, 333 and 400 MHz	400, 533, 677 and 800 MHz	800, 1066, 1330 and 1600 MHz	Same as DDR3
Termination	Motherboard termination to VTT for all signals	On-die termination for data group. VTT termination for address, command and control signals	On-die termination for data group. VTT termination for address, command and control signals	Same as DDR3
Termination Current Demand	Max source/sink transient currents of up to 2.6A to 2.9A	Not as demanding • Only 34 signals (address, command, control) tied to VTT • ODT handles data signals Less than 1A of burst current	Not as demanding • Only 34 signals (address, command, control) tied to VTT • ODT handles data signals Less than 1A of burst current	Same as DDR3
Voltage Level	2.5V Core and I/O 1.25V VTT	1.8V Core and I/O 0.9V VTT	1.5V Core and I/O 0.75V VTT	1.2V Core and I/O 0.6V VTT

The TPS51200 is designed as a Gm driven LDO. The voltage droop between the reference input and the output regulator is determined by the transconductance and output current of the device. The typical Gm is 250 S at 2 A and changes with respect to the load in order to conserve the quiescent current (that is, the Gm is very low at no load condition). The Gm LDO regulator is a single pole system. Its unity gain bandwidth for the voltage loop is only determined by the output capacitance, as a result of the bandwidth nature of the Gm (see Equation 1) .

$$F_{UGBW} = \frac{Gm}{2 \times \pi \times C_{OUT}} \quad (1)$$

where

- F_{UGBW} is the unity gain bandwidth
- Gm is transconductance
- C_{OUT} is the output capacitance

There are two limitations to this type of regulator when it comes to the output bulk capacitor requirement. In order to maintain stablility, the zero location contributed by the ESR of the output capacitors should be greater than the -3-dB point of the current loop. This constraint means that higher ESR capacitors should not be used in the design. In addition, the impedance characteristics of the ceramic capacitor should be well understood in order to prevent the gain peaking effect around the Gm –3-dB point because of the large ESL, the output capacitor and parasitic inductance of the VO trace.

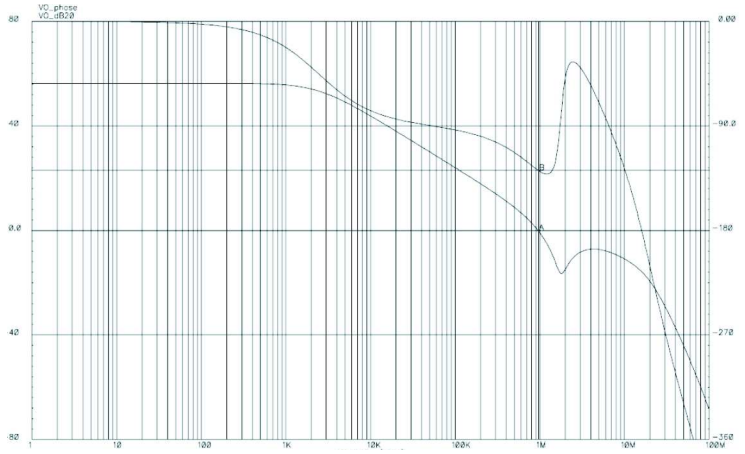


Figure 5. Bode Plot for a Typical DDR3 Configuration

Figure 5 shows the bode plot simulation for a typical DDR3 configuration of the TPS51200, where:

- V_{IN} = 3.3 V
- V_{VLDOIN} = 1.5 V
- V_{VO} = 0.75 V
- I_{IO} = 2 A
- 3 × 10-µF capacitors included
- ESR = 2.5 mΩ
- ESL = 800 pH

The unity-gain bandwidth is approximately 1 MHz and the phase margin is 52°. The 0-dB level is crossed, the gain peaks because of the ESL effect. However, the peaking is kept well below 0 dB.

Figure 6 shows the load regulation and Figure 7 shows the transient response for a typical DDR3 configuration. When the regulator is subjected to ±1.5-A load step and release, the output voltage measurement shows no difference between the dc and ac conditions.

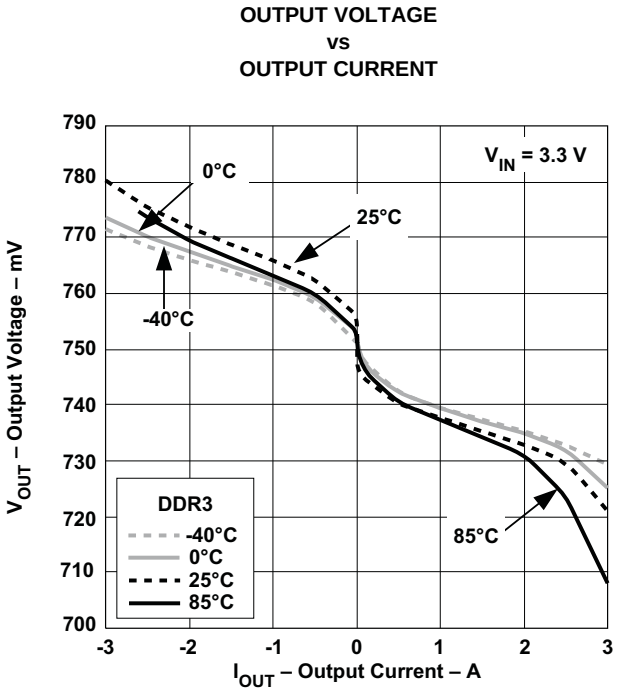


Figure 6. DC Regulaltion

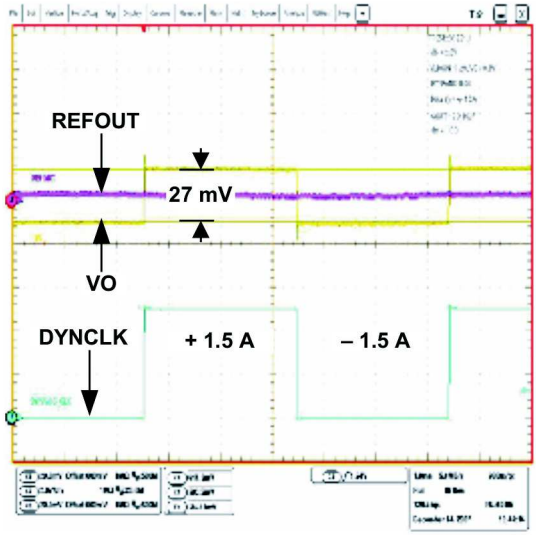


Figure 7. Transient

LDO Design Guidelines

The minimum input to output voltage difference (headroom) decides the lowest usable supply voltage Gm-driven to drive a certain load. For TPS51200, a minimum of 300 mV ($VLDOIN_{MIIN}$ – VO_{MAX}) is needed in order to support a Gm driven sourcing current of 2 A based on a design of V_{IN} = 3.3 V and C_{OUT} = 3 × 10µF. Because the TPS51200 is essentially a Gm driven LDO, its impedance characteristics are both a function of the 1/Gm and $R_{DS(on)}$ of the sourcing MOSFET (see Figure 8). The current inflection point of the design is between 2 A and 3 A. When I_{SRC} is less than the inflection point, the LDO is considered to be operating in the Gm region; when I_{SRC} is greater than the inflection point but less than the overcurrent limit point, the LDO is operating in the $R_{DS(on)}$ region. The maximum sourcing $R_{DS(on)}$ is 0.144 Ω with V_{IN} = 3.0 V and T_J = 125°C.

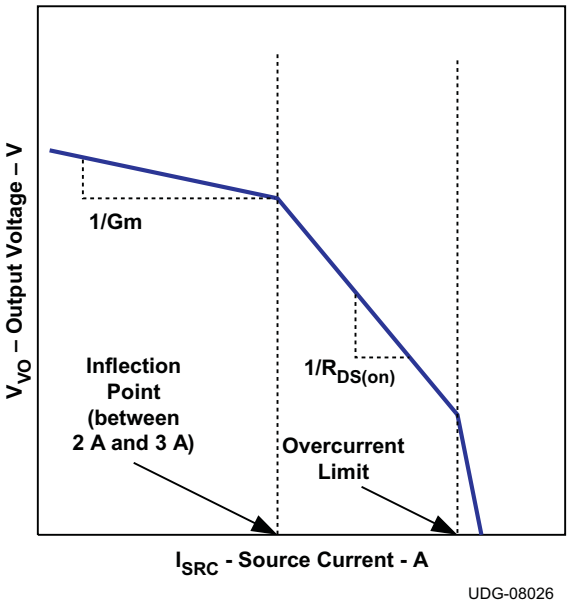


Figure 8. TPS51200 Impedance Characteristics

THERMAL DESIGN

Because the TPS51200 is a linear regulator, the VO current flows in both source and sink directions, thereby dissipating power from the device. When the device is sourcing current, the voltage difference between VLDOIN and VO times IO (I_{IO}) current becomes the power dissipation as shown in Equation 2.

$$P_{DISS\_SRC} = (V_{VLDOIN} - V_{VO}) \times I_{O\_SRC} \quad (2)$$

In this case, if VLDOIN is connected to an alternative power supply lower than the VDDQ voltage, overall power loss can be reduced. For the sink phase, VO voltage is applied across the internal LDO regulator, and the power dissipation, P_{DISS_SNK} can be calculated by Equation 3.

$$P_{DISS\_SNK} = V_{VO} \times I_{O\_SNK} \quad (3)$$

Because the device does not sink and source current at the same time and the IO current may vary rapidly with time, the actual power dissipation should be the time average of the above dissipations over the thermal relaxation duration of the system. Another source of power consumption is the current used for the internal current control circuitry from the VIN supply and the VLDOIN supply. This can be estimated as 5 mW or less during normal operatiing conditions. This power must be effectively dissipated from the package.

Maximum power dissipation allowed by the package is calculated by Equation 4.

$$P_{PKG} = [T_{J(MAX)} - T_{A(MAX)}] / \theta_{JA}$$

$$P_{PKG} = \frac{(T_{J(max)} \times T_{A(max)})}{\theta_{JA}} \quad (4)$$

where

- $T_{J(MAX)}$ is +125°C
- $T_{A(MAX)}$ is the maximum ambient temperature in the system
- θ_{JA} is the thermal resistance from junction to ambient

The thermal performance of an LDO depends on the printed circuit board (PCB) layout. The TPS51200 is housed in a thermally-enhanced PowerPAD™ package that has an exposed die pad underneath the body. For improved thermal performance, this die pad must be attached to ground via thermal land on the PCB. This ground trace acts as a both a heatsink and heatspreader. The typical thermal resistance, θ_{JA}, 52.06°C/W, is achieved based on a land pattern of 3 mm × 1.9 mm with four vias (0.33-mm via diameter, the standard thermal via size) without air flow (see Figure 9).

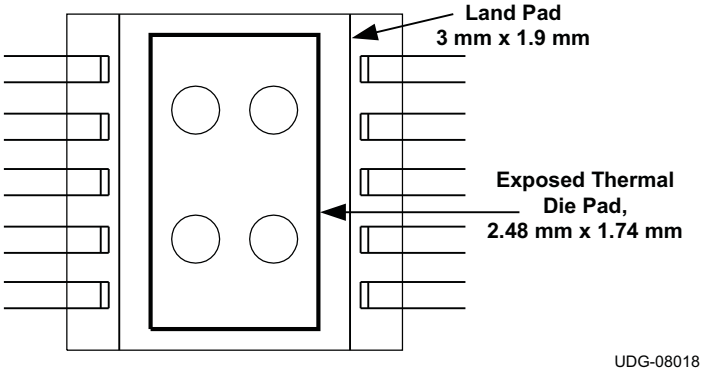


Figure 9. Recommend Land Pad Pattern for TPS51200

To further improve the thermal performance of this device, using a larger than recommended thermal land as well as increasing the number of vias helps lower the thermal resistance from junction to thermal pad. The typical thermal resistance from junction to thermal pad, θ_{JP}, is 10.24°C/W (based on the recommend land pad and four standard thermal vias).

For further information regarding the PowerPAD™ package and the recommended board layout, refer to the PowerPAD™ package application note (SLMA002). This document is available at www.ti.com.

LAYOUT CONSIDERATIONS

Consider the following points before starting the TPS51200 layout design.

- The input bypass capacitor for VLDOIN should be placed as close as possible to the pin with short and wide connections.
- The output capacitor for VO should be placed close to the pin with short and wide connection in order to avoid additional ESR and/or ESL trace inductance.
- VOSNS should be connected to the positive node of VO output capacitor(s) as a separate trace from the high current power line. This configuration is strongly recommended to avoid additional ESR and/or ESL. If sensing the voltage at the point of the load is required, it is recommended to attach the output capacitor(s) at that point. Also, it is recommended to minimize any additional ESR and/or ESL of ground trace between the GND pin and the output capacitor(s).
- Consider adding low-pass filter at VOSNS if the ESR of the VO output capacitor(s) is larger than 2 mΩ.
- REFIN can be connected separately from VLDOIN. Remember that this sensing potential is the reference voltage of REFOUT. Avoid any noise-generating lines.
- The negative node of the VO output capacitor(s) and the REFOUT capacitor should be tied together by avoiding common impedance to the high current path of the VO source/sink current.
- The GND and PGND pins should be connected to the thermal land underneath the die pad with multiple vias connecting to the internal system ground planes (for better result, use at least two internal ground planes). Use as many vias as possible to reduce the impedance between PGND/GND and the system ground plane. Also, place bulk caps close to the DIMM load point, route the VOSNS to the DIMM load sense point.
- In order to effectively remove heat from the package, properly prepare the thermal land. Apply solder directly to the package's thermal pad. The wide traces of the component and the side copper connected to the thermal land pad help to dissipate heat. Numerous vias 0,33 mm in diameter connected from the thermal land to the internal/solder side ground plane(s) should also be used to help dissipation.
- Please consult the TPS51200-EVM User's Guide (SLUUxxx) for detailed layout recommendations.

TYPICAL CHARACTERISTICS

For Figure 10 through Figure 24, 3 × 10-µF MLCCs (0805) are used on the output.

OUTPUT VOLTAGE vs OUTPUT CURRENT

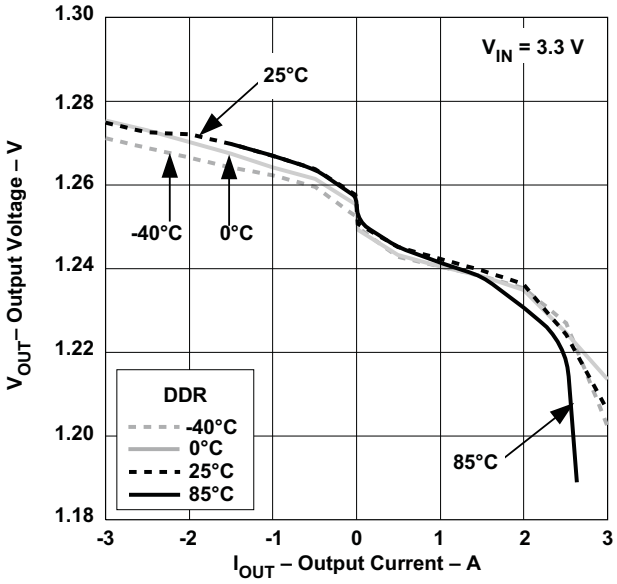


Figure 10.

OUTPUT VOLTAGE vs OUTPUT CURRENT

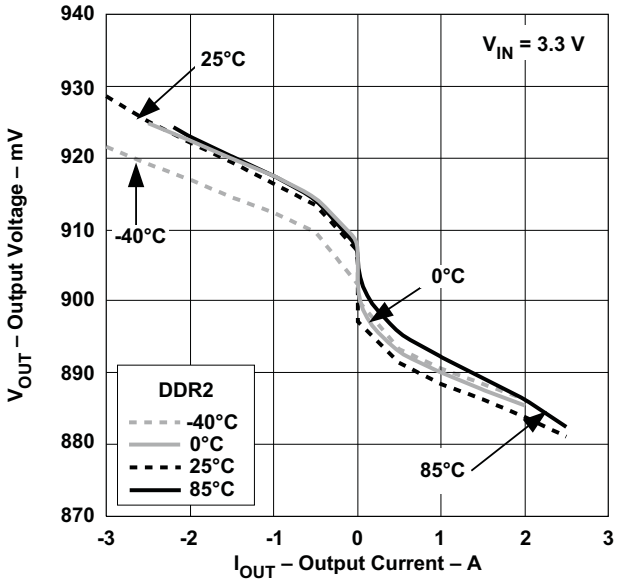


Figure 11.

OUTPUT VOLTAGE vs OUTPUT CURRENT

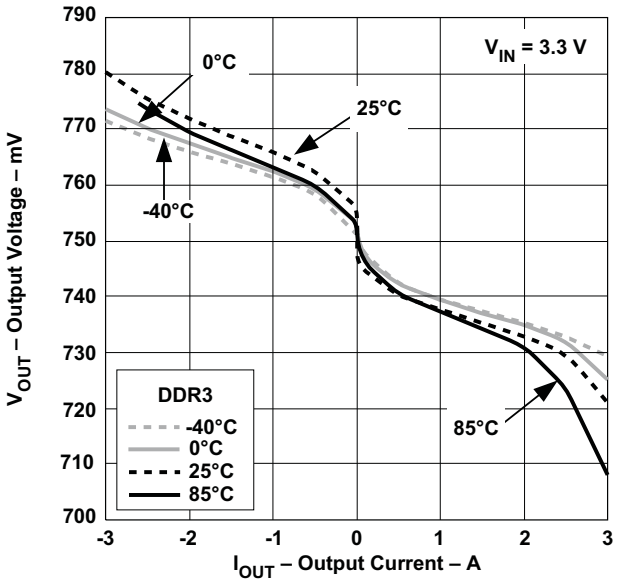


Figure 12.

OUTPUT VOLTAGE vs OUTPUT CURRENT

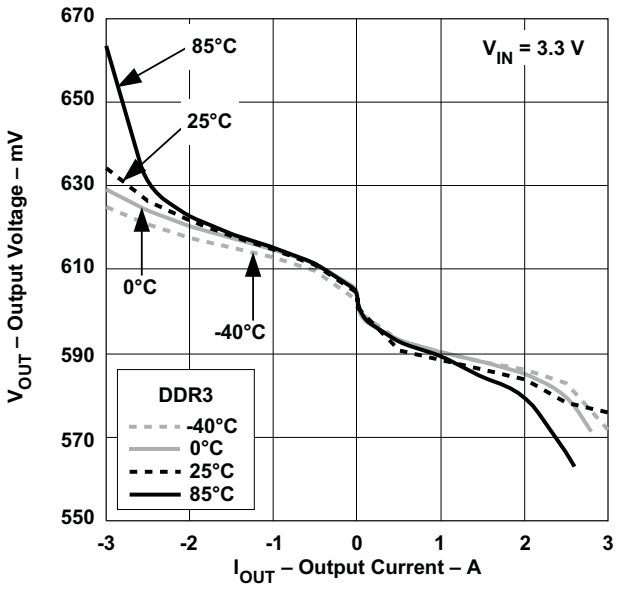


Figure 13.

TYPICAL CHARACTERISTICS (continued)

For Figure 10 through Figure 24, 3 × 10-µF MLCCs (0805) are used on the output.

OUTPUT VOLTAGE vs OUTPUT CURRENT

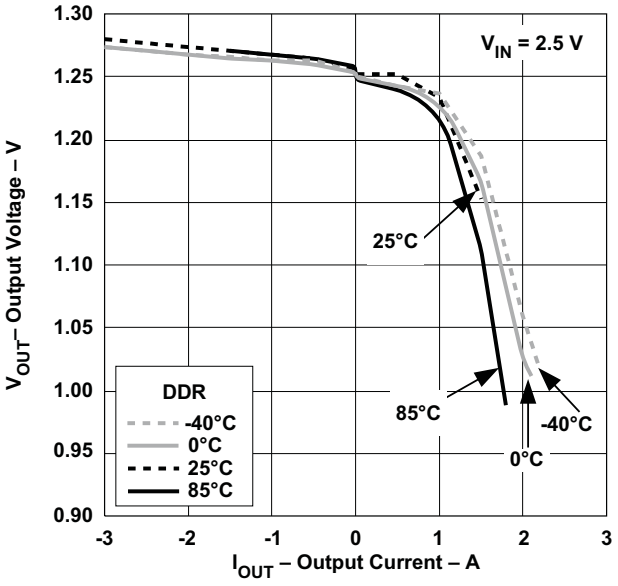


Figure 14.

OUTPUT CURRENT vs OUTPUT VOLTAGE

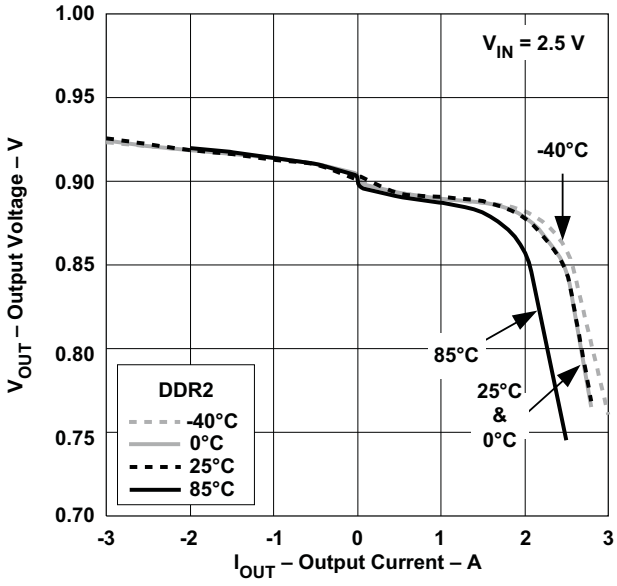


Figure 15.

OUTPUT VOLTAGE vs OUTPUT CURRENT

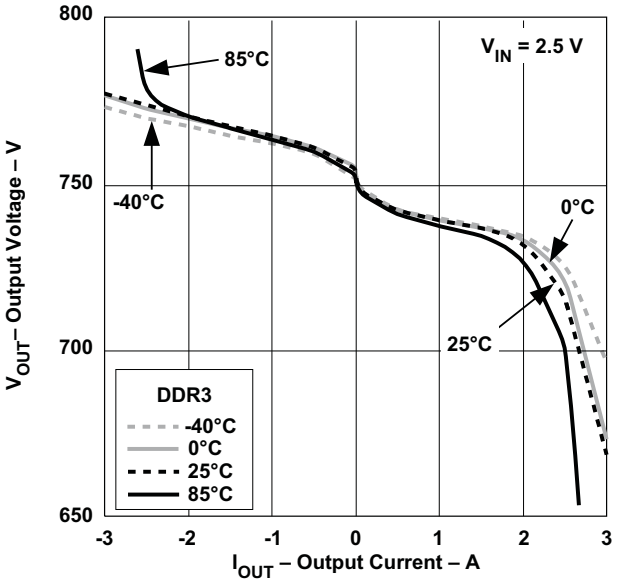


Figure 16.

OUTPUT VOLTAGE vs OUTPUT CURRENT

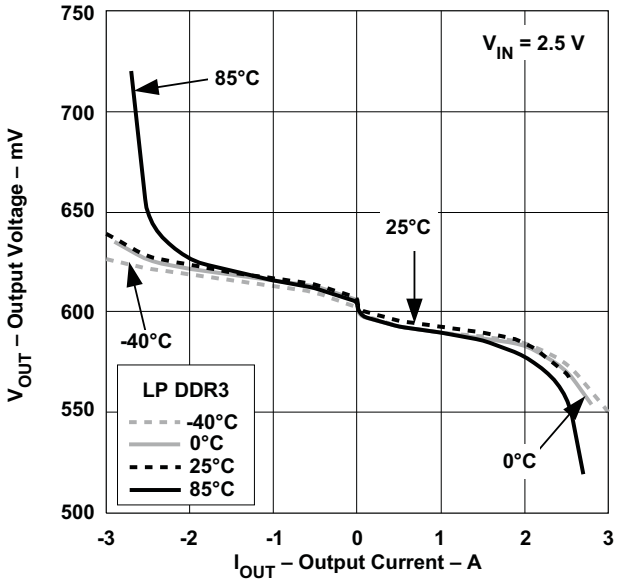


Figure 17.

TYPICAL CHARACTERISTICS (continued)

For Figure 10 through Figure 24, 3 × 10-µF MLCCs (0805) are used on the output.

REFOUT VOLTAGE vs REFOUT CURRENT

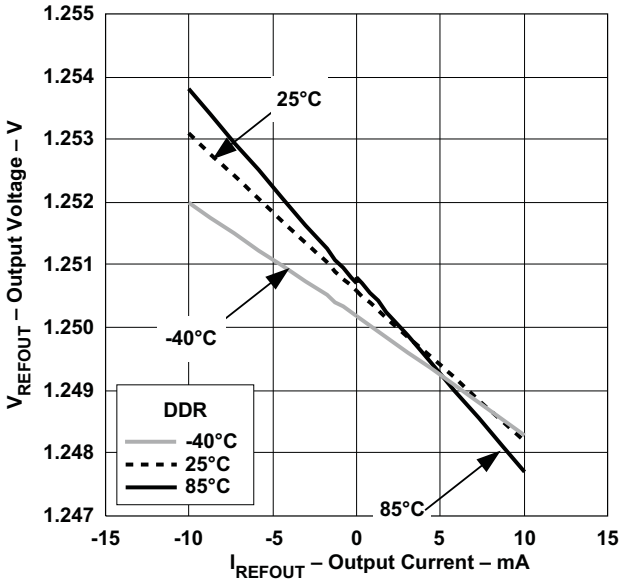


Figure 18.

REFOUT VOLTAGE vs REFOUT CURRENT

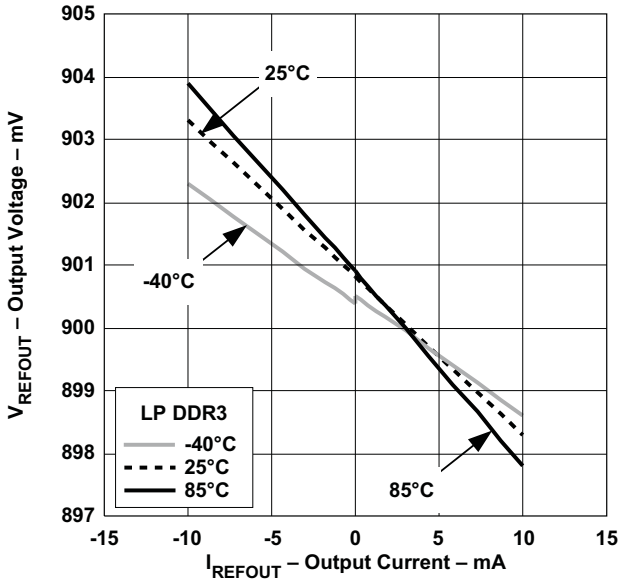


Figure 19.

REFOUT VOLTAGE vs REFOUT CURRENT

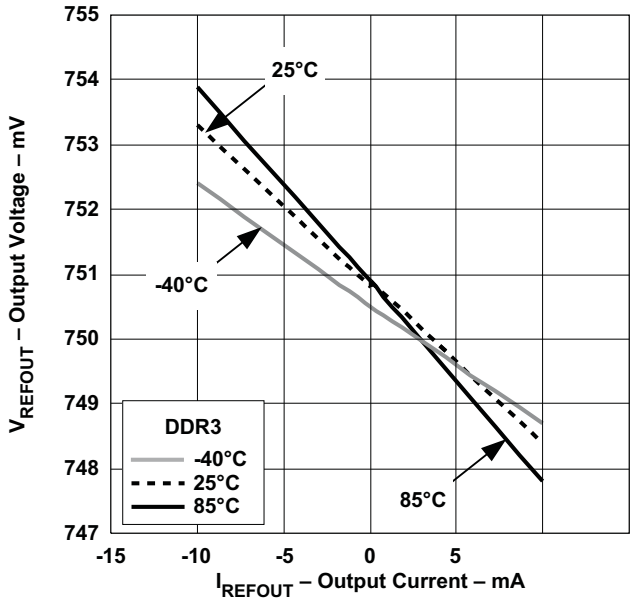


Figure 20.

REFOUT VOLTAGE vs REFOUT CURRENT

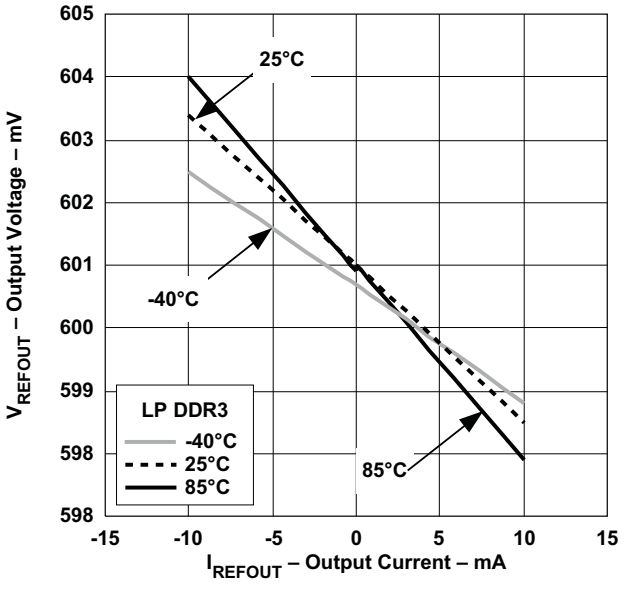


Figure 21.

TYPICAL CHARACTERISTICS (continued)

For Figure 10 through Figure 24, 3 × 10-µF MLCCs (0805) are used on the output.

DROPOUT VOLTAGE vs OUTPUT CURRENT

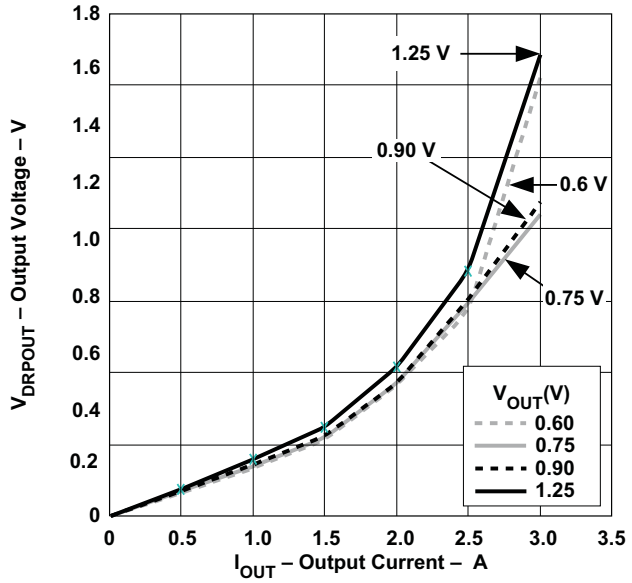


Figure 22.

GAIN AND PHASE vs FREQUENCY

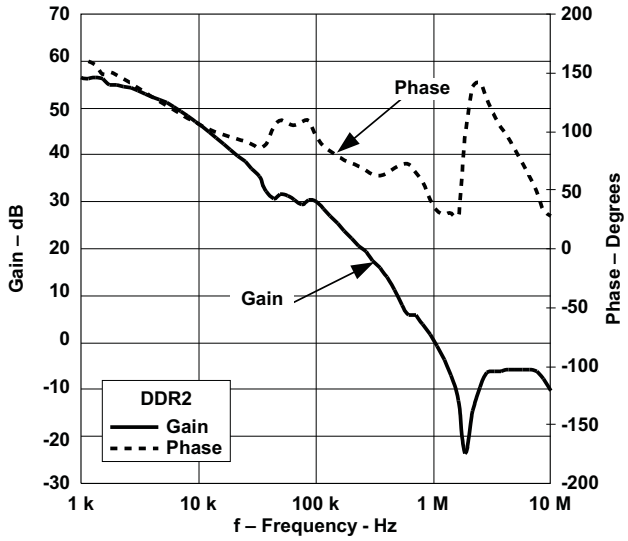


Figure 23.

GAIN AND PHASE vs FREQUENCY

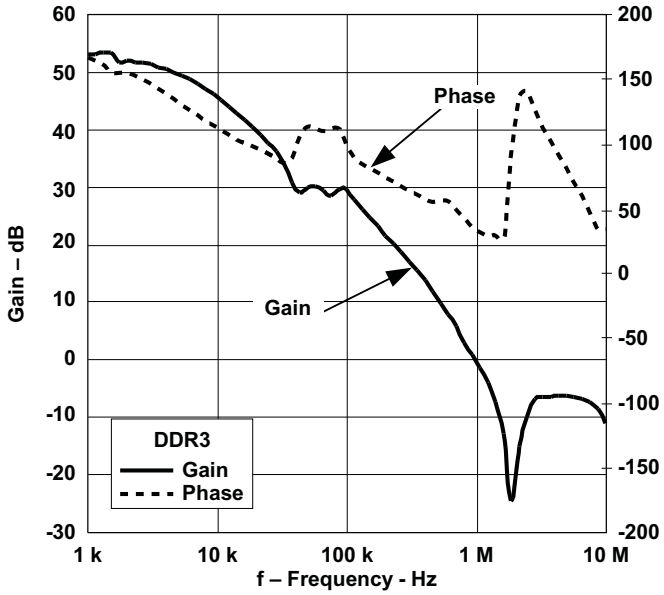


Figure 24.

DESIGN EXAMPLES

Design Example 1

This design example describes a 3.3-V_{IN}, DDR2 Configuration

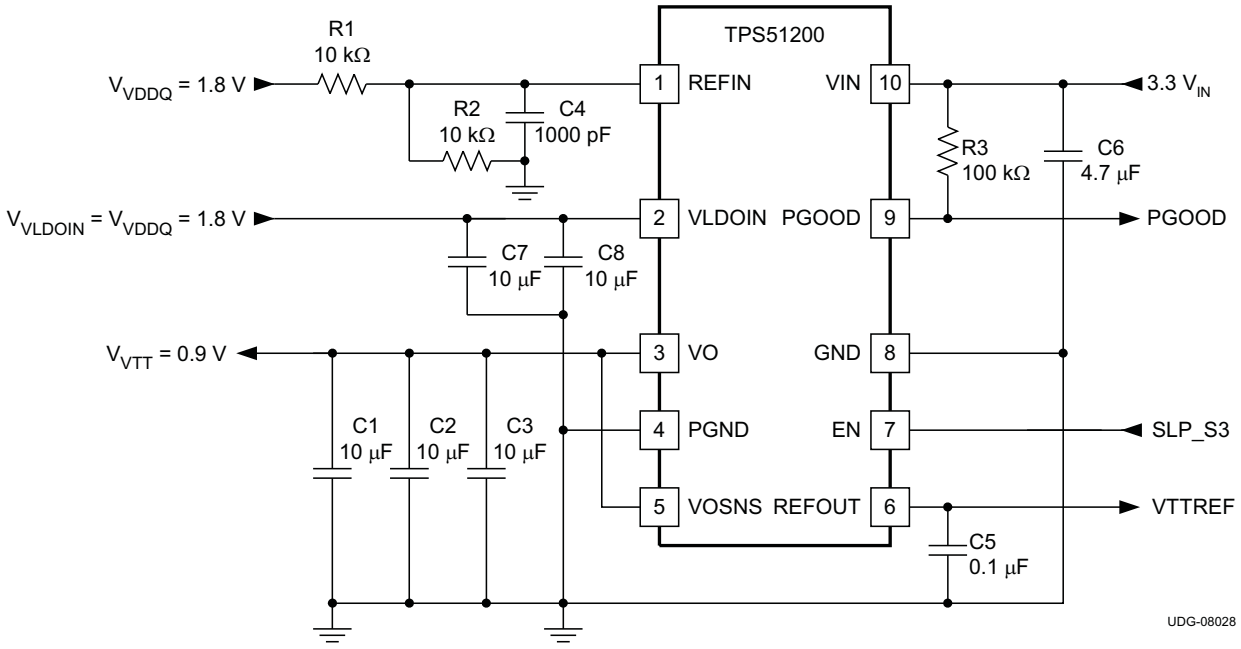


Figure 25. 3.3-V_{IN}, DDR2 Configuration

Table 2. Design Example 1 List of Materials

REFERENCE DESIGNATOR	DESCRIPTION	SPECIFICATION	PART NUMBER	MANUFACTURER
R1, R2	Resistor	10 kΩ		
R3		100 kΩ		
C1, C2, C3	Capacitor	10 µF, 6.3 V	GRM21BR70J106KE76L	Murata
C4		1000 pF		
C5		0.1 µF		
C6		4.7 µF, 6.3 V	GRM21BR60J475KA11L	Murata
C7, C8		10 µF, 6.3 V	GRM21BR70J106KE76L	Murata

Design Example 2

This design example describes a 3.3-V_{IN}, DDR3 Configuration

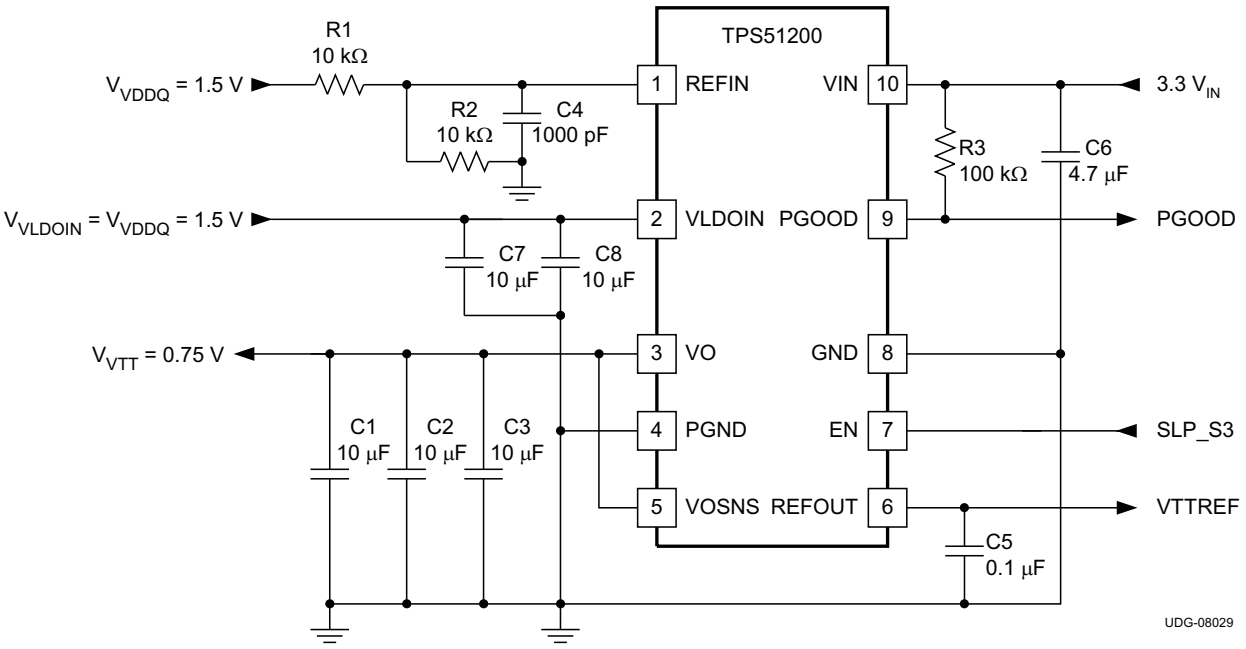


Figure 26. 3.3-V_{IN}, DDR3 Configuration

Table 3. Design Example 2 List of Materials

REFERENCE DESIGNATOR	DESCRIPTION	SPECIFICATION	PART NUMBER	MANUFACTURER
R1, R2	Resistor	10 kΩ		
R3		100 kΩ		
C1, C2, C3	Capacitor	10 µF, 6.3 V	GRM21BR70J106KE76L	Murata
C4		1000 pF		
C5		0.1 µF		
C6		4.7 µF, 6.3 V	GRM21BR60J475KA11L	Murata
C7, C8		10 µF, 6.3 V	GRM21BR70J106KE76L	Murata

Design Example 3

This design example describes a 2.5-V_{IN}, DDR3 Configuration

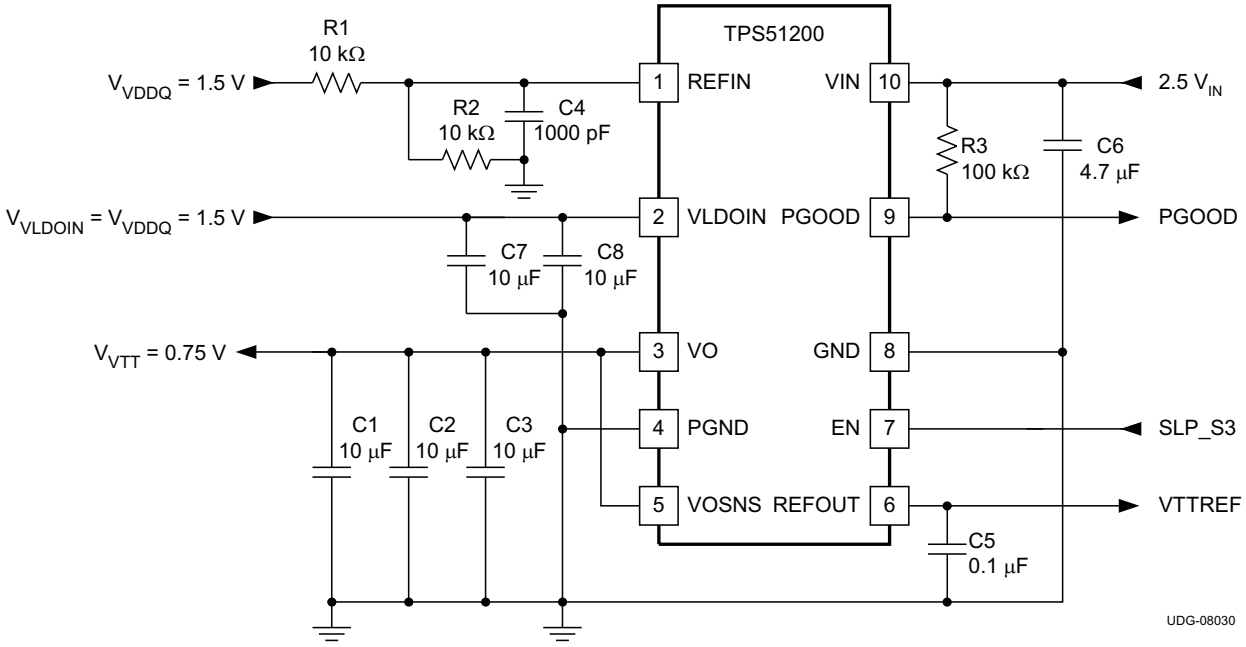


Figure 27. 2.5-V_{IN}, DDR3 Configuration

Table 4. Design Example 3 List of Materials

REFERENCE DESIGNATOR	DESCRIPTION	SPECIFICATION	PART NUMBER	MANUFACTURER
R1, R2	Resistor	10 kΩ		
R3		100 kΩ		
C1, C2, C3	Capacitor	10 µF, 6.3 V	GRM21BR70J106KE76L	Murata
C4		1000 pF		
C5		0.1 µF		
C6		4.7 µF, 6.3 V	GRM21BR60J475KA11L	Murata
C7, C8		10 µF, 6.3 V	GRM21BR70J106KE76L	Murata

Design Example 4

This design example describes a 3.3-V_{IN}, LP DDR3 Configuration

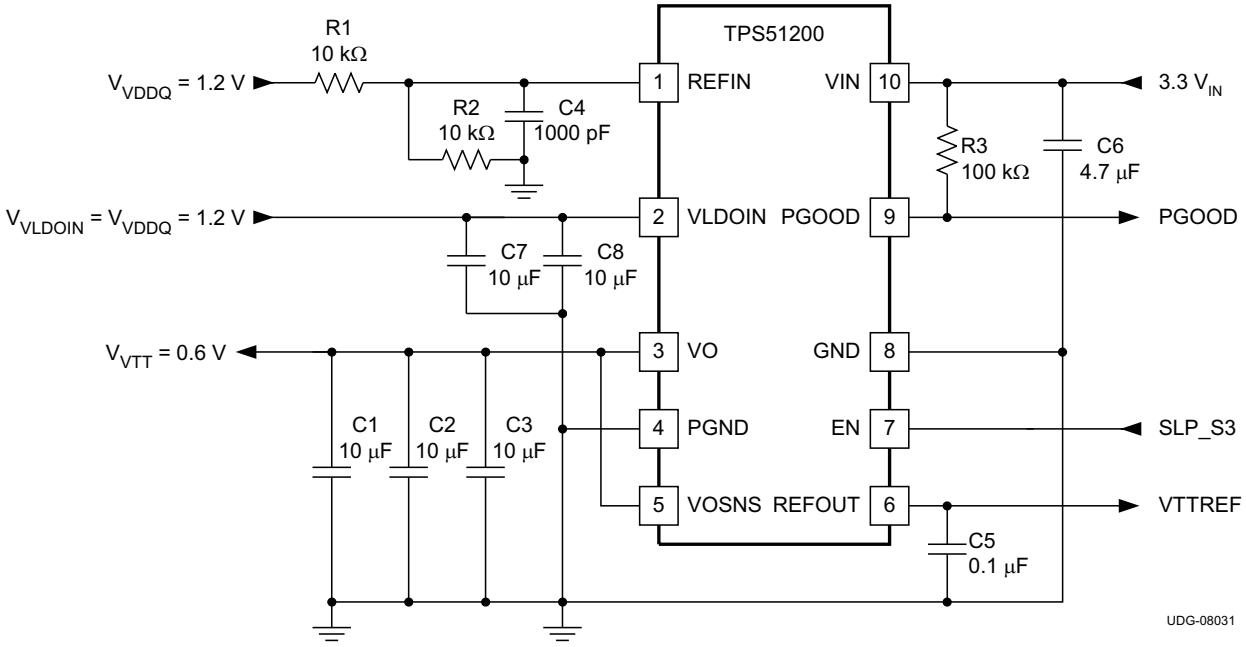


Figure 28. 3.3-V_{IN}, LP DDR3 Configuration

Table 5. Design Example 4 List of Materials

REFERENCE DESIGNATOR	DESCRIPTION	SPECIFICATION	PART NUMBER	MANUFACTURER
R1, R2	Resistor	10 kΩ		
R3		100 kΩ		
C1, C2, C3	Capacitor	10 µF, 6.3 V	GRM21BR70J106KE76L	Murata
C4		1000 pF		
C5		0.1 µF		
C6		4.7 µF, 6.3 V	GRM21BR60J475KA11L	Murata
C7, C8		10 µF, 6.3 V	GRM21BR70J106KE76L	Murata

Design Example 5

This design example describes a 3.3-V_{IN}, DDR3 Tracking Configuration

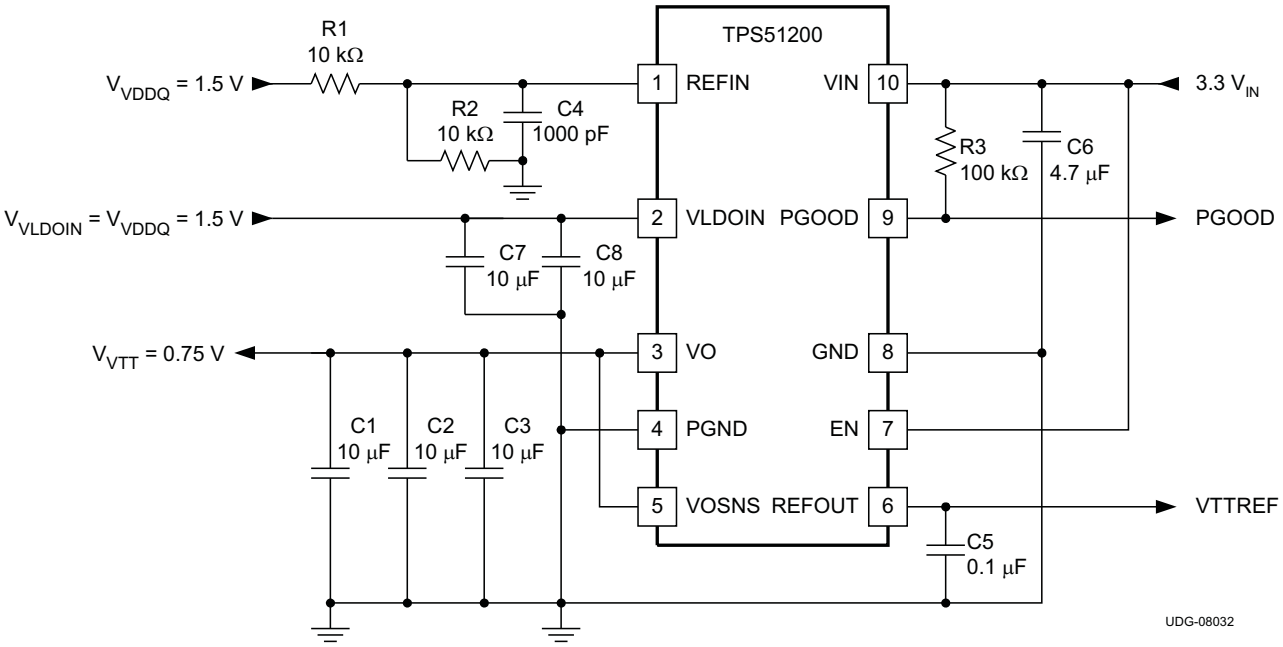


Figure 29. 3.3-V_{IN}, DDR3 Tracking Configuration

Table 6. Design Example 5 List of Materials

REFERENCE DESIGNATOR	DESCRIPTION	SPECIFICATION	PART NUMBER	MANUFACTURER
R1, R2	Resistor	10 kΩ		
R3		100 kΩ		
C1, C2, C3	Capacitor	10 µF, 6.3 V	GRM21BR70J106KE76L	Murata
C4		1000 pF		
C5		0.1 µF		
C6		4.7 µF, 6.3 V	GRM21BR60J475KA11L	Murata
C7, C8		10 µF, 6.3 V	GRM21BR70J106KE76L	Murata

Design Example 6

This design example describes a 3.3-V_{IN}, LDO Configuration.

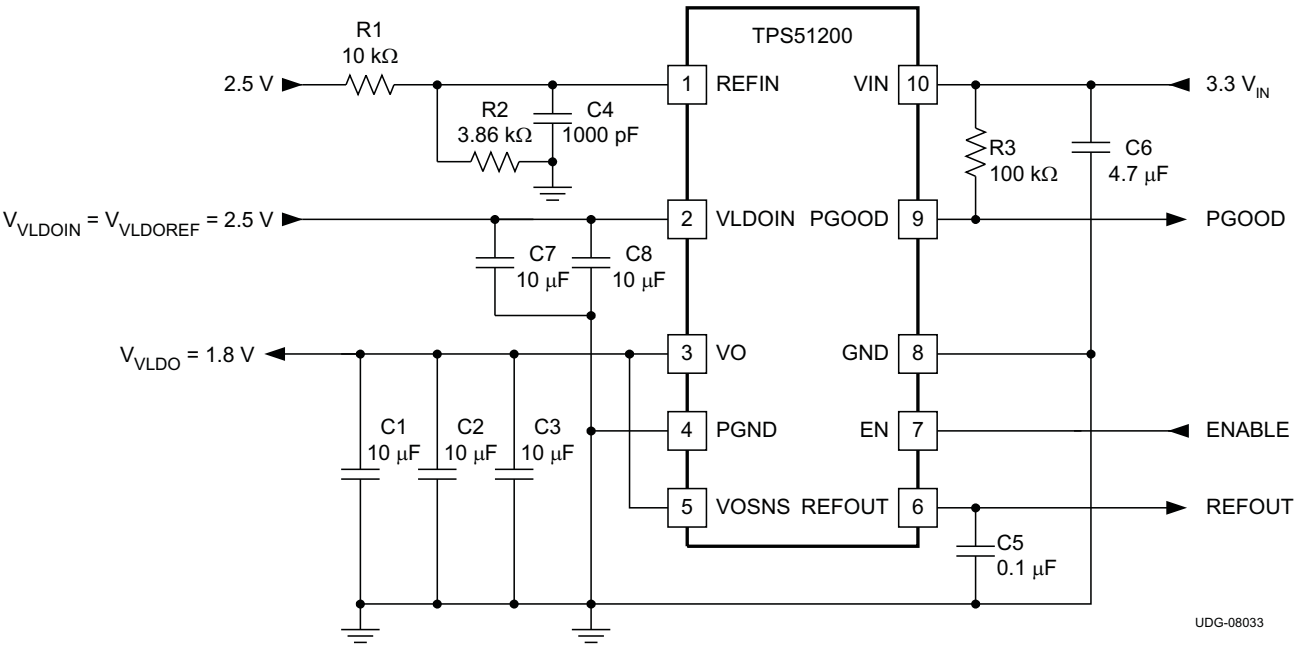


Figure 30. 3.3-V_{IN}, LDO Configuration

Table 7. Design Example 6 List of Materials

REFERENCE DESIGNATOR	DESCRIPTION	SPECIFICATION	PART NUMBER	MANUFACTURER
R1	Resistor	10 kΩ		
R2		3.86 kΩ		
R3		100 kΩ		
C1, C2, C3	Capacitor	10 µF, 6.3 V	GRM21BR70J106KE76L	Murata
C4		1000 pF		
C5		0.1 µF		
C6		4.7 µF, 6.3 V	GRM21BR60J475KA11L	Murata
C7, C8		10 µF, 6.3 V	GRM21BR70J106KE76L	Murata

Design Example 7

This design example describes a 3.3-V_{IN}, DDR3 Configuration with LFP.

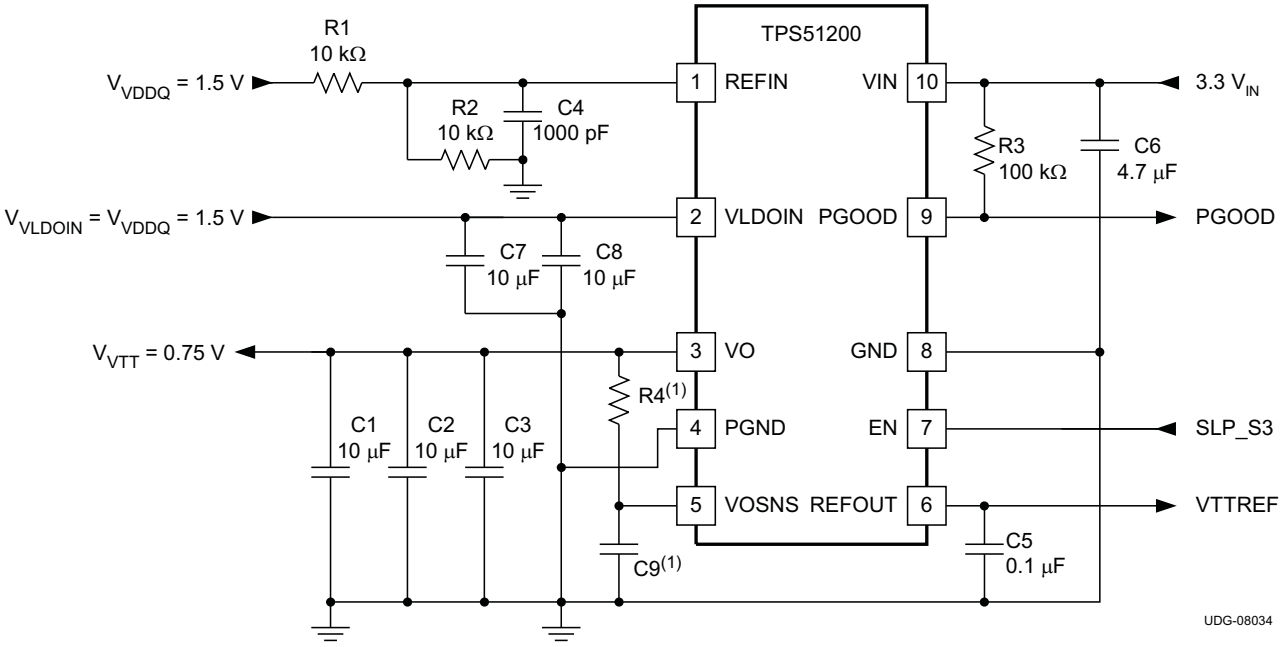


Figure 31. 3.3-V_{IN}, DDR3 Configuration with LFP

Table 8. Design Example 7 List of Materials

REFERENCE DESIGNATOR	DESCRIPTION	SPECIFICATION	PART NUMBER	MANUFACTURER
R1, R2	Resistor	10 kΩ		
R3		100 kΩ		
R4 (1)				
C1, C2, C3	Capacitor	10 µF, 6.3 V	GRM21BR70J106KE76L	Murata
C4		1000 pF		
C5		0.1 µF		
C6		4.7 µF, 6.3 V	GRM21BR60J475KA11L	Murata
C7, C8		10 µF, 6.3 V	GRM21BR70J106KE76L	Murata
C9(1)				

(1) The values of R4 and C9 should be chosen to reduce the parasitic effect of the trace (between VO and the output MLCCs) and the output capacitors (ESR and ESL).

REVISION HISTORY

Changes from Original (November, 2009) to Revision A	Page
• Added thermal table information for DRC package.	2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TPS51200QDRCRQ1	ACTIVE	SON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

OTHER QUALIFIED VERSIONS OF TPS51200-Q1 :

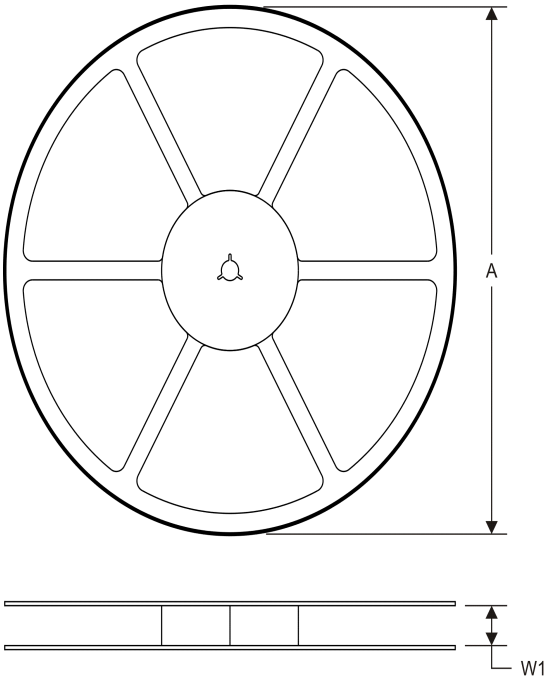
- Catalog: TPS51200

NOTE: Qualified Version Definitions:

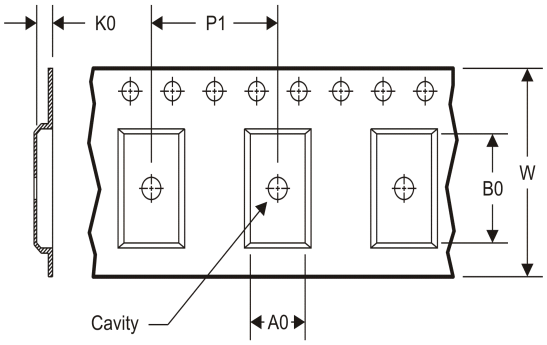
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



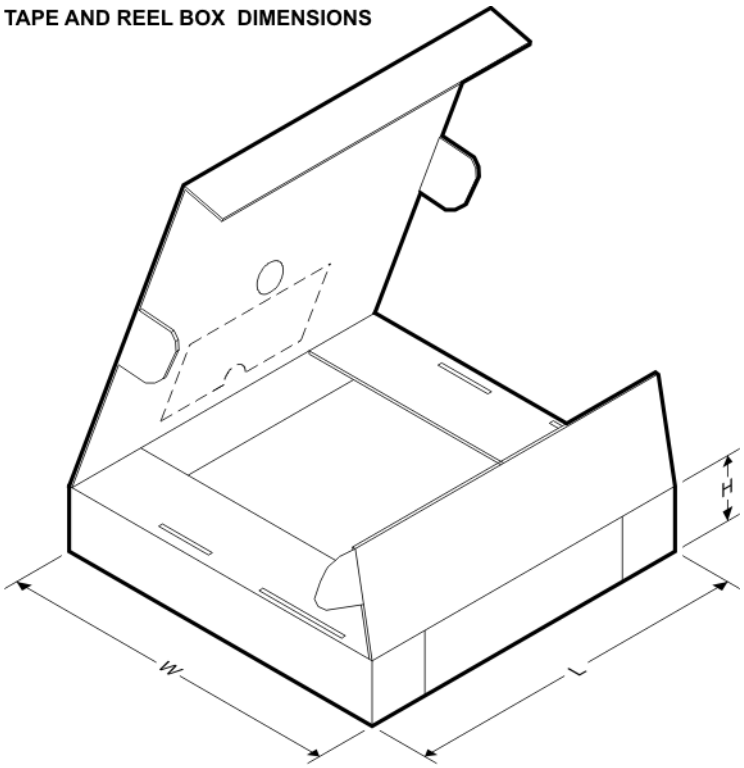
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS51200QDRCRQ1	SON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

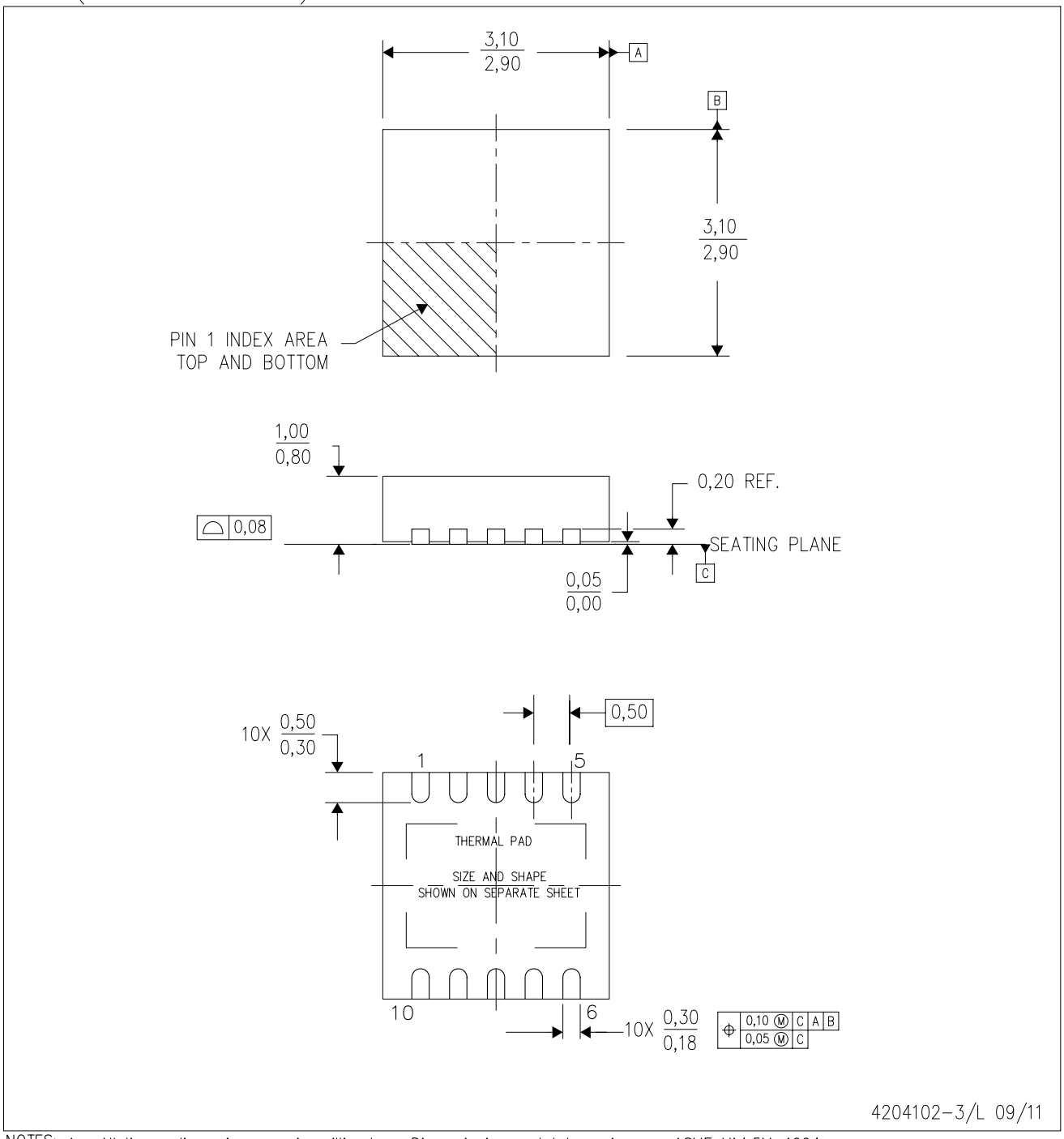
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS51200QDRCRQ1	SON	DRC	10	3000	367.0	367.0	35.0

DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance, if present.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions, if present

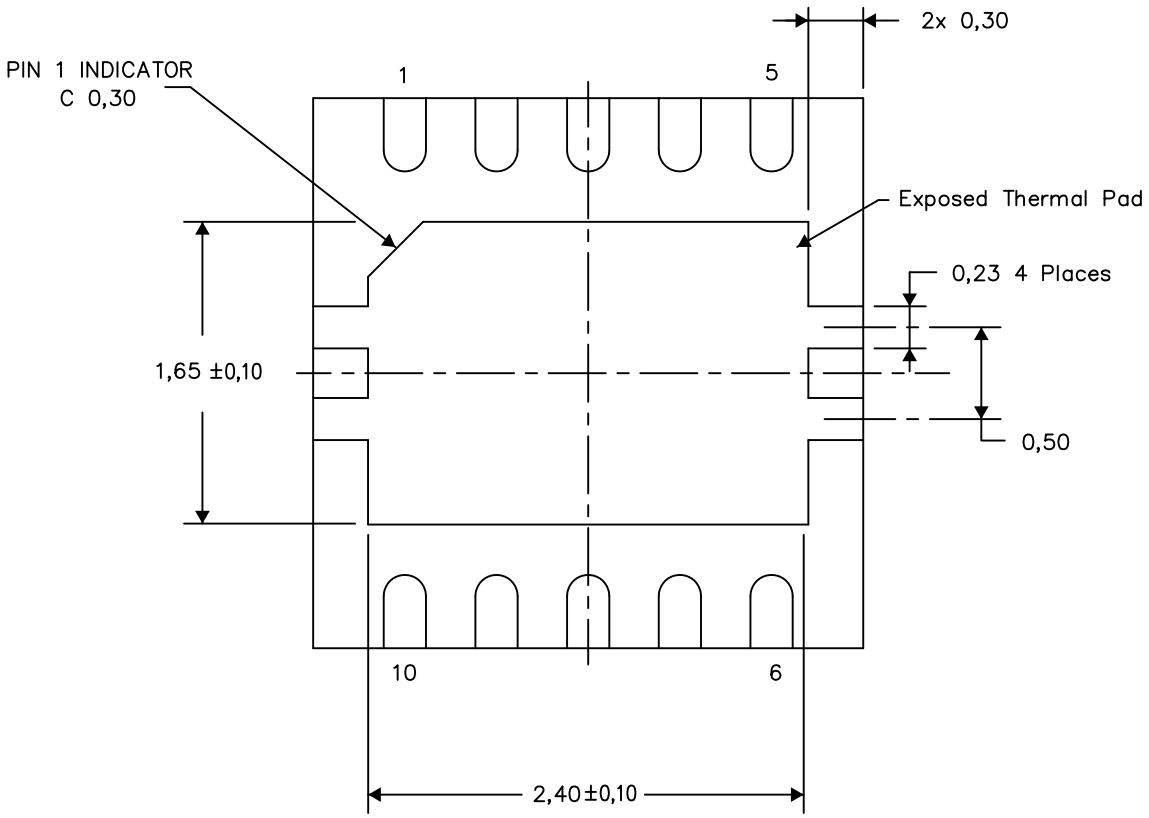
DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



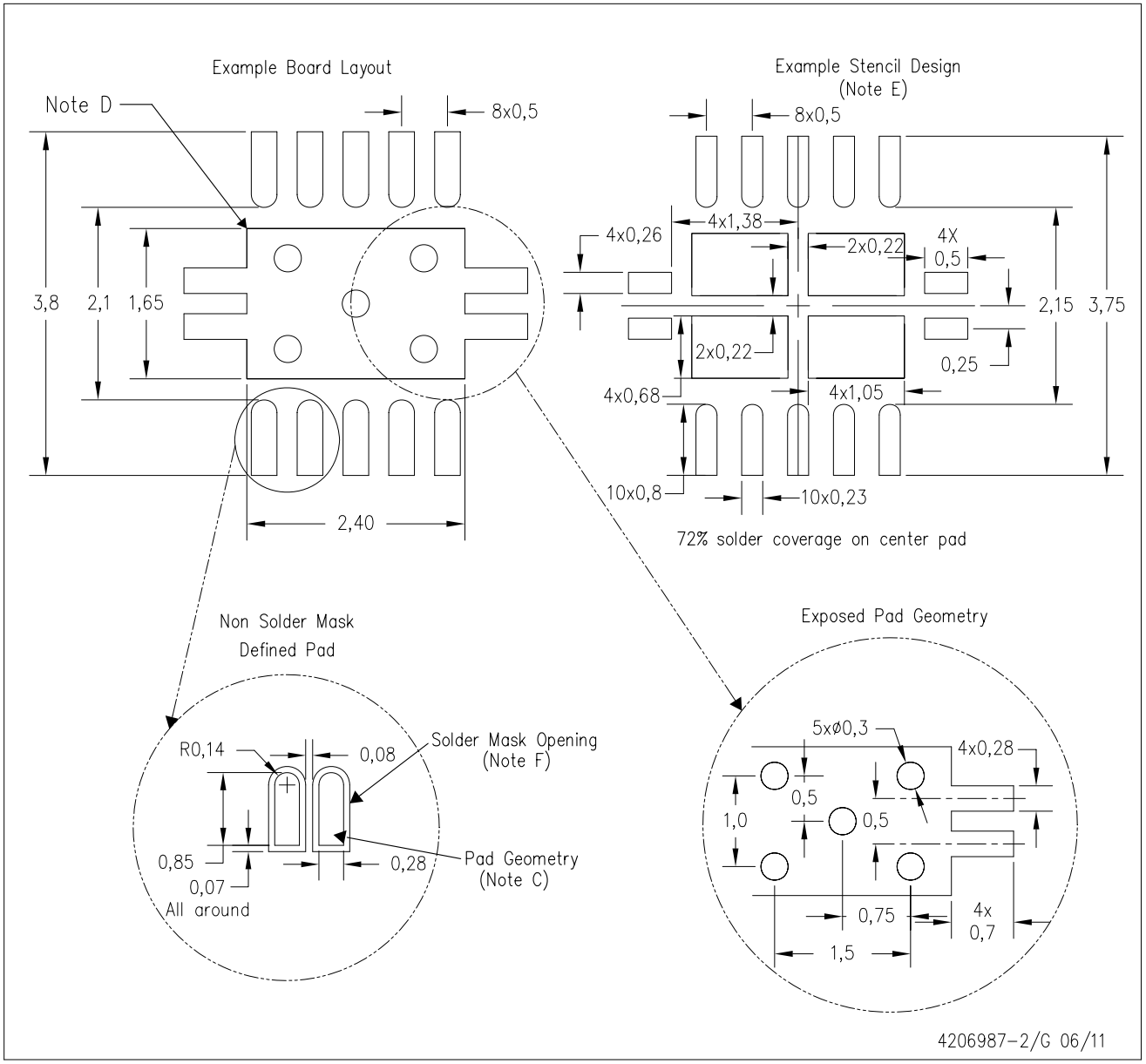
Bottom View

Exposed Thermal Pad Dimensions

4206565–3/N 07/12

NOTE: A. All linear dimensions are in millimeters

DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46C and to discontinue any product or service per JESD48B. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components which meet ISO/TS16949 requirements, mainly for automotive use. Components which have not been so designated are neither designed nor intended for automotive use; and TI will not be responsible for any failure of such components to meet such requirements.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Mobile Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265