Voltage Protection with Automatic Cell Balance for 2-Series Cell Li-Ion Batteries

Check for Samples: bq29200 , bq29209

FEATURES

- **2-Series Cell Secondary Protection**
- **Automatic Cell Imbalance Correction with External Enable Control**
  - **±30 mV Enable, 0 mV Disable Thresholds Typical**
- **External Capacitor-Controlled Delay Timer**
- **External Resistor-Controlled Cell Balance Current**
- **Low Power Consumption I_{CC} < 3 µA Typical (V_{CELL}(ALL) < $V_{PROTECT}$)**
- **Internal Cell Balancing Handles Current up to 15 mA**
- **External Cell Balancing Mode Supported**
- **High-Accuracy Overvoltage Protection:**
  - **±25 mV with T_A = 0°C to 60°C**
- **Fixed Overvoltage Protection Thresholds: 4.30 V, 4.35 V**
- **Small 8L DRB Package**

APPLICATIONS

- **2nd Level Protection in Li-Ion Battery Packs**
  - **Netbook Computers**
  - **Power Tools**
  - **Portable Equipment and Instrumentation**
  - **Battery Backup Systems**

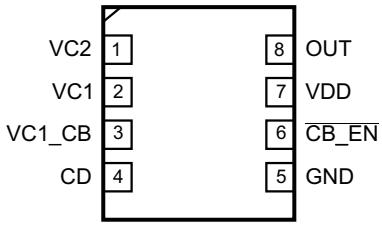
DESCRIPTION

The bq2920x device is a secondary overvoltage protection IC for 2-series cell lithium-ion battery packs that incorporates a high-accuracy precision overvoltage detection circuit and automatic cell imbalance correction.

The voltage of each cell in a 2-series cell battery pack is compared to an internal reference voltage. If either cell reaches an overvoltage condition, the bq2920x device starts a timer that provides a delay proportional to the capacitance on the CD pin. Upon expiration of the internal timer, the OUT pin changes from low to high state.

If enabled, the bq2920x performs automatic cell imbalance correction where the two cells are automatically corrected for voltage imbalance by loading the cell with the higher charge voltage with a small balancing current. When the cells are measured to be equal within nominally 0 mV, the load current is removed. It will be re-applied if the imbalance exceeds nominally 30 mV. The cell mismatch correction circuitry is enabled by pulling the CB_EN pin low, and disabled when CB_EN is pulled to VDD or greater than 2.2 V.

If the internal cell balancing current of up to 15 mA is insufficient, the bq2920x may be configured via external circuitry to support much higher external cell balancing current.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_A	PART NUMBER	PACKAGE	PACKAGE DESIGNATOR	PACKAGE MARKING	OVP	ORDERING INFORMATION	
						TAPE AND REEL (LARGE)	TAPE AND REEL (SMALL)
–40°C to +110°C	BQ29200	QFN-8	DRB	200	4.35 V	BQ29200DRBR	BQ29209DRBT
	BQ29209			209	4.30 V	BQ29209DRBR	BQ29209DRBT

THERMAL INFORMATION

THERMAL METRIC(1)		bq2920x DRB 8 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	50.5	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance (3)	25.1	
θ_{JB}	Junction-to-board thermal resistance (4)	19.3	
ψ_{JT}	Junction-to-top characterization parameter (5)	0.7	
ψ_{JB}	Junction-to-board characterization parameter (6)	18.9	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance (7)	5.2	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

PIN FUNCTIONS

PIN NAME	NO.	DESCRIPTION
$\overline{CB\_EN}$	6	Cell balance enable
CD	4	Connection to external capacitor for programmable delay time
GND	5	Ground pin
OUT	8	Output
VC1	2	Sense voltage input for bottom cell
VC1_CB	3	Cell balance input for bottom cell
VC2	1	Sense voltage input for top cell
VDD	7	Power supply

FUNCTIONAL BLOCK DIAGRAM

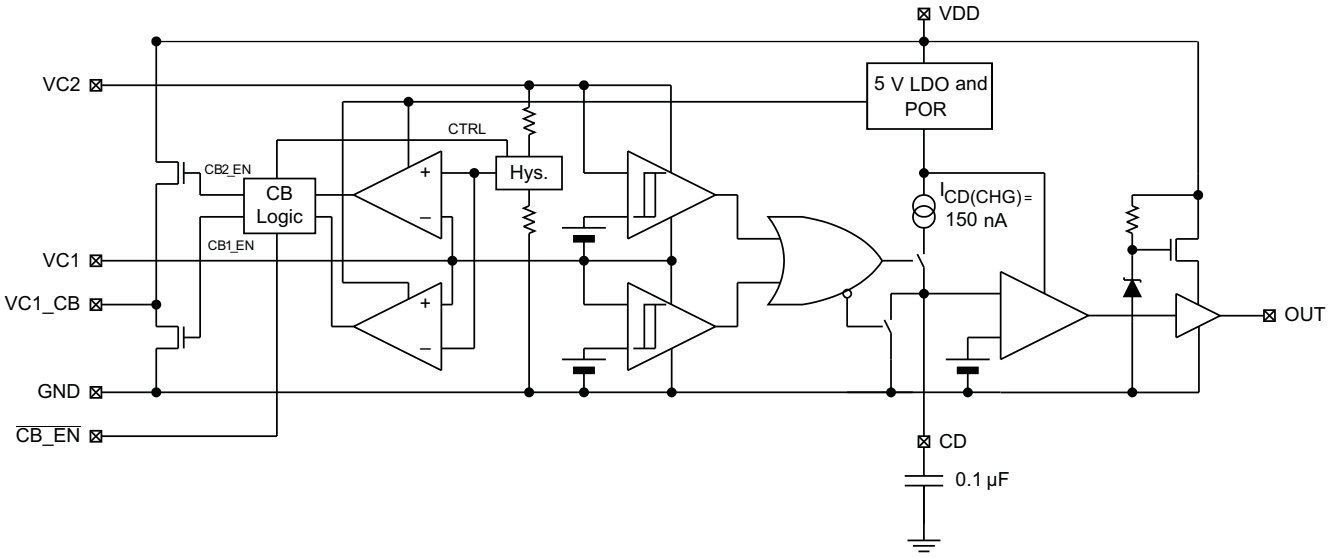


Figure 1. Block Diagram

ABSOLUTE MAXIMUM RATINGS

Over-operating free-air temperature range (unless otherwise noted)(1)

		VALUE/UNIT
Supply voltage range, V_{MAX}	VDD–GND	–0.3 V to 16 V
Input voltage range, V_{IN}	VC2–GND, VC1–GND	–0.3 V to 16 V
	VC2–VC1, CD–GND	–0.3 V to 8 V
	$\overline{CB\_EN}$–GND	–0.3 V to 16 V
Output voltage range, V_{OUT}	OUT–GND	–0.3 V to 16 V
Continuous total power dissipation, P_{TOT}		See package dissipation rating
Storage temperature range, T_{STG}		–65°C to 150°C
Lead temperature (soldering, 10 s), T_{SOLDER}		300°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply voltage, VDD		4		10	V
Input voltage range	VC2–VC1, VC1–GND	0		5	V
Delay time capacitance, $t_{d(CD)}$	C_{CD} (See Figure 8.)		0.1		µF
Voltage monitor filter resistance	R_{IN} (See Figure 8.)	100	1K		Ω
Voltage monitor filter capacitance	C_{IN} (See Figure 8.)	0.01	0.1		µF
Supply voltage filter resistance	R_{VD} (See Figure 8.)		100	1K	Ω
Supply voltage filter capacitance	C_{VD} (See Figure 8.)		0.1		µF
Cell balance resistance	R_{CB} (See Figure 8 and PROTECTION (OUT) TIMING.)	100		4.7K	Ω
Operating ambient temperature range, T_A		–40		110	°C

ELECTRICAL CHARACTERISTICS

Typical values stated where T_A = 25°C and VDD = 7.2 V. Min/Max values stated where T_A = –40°C to 110°C and VDD = 4 V to 10 V (unless otherwise noted).

PARAMETER			TEST CONDITION	MIN	NOM	MAX	UNIT
$V_{PROTECT}$	Overvoltage detection voltage	bq29209			4.30		V
		bq29200			4.35		
V_{HYS}	Overvoltage detection hysteresis			200	300	400	mV
V_{OA}	Overvoltage detection accuracy		T_A = 25°C	–10		10	mV
V_{OA_DRIFT}	Overvoltage threshold temperature drift		T_A = 0°C to 60°C	–0.4		0.4	mV°/C
			T_A = –40°C to 110°C	–0.6		0.6	
X_{DELAY}	Overvoltage delay time scale factor		T_A = 0°C to 60°C Note: Does not include external capacitor variation.	6.0	9.0	12.0	s/µF
			T_A = –40°C to 110°C Note: Does not include external capacitor variation.	5.5	9.0	13.5	
X_{DELAY_CTM} (1)	Overvoltage delay time scale factor in Customer Test Mode				0.08		s/µF
$I_{CD(CHG)}$	Overvoltage detection charging current				150		nA
$I_{CD(DSG)}$	Overvoltage detection discharging current				60		µA
V_{CD}	Overvoltage detection external capacitor comparator threshold				1.2		V
I_{CC}	Supply current		(VC2–VC1) = (VC1–GND) = 3.5 V (See Figure 4.)		3.0	6.0	µA
V_{OUT}	OUT pin drive voltage		(VC2–VC1) or (VC1–GND) > $V_{PROTECT}$, VDD = 10 V, I_{OH} = 0	6	8.25	9.5	V
			(VC2–VC1) or (VC1–GND) = $V_{PROTECT}$, VDD = $V_{PROTECT}$, I_{OH} = –100 µA, T_A = 0°C to 60°C	1.75	2.5		V
			(VC2–VC1) and (VC1–GND) < $V_{PROTECT}$, I_{OL} = 100 µA, T_A = 25°C			200	mV
			(VC2–VC1) and (VC1–GND) < $V_{PROTECT}$, I_{OL} = 0 µA, T_A = 25°C		0	10	mV
			VC2 = VC1 = VDD = 4 V, I_{OL} = 100 µA			200	mV
I_{OH}	High-level output current		OUT = 1.75 V, (VC2–VC1) or (VC1–GND) = $V_{PROTECT}$, VDD = $V_{PROTECT}$ to 10 V, T_A = 0°C to 60°C	–100			µA
I_{OL}	Low-level output current		OUT = 0.05 V, (VC2–VC1) or (VC1–GND) < $V_{PROTECT}$, VDD = $V_{PROTECT}$ to 10 V, T_A = 0°C to 60°C	30		85	µA
I_{OH_ZV}	High-level short-circuit output current		OUT = 0 V, (VC2–VC1) = (VC1–GND) = $V_{PROTECT}$ VDD = 4 to 10 V			–8.0	mA
I_{IN}	Input current at VCx pins		Measured at VC1, (VC2–VC1) = (VC1–GND) = 3.5 V, T_A = 0°C to 60°C (See Figure 4.)	–0.2		0.2	µA
			Measured at VC2, (VC2–VC1) = (VC1–GND) = 3.5 V, T_A = 0°C to 60°C (See Figure 4.)			2.5	µA
$V_{MM\_DET\_ON}$	Cell mismatch detection threshold for turning ON		(VC2–VC1) versus (VC1–GND) and vice-versa when cell balancing is enabled. VC2 = VDD = 7.6 V	17	30	45	mV
$V_{MM\_DET\_OFF}$	Cell mismatch detection threshold for turning OFF		Delta between (VC2–VC1) and (VC1–GND) when cell balancing is disabled. VC2 = VDD = 7.6 V	–9	0	9	mV
$V_{CB\_EN\_ON}$	Cell balance enable ON threshold		Active LOW pin at $\overline{CB\_EN}$			1	V
$V_{CB\_EN\_OFF}$	Cell balance enable OFF threshold		Active HIGH at $\overline{CB\_EN}$	2.2			V
I_{CB_EN}	Cell balance enable ON input current		$\overline{CB\_EN}$ = GND (See Figure 5.)			0.2	µA

(1) Specified by design. Not 100% tested in production.

RECOMMENDED CELL BALANCING CONFIGURATIONS

Typical values stated where T_A = 25°C and (VC2–VC1), (VC1–GND) = 3.8 V. Min/Max values stated where T_A = –40°C to 110°C, VDD = 4 V to 10 V, and (VC2–VC1), (VC1–GND) = 3.0 V to 4.2 V. All values assume recommended supply voltage filter resistance R_{VD} of 100 Ω and 5% accurate or better cell balance resistor R_{CB}.

PARAMETER		TEST CONDITION	MIN	NOM	MAX	UNIT
I_{CB}	Cell balance input current	R_{CB} = 4700 Ω	0.5	0.75	1	mA
		R_{CB} = 2200 Ω	1	1.5	2	
		R_{CB} = 910 Ω	2	3	4	
		R_{CB} = 560 Ω	3	4.5	6	
		R_{CB} = 360 Ω	3.5	6	8.5	
		R_{CB} = 240 Ω	4	7.5	11	
		R_{CB} = 120 Ω	5	10	15	

The cell balancing current may be calculated as follows:

Cell 1 (VC1–GND):

$$I_{CB1} = \frac{VC1}{R_{CB}}$$

Cell 2 (VC2–VC1):

$$I_{CB2} = \frac{(VC2 - VC1)}{(R_{CB} + R_{VD})}$$

TYPICAL CHARACTERISTICS

I_{CD} CHARGE CURRENT vs TEMPERATURE

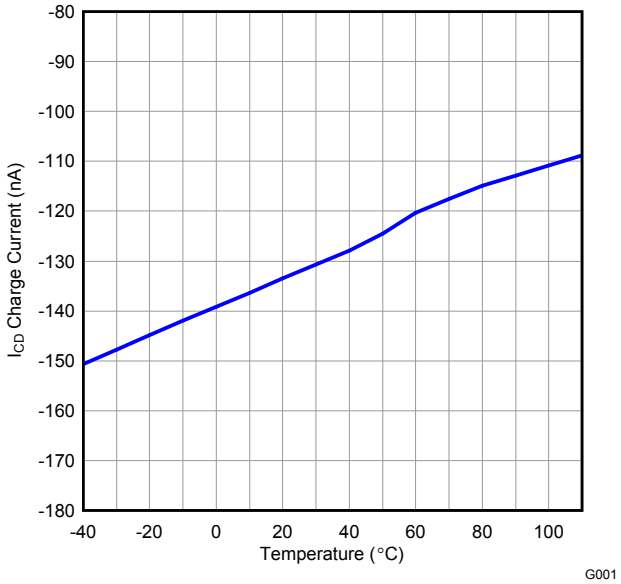


Figure 2. I_{CD} Charge Current

I_{CD} DISCHARGE CURRENT vs TEMPERATURE

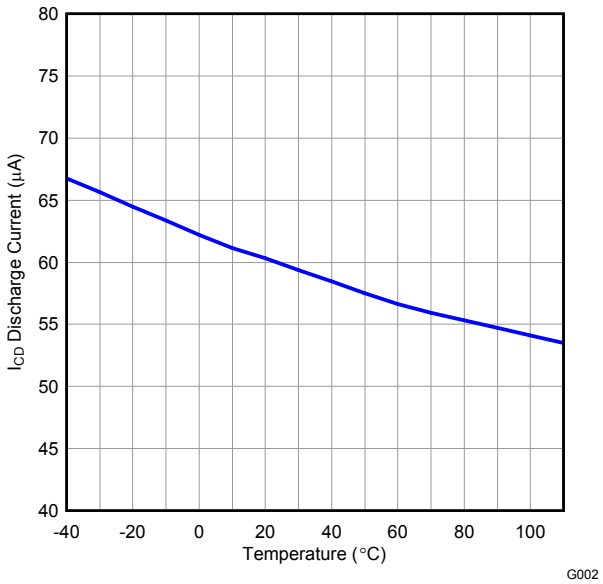


Figure 3. I_{CD} Discharge Current

TEST CONDITIONS

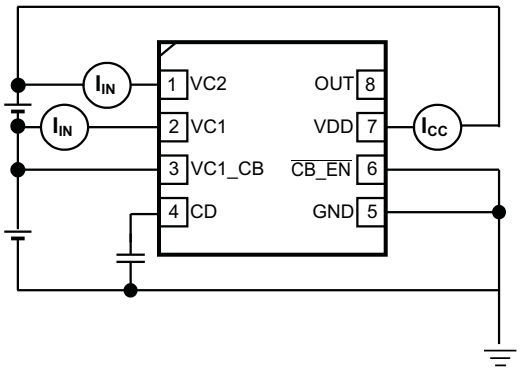


Figure 4. I_{CC}, I_{IN} Measurement

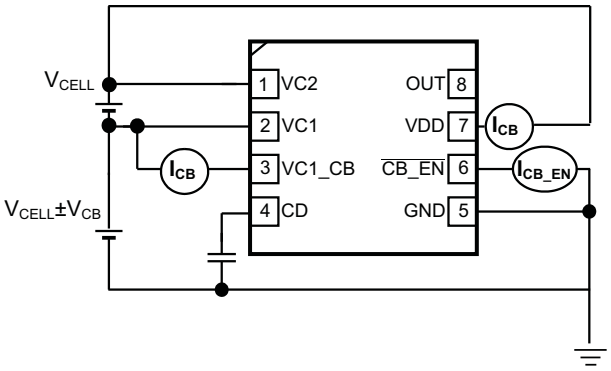


Figure 5. I_{CB} Measurement

PROTECTION (OUT) TIMING

Sizing the external capacitor is based on the desired delay time as follows:

$$C_{CD} = \frac{t_d}{X_{DELAY}}$$

Where t_d is the desired delay time and X_{DELAY} is the overvoltage delay time scale factor, expressed in seconds per microFarad. X_{DELAY} is nominally 9.0 s/µF. For example, if a nominal delay of 3 seconds is desired, use a C_{CD} capacitor that is 3 s / 9.0 s/µF = 0.33 µF.

The delay time is calculated as follows:

$$t_d = C_{CD} \times X_{DELAY}$$

If the cell overvoltage condition is removed before the external capacitor reaches the reference voltage, the internal current source is disabled and an internal discharge block is employed to discharge the external capacitor down to 0 V. In this instance, the OUT pin remains in a low state.

Cell Voltage > $V_{PROTECT}$

When one or both of the cell voltages rises above $V_{PROTECT}$, the internal comparator is tripped, and the delay begins to count to t_d. If the input remains above $V_{PROTECT}$ for the duration of t_d, the bq2920x output changes from a low to a high state, by means of an internal pull-up network, to a regulated voltage of no more than 9.5 V when I_{OH} = 0 mA.

The external delay capacitor should charge up to no more than the internal LDO voltage (approximately 5 V typically), and will fully discharge in approximately under 100 ms when the overvoltage condition is removed.

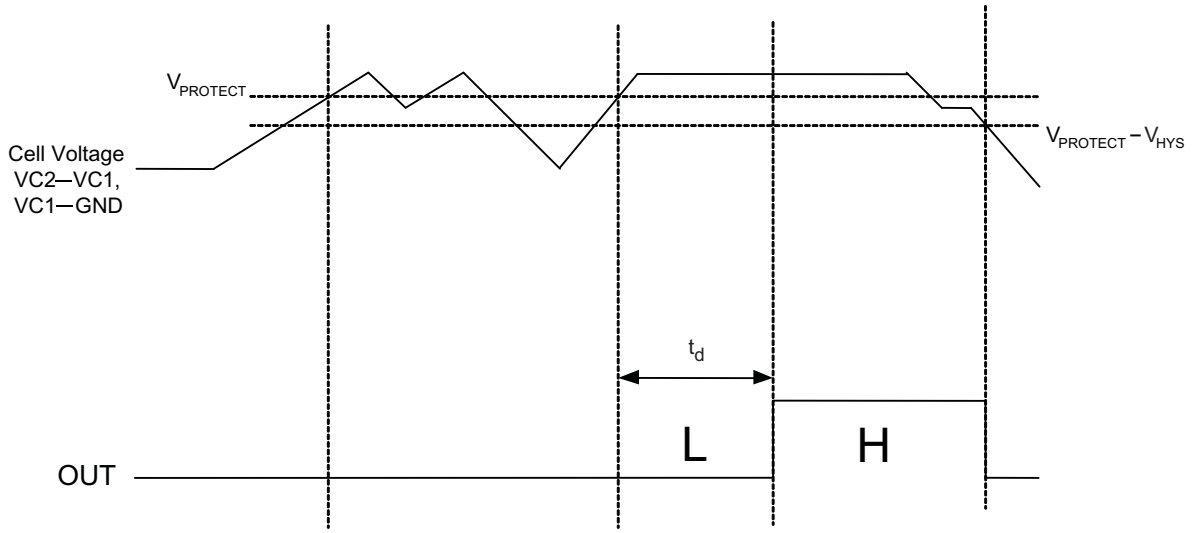


Figure 6. Timing for Overvoltage Sensing

CELL CONNECTION SEQUENCE

NOTE

Before connecting the cells, propagate the overvoltage delay timing capacitor, C_{CD}.

The recommended cell connection sequence begins from the bottom of the stack, as follows:

1. GND
2. VC1
3. VC2

While not advised, connecting the cells in a sequence other than that described above does not result in errant activity on the OUT pin. For example:

1. GND
2. VC2 or VC1
3. Remaining VCx pin

CELL BALANCE ENABLE CONTROL

To avoid prematurely discharging the cells, it is recommended to turn off (pull high) the active-low Cell Balance Enable Control pin at lower State of Charge (SOC) levels.

CELL IMBALANCE AUTO-DETECTION (VIA CELL VOLTAGE)

The $V_{MM\_DET\_ON}$ and $V_{MM\_DET\_OFF}$ specifications are calibrated where VDD = VC2 = 7.6 V and VC1 = 3.8 V. The recommended range of cell balancing is VC2 and VDD between 6.0 V and 8.4 V, and VC1 between 3.0 V and 4.2 V. Below VDD = 6.0 V, it is recommended to pull $\overline{CB\_EN}$ high to disable the cell balancing function.

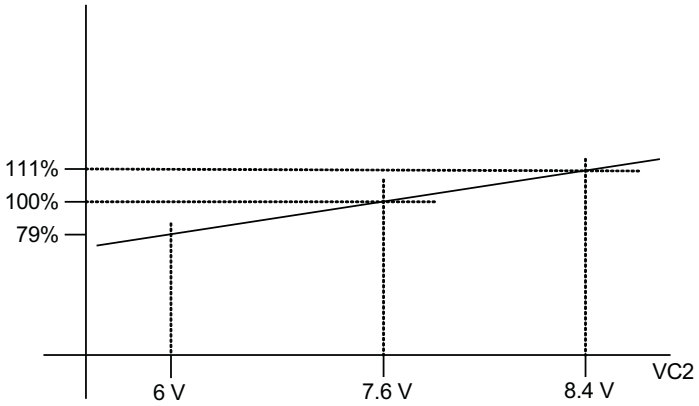


Figure 7. $V_{MM\_DET\_ON}$ and $V_{MM\_DET\_OFF}$ Threshold

BATTERY CONNECTION

Figure 8 shows the configuration for the 2-series cell battery connection.

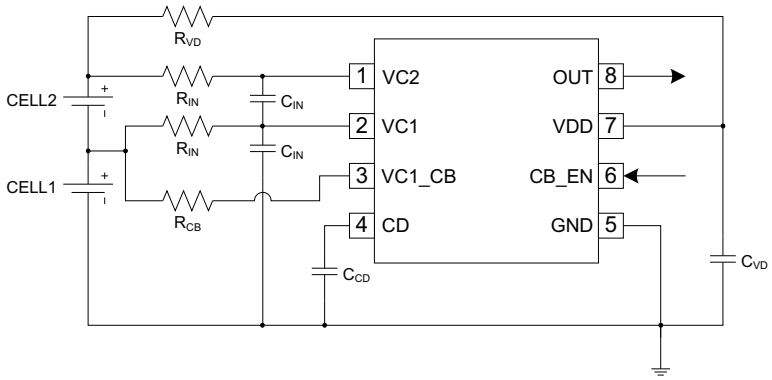


Figure 8. 2-Series Cell Configuration

EXTERNAL CELL BALANCING

Higher cell balancing currents can be supported by means of a simple external network, as shown in Figure 9.

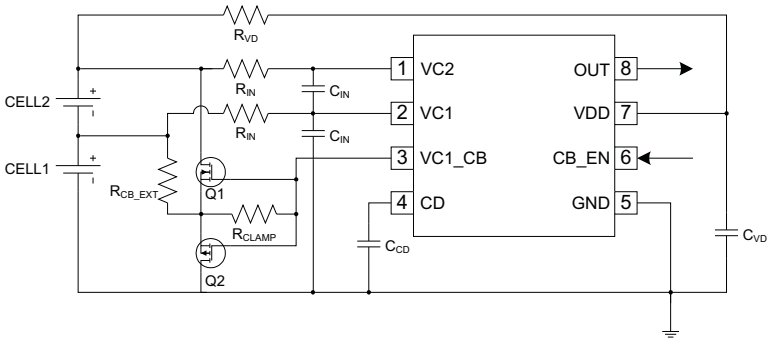


Figure 9. External Cell Balancing Configuration

R_{CLAMP} ensures that both Q1 and Q2 remain off when balancing is disabled, and should be sized above 2 kΩ to prevent excessive internal device current when the balancing network is activated. R_{CB_EXT} determines the value of the balancing current, and is dependent on the voltage of the balanced cell, as follows:

$$I_{bal} = \frac{V_{CELL}}{R_{CB\_EXT}}$$

CUSTOMER TEST MODE

Customer Test Mode (CTM) helps to greatly reduce the overvoltage detection delay time and enable quicker customer production testing. This mode is intended for quick-pass board-level verification tests, and, as such, individual cell overvoltage levels may deviate slightly from the specifications ($V_{PROTECT}$, V_{OA}). If accurate overvoltage thresholds are to be tested, use the standard delay settings that are intended for normal use.

To enter CTM, VDD should be set to approximately 9.5 V higher than VC2. When CTM is entered, the device switches from the normal overvoltage delay time scale factor, X_{DELAY}, to a significantly reduced factor of approximately 0.08, thereby reducing the delay time during an overvoltage condition.

CAUTION

Avoid exceeding any Absolute Maximum Voltages on any pins when placing the part into CTM. Also, avoid exceeding Absolute Maximum Voltages for the individual cell voltages (VC1–GND) and (VC2–VC1). Stressing the pins beyond the rated limits may cause permanent damage to the device.

To exit CTM, power off the device and then power it back on.

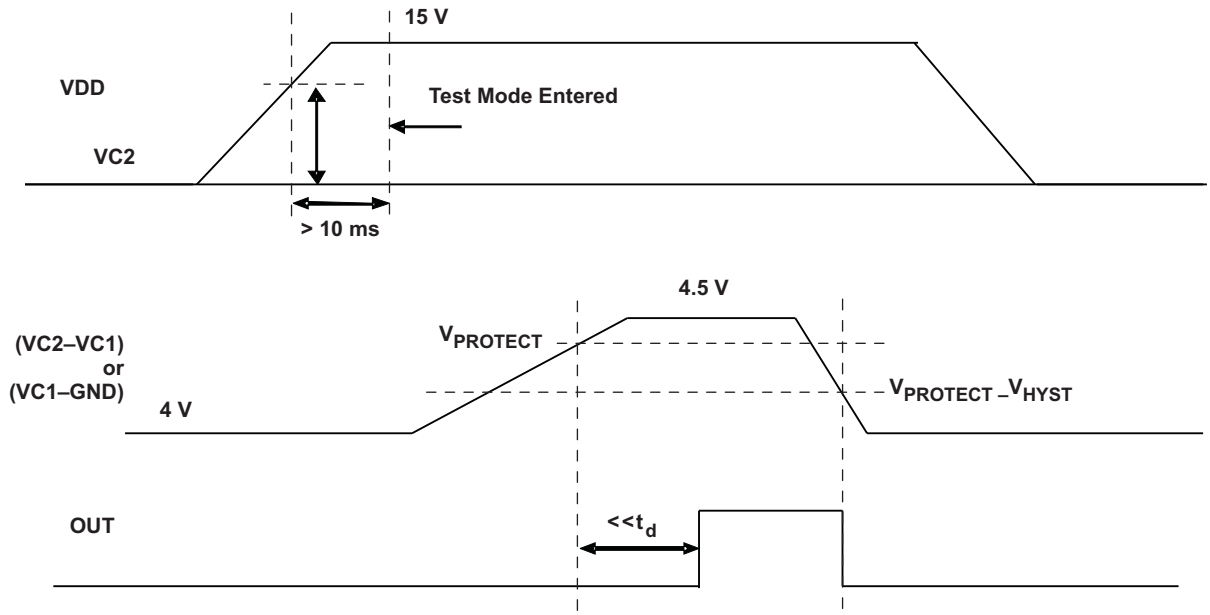


Figure 10. Voltage Test Limits

REVISION HISTORY

Changes from Original (June 2010) to Revision A **Page**

- Changed values in X_{DELAY} and X_{DELAY_CTM} electrical characteristics 4
- Changed specifications for V_{OUT} 4
- Changed test conditions for V_{OUT}, I_{OH}, and I_{OL} 4
- Added $V_{MM\_DET\_ON}$: VC2 = VDD = 7.6 V 4
- Changed $V_{MM\_DET\_OFF}$: From VDD – VC2 – 7.6 V to VC2 = VDD = 7.6 V 4
- Changed content in Recommended Cell Balancing Configurations section 5
- Added I_{CD} Charge Current figure 5
- Added I_{CD} Discharge Current figure 5
- Changed X_{DELAY} from nominally 8.0 s/µF to nominally 9.0 s/µF 6
- Changed Timing for Overvoltage Sensing figure 6
- Added Cell Imbalance Auto-Detection (Via Cell Voltage) section 7
- Added External Cell Balancing section 8
- Changed VDD value in Customer Test Mode from 8.5 V to 9.5 V 9
- Changed the Voltage Test Limits figure 9

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
BQ29200DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	200	Samples
BQ29200DRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	200	Samples
BQ29209DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	209	Samples
BQ29209DRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	209	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

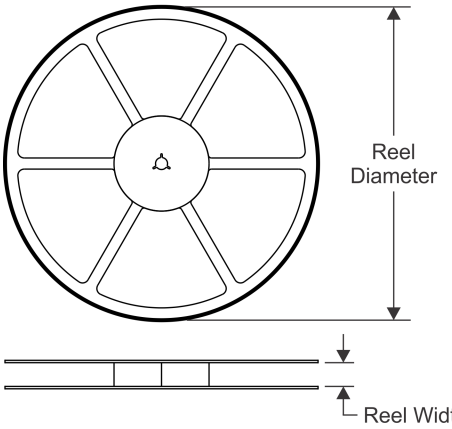
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

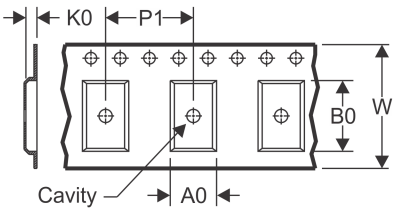
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

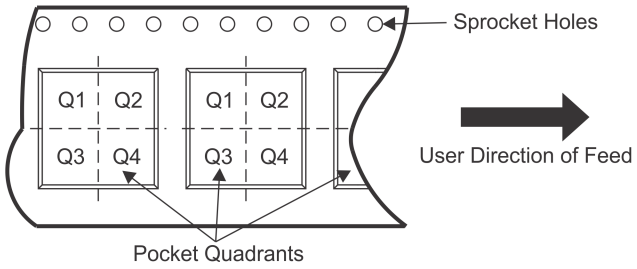


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

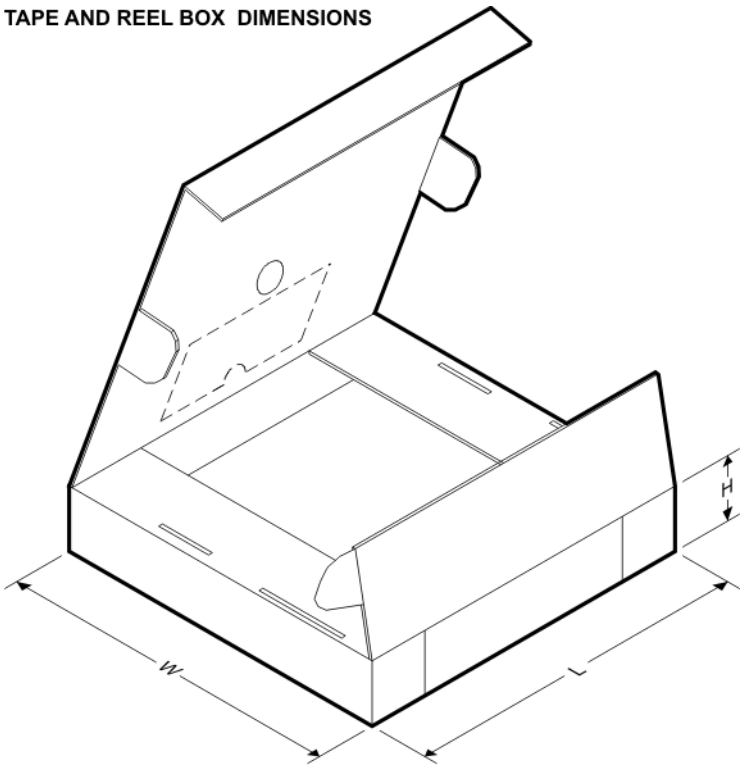
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ29200DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ29200DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ29209DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ29209DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

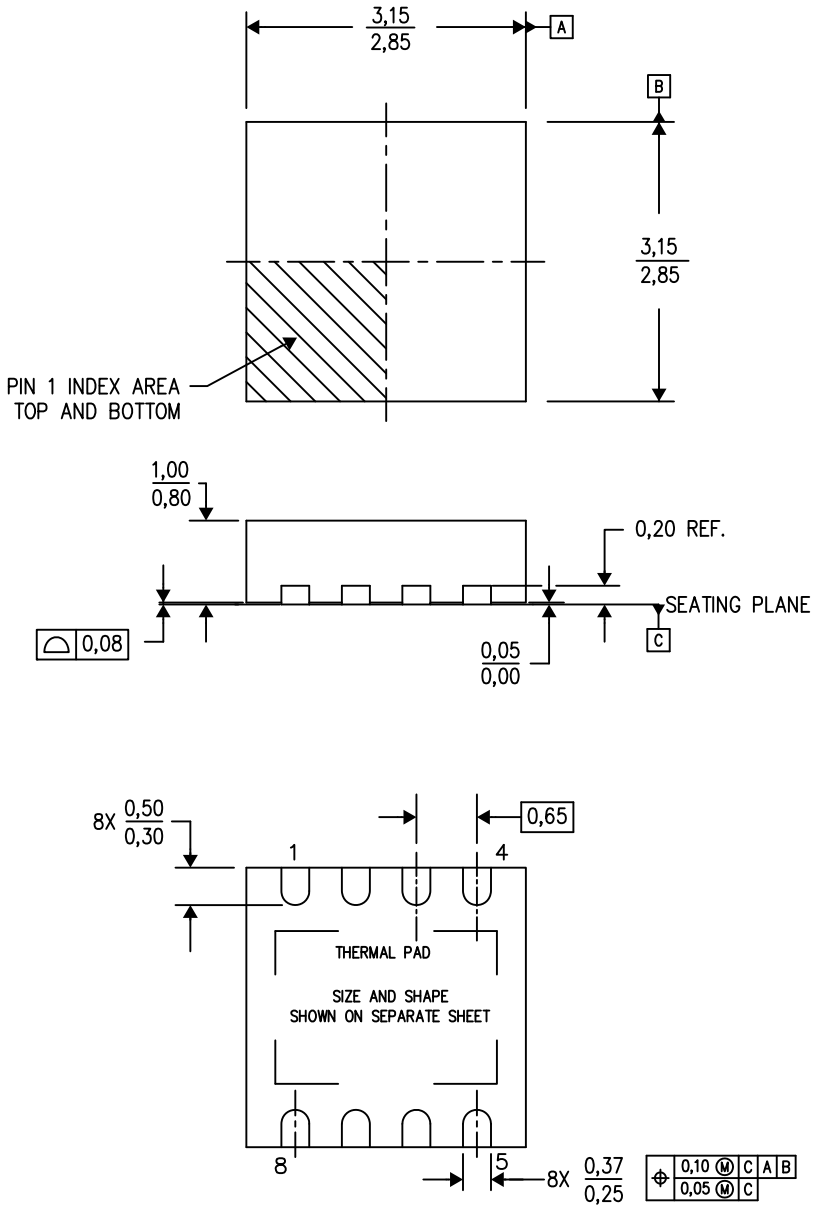
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ29200DRBR	SON	DRB	8	3000	367.0	367.0	35.0
BQ29200DRBT	SON	DRB	8	250	210.0	185.0	35.0
BQ29209DRBR	SON	DRB	8	3000	367.0	367.0	35.0
BQ29209DRBT	SON	DRB	8	250	210.0	185.0	35.0

DRB (S–PVSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



4203482–2/K 06/12

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

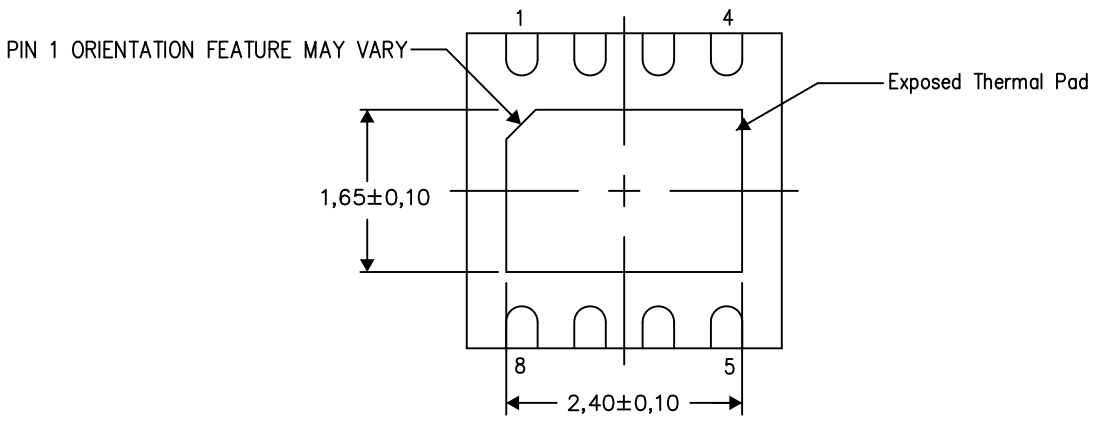
DRB (S–PVSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



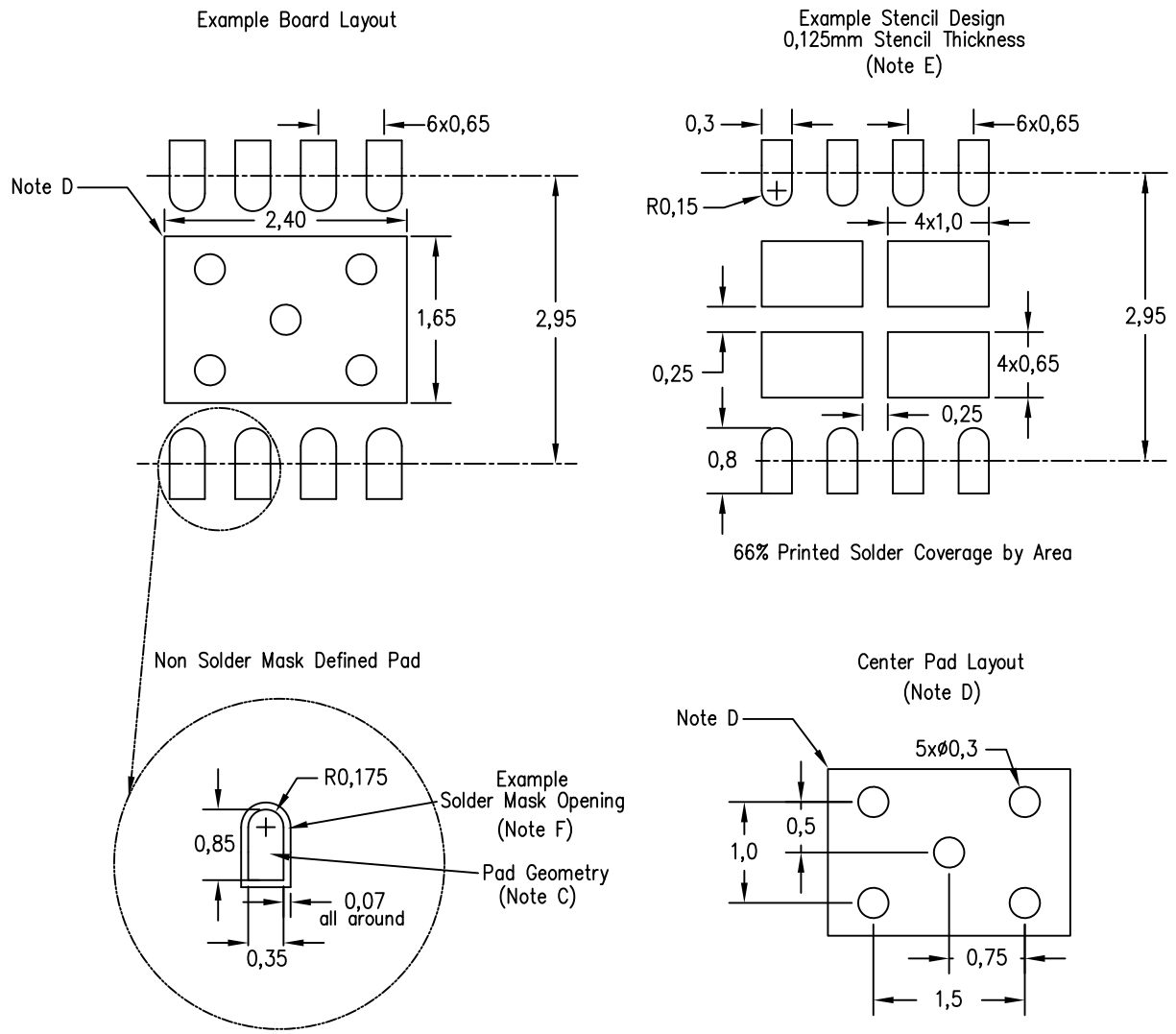
Bottom View

Exposed Thermal Pad Dimensions

4206340–3/N 09/12

NOTE: All linear dimensions are in millimeters

DRB (S–PVSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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