High Performance, Single-Synchronous Step-Down Controller with Differential Voltage Feedback

FEATURES

- **Differential Voltage Feedback**
- **DC Compensation for Accurate Regulation**
- **Wide Input Voltage Range: 3 V to 28 V**
- **Output Voltage Range: 0.5 V to 2.0 V with Fixed Options of 1.05 V and 1.00 V**
- **Wide Output Load Range: 0 A to 20 A+**
- **Adaptive On-Time Modulation with Selectable Control Architecture and Frequency**
  - **D-CAP™ Mode at 300 kHz/400 kHz for Fast Transient Response**
  - **D-CAP2™ Mode at 500 kHz/670 kHz for Ceramic Output Capacitor**
- **4700 ppm/°C, Low-Side $R_{DS(on)}$ Current Sensing**
- **R_{SENSE} Accurate Current Sense Option**
- **Internal, 1-ms Voltage Servo Softstart**
- **Built-In Output Discharge**
- **Power Good Output**
- **Integrated Boost Switch**
- **Built-In OVP/UVP/OCP**
- **Thermal Shutdown (Non-latched)**
- **3 mm × 3 mm, 16-Pin, QFN (RTE) Package**

APPLICATIONS

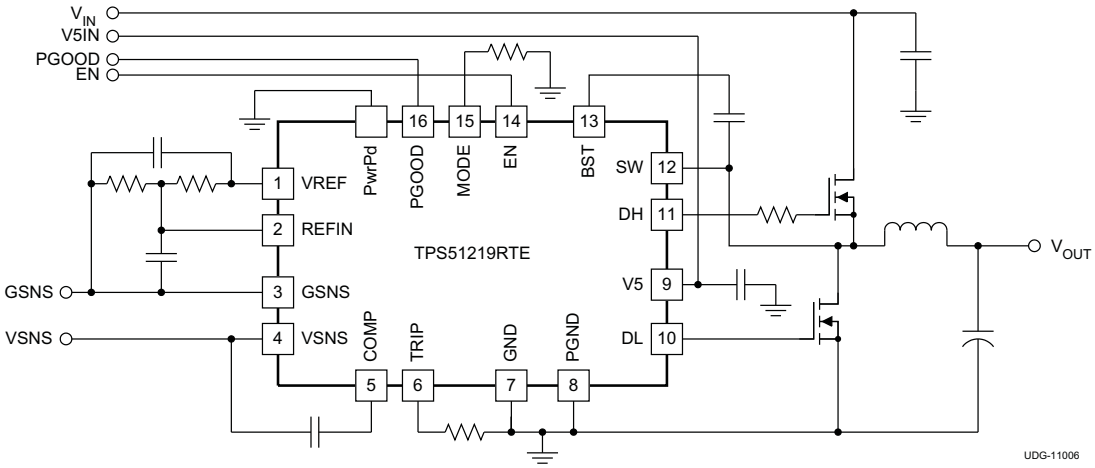
- **Notebook Computers**
- **I/O Supplies**

DESCRIPTION

The TPS51219 is a small-sized single buck controller with adaptive on-time control. It provides a choice of control modes (D-CAP™ or D-CAP2™) to meet a wide range of system requirements. It is designed for tight DC regulation requirements such as the VCCIO application for Intel® notebooks. The performance and flexibility of the TPS51219 makes it suitable for low output voltage, high current, PC system power rails and similar point-of-load (POL) power supplies. Differential voltage feedback and the voltage compensation function combine to provide high precision power to load devices.

A small package, fixed voltage options and minimal external component count saves cost and space, while a dedicated EN pin and pre-set frequency selections minimize design effort. The skip-mode at light load condition, strong gate drivers, and low-side FET $R_{DS(on)}$ current sensing provides high efficiency operation over a broad load range. The external resistor current sense option enables accurate current sensing. The conversion input voltage (the high-side FET drain voltage) ranges from 3 V to 28 V and output voltage ranges from 0.5 V to 2.0 V. The device requires an external 5-V supply.

The TPS51219 is available in a 16-pin, QFN package and is specified for ambient temperature from -40°C to 85°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

D-CAP, D-CAP2 are trademarks of Texas Instruments.
Intel is a registered trademark of Intel.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

T_A	PACKAGE	ORDERABLE DEVICE NUMBER	PINS	OUTPUT SUPPLY	MINIMUM QUANTITY
–40°C to 85°C	Plastic Quad Flat Pack (QFN)	TPS51219RTER	16	Tape and reel	3000
		TPS51219RTET		Mini-reel	250

(1) For the most current package and ordering information see the *Package Option Addendum* at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE		UNIT
		MIN	MAX	
Input voltage range(2)	BST	–0.3	36	V
	BST(3)	–0.3	6	
	SW	–5	30	
	EN, MODE, TRIP, V5	–0.3	6.0	
	COMP, REFIN, VSNS	–0.3	3.6	
	GSNS	–0.35	0.35	
	PGND	–0.3	0.3	
Output voltage range(2)	DH	–5	36	V
	DH(3)	–0.3	6	
	DL	–0.3	6	
	PGOOD	–0.3	6	
	VREF	–0.3	3.6	
Junction temperature range, T_J			125	°C
Storage temperature range, T_{STG}		–55	150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal unless otherwise noted.
(3) Voltage values are with respect to the SW terminal.

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
Supply voltage	V5	4.5		5.5	V
Input voltage range	BST	–0.1		33.5	V
	BST(1)	–0.1		5.5	
	SW	-3		28	
	SW(2)	–4.5		28	
	EN, TRIP, MODE	–0.1		5.5	
	REFIN, VSNS, COMP	–0.1		3.5	
	GSNS	–0.3		0.3	
	PGND	–0.1		0.1	
Output voltage range	DH	–3		33.5	V
	DH(1)	–0.1		5.5	
	DH(2)	–4.5		33.5	
	DL	–0.1		5.5	
	PGOOD	–0.1		5.5	
	VREF	–0.1		3.5	
T_A	Operating free-air temperature	–40		85	°C

(1) Voltage values are with respect to the SW terminal.
(2) This voltage should be applied for less than 30% of the repetitive period.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS51219 RTE 16 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	48.5	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	49.5	
θ_{JB}	Junction-to-board thermal resistance(4)	22.1	
ψ_{JT}	Junction-to-top characterization parameter(5)	0.7	
ψ_{JB}	Junction-to-board characterization parameter(6)	22.1	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	7.1	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range, V_{V5} = 5 V, V_{MODE}= 0 V, V_{EN}= 5 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{V5}	V5 supply current	T_A = 25°C, No load, V_{EN} = 5 V		560		µA
I_{V5SDN}	V5 shutdown current	T_A = 25°C, No load, V_{EN} = 0 V		0.5	2.0	µA
VREF OUTPUT						
V_{VREF}	Output voltage	I_{VREF} = 0 µA wrt GSNS		2.000		V
$V_{VREF(tol)}$	Output voltage tolerance	0 µA ≤ I_{VREF} < 30 µA, T_A = 0°C to 85°C	-0.8%		0.8%	
		0 µA ≤ I_{VREF} < 300 µA, T_A = –40°C to 85°C	-1.2%		1.2%	
$I_{VREF(ocl)}$	Current limit	$V_{VREF-GSNS}$ = 1.7 V	0.4	1.0		mA
OUTPUT VOLTAGE						
V_{VSNS}	VSNS sense voltage	V_{REFIN} = 0 V		1.000		V
		V_{REFIN} = 3.3 V		1.050		V
		0.5 V ≤ V_{REFIN} ≤ 2 V		V_{REFIN}		V
$V_{VSNS(tol)}$	VSNS regulation voltage tolerance	V_{REFIN} = 0 V, 0°C ≤ T_A ≤ 85°C	–9		9	mV
		V_{REFIN} = 0 V, -40°C ≤ T_A ≤ 85°C	-14		14	
		V_{REFIN} = 3.3 V, 0°C ≤ T_A ≤ 85°C	–9		9	
		V_{REFIN} = 3.3 V, -40°C ≤ T_A ≤ 85°C	-14		14	
		V_{REFIN} = 0.5 V and V_{REFIN} = 2.0 V	-5		5	
V_{REFIN1}	REFIN voltage for 1.00-V output				0.3	V
$V_{REFIN1P05}$	REFIN voltage for 1.05-V output		2.2			V
V_{OFF_LPCMP}	Loop comparator offset voltage	V_{REFIN} = 1 V, VSNS shorted to COMP	-5		5	mV
$V_{COMPCLP}$	COMP clamp voltage	V_{REFIN} = 0 V, V_{VSNS} = 0.95 V		0.885		V
		V_{REFIN} = 0 V, V_{VSNS} = 1.05 V		1.115		V
g_M	Error amplifier transconductance	V_{REFIN} = 0 V		130		µS
I_{VSNS}	VSNS input current	V_{VSNS} = 1.05 V	-1		1	µA
I_{REFIN}	REFIN input current	V_{REFIN} = 0 V	–1		1	µA
$I_{VSNS(dis)}$	VSNS discharge current	V_{EN} = 0 V, V_{VSNS} = 0.5 V	5	12		mA
SWITCH MODE POWER SUPPLY (SMPS) FREQUENCY						
f_{SW}	Switching frequency	V_{IN} = 12 V, V_{VSNS} = 1.8 V, V_{MODE} = 2.5 V		400		kHz
		V_{IN} = 12 V, V_{VSNS} = 1.8 V, V_{MODE} = 1.67 V		300		
		V_{IN} = 12 V, V_{VSNS} = 1.8 V, V_{MODE} = 0.2 V		670		
		V_{IN} = 12 V, V_{VSNS} = 1.8 V, V_{MODE} = 0.033 V		500		
$t_{ON(min)}$	Minimum on time	DH rising to falling (1)		60		ns
$t_{OFF(min)}$	Minimum off time	DH falling to rising		320		
MOSFET DRIVERS						
R_{DH}	DH resistance	Source, I_{DH} = –50 mA		1.6	3.0	Ω
		Sink, I_{DH} = 50 mA		0.6	1.5	
R_{DL}	DL resistance	Source, I_{DL} = –50 mA		0.9	2.0	
		Sink, I_{DL} = 50 mA		0.5	1.2	
t_{DEAD}	Dead time	DH-off to DL-on		10		ns
		DL-off to DH-on		20		
INTERNAL BOOT STRAP SWITCH						
V_{FBST}	Forward voltage	V_{V5-BST}, T_A = 25°C, I_F = 10 mA		0.1	0.2	V
I_{BSTLK}	BST leakage current	T_A = 25°C, V_{BST} = 33 V, V_{SW} = 28 V		0.01	1.5	µA

(1) Ensured by design. Not production tested.

ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range, V_{V5} = 5 V, V_{MODE}= 0 V, V_{EN}= 5 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
LOGIC THRESHOLD						
I_{MODE}	MODE source current		15.6	16.7	17.8	µA
V_{THMODE}	MODE threshold voltage	MODE 0-1	113	143	173	mV
		MODE 1-2	253	283	313	
		MODE 2-3	433	458	483	
		MODE 3-4	644	667	690	
		MODE 4-5	914	949	984	
		MODE 5-6	1329	1369	1409	
		MODE 6-7	1950	2000	2050	
V_{LL}	EN low-level voltage				0.5	V
V_{LH}	EN high-level voltage		1.8			
V_{LHYST}	EN hysteresis voltage			0.25		
I_{LLK}	EN input leakage current		–1	0	1	µA
SOFT START						
t_{SS}	Soft-start time	Internal soft-start time		1.1		ms
POWERGOOD COMPARATOR						
V_{THPG}	PGOOD threshold	PGOOD in from higher	106%	108%	110%	
		PGOOD in from lower	90%	92%	94%	
		PGOOD out to higher	114%	116%	118%	
		PGOOD out to lower	82%	84%	86%	
I_{PG}	PGOOD sink current	V_{PGOOD} = 0.5 V	3	6		mA
t_{PGDLY}	PGOOD delay time	Delay for PGOOD in	0.8	1.0	1.2	ms
		Delay for PGOOD out, with 100 mV over drive		0.25		µs
$t_{PGCMPSS}$	PGOOD start-up delay	PGOOD comparator wake-up delay		2.5		ms
$I_{PG(leak)}$	PGOOD leakage current		-1	0	1	µA
CURRENT DETECTION						
I_{TRIP}	TRIP source current	T_A = 25°C, V_{TRIP} = 0.4 V, $R_{DS(on)}$ sensing	9	10	11	µA
TC_{ITRIP} (2)	TRIP source current temperature coefficient (2)	$R_{DS(on)}$ sensing		4700		ppm/°C
V_{TRIP}	V_{TRIP} voltage range	$R_{DS(on)}$ sensing	0.2		3	V
V_{OCL}	Current limit threshold	V_{TRIP} = 3.0 V, $R_{DS(on)}$ sensing	360	375	390	mV
		V_{TRIP} = 1.6 V, $R_{DS(on)}$ sensing	190	200	210	
		V_{TRIP} = 0.2 V, $R_{DS(on)}$ sensing	20	25	30	
V_{OCLN}	Negative current limit threshold	V_{TRIP} = 3.0 V, $R_{DS(on)}$ sensing	–390	–375	–360	mV
		V_{TRIP} = 1.6 V, $R_{DS(on)}$ sensing	–212	–200	–188	
		V_{TRIP} = 0.2 V, $R_{DS(on)}$ sensing	–30	–25	–20	
V_{RTRIP}	Resistor sense trip voltage	Resistor sensing		25		mV
V_{ZC}	Zero cross detection offset			0		mV

(2) Ensured by design. Not production tested.

ELECTRICAL CHARACTERISTICS (continued)

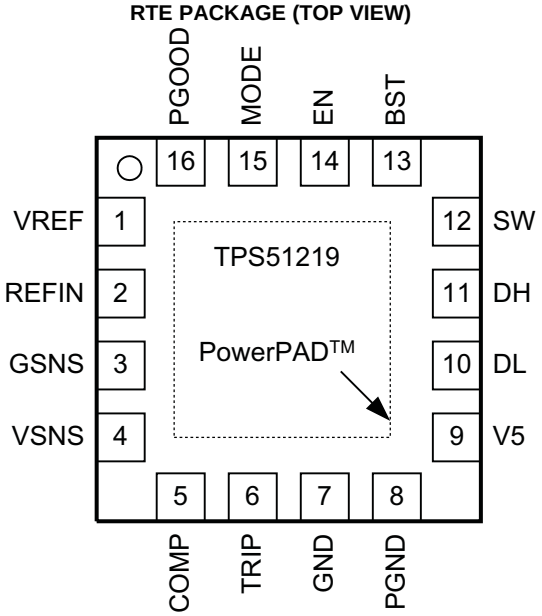
over operating free-air temperature range, V_{V5} = 5 V, V_{MODE}= 0 V, V_{EN}= 5 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
PROTECTIONS						
V_{UVLO}	V5 UVLO threshold voltage	Wake-up	4.2	4.4	4.5	V
		Shutdown	3.7	3.9	4.1	
V_{OVP}	OVP threshold voltage	OVP detect voltage	118%	120%	122%	
t_{OVPDLY}	OVP propagation delay	With 100 mV over drive		370		ns
V_{UVP}	UVP threshold voltage	UVP detect voltage	66%	68%	70%	
t_{UVPDLY}	UVP delay			1		ms
$t_{UVPENDLY}$	UVP enable delay			1.4		ms
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown threshold	Shutdown temperature(3)		140		°C
		Hysteresis(3)		10		

(3) Ensured by design. Not production tested.

DEVICE INFORMATION

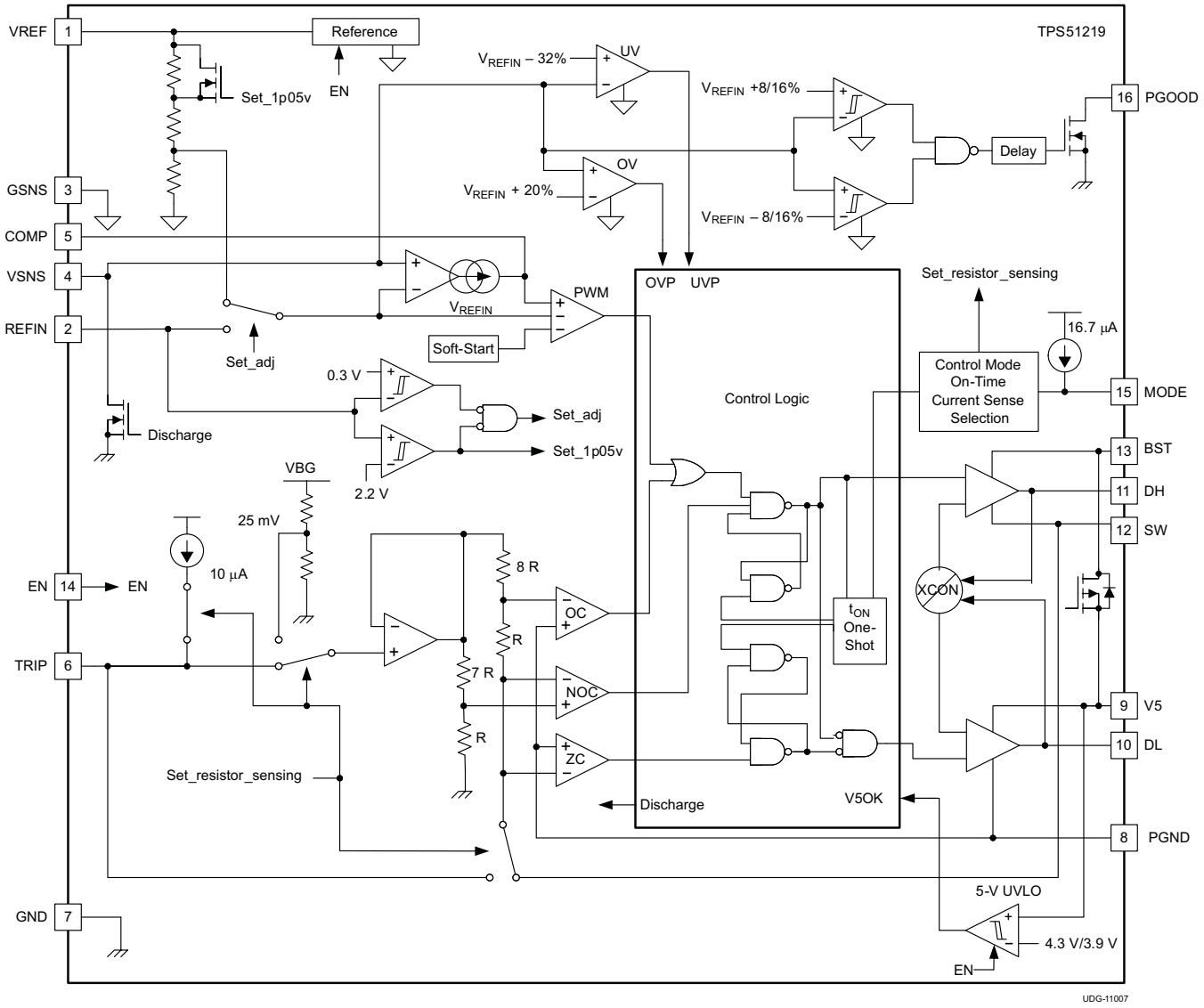
RTE PACKAGE (TOP VIEW)



PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
BST	13	I	High-side MOSFET gate driver bootstrap voltage input. Connect a capacitor from the BST pin to the SW pin.
COMP	5	I	Connection for the DC compensation integrator for improved load-line performance. Connect a capacitor from this pin to the VSNS pin (when operating in D-CAP2 mode), or to the positive terminal of the output capacitor (when operating in D-CAP mode). Connect directly to the VSNS pin without capacitor to disable the integrator function.
DH	11	O	High-side MOSFET gate driver output.
DL	10	O	Low-side MOSFET gate driver output.
EN	14	I	Enable pin. 3.3-V I/O level, 100 ns de-bounce. Short to GND to disable the device.
GND	7	–	Device analog ground; Connect to a quiet point on the system GND plane
GSNS	3	I	Voltage sense return tied directly to the GND sense point of the load. Short to GND if remote sense is not used.
MODE	15	I	Connect a resistor to GND to configure switching frequency, control mode and current sense scheme. (See Table 2)
PGND	8	–	Synchronous low-side MOSFET gate driver return. Also serve as the current sensing input (+). Connect to the GND pin as close as possible to the device.
PGOOD	16	O	Powergood signal open drain output. PGOOD goes high when the output voltage is within the target range.
REFIN	2	I	Output voltage setting pin. See the VREF and REFIN, Output Voltage section.
SW	12	I/O	High-side MOSFET gate driver return. $R_{DS(on)}$ current sensing input (–) when using $R_{DS(on)}$ current sensing.
TRIP	6	I	Current sense comparator input (-) for resistor current sensing. Or overcurrent threshold setting pin for $R_{DS(on)}$ current sensing if connected to GND through an OCL setting resistor. For $R_{DS(on)}$ current sensing operation, 10 µA at room temperature, T_C=4700ppm/°C, is sourced to set the trip voltage.
VSNS	4	I	Voltage sense line tied directly to the load voltage sense point.
VREF	1	O	2.0-V ±0.8% voltage reference output.
V5	9	I	5V power supply input for internal circuits and MOSFET gate drivers.
Thermal pad	–	–	Thermal pad. Connect directly to system GND plane with multiple vias.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

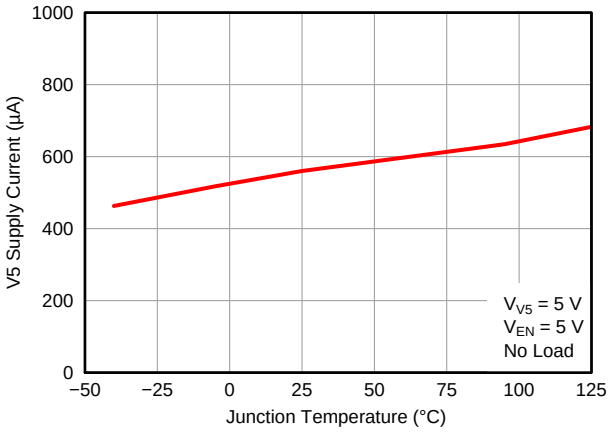


Figure 1. V5 Supply Current vs Junction Temperature

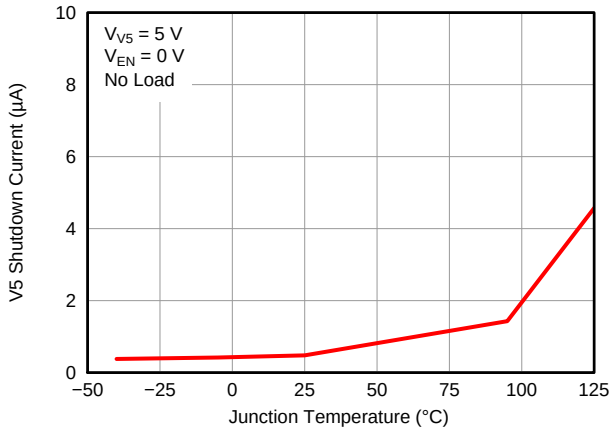


Figure 2. V5 Shutdown Current vs Junction Temperature

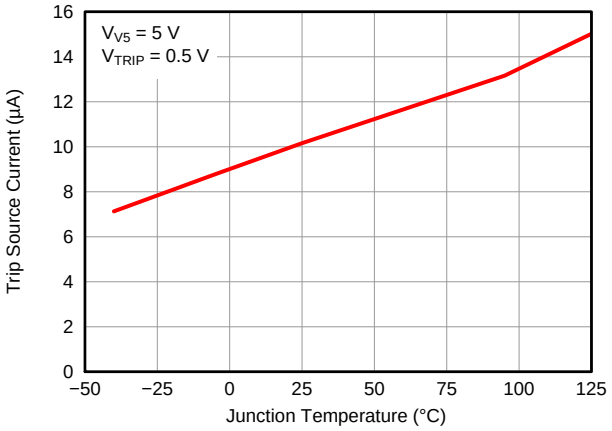


Figure 3. Current Sense Current vs Junction Temperature

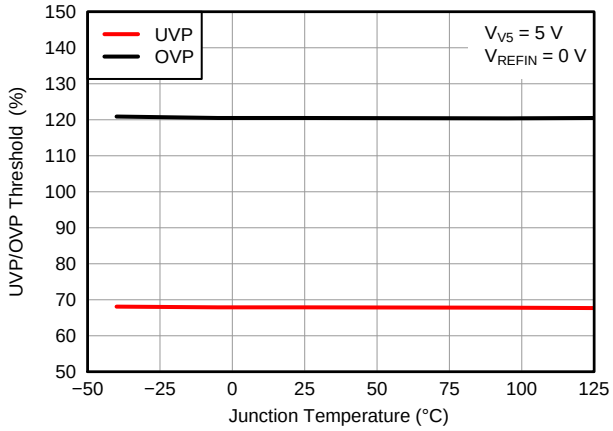


Figure 4. OVP/UVP Threshold vs Junction Temperature

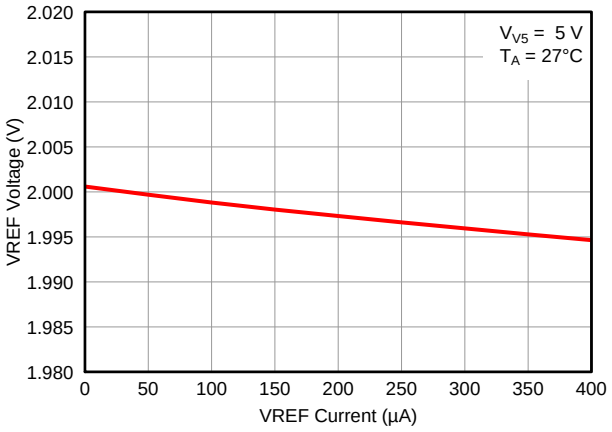


Figure 5. VREF Load Regulation

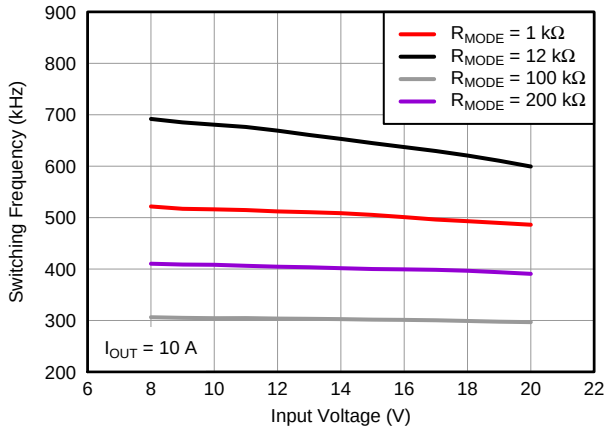


Figure 6. Switching Frequency vs Input Voltage

TYPICAL CHARACTERISTICS

Figure 11 and Figure 12 refer to the application schematic in Figure 33.

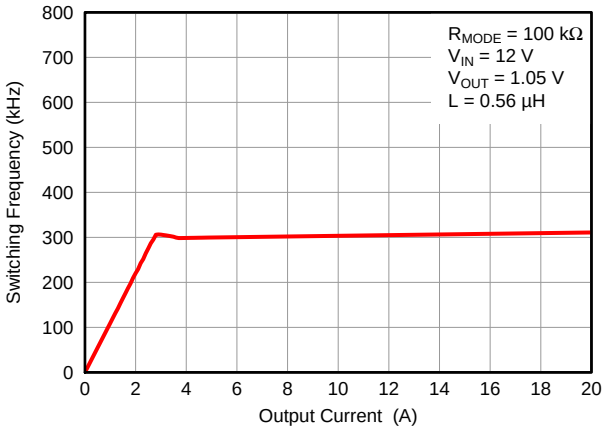


Figure 7. Switching Frequency vs Load Current

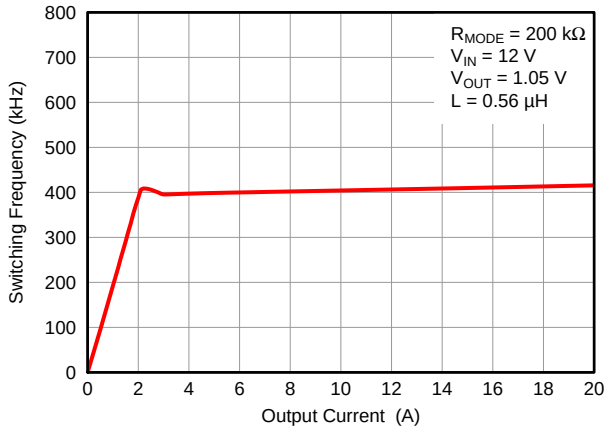


Figure 8. Switching Frequency vs Load Current

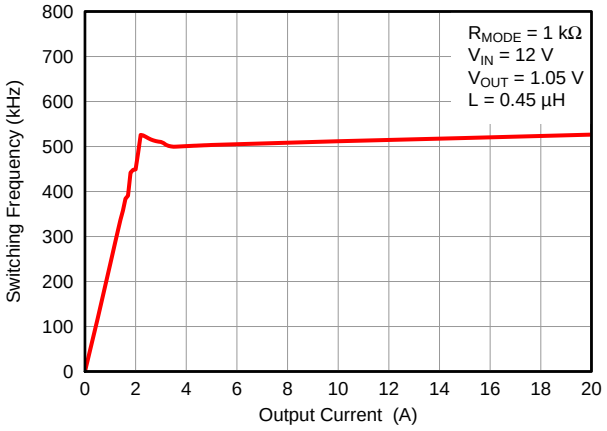


Figure 9. Switching Frequency vs Load Current

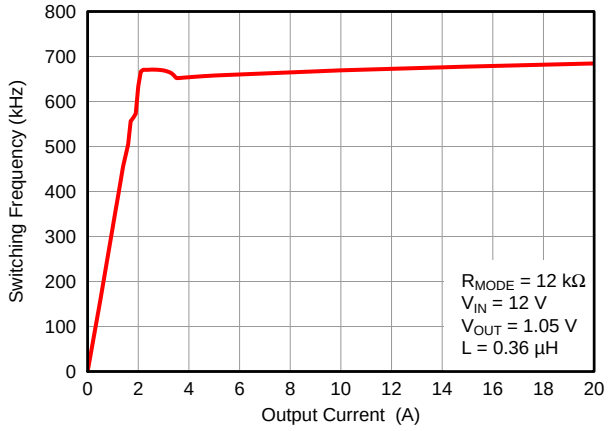


Figure 10. Switching Frequency vs Load Current

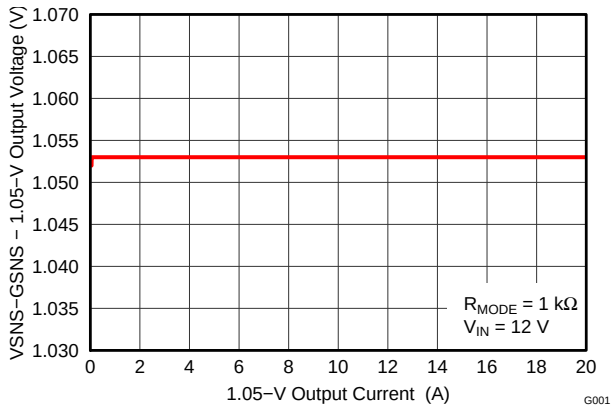


Figure 11. 1.05-V Output Load Regulation

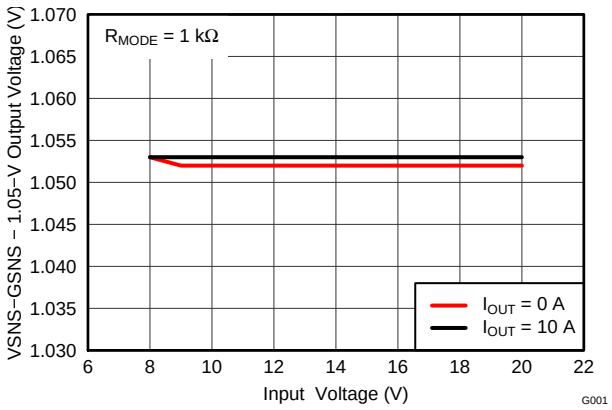


Figure 12. 1.05-V Output Line Regulation

TYPICAL CHARACTERISTICS

Figure 11, Figure 12, and Figure 13 refer to the application schematic in Figure 33.
Figure 14, Figure 15 and Figure 16, refer to the application schematic in Figure 33 except the parameters of L1 (0.56 µH), C7 (2 × 330 µF) and Q3 (not used).

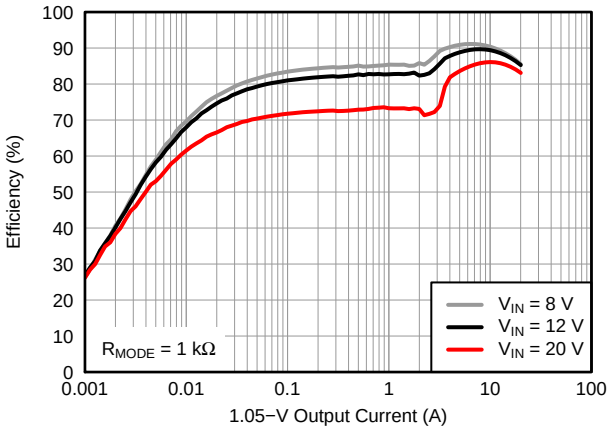


Figure 13. 1.05-V Output Efficiency

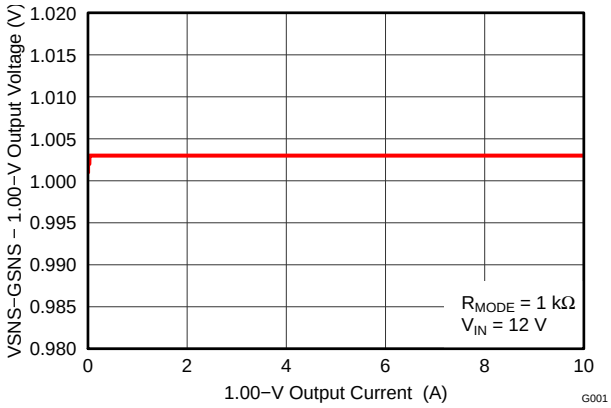


Figure 14. 1.00-V Output Load Regulation

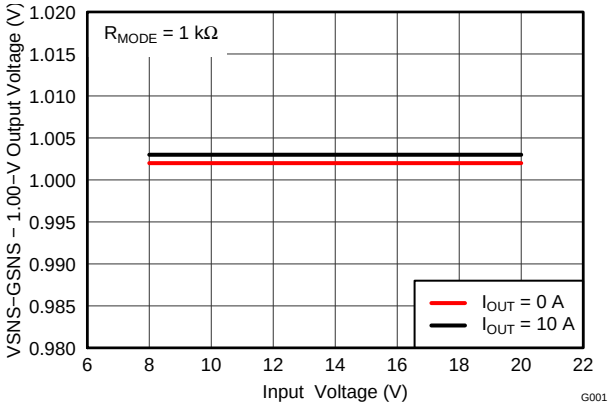


Figure 15. 1.00-V Output Line Regulation

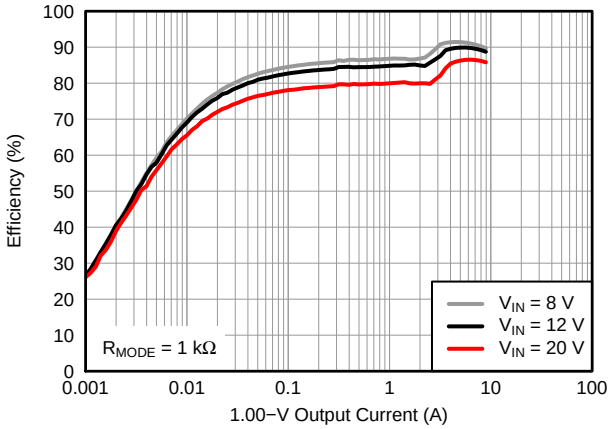


Figure 16. 1.00-V Output Efficiency

TYPICAL CHARACTERISTICS

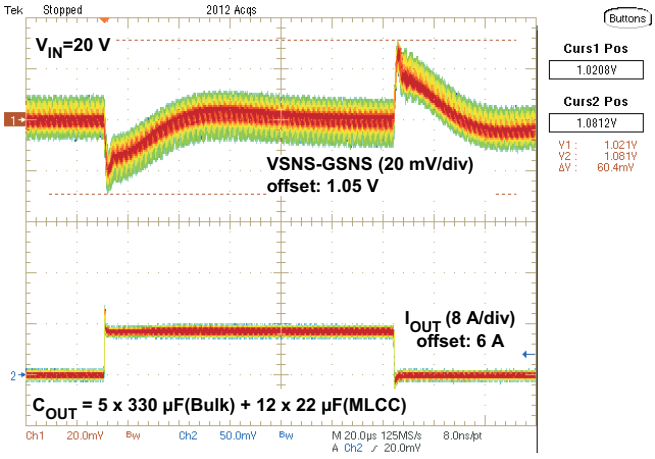


Figure 17. 1.05-V Load Transient Response

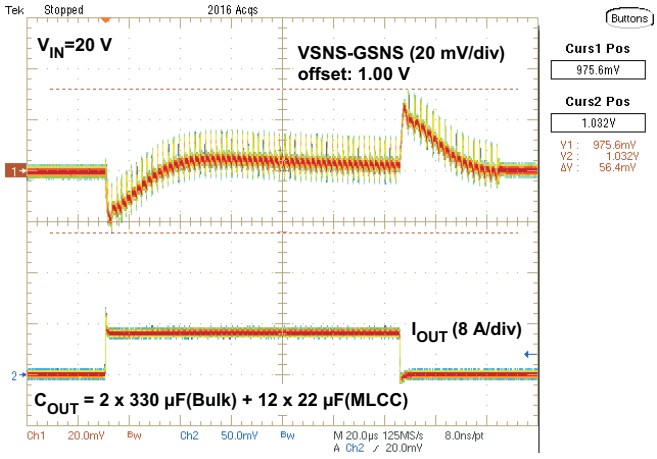
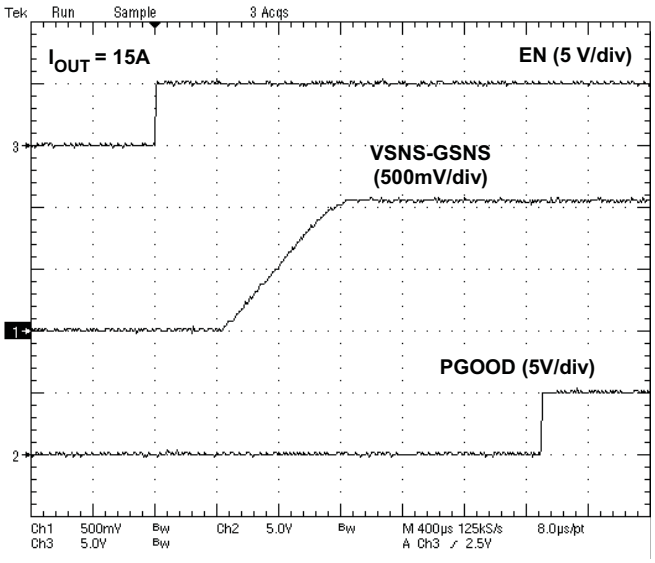
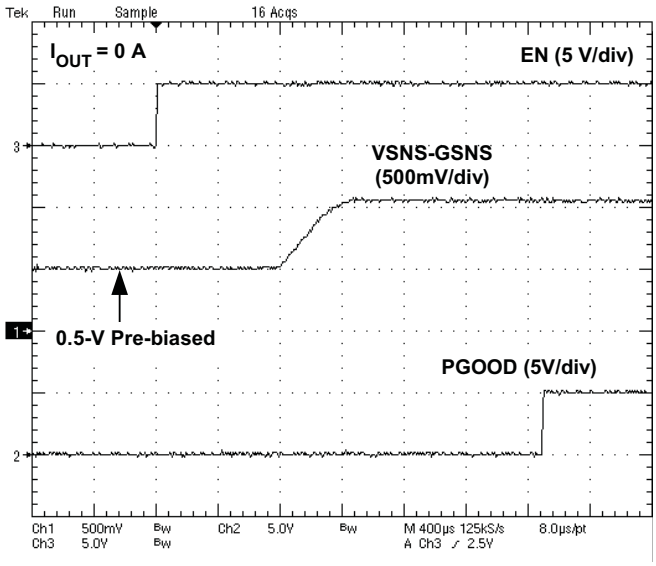


Figure 18. 1.00-V Load Transient Response



Time (400 µs/div)

Figure 19. 1.05-V Startup Waveforms

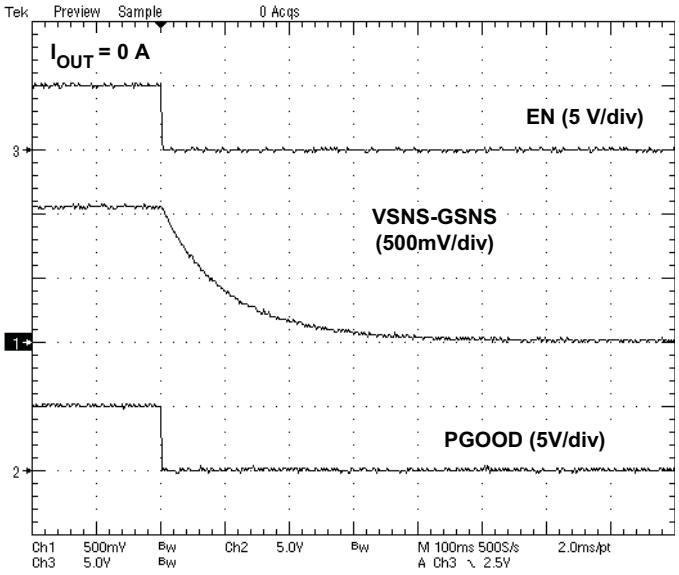


Time (400 µs/div)

Figure 20. 1.05-V Startup Waveforms (0.5-V Pre-Biased)

TYPICAL CHARACTERISTICS

Figure 22 refers to application schematic of Figure 33.



Time (100 ms/div)

Figure 21. 1.05-V Soft-stop Waveforms

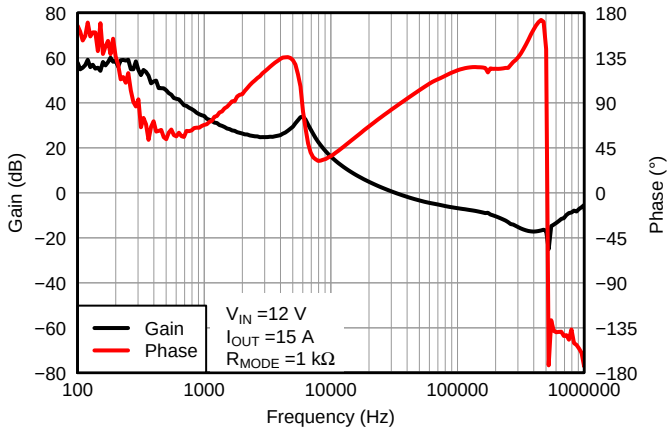


Figure 22. Bode Plot, V_{OUT}=1.05 V

APPLICATION INFORMATION

Swtich Mode Power Supply Control

The TPS51219 is a high performance, single-synchronous step-down controller with differential voltage feedback. The TPS51219 realizes accurate regulation at the specific load point over wide load range with the combination of three functions.

- **2-V Reference with 0.8% Tolerance**. Internal voltage divider provides precise reference (See Table 1 in the VREF and REFIN, Output Voltage section). A value of 0.1µF is recommended as the decoupling capacitance between VREF and GSNS pins.
- **Integrator**. Feedback capacitance connected from the output (COMP pin) to the input (VSNS pin) of the error amplifier comprises integrator, which increases gain at DC to low frequency region and improves load regulation of the output voltage. 10nF is recommended as the capacitance between VSNS and COMP pins.
- **Differential remote sensing**. Differential feedback provides precise output voltage control at the point of load. Connect VSNS and GSNS directly to output voltage sense point and ground return point at the load device, respectively. Short GSNS to GND if remote sense is not used.

The TPS51219 supports two control architectures, D-CAP™ mode and D-CAP2™ mode. Both control modes do not require complex external compensation networks and are suitable for designs with small external components counts. The D-CAP™ mode provides fast transient response with appropriate amount of equivalent series resistance (ESR) on the output capacitors. The D-CAP2™ mode is dedicated for a configuration with very low ESR output capacitors such as multi-layer ceramic capacitors (MLCC). For the both modes, an adaptive on-time control scheme is used to achieve pseudo-constant frequency. The TPS51219 adjusts the on-time (t_{ON}) to be inversely proportional to the input voltage (V_{IN}) and proportional to the SMPS output voltage (V_{OUT}). The switching frequency remains nearly constant over the variation of input voltage at the steady-state condition. Control modes and switching frequency are selected by the MODE pin described in Table 2.

VREF and REFIN, Output Voltage

The device provides a 2.0-V, ±0.8% accurate, voltage reference from VREF. This output has a 300-µA current capability to drive the REFIN input voltage through a voltage divider circuit. A capacitor with a value of 0.1-µF or larger should be attached close to the VREF terminal.

The SMPS output voltage is defined by REFIN voltage, within the range between 0.5 V and 2.0 V, programmed by the resister-divider connected between VREF and GSNS. (See Figure 23 and External Components Selection section.) A few nano-farads of capacitance from REFIN to GSNS is recommended for stable operation. A voltage divider and a filter capacitor to this pin should be referenced to GSNS. Fixed output voltage can be set as shown in Table 1.

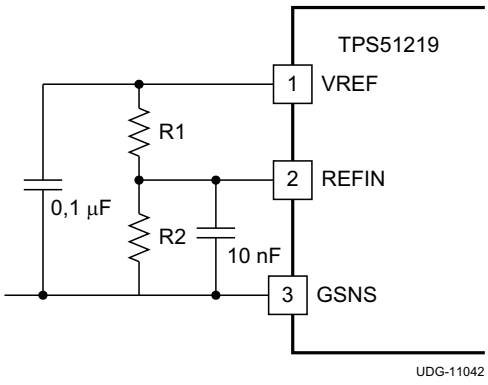


Figure 23. Voltage Reference Connections

Table 1. Output Voltage Selection

REFIN VOLTAGE (V)	OUTPUT VOLTAGE (V)
3.3	1.05
GSNS	1.00
Resistor Divider	Adjustable

Soft-Start and Powergood

Provide a voltage supply to VIN and V5 before asserting EN to high. TPS51219 provides integrated soft-start functions to suppress in-rush current at start-up. The soft-start is achieved by controlling internal reference voltage ramping up. Figure 24 shows the start-up waveforms. The switching regulator waits for 400µs after EN assertion. The MODE pin voltage is read in this period. A typical V_{OUT} ramp up duration is 700 µs.

THe TPS51219 has a powergood open-drain output that indicates the V_{OUT} voltage is within the target range. The target voltage window and transition delay times of the PGOOD comparator are ±8% (typ) and 1-ms delay for assertion (low to high), and ±16% (typ) and 2-µs delay for de-assertion (high to low) during running. The PGOOD start-up delay is 2.5 ms after EN is asserted to high. The time constant, which is composed of the REFIN capacitor and a resistor divider, needs to be short enough to reach the target value before PGOOD comparator enabled.

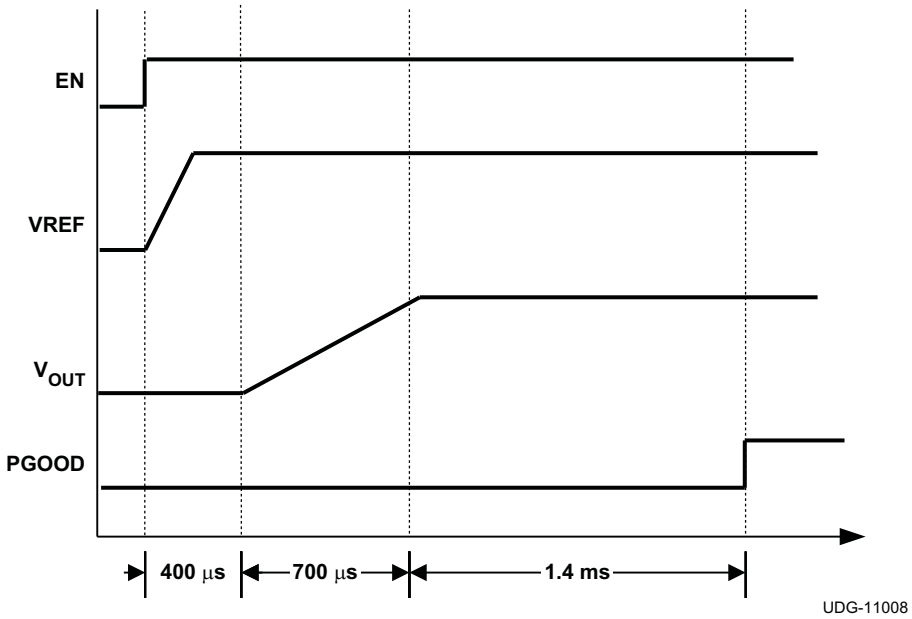


Figure 24. Typical Start-up Waveforms

MODE Pin Configuration

The TPS51219 reads the MODE pin voltage when the EN signal is raised high and stores the status in a register. A 16.7-µA current is sourced from the MODE pin during this time to read the voltage across the resistor connected between the pin and GND. Table 2 shows resistor values, corresponding control mode, switching frequency and current sense operation configurations.

Table 2. MODE Selection

MODE NO.	RESISTANCE BETWEEN MODE AND GND (kΩ)	CONTROL MODE	SWITCHING FREQUENCY (kHz)	CURRENT SENSE OPERATION
7	200	D-CAP™	400	$R_{DS(on)}$
6	100		300	
5	68		300	Resistor
4	47		400	
3	33	D-CAP2™	500	Resistor
2	22		670	
1	12		670	$R_{DS(on)}$
0	1		500	

D-CAP™ Mode

Figure 25 shows a simplified model of D-CAP™ mode architecture in the TPS51219.

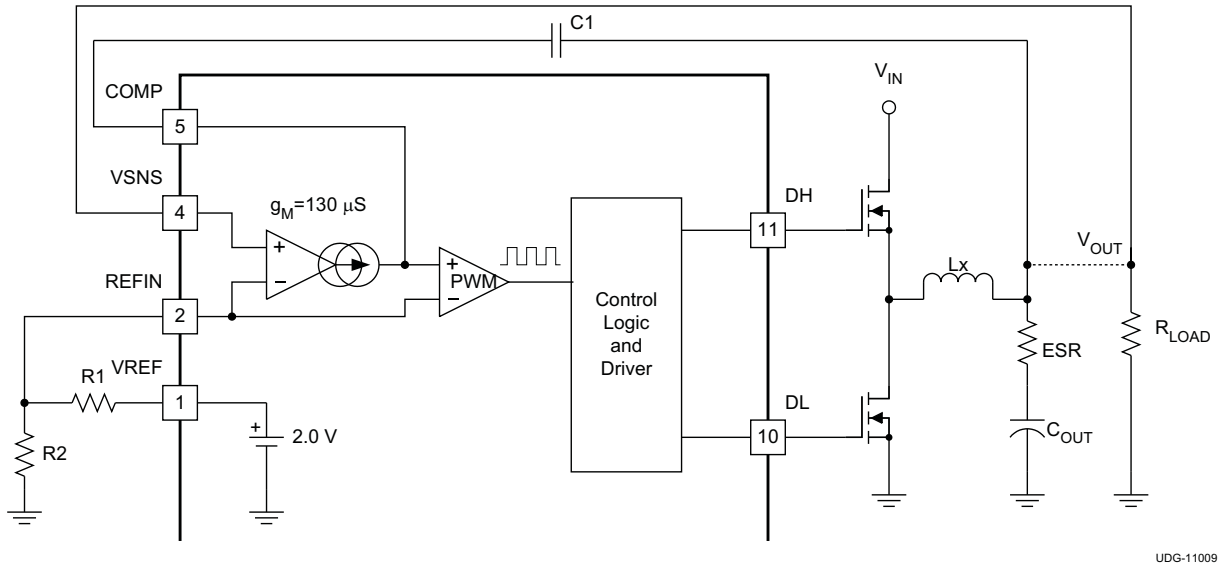


Figure 25. Simplified D-CAP™ Model

The transconductance amplifier and the capacitance C1 configure an integrator. The VSNS voltage is compared with REFIN voltage. Ripple voltage generated by ESR of the output capacitance is fed back through the C1 so that C1 should be properly connected to the positive terminal of output capacitor, not at the remote point of load. The PWM comparator creates a set signal to turn on the high-side MOSFET each cycle. The D-CAP™ mode offers flexibility on output inductance and capacitance selections with ease-of-use without complex feedback loop calculation and external components. However, it does require sufficient amount of ESR that represents inductor current information for stable operation and good jitter performance. Organic semiconductor capacitor(s) or specialty polymer capacitor(s) are recommended.

The requirement for loop stability is simple and is described in Equation 1. The 0-dB frequency, f_0, is recommended to be lower than 1/3 of the switching frequency to secure proper phase margin. The integrator time constant should be long enough compared to f_0, for example one decade low, as described in Equation 2.

$$f_0 = \frac{1}{2\pi \times ESR \times C_{OUT}} \leq \frac{f_{SW}}{3} \quad (1)$$

where

- ESR is the effective series resistance of the output capacitor
- C_{OUT} is the capacitance of the output capacitor
- f_{SW} is the switching frequency

$$\frac{g_M}{2\pi \times C1} \leq \frac{f_0}{10} \quad (2)$$

where

- g_M is transconductance of the error amplifier (typically 130 µS)

Jitter is another attribute caused by signal-to-noise ratio of the feedback signal. One of the major factors that determine jitter performance in D-CAP™ mode is the down-slope angle of the VSNS ripple voltage. Figure 26 shows, in the same noise condition, that jitter is improved by making the slope angle larger.

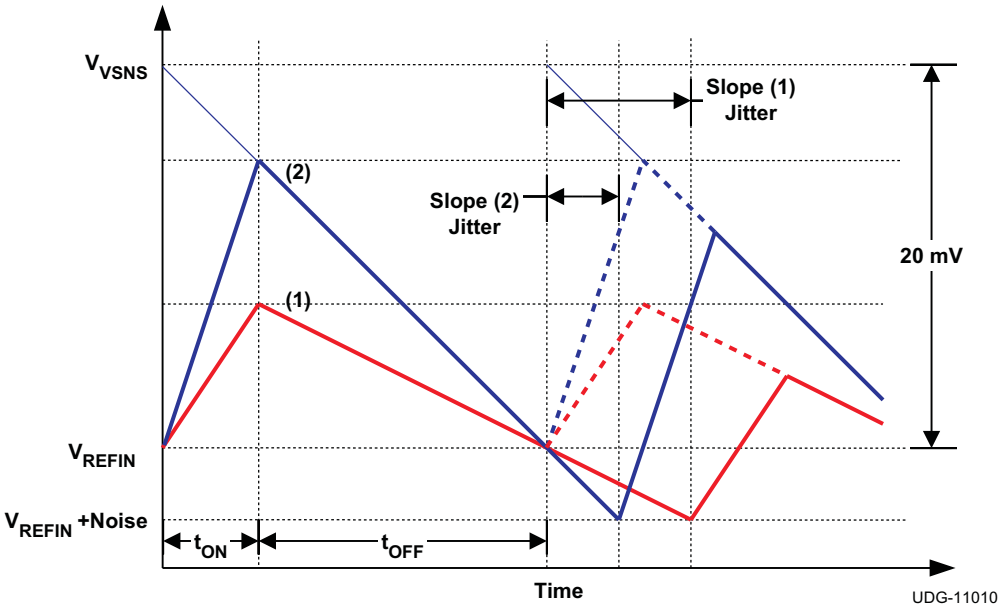


Figure 26. Ripple Voltage Slope and Jitter Performance

For a good jitter performance, use the recommended down slope of approximately 20 mV per switching period as shown in Figure 26 and Equation 3.

$$\frac{V_{OUT} \times ESR}{f_{SW} \times L_X} \geq 20\,mV \quad (3)$$

where

- V_{OUT} is the SMPS output voltage
- L_X is the inductance

D-CAP2™ Mode Operation

Figure 27 shows simplified model of D-CAP2™ architecture.

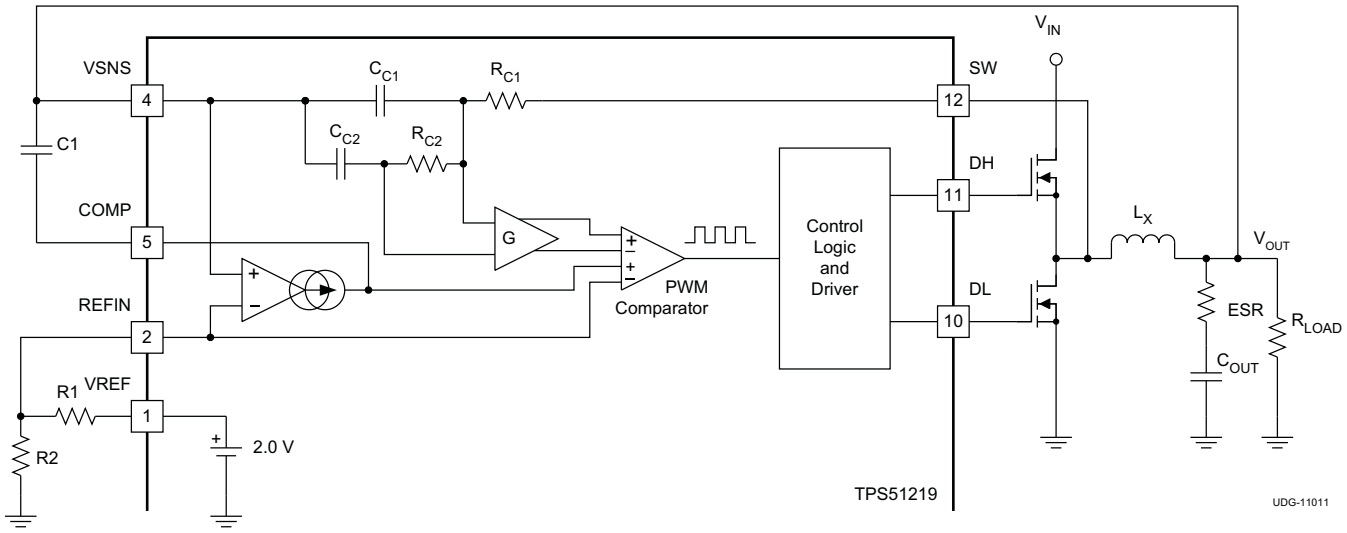


Figure 27. Simplified Modulator Using D-CAP2™ Mode

When the TPS51219 operates in D-CAP2™ mode, connect the COMP and VSNS pins as shown in Figure 27. The transconductance amplifier and the capacitance C1 configures the integrator. The D-CAP2™ mode in the TPS51219 includes an internal feedback network enabling the use of very low ESR output capacitor(s) such as multi-layer ceramic capacitors (MLCC). The role of the internal network is to sense the ripple component of the inductor current information and then combine it with the voltage feedback signal.

Using $R_{C1}=R_{C2}\equiv R_C$ and $C_{C1}=C_{C2}\equiv C_C$, 0-dB frequency of the D-CAP2™ mode is given by Equation 4. f_0 is recommended to be lower than 1/3 of the switching frequency to secure proper phase margin. The integrator time constant should be long enough compared to f_0, for example one decade low, as described in Equation 5.

$$f_0 = \frac{R_C \times C_C}{2\pi \times G \times L_X \times C_{OUT}} \le \frac{f_{SW}}{3} \quad (4)$$

where

- G is gain of the amplifier which amplifies the ripple current information generated by the compensation circuit

$$\frac{g_M}{2\pi \times C1} \le \frac{f_0}{10} \quad (5)$$

The typical G value is 0.25, and typical $R_C C_C$ time constant values for 500 kHz and 670 kHz operation are 32 µs and 23 µs, respectively.

For example, when f_{SW} = 500 kHz and L_X=0.45 µH, C_{OUT} should be larger than 272 µF. At the selection of capacitor, pay attention to its characteristics. For MLCC use X5R or better dielectric and take into account derating of the capacitance by both DC bias and AC bias. When derating by DC bias and AC bias are 80% and 50%, respectively, the effective derating is 40% because 0.8 x 0.5 = 0.4. The capacitance of specialty polymer capacitors may change depending on the operating frequency. Consult capacitor manufacturers for specific characteristics.

Light-Load Operation

In auto-skip mode, the TPS51219 SMPS control logic automatically reduces its switching frequency to improve light-load efficiency. To achieve this intelligence, a zero cross detection comparator is used to prevent negative inductor current by turning off the low-side MOSFET. Equation 6 shows the boundary load condition of this skip mode and continuous conduction operation.

$$I_{LOAD(LL)} = \frac{(V_{IN} - V_{OUT})}{2 \times L_X} \times \frac{V_{OUT}}{V_{IN}} \times \frac{1}{f_{SW}} \quad (6)$$

Current Sensing

In order to provide both cost effective solution and good accuracy, TPS51219 supports both of MOSFET $R_{DS(on)}$ sensing and external resistor sensing. For $R_{DS(on)}$ sensing scheme, TRIP pin should be connected to GND through the trip voltage setting resistor, R_{TRIP}. In this scheme, TRIP terminal sources 10μA of I_{TRIP} current and the trip level is set to 1/8 of the voltage across the R_{TRIP}. The inductor current is monitored by the voltage between the PGND pin and the SW pin so that the SW pin is connected to the drain terminal of the low-side MOSFET. I_{TRIP} has a 4700ppm/°C temperature slope to compensate the temperature dependency of the $R^{DS(on)}$. For resistor sensing scheme, an appropriate current sensing resistor should be connected between the source terminal of the low-side MOSFET and PGND. The TRIP pin is connected to the MOSFET source terminal node. The inductor current is monitored by the voltage between PGND pin and TRIP pin. In either scheme, PGND is used as the positive current sensing node so that PGND should be connected to the proper current sensing device, i.e. the sense resistor or the source terminal of the low-side MOSFET.

Overcurrent Protection

TPS51219 has cycle-by-cycle overcurrent limiting protection. The inductor current is monitored during the off-state and the controller maintains the off-state when the inductor current is larger than the overcurrent trip level. The trip level and current sense operation are determined by the MODE pin setting and TRIP pin connection (See Table 2 and Current Sensing section). For $R_{DS(on)}$ sensing scheme, TRIP terminal sources 10 μA and the trip level is set to 1/8 of the voltage across this R_{TRIP} resistor. The overcurrent trip level, V_{OCTRIP}, is determined by Equation 7.

$$V_{OCTRIP} = R_{TRIP} \times \left(\frac{I_{TRIP}}{8} \right) \quad (7)$$

For a resistor sensing scheme, the trip level, V_{OCTRIP}, is a fixed value of 25 mV.

Because the comparison is made during the off-state, V_{OCTRIP} sets the valley level of the inductor current. The load current OCL level, I_{OCL}, can be calculated by considering the inductor ripple current.

Overcurrent limiting using $R_{DS(on)}$ sensing is shown in Equation 8.

$$I_{OCL} = \left(\frac{V_{OCTRIP}}{R_{DS(on)}} \right) + \frac{I_{IND(ripple)}}{2} = \left(\frac{V_{OCTRIP}}{R_{DS(on)}} \right) + \frac{1}{2} \times \frac{V_{IN} - V_{OUT}}{L_X} \times \frac{V_{OUT}}{f_{SW} \times V_{IN}} \quad (8)$$

where

- $I_{IND(ripple)}$ is inductor ripple current

Overcurrent limiting using resistor sensing is shown in Equation 9.

$$I_{OCL} = \left(\frac{25mV}{R_{EXT}}\right) + \frac{I_{IND(ripple)}}{2} = \left(\frac{25mV}{R_{EXT}}\right) + \frac{1}{2} \times \frac{V_{IN} - V_{OUT}}{L_X} \times \frac{V_{OUT}}{f_{SW} \times V_{IN}}$$

where

- $I_{IND(ripple)}$ is inductor ripple current
- R_{EXT} is the external current sense resistance (9)

In an overcurrent condition, the current to the load exceeds the current to the output capacitor, thus the output voltage tends to fall down. Eventually, it crosses the undervoltage protection threshold and shuts down.

Overvoltage and Undervoltage Protection

The TPS51219 sets the overvoltage protection (OVP) when VSNS voltage reaches a level 20% (typ) higher than the REFIN voltage. When an OV event is detected, the controller changes the output target voltage to 0 V. This usually turns off DH and forces DL to be on. When the inductor current begins to flow through the low-side MOSFET and reaches the negative OCL, DL is turned off and DH is turned on, for a minimum on-time.

After the minimum on-time expires, DH is turned off and DL is turned on again. This action minimizes the output node undershoot due to LC resonance. When the VSNS reaches 0 V, the driver output is latched as DH off, DL on.

The undervoltage protection (UVP) latch is set when the VSNS voltage remains lower than 68% (typ) of the REFIN voltage for 1 ms or longer. In this fault condition, the controller latches DH low and DL low and discharges the V_{OUT}. UVP detection function is enabled after 1.2 ms of SMPS operation to ensure startup.

To release the OVP and UVP latches, toggle EN or adjust the V5 voltage down and up beyond the undervoltage lockout threshold.

V5 Undervoltage Lockout Protection

TPS51219 has a 5-V supply undervoltage lockout protection (UVLO) threshold. When the V5 voltage is lower than UVLO threshold voltage, typically 3.9 V, V_{OUT} is shut off. This is a non-latch protection.

Thermal Shutdown

TPS51219 includes an internal temperature monitor. If the temperature exceeds the threshold value, 140°C (typ), V_{OUT} is shut off. The state of V_{OUT} is open at thermal shutdown. This is a non-latch protection and the operation is restarted with soft-start sequence when the device temperature is reduced by 10°C (typ).

External Components Selection

The external components selection is simple in D-CAP™ mode.

1. DETERMINE THE VALUE OF R1 AND R2

The output voltage is determined by the value of the voltage-divider resistor, R1 and R2 as shown in Figure 25. R1 is connected between VREF and REFIN pins, and R2 is connected between the REFIN pin and GSNS. Setting R1 as 10-kΩ is a good starting point. Determine R2 using Equation 10.

$$R2 = \frac{R1}{\left(\frac{2.0}{V_{OUT} - \left(\frac{I_{IND(ripple)} \times ESR}{2} \right)} \right) - 1} \tag{10}$$

2. CHOOSE THE INDUCTOR

The inductance value should be determined to yield a ripple current of approximately ¼ to ½ of maximum output current. Larger ripple current increases output ripple voltage and improves the signal-to-noise ratio and helps stable operation.

$$L_X = \frac{1}{I_{IND(ripple)} \times f_{SW}} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} = \frac{3}{I_{O(max)} \times f_{SW}} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} \tag{11}$$

The inductor needs a low direct current resistance (DCR) to achieve good efficiency, as well as enough room above peak inductor current before saturation. The peak inductor current can be estimated in Equation 12.

$$I_{IND(peak)} = \frac{V_{TRIP}}{8 \times R_{DS(on)}} + \frac{1}{L_X \times f_{SW}} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} \tag{12}$$

3. CHOOSE THE OCL SETTING RESISTANCE

R_{TRIP} for $R_{DS(on)}$ Sensing

Combining Equation 7 and Equation 8, R_{TRIP} can be obtained using Equation 13.

$$R_{TRIP} = \frac{8 \times \left(I_{OCL} - \left(\frac{\left(V_{IN} - V_{OUT}\right)}{\left(2 \times L_X\right)} \right) \times \frac{V_{OUT}}{\left(f_{SW} \times V_{IN}\right)} \right) \times R_{DS(on)}}{I_{TRIP}} \tag{13}$$

R_{EXT} for Resistor Setting

Combining Equation 7 and Equation 9, R_{EXT} can be obtained using Equation 14.

$$R_{EXT} = \frac{25\,mV}{I_{OCL} - \left(\frac{V_{IN} - V_{OUT}}{2 \times L_X} \right) \times \frac{V_{OUT}}{f_{SW} \times V_{IN}}} \tag{14}$$

For more accurate current sensing with an external resistor, the following technique is recommended. Adding an RC filter to cancel the parasitic inductance (ESL) of resistor, this filter value is calculated using Equation 15.

$$C_X \times R_X = \frac{ESL}{R_{EXT}} \tag{15}$$

The time-constant of C_X and R_X should match the one of ESL and R_{EXT}. Even when C_X is not used, an R_X of 100 Ω is recommended for noise suppression.

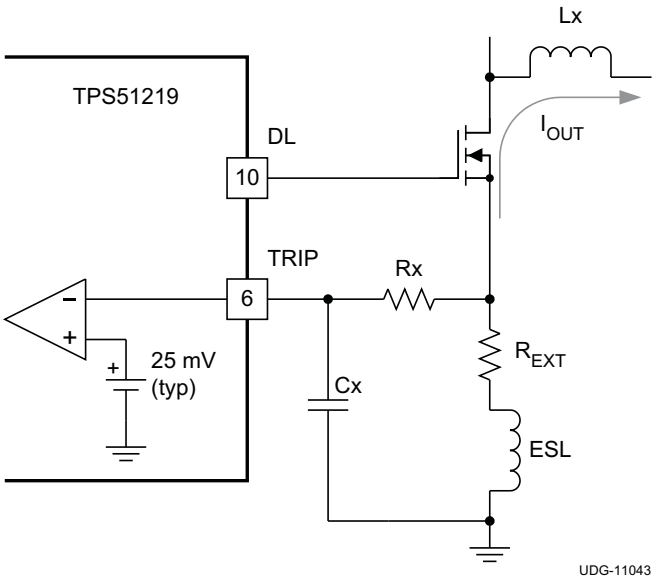


Figure 28. Resistor Sensing with Compensation

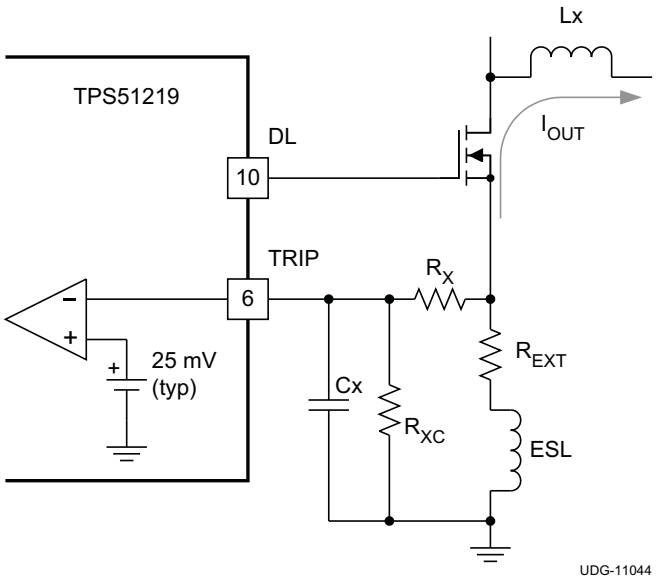


Figure 29. Adjustment of Overcurrent Limitation in Resistor Sensing

A voltage divider can be configured to adjust for overcurrent limitation, as described in Figure 29. For R_X, R_{XC} and C_X can be calculated as shown in Equation 16, and the overcurrent limitation value can be calculated as shown in Equation 17.

$$C_X \times \left(R_X \| R_{XC}\right) = \frac{ESL}{R_{EXT}} \tag{16}$$

$$I_{OCL} = \left(\frac{25mV}{R_{EXT}}\right) + \frac{R_X + R_{XC}}{R_{XC}} + \left(\frac{V_{IN} - V_{OUT}}{2 \times L_X}\right) \times \frac{V_{OUT}}{f_{SW} \times V_{IN}} \tag{17}$$

Therefore, R_{EXT} can be obtained using Equation 18.

$$R_{EXT} = \frac{25mV}{I_{OCL} - \left(\frac{\left(V_{IN} - V_{OUT}\right)}{2 \times L_X}\right) \times \frac{V_{OUT}}{f_{SW} \times V_{IN}}} \times \left(\frac{\left(R_X + R_{XC}\right)}{R_{XC}}\right) \tag{18}$$

4. CHOOSE THE OUTPUT CAPACITORS

D-CAP™ Mode

Organic semiconductor capacitor(s) or specialty polymer capacitor(s) are recommended. Determine the ESR value to meet small signal stability and recommended ripple voltage. A quick reference is shown in Equation 19 and Equation 20.

$$f_0 = \frac{1}{2\pi \times ESR \times C_{OUT}} \le \frac{f_{SW}}{3} \tag{19}$$

$$\frac{g_M}{2\pi \times C1} \le \frac{f_0}{10}$$

where

- g_M is 130 µS (typ)
- C1 is the capacitance connected between the VSNS and COMP pins

(20)

$$\frac{V_{OUT} \times ESR}{f_{SW} \times Lx} \ge 20mV \tag{21}$$

D-CAP2™ Mode

Determine output capacitance to meet small signal stability as shown in Equation 22 and Equation 23.

$$\frac{(R_C \times C_C)}{2\pi \times G \times L_X \times C_{OUT}} \leq \frac{f_{SW}}{3} \quad (22)$$

where

- G = 0.25

$$\frac{g_M}{2\pi \times C1} \leq \frac{f_0}{10} \quad (23)$$

where

- the $R_C \times C_C$ time constant is 32 µs for operation at 500 kHz. (23 µs for operation at 670 kHz)

Layout Considerations

Certain issues must be considered before designing a layout using the TPS51219.

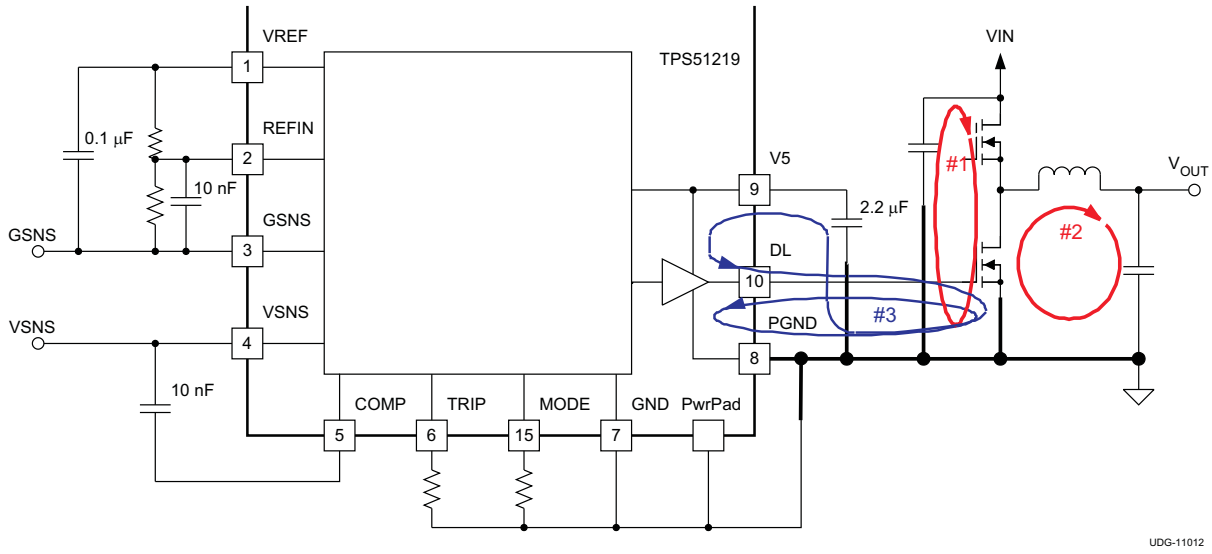


Figure 30. DC/DC Converter Ground System

- V_{IN} capacitor(s), V_{OUT} capacitor(s) and MOSFETs are the power components and should be placed on one side of the PCB (solder side). Other small signal components should be placed on another side (component side). At least one inner plane should be inserted, connected to ground, in order to shield and isolate the small signal traces from noisy power lines.
- All sensitive analog traces and components such as VSNS, COMP, MODE, REFIN, VREF and TRIP should be placed away from high-voltage switching nodes such as SW, DH, DL or BST to avoid coupling. Use internal layer(s) as ground plane(s) and shield feedback trace from power traces and components.
- The DC/DC converter has several high-current loops. The area of these loops should be minimized in order to suppress generating switching noise.
  - Loop #1. The most important loop to minimize the area of is the path from the V_{IN} capacitor(s) through the high and low-side MOSFETs, and back to the capacitor(s) through ground. Connect the negative node of the V_{IN} capacitor(s) and the source of the low-side MOSFET at ground as close as possible. (Refer to loop #1 of Figure 30)
  - Loop #2. The second important loop is the path from the low-side MOSFET through inductor and V_{OUT} capacitor(s), and back to source of the low-side MOSFET through ground. Connect source of the low-side MOSFET and negative node of V_{OUT} capacitor(s) at ground as close as possible. (Refer to loop #2 of Figure 30)
  - Loop #3. The third important loop is of gate driving system for the low-side MOSFET. To turn on the low-side MOSFET, high current flows from V5 capacitor through gate driver and the low-side MOSFET, and back to negative node of the capacitor through ground. To turn off the low-side MOSFET, high current flows from gate of the low-side MOSFET through the gate driver and PGND, and back to source of the low-side MOSFET through ground. Connect negative node of V5 capacitor, source of the low-side MOSFET and PGND at ground as close as possible. (Refer to loop #3 of Figure 30)
- Connect the PGND and GND pins directly at the device.

- Connect VSNS directly to the output voltage sense point at the load device. Connect GSNS to ground return points at the load device. Insert a 10-Ω, 1-nF, R-C filter between the sense point and the VSNS pin where the COMP capacitance is connected as shown in Case 1 (Figure 31). When the COMP pin capacitance is connected to output bulk capacitance, connect the R-C filter in series to both the VSNS pin and the COMP capacitance as shown in Case 2 (Figure 32).

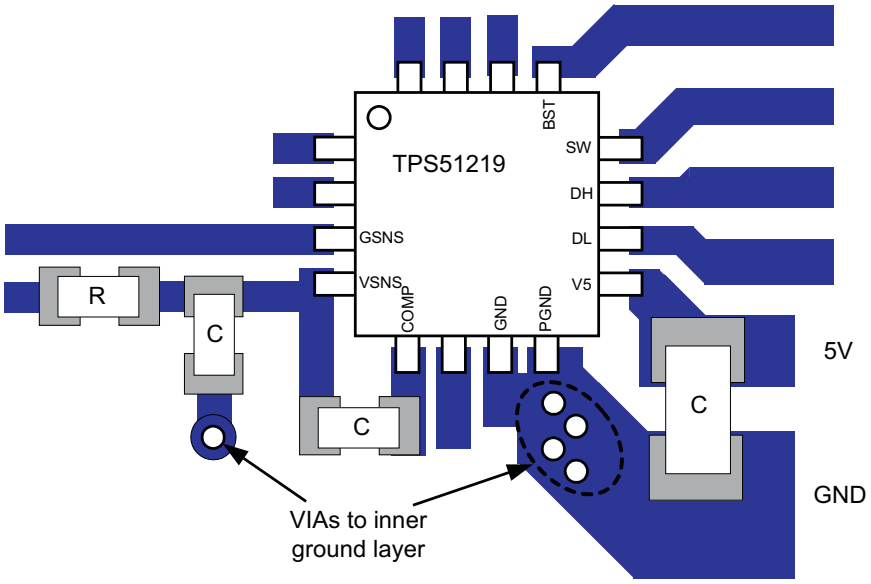


Figure 31. Case 1: COMP Pin Capacitance Connected to VSNS

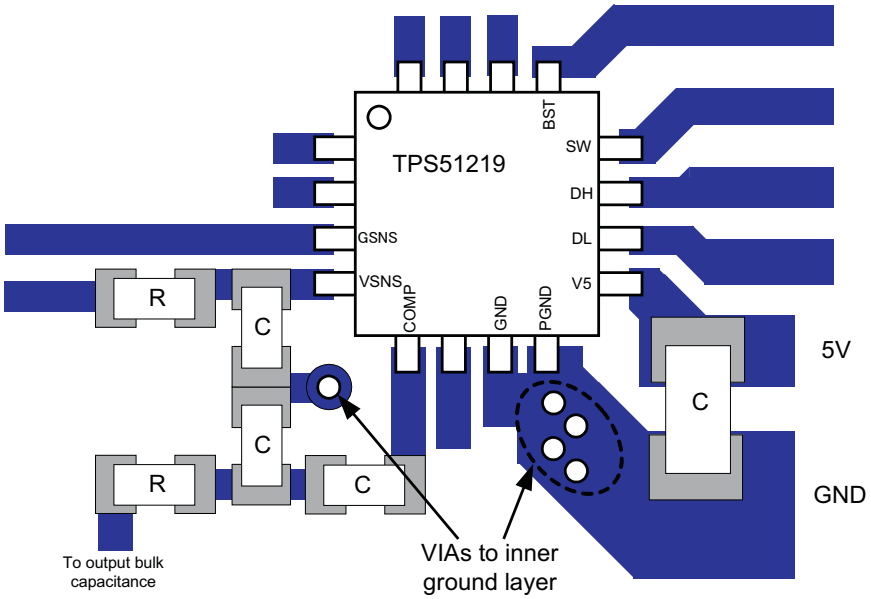


Figure 32. Case 2: COMP Pin Capacitance Connected to Output Bulk Capacitance

- Connect the overcurrent setting resistors from TRIP pin to ground and make the connections as close as possible to the device. The trace from TRIP pin to resistor and from resistor to ground should avoid coupling to a high-voltage switching node.
- Connect the frequency and mode setting resistor from MODE pin to ground, and make the connections as close as possible to the device. The trace from the MODE pin to the resistor and from the resistor to ground should avoid coupling to a high-voltage switching node.

- Connections from gate drivers to the respective gate of the high-side or the low-side MOSFET should be as short as possible to reduce stray inductance. Use 0.65 mm (25 mils) or wider trace and via(s) of at least 0.5 mm (20 mils) diameter along this trace.
- The PCB trace defined as SW node, which connects to the source of the switching MOSFET, the drain of the rectifying MOSFET and the high-voltage side of the inductor, should be as short and wide as possible.
- In order to effectively remove heat from the package, prepare the thermal land and solder to the package thermal pad. Wide trace of the component-side copper, connected to this thermal land, helps to dissipate heat. Numerous vias with a 0.3-mm diameter connected from the thermal land to the internal/solder-side ground plane(s) should be used to help dissipation.

TPS51219 1.05-V/20-A, D-CAP2™ 500-kHz, $R_{DS(on)}$ Sensing Application Circuit

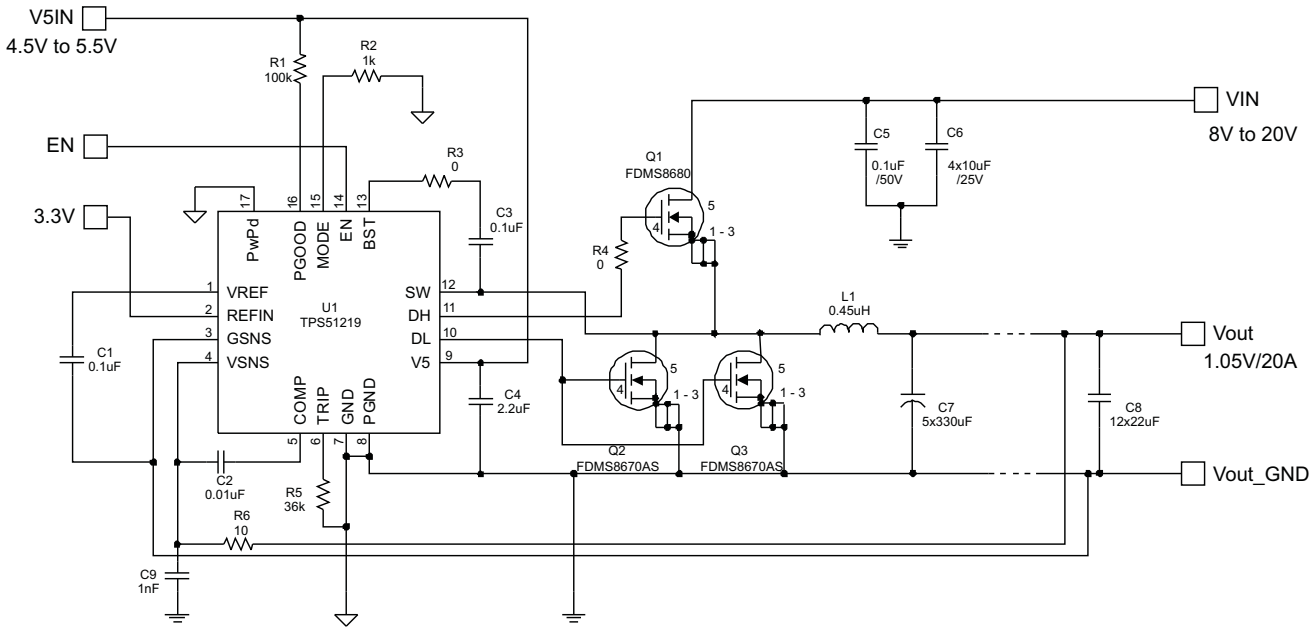


Figure 33. 1.05-V/20-A, D-CAP2™ 500-kHz, $R_{DS(on)}$ Sensing

Table 3. 1.05-V/20-A, D-CAP2™ 500-kHz, $R_{DS(on)}$ Sensing, List of Materials

REFERENCE DESIGNATOR	QTY	SPECIFICATION	MANUFACTURE	PART NUMBER
C6	4	10 µF, 25 V	Taiyo Yuden	TMK325BJ106MM
C7	5	330 µF, 2 V, 6 mΩ	Panasonic	EEFSX0D331XE
C8	12	22 µF, 6.3 V	Murata	GRM21BB30J226ME38
L1	1	0.45 µH, 17 A, 1.1 mΩ	Panasonic	ETQP4LR45XFC
Q1	1	30 V, 35 A, 8.5 mΩ	Fairchild	FDMS8680
Q2, Q3	2	30 V, 42 A, 3.5 mΩ	Fairchild	FDMS8670AS

1.05-V/20-A, D-CAP™ 400-kHz, $R_{DS(on)}$ Sensing Application Circuit

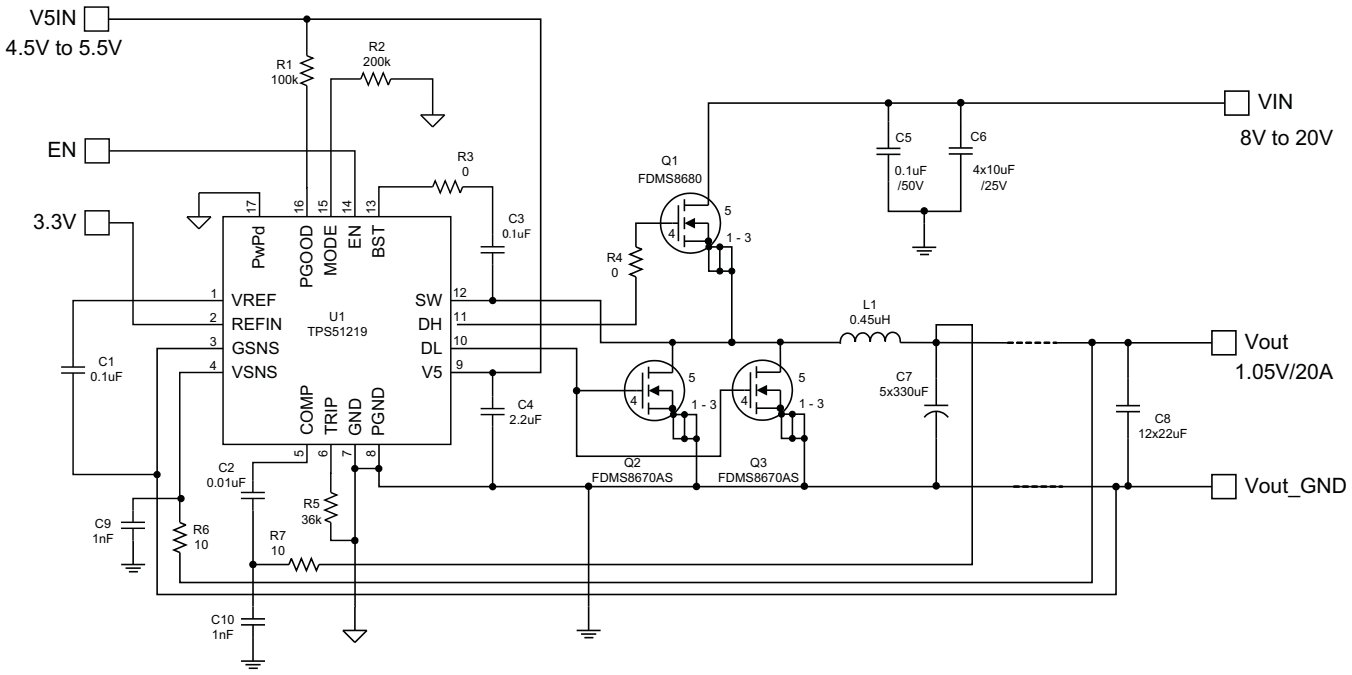


Figure 34. 1.05-V/20-A, D-CAP™ 400-kHz, $R_{DS(on)}$ Sensing

Table 4. 1.05-V/20-A, D-CAP™ 400-kHz, $R_{DS(on)}$ Sensing, List of Materials

REFERENCE DESIGNATOR	QTY	SPECIFICATION	MANUFACTURE	PART NUMBER
C6	4	10 µF, 25 V	Taiyo Yuden	TMK325BJ106MM
C7	5	330 µF, 2.5 V, 18 mΩ	Sanyo	2R5TPE330MI
C8	12	22 µF, 6.3 V	Murata	GRM21BB30J226ME38
L1	1	0.45 µH, 17 A, 1.1 mΩ	Panasonic	ETQP4LR45XFC
Q1	1	30 V, 35 A, 8.5 mΩ	Fairchild	FDMS8680
Q2,Q3	2	30 V, 42 A, 3.5 mΩ	Fairchild	FDMS8670AS

TPS51219 1.00-V/10.4-A, D-CAP2™ 500-kHz, Resistor Sensing Application Circuit

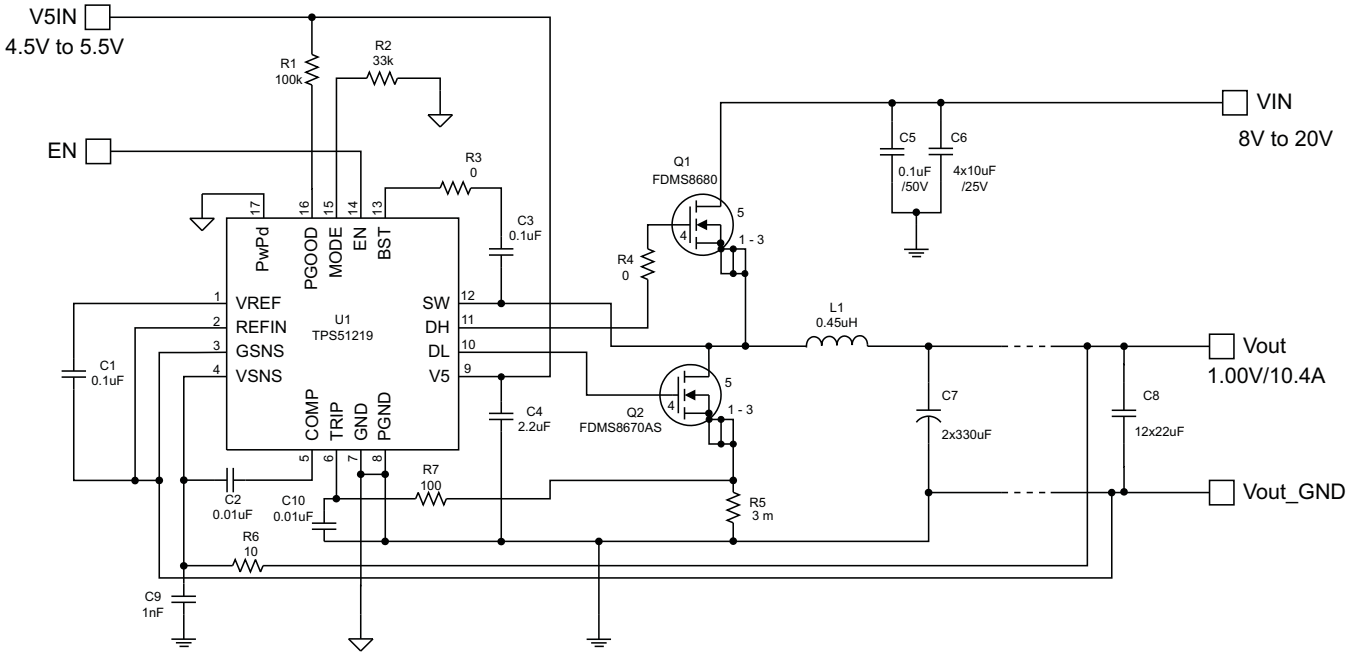


Figure 35. 1.00-V/10.4-A, D-CAP2™ 500-kHz, Resistor Sensing

Table 5. 1.00-V/10.4-A, D-CAP2™ 500-kHz, Resistor Sensing, List of Materials

REFERENCE DESIGNATOR	QTY	SPECIFICATION	MANUFACTURE	PART NUMBER
C6	4	10 µF, 25 V	Taiyo Yuden	TMK325BJ106MM
C7	2	330 µF, 2 V, 6 mΩ	Panasonic	EEFSX0D331XE
C8	12	22 µF, 6.3 V	Murata	GRM21BB30J226ME38
L1	1	0.45 µH, 17 A, 1.1 mΩ	Panasonic	ETQP4LR45XFC
Q1	1	30 V, 35 A, 8.5 mΩ	Fairchild	FDMS8680
Q2	1	30 V, 42 A, 3.5 mΩ	Fairchild	FDMS8670AS
R5	1	3 mΩ, 1 W	KOA	TLR2HDTD3L00F

TPS51219 1.00-V/10.4-A, D-CAP™ 400-kHz, Resistor Sensing Application Circuit

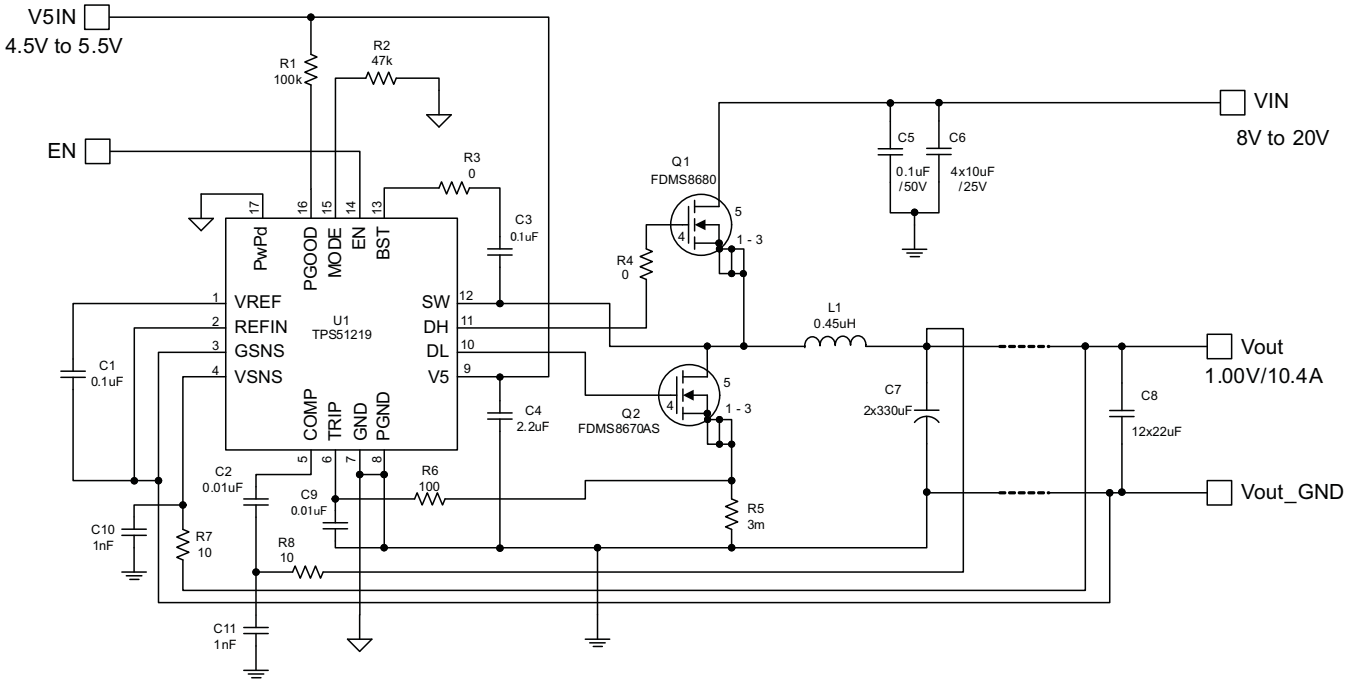


Figure 36. 1.00-V/10.4-A, D-CAP™ 400-kHz, Resistor Sensing

Table 6. 1.00-V/10.4-A, D-CAP™ 400-kHz, Resistor Sensing, List of Materials

REFERENCE DESIGNATOR	QTY	SPECIFICATION	MANUFACTURE	PART NUMBER
C6	4	10 µF, 25 V	Taiyo Yuden	TMK325BJ106MM
C7	2	330 µF, 2 V, 9 mΩ	Panasonic	EEFSX0D331ER
C8	12	22 µF, 6.3 V	Murata	GRM21BB30J226ME38
L1	1	0.45 µH, 17 A, 1.1 mΩ	Panasonic	ETQP4LR45XFC
Q1	1	30 V, 35 A, 8.5 mΩ	Fairchild	FDMS8680
Q2	1	30 V, 42 A, 3.5 mΩ	Fairchild	FDMS8670AS
R5	1	3 mΩ, 1 W	KOA	TLR2HDTD3L00F

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS51219RTER	ACTIVE	WQFN	RTE	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	51219	Samples
TPS51219RTET	ACTIVE	WQFN	RTE	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	51219	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

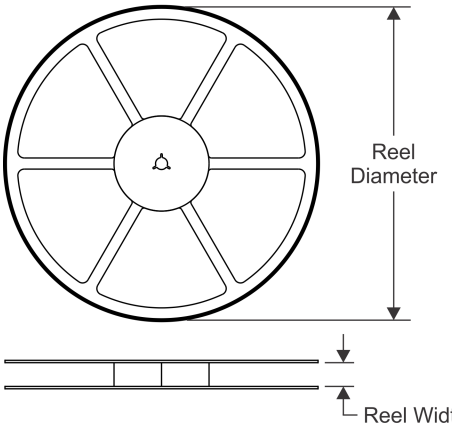
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

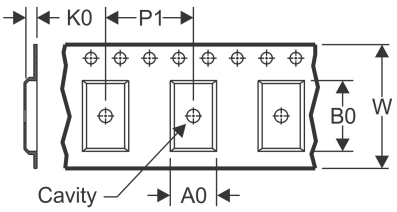
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

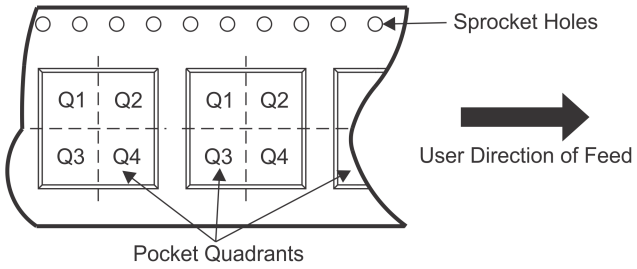


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

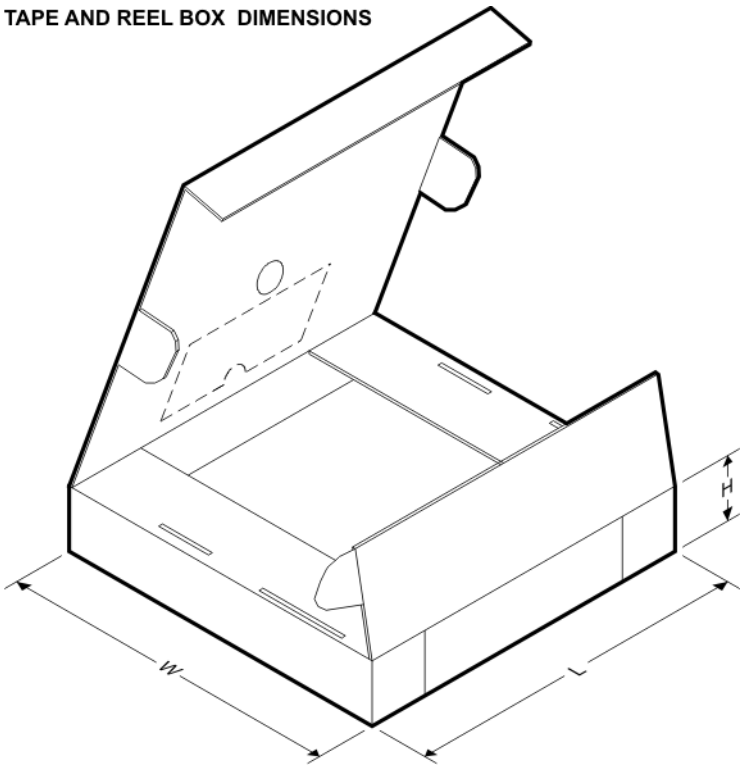
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS51219RTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS51219RTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS51219RTET	WQFN	RTE	16	250	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

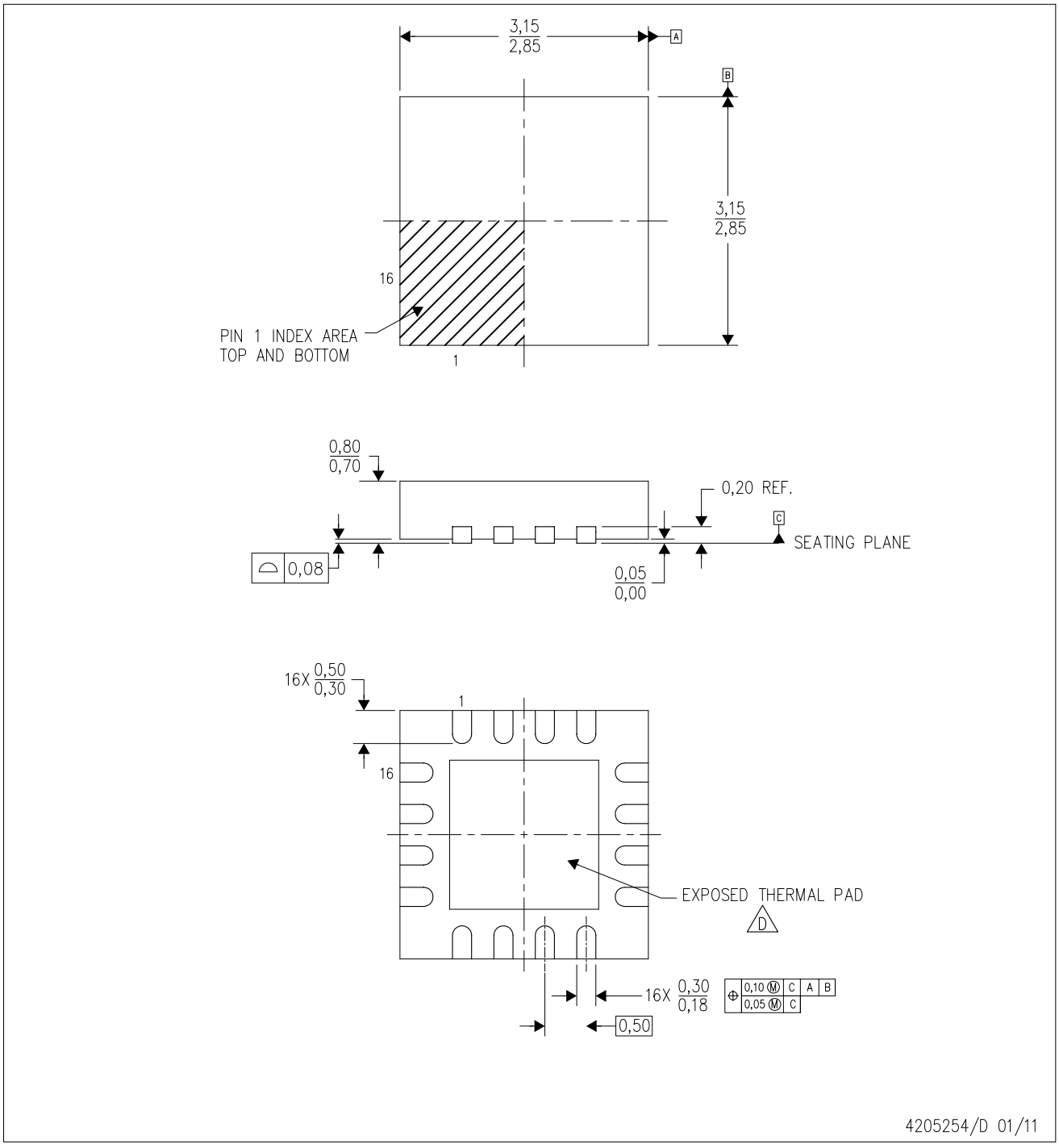
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS51219RTER	WQFN	RTE	16	3000	367.0	367.0	35.0
TPS51219RTER	WQFN	RTE	16	3000	338.0	355.0	50.0
TPS51219RTET	WQFN	RTE	16	250	338.0	355.0	50.0

RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

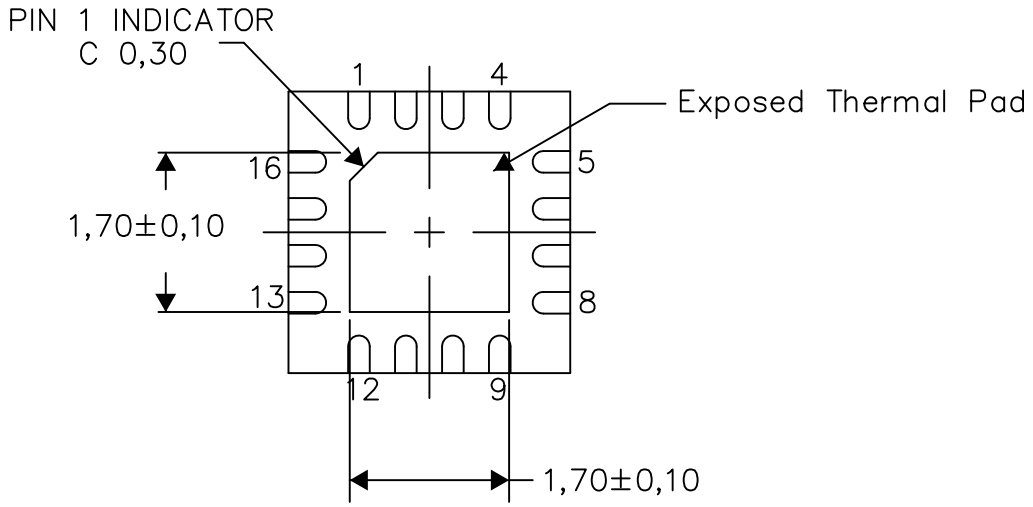
RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



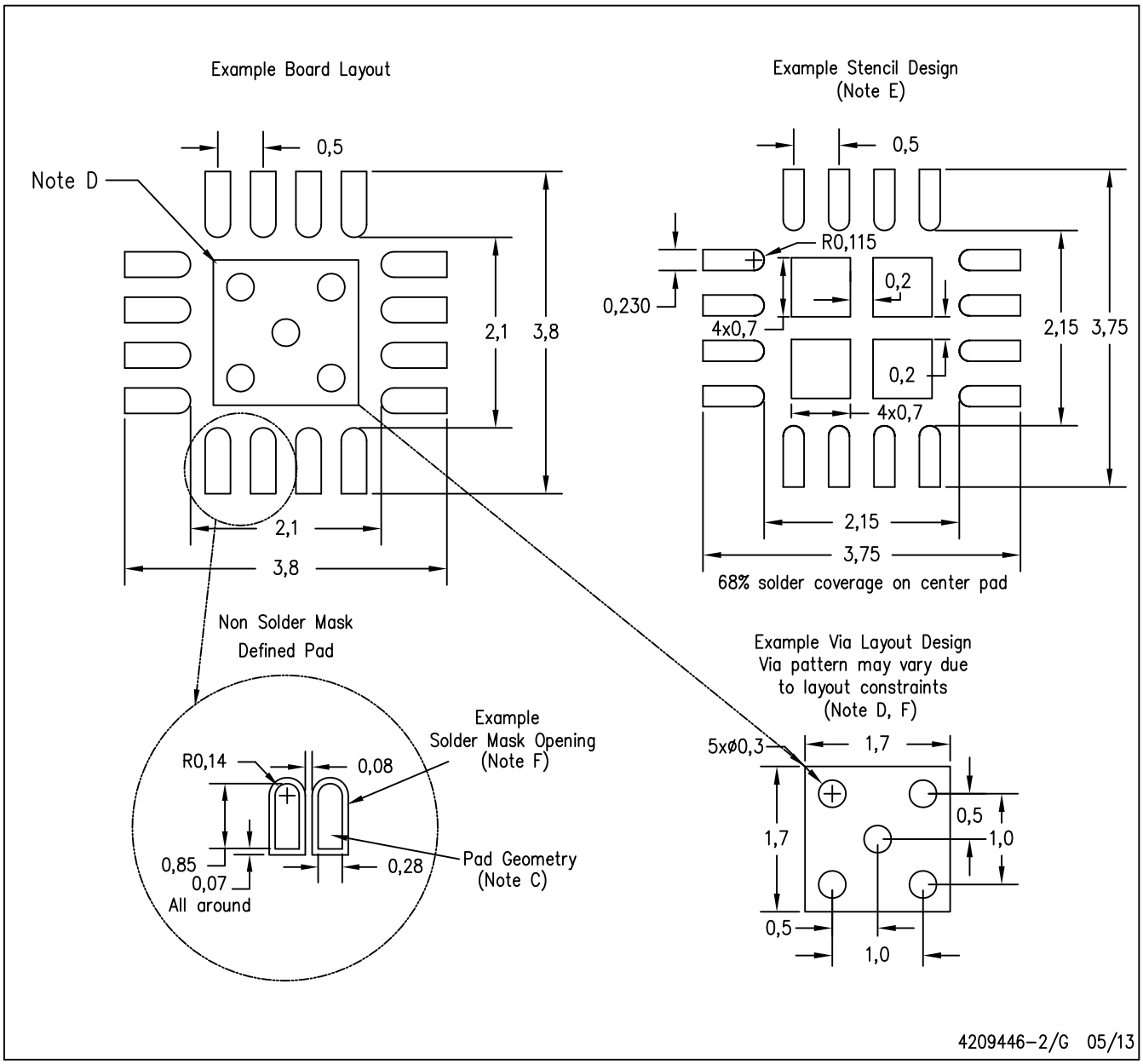
Bottom View

Exposed Thermal Pad Dimensions

4206446–3/M 05/13

NOTE: A. All linear dimensions are in millimeters

RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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