2.5A, Single Input, Single Cell Switchmode Li-Ion Battery Charger with Power Path Management

Check for Samples: bq24272

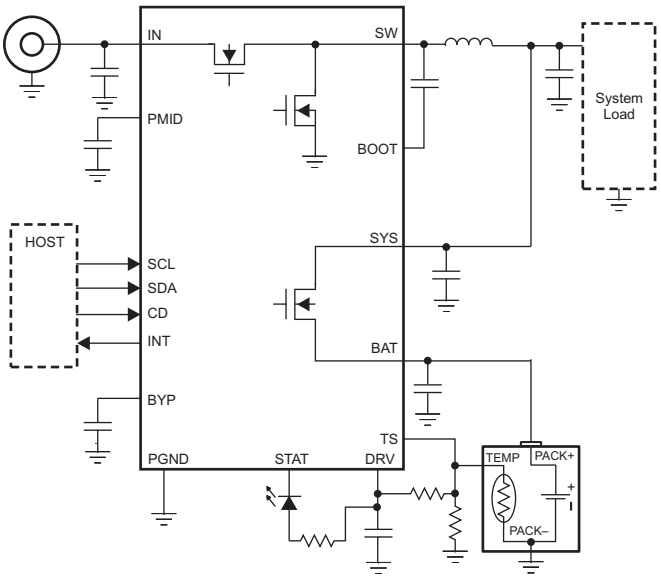
FEATURES

- High-Efficiency Switch Mode Charger with Separate Power Path Control
  - Instantly Startup System from a Deeply Discharged Battery or No Battery
- 20V input rating, with 10.5V Over-Voltage Protection (OVP)
- Integrated FETs for Up to 2.5A Charge Rate
- Highly Integrated Battery N-Channel MOSFET Controller for Power Path Management
- Safe and Accurate Battery Management Functions
  - 0.5% Battery Regulation Accuracy
  - 10% Charge Current Accuracy
- Voltage-based, NTC Monitoring Input (TS)
  - JEITA Compatible
- Thermal Regulation Protection for Output Current Control
- BAT Short-Circuit Protection
- Soft-Start Feature to Reduce Inrush Current
- Thermal Shutdown and Protection
- Available in Small 49-ball WCSP or QFN-24 Packages

APPLICATIONS

- Handheld Products
- Portable Media Players
- Portable Equipment
- Tablets and Portable Internet Devices

APPLICATION SCHEMATIC



DESCRIPTION

The bq24272 is a highly integrated single cell Li-Ion battery charger and system power path management device targeted for space-limited, portable applications with high capacity batteries. The single cell charger operates from a dedicated power source such as a wall adapter or wireless power supply for a versatile solution.

The power path management feature allows the bq24272 to power the system from a high efficiency DC to DC converter while simultaneously and independently charging the battery. The charger monitors the battery current at all times and reduces the charge current when the system load requires current above the input current limit. This allows for proper charge termination and timer operation. The system voltage is regulated to the battery voltage but will not drop below 3.5V. This minimum system voltage support enables the system to run with a defective or absent battery pack and enables instant system turn-on even with a totally discharged battery or no battery. The power-path management architecture also permits the battery to supplement the system current requirements when the adapter cannot deliver the peak system currents. This enables the use of a smaller adapter.

The battery is charged in three phases: conditioning, constant current and constant voltage. In all charge phases, an internal control loop monitors the IC junction temperature and reduces the charge current if the internal temperature threshold is exceeded. Additionally, the bq24272 offers a voltage-based battery pack thermistor monitoring input (TS) that monitors battery temperature for safe charging.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

PART NUMBER	OVP	NTC MONITORING (TS)	JEITA COMPATIBLE	MINIMUM SYSTEM VOLTAGE	PACKAGE
bq24272YFFR	10.5 V	Yes	No	3.5 V	WCSP
bq24272YFFT	10.5 V	Yes	No	3.5 V	WCSP
bq24272RGER	10.5 V	Yes	No	3.5 V	QFN
bq24272RGET	10.5 V	Yes	No	3.5 V	QFN

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Pin voltage range (with respect to VSS)	IN	–2	20	V
	BYP, PMID, BOOT	–0.3	20	V
	SW	–0.7	12	V
	SYS, BAT, BGATE, DRV, STAT, INT, SDA, SCL, CD, TS	–0.3	7	V
BOOT to SW		–0.3	7	V
Output Current (Continuous)	SW		4.5	A
	SYS		3.5	a
Input Current (Continuous)	IN		2.75	A
Output Sink Current	STAT, INT		10	mA
Operating free-air temperature range		–40	85	°C
Junction temperature, T_J		–40	125	°C
Storage temperature, T_{STG}		–65	150	°C
Lead temperature (soldering, 10 s)			300	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.

THERMAL INFORMATION

THERMAL METRIC(1)		bq24272		UNITS
		49 PINS (YFF)	24 PINS (QFN)	
θ_{JA}	Junction-to-ambient thermal resistance	49.8	32.6	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	0.2	30.5	
θ_{JB}	Junction-to-board thermal resistance	1.1	3.3	
ψ_{JT}	Junction-to-top characterization parameter	1.1	0.4	
ψ_{JB}	Junction-to-board characterization parameter	6.6	9.3	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	n/a	2.6	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNITS
V_{IN}	IN voltage range	4.2	18(1)	V
	IN operating range	4.2	10	
I_{IN}	Input current		2.5	A
I_{SYS}	Output current from SW, DC		3	A
I_{BAT}	Charging		2.5	A
	Discharging, using internal battery FET		2.5	
T_J	Operating junction temperature range	0	125	°C

(1) The inherent switching noise voltage spikes should not exceed the absolute maximum rating on either the BOOT or SW pins. A tight layout minimizes switching noise.

ELECTRICAL CHARACTERISTICS

Circuit of , $V_{UVLO} < V_{IN} < V_{OVP}$ AND $V_{IN}>V_{BAT}+V_{SLP}$, T_J = 0°C – 125°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNITS
I_{IN}	Input quiescent current	$V_{UVLO} < V_{IN} < V_{OVP}$ AND $V_{IN} > V_{BAT}+V_{SLP}$, PWM switching			15		mA
		$V_{UVLO} < V_{IN} < V_{OVP}$ AND $V_{IN} > V_{BAT}+V_{SLP}$, PWM NOT switching				5	
		0°C< T_J < 85°C, High-Z Mode				175	µA
$I_{BATLEAK}$	Leakage current from BAT to the supply	0°C< T_J < 85°C, V_{BAT} = 4.2V, V_{IN} = 0V				5	µA
I_{BAT_HIZ}	Battery discharge current in high impedance mode, (BAT, SW, SYS)	0°C< T_J < 85°C, V_{BAT} = 4.2 V, V_{IN} = 0 V or 5 V, High-Z mode				55	µA
POWER PATH MANAGEMENT							
$V_{SYS(REG)}$	System regulation voltage	$V_{BAT} < V_{MINSYS}$		3.6	3.7	3.82	V
$V_{SYSREGFETOFF}$		Battery FET turned off, Charge disable or termination		V_{BATREG} +1.5%	V_{BATREG} +3.0%	V_{BATREG} +4.17%	
V_{MINSYS}	Minimum system regulation voltage	$V_{BAT} < V_{MINSYS}$, Input current limit or V_{INDPM} active		3.4	3.5	3.62	V
V_{BSUP1}	Enter supplement mode threshold	V_{BAT} > 2.5 V			V_{BAT} –30mV		V
V_{BSUP2}	Exit supplement mode threshold	V_{BAT} > 2.5 V			V_{BAT} –10mV		V
$I_{LIM(Discharge)}$	Current limit, discharge or supplement mode	Current monitored in internal FET only			7		A
$t_{DGL(SC1)}$	Deglitch Time, OUT short circuit during discharge or supplement mode	Measured from (VB_{AT} -V_{SYS}) = 300 mV to V_{BGATE} = (V_{BAT} - 600 mV)			250		µs
$t_{REC(SC1)}$	Recovery time, OUT short circuit during discharge or supplement mode				60		ms
	Battery range for BGATE operation			2.5		4.5	V
BATTERY CHARGER							
$R_{ON(BAT-CS+)}$	Internal battery charger MOSFET on-resistance	Measured from BAT to SYS, V_{BAT} = 4.2V	YFF pkg		37	57	mΩ
			RGE pkg		50	70	
V_{BATREG}	Battery regulation voltage			3.5		4.44	V
	Battery regulation voltage accuracy	T_A = 25°C		–0.5%		0.5%	
		Over temperature		–1%		1%	
I_{CHARGE}	Charge current programmable range	$V_{BATSHRT} < V_{BAT} < V_{BATREG}$		550		2000	mA
	Fast charge current accuracy	0°C to 125°C		–10%		10%	
$V_{BATSHRT}$	Battery short threshold	V_{BAT} Rising, 100 mV Hysteresis		2.9	3.0	3.1	V
$I_{BATSHRT}$	Battery short current	$V_{BAT} < V_{BATSHRT}$			50.0		mA
$t_{DGL(BATSHRT)}$	Deglitch time for battery short to fast charge transition				32		ms
I_{TERM}	Termination charge current accuracy	I_{CHARGE} = 50 mA		–35%		35%	
		I_{CHARGE} > 50 mA		–15%		15%	
$t_{DGL(TERM)}$	Deglitch time for charge termination	Both rising and falling, 2-mV over-drive, t_{RISE}, t_{FALL} = 100 ns			32		ms
V_{RCH}	Recharge threshold voltage	Below V_{BATREG}			120		mV
$t_{DGL(RCH)}$	Deglitch time	V_{BAT} falling below V_{RCH}, t_{FALL} = 100ns			32		ms
V_{DETECT}	Battery detection voltage threshold	During battery detection source cycle			3.3		V
		During battery detection sink cycle			3.0		

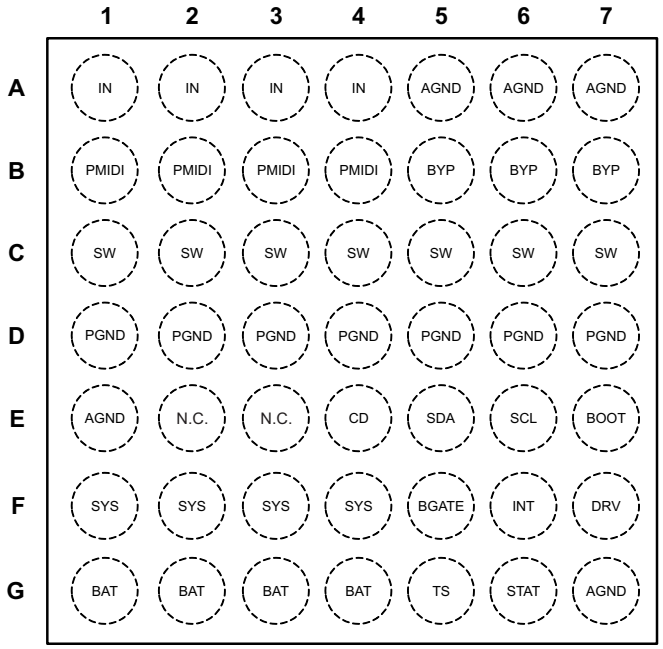
ELECTRICAL CHARACTERISTICS (continued)

Circuit of , $V_{UVLO} < V_{IN} < V_{OVP}$ AND $V_{IN}>V_{BAT}+V_{SLP}$, T_J = 0°C – 125°C and T_J = 25°C for typical values (unless otherwise noted)

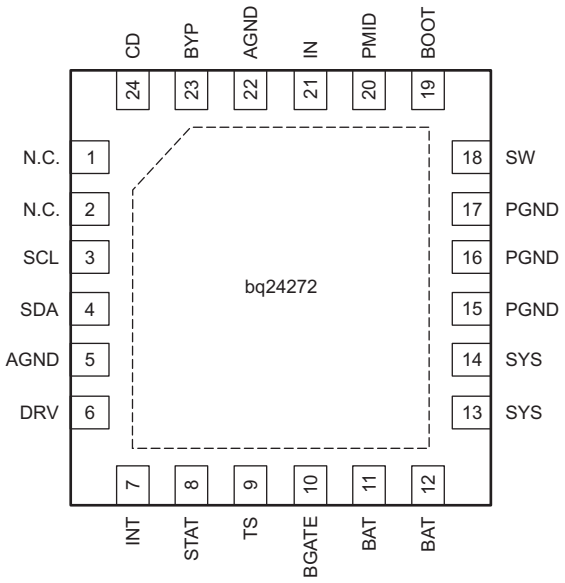
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNITS
I_{DETECT}	Battery detection current before charge done (sink current)				2.5		mA
t_{DETECT}	Battery detection time				250		ms
$V_{IH(CD)}$	CD input high logic level			1.3			V
$V_{IL(CD)}$	CD input low logic level				0.4		V
INPUT PROTECTION							
I_{INLIM}	Input current limit	VIN=5V, DC current pulled from SW	I_{INLIM} = 1.5 A	1.35	1.5	1.65	A
			I_{INLIM} = 2.5 A	2.3	2.5	2.8	
V_{IN_DPM}	Input DPM threshold			4.2		4.76	V
	Input DPM accuracy			–2%		2%	
V_{DRV}	Internal bias regulator voltage			5	5.2	5.45	V
I_{DRV}	DRV Output current			10			mA
V_{DO_DRV}	DRV Dropout voltage ($V_{IN} – V_{DRV}$)	I_{IN} = 1A, V_{IN} = 5V, I_{DRV} = 10mA				450	mV
V_{UVLO}	IC active threshold voltage	V_{IN} rising, 150 mV hysteresis		3.6	3.8	4.0	V
V_{SLP}	Sleep-mode entry threshold, V_{IN}-V_{BAT}	2.0 V ≤ V_{BAT} ≤ V_{OREG}, V_{IN} falling		0	40	100	mV
V_{SLP_EXIT}	Sleep-mode exit hysteresis	2.0 V ≤ V_{BAT} ≤ V_{OREG}		40	100	160	mV
	Deglitch time for supply rising above V_{SLP}+V_{SLP_EXIT}	Rising voltage, 2-mV over drive, t_{RISE}=100ns			30		ms
V_{OVP}	Input supply OVP threshold voltage	IN, V_{IN} Rising, 100 mV hysteresis		10.3	10.5	10.7	V
V_{BOVP}	Battery OVP threshold voltage	V_{BAT} threshold over V_{OREG} to turn off charger during charge		1.025 × V_{BATREG}	1.05 × V_{BATREG}	1.075 × V_{BATREG}	V
	V_{BOVP} hysteresis	Lower limit for V_{BAT} falling from above V_{BOVP}			1		% of V_{BATREG}
$V_{BATUVLO}$	Battery UVLO threshold voltage				2.5		V
V_{BAT_SOURCE}	Bad source detection threshold				V_{IN_DPM} – 80mV		V
	Bad source detection deglitch				32		ms
I_{LIMIT}	Cycle by cycle current limit			4.1	4.9	5.6	A
$T_{SHUTDWN}$	Thermal shutdown	10°C Hysteresis			165		C
T_{REG}	Thermal regulation threshold				120		C
	Safety timer accuracy			–20%		20%	
STAT, INT							
I_{IH}	High-level leakage current	$V_{/CHG}$ = $V_{/PG}$ = 5 V				1	µA
V_{OL}	Low-level output saturation voltage	IO = 10 mA, sink current				0.4	V
PWM CONVERTER							
	Internal top reverse blocking MOSFET on-resistance	I_{IN_LIMIT} = 1.5 A, Measured from V_{IN} to PMIDU			45	80	mΩ
	Internal top N-channel Switching MOSFET on-resistance	Measured from PMID to SW			65	110	mΩ
	Internal bottom N-channel MOSFET on-resistance	Measured from SW to PGND			65	115	mΩ
f_{OSC}	Oscillator frequency			1.35	1.50	1.65	MHz
D_{MAX}	Maximum duty cycle				95%		
D_{MIN}	Minimum duty cycle			0			
BATTERY-PACK NTC MONITOR							
V_{HOT}	High temperature threshold	V_{TS} falling, 1%V_{DRV} Hysteresis		29.7	30	30.5	%VDRV
V_{COLD}	Low temperature threshold	V_{TS} rising, 1%V_{DRV} Hysteresis		59.5	60	60.4	%VDRV
TS_{OFF}	TS Disable threshold	V_{TS} rising, 2%V_{DRV} Hysteresis		70		73	%VDRV
$t_{DGL(TS)}$	Deglitch time on TS change				50		ms
V_{IH}	Input high threshold	V_{PULLUP} = 1.8 V, SDA and SCL		1.3			V
V_{IL}	Input low threshold	V_{PULLUP} = 1.8 V, SDA and SCL				0.4	V
V_{OL}	Output low threshold	I_{SDA} = 10 mA, sink current				0.4	V
I_{IH}	Input high leakage current	V_{PULLUP} = 1.8 V, SDA and SCL			1		µA
$t_{WATCHDOG}$	Watchdog timer timeout			30			s

PIN CONFIGURATION

49-Ball WCSP (Top View)



24-PIN QFN (Top View)



(Contact the factory for the latest pinout)

PIN FUNCTIONS

PIN NAME	PIN NO. bq24272		I/O	DESCRIPTION
	YFF	RGE		
IN	A1–A4	21	I	Input power supply. IN is connected to the external DC supply (AC adapter or alternate power source). Bypass IN to PGND with at least a 1µF ceramic capacitor.
PMID	B1–B4	20	O	Reverse Blocking MOSFET and High Side MOSFET Connection Point for High Power Input. Bypass PMID to GND with at least a 4.7µF ceramic capacitor. Use caution when connecting an external load to PMID. The PMID output is not current limited. Any short on PMID will result in damage to the IC.
BYP	B5–B7	23	O	Bypass for internal circuits. Bypass BYP to GND with at least 0.1µF of capacitance. Do not connect any external load to BYP.
SW	C1–C7	18	O	Inductor Connection. Connect to the switched side of the external inductor.
AGND	A5–A7, E1, G7	5, 22	—	Ground terminal.
PGND	D1–D7	15, 16, 17	—	Ground terminal. Connect to the thermal pad (for QFN only) and the ground plane of the circuit.
N.C.	E2, E3	1, 2	I	No connection. Leave N.C. unconnected.
CD	E4	24	I	IC Hardware Disable Input. Drive CD high to place the bq24272 in High-Z mode. Drive CD low for normal operation.
SDA	E5	4	I/O	I2C Interface Data. Connect SDA to the logic rail through a 10kΩ resistor.
SCL	E6	3	I	I2C Interface Clock. Connect SCL to the logic rail through a 10kΩ resistor.
BOOT	E7	19	I	High Side MOSFET Gate Driver Supply. Connect a 0.01µF ceramic capacitor (voltage rating > 10V) from BOOT to SW to supply the gate drive for the high side MOSFETs.
SYS	F1–F4	13, 14	I	System Voltage Sense and Charger FET Connection. Connect SYS to the system output at the output bulk capacitors. Bypass SYS locally with 10µF.
BGATE	F5	10	O	External Discharge MOSFET Gate Connection. BGATE drives an external P-Channel MOSFET to provide a very low resistance discharge path. Connect BGATE to the gate of the external MOSFET. BGATE is low during supplement mode and when no input is connected.
INT	F6	7	O	Status Output. INT is an open-drain output that signals charging status and fault interrupts. INT pulls low during charging. INT is high impedance when charging is complete or the charger is disabled. When a fault occurs, a 128µs pulse is sent out as an interrupt for the host. INT is enabled /disabled using the EN_STAT bit in the control register. Connect INT to a logic rail through a 100kΩ resistor to communicate with the host processor.
DRV	F7	6	O	Gate Drive Supply. DRV is the bias supply for the gate drive of the internal MOSFETs. Bypass DRV to PGND with a 1µF ceramic capacitor. DRV may be used to drive external loads up to 10mA. DRV is active whenever the input is connected and $V_{IN} > V_{UVLO}$ and $V_{SUPPLY} > (V_{BAT} + V_{SLP})$
BAT	G1–G4	11, 12	I/O	Battery Connection. Connect to the positive terminal of the battery. Additionally, bypass BAT to GND with a 1µF capacitor.
TS	G5	9	I	Battery Pack NTC Monitor. Connect TS to the center tap of a resistor divider from DRV to GND. The NTC is connected from TS to GND. The TS function provides 4 thresholds for JEITA compatibility. TS faults are reported by the I^2C interface. See the *NTC Monitor* section for more details on operation and selecting the resistor values.
STAT	G6	8	O	Status Output. STAT is an open-drain output that signals charging status and fault interrupts. STAT pulls low during charging. STAT is high impedance when charging is complete or the charger is disabled. When a fault occurs, a 128µs pulse is sent out as an interrupt for the host. STAT is enabled /disabled using the EN_STAT bit in the control register. Connect STAT to a logic rail using an LED for visual indication or through a 10kΩ resistor to communicate with the host processor.
Thermal PAD	—	Pad	—	There is an internal electrical connection between the exposed thermal pad and the VSS pin of the device. The thermal pad must be connected to the same potential as the VSS pin on the printed circuit board. Do not use the thermal pad as the primary ground input for the device. VSS pin must be connected to ground at all times.

TYPICAL APPLICATION CIRCUIT

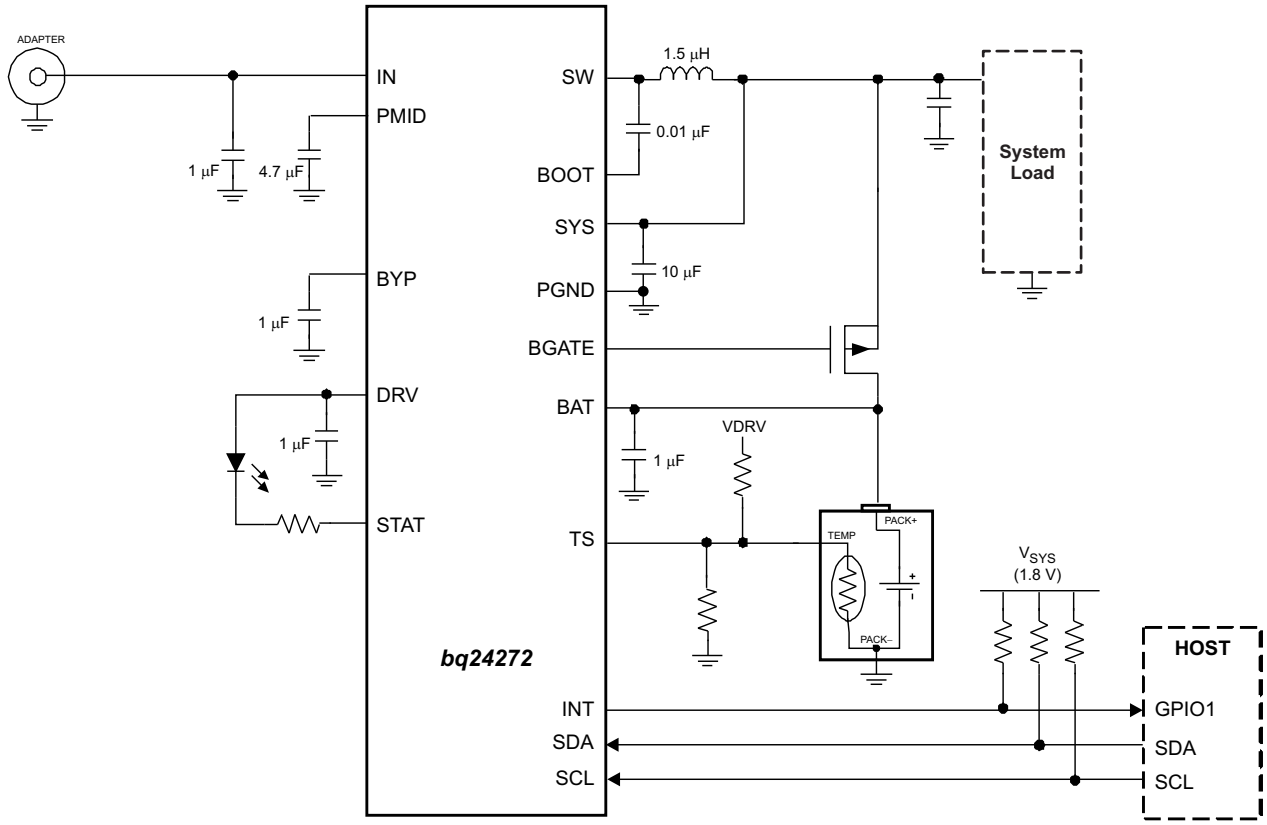


Figure 1. bq24272 Application Circuit, External Discharge FET Connected

DETAILED DESCRIPTION

The bq24272 is a highly integrated single cell Li-Ion battery charger and system power path management devices targeted for space-limited, portable applications with high capacity batteries. The single-input, single cell charger operates from a dedicated power source (i.e. wall adapter or wireless power input).

The power path management feature allows the bq24272 to power the system from a high efficiency DC to DC converter while simultaneously and independently charging the battery. The charger monitors the battery current at all times and reduces the charge current when the system load requires current above the input current limit. This allows for proper charge termination and enables the system to run with a defective or absent battery pack. Additionally, this enables instant system turn-on even with a totally discharged battery or no battery. The power-path management architecture also permits the battery to supplement the system current requirements when the adapter cannot deliver the peak system currents. This enables the use of a smaller adapter. The charge parameters are programmable using the I2C interface.

The battery is charged in three phases: conditioning, constant current and constant voltage. In all charge phases, an internal control loop monitors the IC junction temperature and reduces the charge current if the internal temperature threshold is exceeded.

Charge Mode Operation

Charge Profile

The internal battery MOSFET is used to charge the battery. When the battery is above the MINSYS voltage, the internal FET is on to maximize efficiency and the PWM converter regulates the charge current into the battery. When battery is less than MINSYS, the SYS is regulated to $V_{SYS(REG)}$ and battery is charged using the battery FET to regulate the charge current. There are 5 loops that influence the charge current:

- Constant current loop (CC)
- Constant voltage loop (CV)
- Thermal-regulation loop
- Minimum system-voltage loop (MINSYS)
- Input-voltage dynamic power-management loop (VIN-DPM)

During the charging process, all five loops are enabled and the one that is dominant takes control. The bq24272 supports a precision Li-Ion or Li-Polymer charging system for single-cell applications. The Dynamic Power Path Management (DPPM) feature regulates the system voltage to a minimum of VMINSYS, so that startup is enabled even for a missing or deeply discharged battery. Figure 2 shows a typical charge profile including the minimum system output voltage feature.

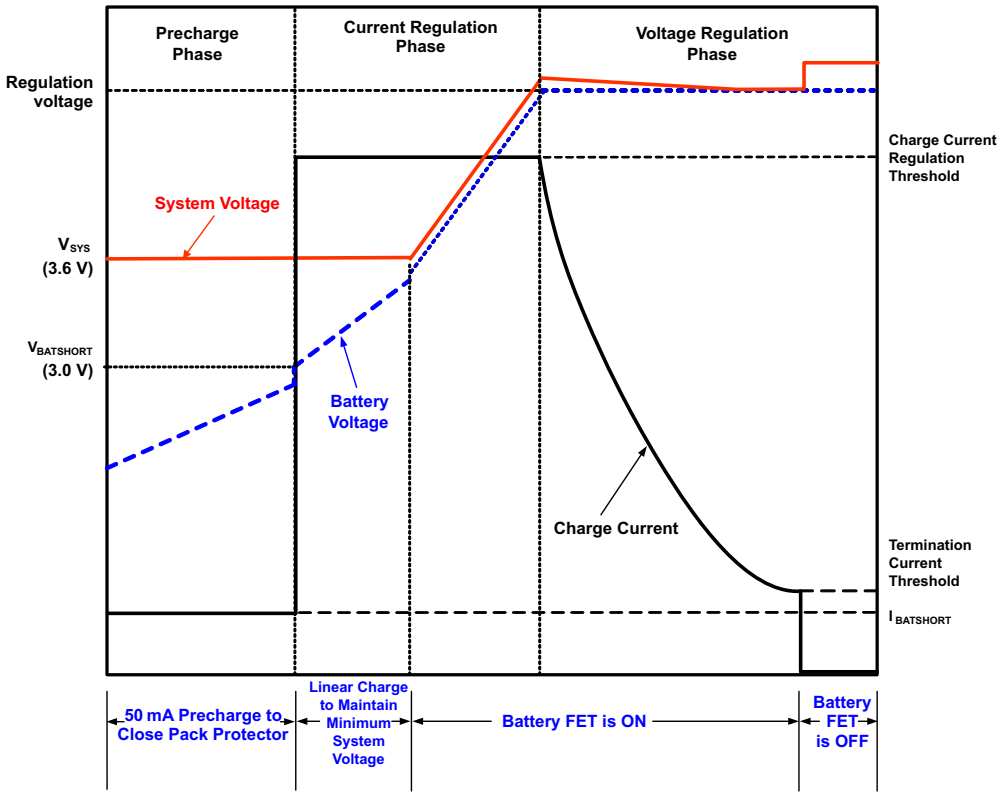


Figure 2. Typical Charging Profile for bq24272

PWM Controller in Charge Mode

The bq24272 provides an integrated, fixed-frequency 1.5MHz voltage-mode controller to power the system and supply the charge current. The voltage loop is internally compensated and provides enough phase margin for stable operation, allowing the use of small ceramic capacitors with very low ESR. The input scheme for the bq24272 prevents battery discharge when the supply voltages are lower than V_{BAT}. The high-side N-MOSFET (Q1) switches to control the power delivered to the output. The DRV LDO provides a supply for the gate drive for the low side MOSFET, while a bootstrap circuit (BST) with an external bootstrap capacitor is used to boost up the gate drive voltage for Q1.

The input is protected by a cycle-by-cycle current limit that is sensed through the internal sense MOSFETs for Q1. The threshold for the current limit is set to a nominal 5-A peak current. The input also utilizes an input current limit that limits the current from the power source.

Battery Charging Process

When the battery is deeply discharged or shorted (V_{BAT}<$V_{BATSHRT}$), the bq24272 applies $I_{BATSHRT}$ for t_{DETECT} to close the pack protector switch and bring the battery voltage up to acceptable charging levels. During this time, the battery FET is linearly regulated and the system output is regulated to $V_{SYS(REG)}$. Once the battery rises above $V_{BATSHRT}$, the charge current is regulated to the value set in the I^2C register. The battery FET is linearly regulated to maintain the system voltage. Under normal conditions, the time spent in this region is a very short percentage of the total charging time, so the linear regulation of the charge current does not affect the overall charging efficiency for very long. If the die temperature does heat up, the thermal regulation circuit reduces the charge current to maintain a die temperature less than 125°C. If the current limit for the SYS output is reached (limited by the input current limit, or V_{IN_DPM}), the SYS output drops to the V_{MINSYS} output voltage. When this happens, the current is reduced to provide the system with all the current that is needed while maintaining the minimum system voltage. If the charge current is reduced to 0mA, pulling further current from SYS causes the output to fall to the battery voltage and enter supplement mode (see the *"Dynamic Power Path Management"* section for more details).

Once the battery is charged enough to where the system voltage begins to rise above $V_{SYS(REG)}$ (approximately 3.5V), the battery FET is turned on fully and the battery is charged with the full programmed charge current set by the I^2C interface, I_{CHARGE}. The slew rate for fast charge current is controlled to minimize the current and voltage over-shoot during transient. The charge current is regulated to I_{CHARGE} until the battery is charged to the regulation voltage. Once the battery voltage is close to the regulation voltage, V_{BATREG}, the charge current is tapered down as shown in Figure 1 while the SYS output remains connected to the battery. The voltage regulation feedback occurs by monitoring the battery-pack voltage between the BAT and PGND pins. The V_{BATREG} is targeted for single-cell voltage batteries and has an adjustable regulation voltage (3.5V to 4.44V) programmed using the I^2C interface.

The bq24272 monitors the charging current during the voltage regulation phase. Once the termination threshold, I_{TERM}, is detected and the battery voltage is above the recharge threshold, the bq24272 terminates charge and turns off the battery charging FET and enters battery detection. If a battery is detected (See *Battery Detection* section), the bq24272 enters charge done. The system output is regulated to the $V_{SYS(REG)}$ and supports the full current available from the input and the battery supplement mode is available (see the *"Dynamic Power Path Management"* section for more details). The termination current level is programmable. To disable the charge current termination, the host sets the charge termination bit (TE) of charge control register to 0, refer to *I^2C section* for details.

A new charge cycle is initiated when one of the following conditions is detected:

1. The battery voltage falls below the V_{BATREG}-V_{RCH} threshold.
2. V_{IN} toggle
3. CE bit toggle or RESET bit is set
4. HI-Z bit toggle

Battery Detection

When termination conditions are met, a battery detection cycle is started. During battery detection, I_{DETECT} is pulled from V_{BAT} for t_{DETECT} to verify there is a battery. If the battery voltage remains above V_{DETECT} for the full duration of t_{DETECT}, a battery is determined to present and the IC enters "Charge Done". If V_{BAT} falls below V_{DETECT}, a *"Battery Not Present"* fault is signaled and battery detection continues. The next cycle of battery detection, the bq24272 turns on $I_{BATSHORT}$ for t_{DETECT}. If V_{BAT} rises to V_{DETECT}, the current source is turned off and after t_{DETECT}, the battery detection continues through another current sink cycle. Battery detection continues until charge is disabled or a battery is detected. Once a battery is detected, the fault status clears and a new charge cycle begins. Battery detection is not run when termination is disabled.

Dynamic Power Path Management (DPPM)

The bq24272 features a SYS output that powers the external system load connected to the battery. This output is active whenever a source is connected to IN or BAT. The following sections discuss the behavior of SYS with a source connected to the supply or a battery source only.

Input Source Connected

When a valid input source is connected, the buck converter turns on to power the load on SYS. The STAT/INT show an interrupt with 128µs pulse to tell the host that something has changed. The FAULT bits read normal, and the Supply Status register shows that a new supply is connected. The $\overline{CE}$ bit (bit 1) in the control register (0x02) determines whether a charge cycle is initiated. By default, the bq24272 (/CE=0) enables a charge cycle when a valid input source is connected. When the $\overline{CE}$ bit is 1 and a valid input source is connected, the battery FET is turned off and the SYS output is regulated to the $V_{SYS(REG)}$ programmed by the V_{BATREG} threshold in the I^2C register. A charge cycle is initiated when the $\overline{CE}$ bit is written to a 0.

When the $\overline{CE}$ bit is a 0 and a valid source is connected to IN, the buck converter starts up and a charge cycle is initiated. When V_{BAT} is high enough that V_{SYS} is > $V_{SYS(REG)}$, the battery FET is turned on and the SYS output is connected to BAT. If the SYS voltage falls to $V_{SYS(REG)}$, it is regulated to that point to maintain the system output even with a deeply discharged or absent battery. In this mode, the SYS output voltage is regulated by the buck converter and the battery FET linearly regulates the charge current into the battery. The current from the supply is shared between charging the battery and powering the system load at SYS. The dynamic power path

management (DPPM) circuitry of the bq24272 monitors the current limits continuously and if the SYS voltage falls to the V_{MINSYS} voltage, it adjusts charge current to maintain the minimum system voltage and supply the load on SYS. If the charge current is reduced to zero and the load increases further, the bq24272 enters battery supplement mode. During supplement mode, the battery FET is turned on and the battery supplements the system load.

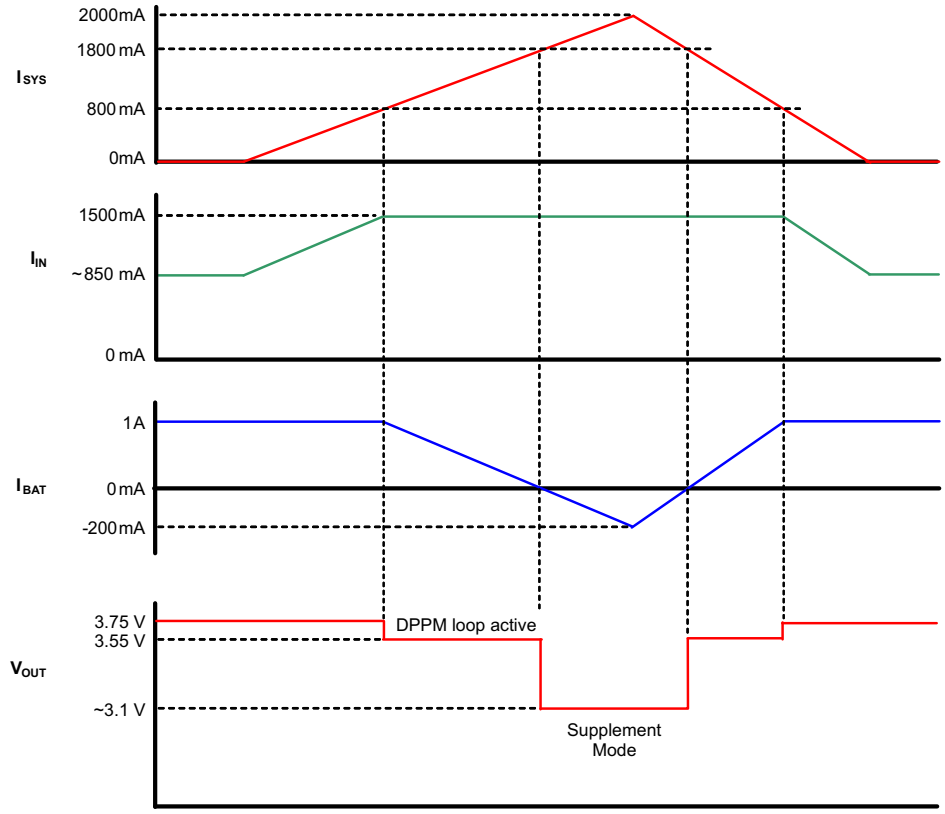


Figure 3. Example DPPM Response (V_{Supply}=5V, VBAT = 3.1V, 1.5A Input current limit)

$V_{BAT(REG)}$ should never be programmed less than V_{BAT}. If the battery is ever 5% above the regulation threshold, the battery OVP circuit shuts the PWM converter off and the battery FET is turned on to discharge the battery to safe operating levels. Battery OVP errors are shown in the I^2C status registers.

Battery Only Connected

When a battery voltage > $V_{BATUVLO}$ is connected with no input source, the battery FET is turned on similar to supplement mode. In this mode, the current is not regulated; however, there is a short circuit current limit. If the short circuit limit is reached, the battery FET is turned off for the deglitch time. After the deglitch time, the battery FET is turned on to test and see if the short has been removed. If it has not, the FET turns off and the process repeats until the short is removed. This process is to protect the internal FET from over current. If an external FET is used for discharge, the body diode prevents the load on SYS from being disconnected from the battery. If the battery voltage is less than $V_{BATUVLO}$, the battery FET (Q3) remains off and BAT is high-impedance. This prevents further discharging deeply discharged batteries.

Battery Discharge FET (BGATE)

The bq24272 contains a MOSFET driver to drive an external discharge FET between the battery and the system output. This external FET provides a low impedance path when supplying the system from the battery. Connect BGATE to the gate of the external discharge MOSFET. BGATE is on under the following conditions:

1. No input supply connected.
2. HZ_MODE = 1
3. CD pin connected high

DEFAULT Mode

DEFAULT mode is used when I^2C communication is not available. DEFAULT mode is entered in the following situations:

1. When the charger is enabled and V_{BAT}<3.6V before I^2C communication is established
2. When the watchdog timer expires without a reset from the I^2C interface and the safety timer has not expired.
3. When the device comes out of any fault condition (sleep mode, OVP, faulty adapter mode, etc.) before I^2C communication is established

In default mode, the I^2C registers are reset to the default values. The 27 min safety timer is reset and starts when DEFAULT mode is entered. The default value for V_{BATREG} is 3.6V, and the default value for I_{CHARGE} is 1A. The input current limit is 1.5A by default. DEFAULT mode is exited by programming the I^2C interface. Note that if termination is enabled and charging has terminated, a new charge cycle is **NOT** initiated when entering DEFAULT mode.

Safety Timer and Watchdog Timer

At the beginning of charging process, the bq24272 starts the safety timer. This timer is active during the entire charging process. If charging has not terminated before the safety timer expires, charging is halted and the $\overline{CE}$ bit is written to a "1". The length of the safety timer is selectable using the I^2C interface. A single 128µs pulse is sent on the STAT and INT outputs and the STATx bits of the status registers are updated in the I^2C. The $\overline{CE}$ bit must be toggled in order to clear the safety timer fault. The safety timer duration is selectable using the TMR_X bits in the Safety Timer Register/NTC Monitor register. Changing the safety timer duration resets the safety timer. If the safety timer expires, charging is disabled ($\overline{CE}$ changed to a "1"). This function prevents continuous charging of a defective battery if the host fails to reset the safety timer.

In addition to the safety timer, the bq24272 contains a watchdog timer that monitors the host through the I^2C interface. Once a read/write is performed on the I^2C interface, a 30-second timer ($t_{WATCHDOG)}$ is started. The 30-second timer is reset by the host using the I^2C interface. This is done by writing a "1" to the reset bit (TMR_RST) in the control register. The TMR_RST bit is automatically set to "0" when the 30-second timer is reset. This process continues until battery is fully charged or the safety timer expires. If the 30-second timer expires, the IC enters DEFAULT mode where the default register values are loaded, the safety timer restarts at 27minutes and charging continues. The I^2C may be accessed again to reinitialize the desired values and restart the watchdog timer as long as the 27 minute safety timer has not expired. The watchdog timer flow chart is shown in Figure 4.

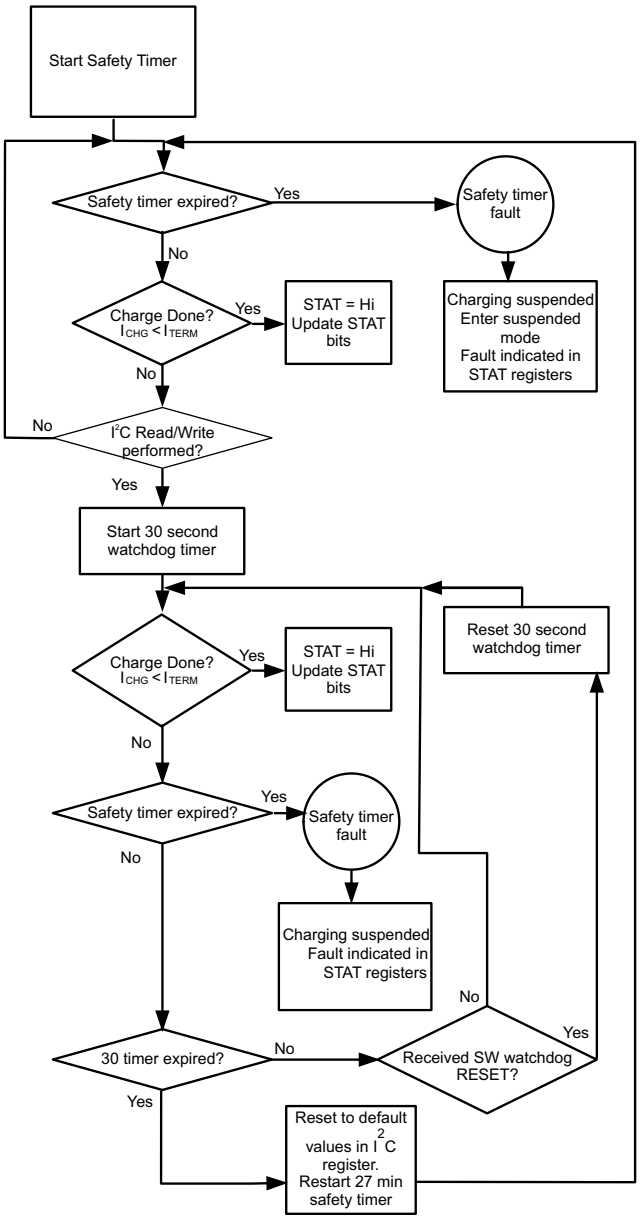


Figure 4. The Watchdog Timer Flow Chart for bq24272

Hardware Chip Disable Input (CD)

The bq24272 contain a CD input pin that is used to disable the IC and place the bq24272 into high-impedance mode. Drive CD low to enable charge and enter normal operation. Drive CD high to disable charge and place the bq24272 into high-impedance mode. Driving CD high during DEFAULT mode resets the safety timer. Driving CD high during HOST mode resets the safety timer.

LDO Output (DRV)

The bq24272 contains a linear regulator (DRV) that is used to supply the internal MOSFET drivers and other circuitry. Additionally, DRV supplies up to 10mA external loads to power the STAT LED or the USB transceiver circuitry. The maximum value of the DRV output is 5.45V so it ideal for protecting voltage sensitive USB circuits from high voltage fluctuations in the supply. The LDO is on whenever a supply is connected to the IN input of the bq24272. The DRV is disabled under the following conditions:

1. V_{IN} < UVLO

2. $V_{IN} < V_{SLP} + V_{BAT}$
3. Thermal Shutdown

External NTC Monitoring (TS)

The I^2C interface allows the user to easily implement the JEITA standard for systems where the battery pack thermistor is monitored by the host. Additionally, the bq24272 provides a flexible, voltage based TS input for monitoring the battery pack NTC thermistor. The voltage at TS is monitored to determine that the battery is at a safe temperature during charging. The bq24272 enables the user to easily implement the JEITA. The JEITA specification is shown in Figure 5.

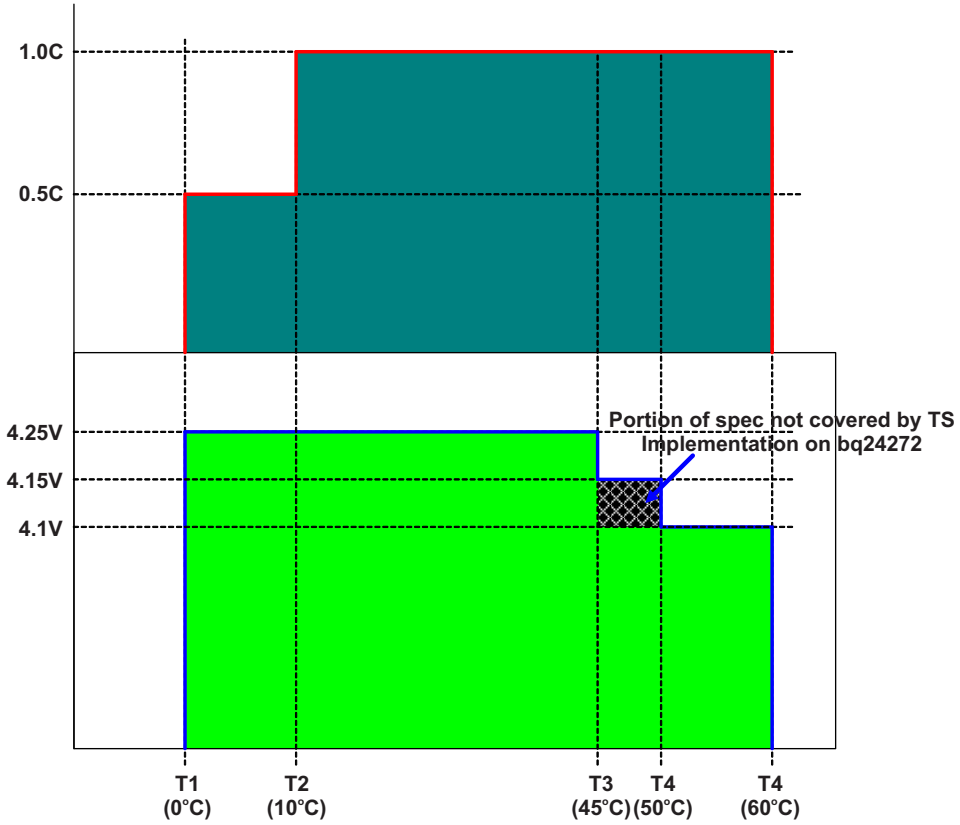


Figure 5. Charge Current/Voltage During TS Conditions

The TS function is voltage based for maximum flexibility. Connect a resistor divider from DRV to GND with TS connected to the center tap to set the threshold. The connections are shown in Figure 6. The resistor values are calculated using the following equations:

$$RLO = \frac{V_{DRV} \times RCOLD \times RHOT \times \left[\frac{1}{V_{COLD}} - \frac{1}{V_{HOT}}\right]}{RHOT \times \left[\frac{V_{DRV}}{V_{HOT}} - 1\right] - RCOLD \times \left[\frac{V_{DRV}}{V_{COLD}} - 1\right]} \quad (1)$$

$$RHI = \frac{\frac{V_{DRV}}{V_{COLD}} - 1}{\frac{1}{RLO} + \frac{1}{RCOLD}} \quad (2)$$

Where:

$V_{COLD} = 0.60 \times V_{DRV}$
$V_{HOT} = 0.60 \times V_{DRV}$

Where RHOT is the NTC resistance at the hot temperature and RCOLD is the NTC resistance at cold temperature.

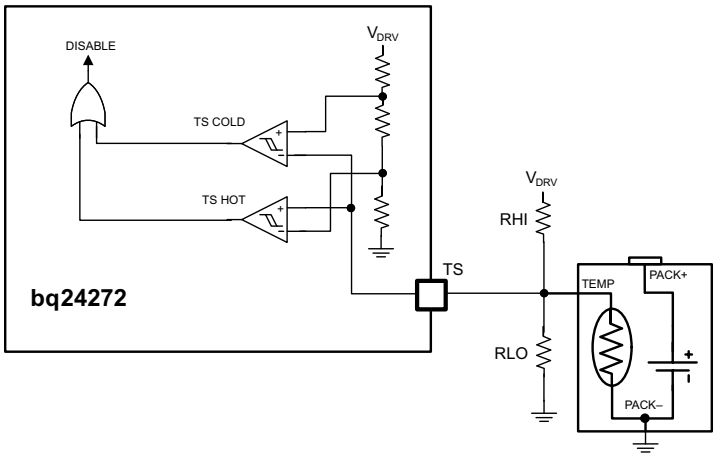


Figure 6. TS Circuit

If the TS function is not used, connect TS to DRV directly to disable the feature. Additionally, the TS function can be disabled in the I^2C by writing to the EN_TS bit. When the TS is disabled, the status registers always read "Normal".

Thermal Regulation and Protection

During the charging process, to prevent chip overheating, bq24272 monitors the junction temperature, T_J, of the die and begins to taper down the charge current once T_J reaches the thermal regulation threshold, T_{REG}. The charge current is reduced to zero when the junction temperature increases about 10°C above T_{REG}. Once the charge current is reduced, the system current is reduced while the battery supplements the load to supply the system. This may cause a thermal shutdown of the bq24272 if the die temperature rises too high. At any state, if T_J exceeds T_{SHTDWN}, bq24272 suspends charging and disables the buck converter. During thermal shutdown mode, the PWM is turned off, all timers are suspended, and a single 128µs pulse is sent on the STAT and INT outputs and the STATx and FAULT_x bits of the status registers are updated in the I^2C. A new charging cycle begins when T_J falls below T_{SHTDWN} by approximately 10°C.

Input Voltage Protection in Charge Mode

Sleep Mode

The bq24272 enters the low-power sleep mode if the voltage on V_{IN} falls below sleep-mode entry threshold, V_{BAT}+V_{SLP}, and V_{VBUS} is higher than the undervoltage lockout threshold, V_{UVLO}. This feature prevents draining the battery during the absence of V_{IN}. When V_{IN} < V_{BAT}+ V_{SLP}, the bq24272 turns off the PWM converter, turns the battery FET on and drives BGATE to GND, sends a single 128µs pulse on the STAT and INT outputs and updates the STATx and FAULT_x bits in the status registers. Once V_{IN} > V_{BAT}+ V_{SLP}, the STATx and FAULT_x bits are cleared and the device initiates a new charge cycle.

Input Voltage Based DPM

During normal charging process, if the input power source is not able to support the programmed or default charging current, the supply voltage will decease. Once the supply drops to V_{IN_DPM} (default 4.2V), the input current limit is reduced down to prevent further supply droop. When the IC enters this mode, the charge current is lower than the set value and the DPM_STATUS bit is set (Bit 5 in Register 05H). This feature ensures IC compatibility with adapters with different current capabilities without a hardware change. Figure 7 shows the V_{IN-DPM} behavior to a current limited source. In this figure the input source has a 750mA current limit and the charging is set to 750mA. The SYS load is then increased to 1.2A.

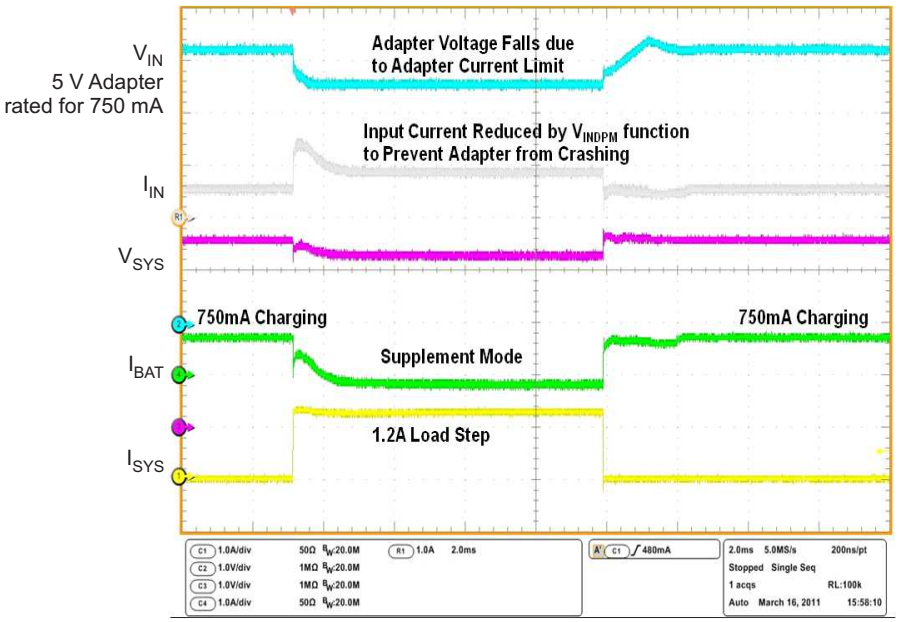


Figure 7. bq24272 V_{IN}-DPM

Bad Source Detection

When a source is connected to IN, the bq24272 runs a Bad Source Detection procedure to determine if the source is strong enough to provide some current to charge the battery. A current sink is turned on (75mA) for 32ms. If the source is valid after the 32ms ($V_{BADSOURCE}$ < V_{IN} < V_{OVP}), the buck converter starts up and normal operation continues. If the supply voltage falls below V_{BAD_SOURCE} during the detection, the current sink shuts off for 2s and then retries, a single 128µs pulse is sent on the STAT and INT outputs and the STATx and FAULT_x bits of the status registers and the battery/supply status registers are updated in the I^2C. The detection circuits retries continuously until either a new source is connected to the other input or a valid source is detected after the detection time. If during normal operation the source falls to V_{BAD_SOURCE}, the bq24272 turns off the PWM converter, turns the battery FET and BGATE on, sends a single 128µs pulse is sent on the STAT and INT outputs and the STATx and FAULT_x bits of the status registers and the battery/supply status registers are updated in the I^2C. Once a good source is detected, the STATx and FAULT_x bits are cleared and the device returns to normal operation.

Input Over-Voltage Protection

The bq24272 provides over-voltage protection on the input that protects downstream circuitry. The built-in input over-voltage protection to protect the device and other components against damage from overvoltage on the input supply (Voltage from V_{IN} to PGND). During normal operation, if V_{IN} > V_{OVP}, the bq24272 turns off the PWM converter, turns the battery FET and BGATE on, sends a single 128µs pulse is sent on the STAT and INT outputs and the STATx and FAULT_x bits of the status registers and the battery/supply status registers are updated in the I^2C. Once the OVP fault is removed, the STATx and FAULT_x bits are cleared and the device returns to normal operation.

Charge Status Outputs (STAT, INT)

The STAT output is used to indicate operation conditions for bq24272. STAT is pulled low during charging when EN_STAT bit in the control register (0x02h) is set to “1”. When charge is complete or disabled, STAT is high impedance. When a fault occurs, a 128-µs pulse (interrupt) is sent out to notify the host. The status of STAT during different operation conditions is summarized in Table 1. STAT drives an LED for visual indication or can be connected to the logic rail for host communication. The EN_STAT bit in the control register (00H) is used to enable/disable the charge status for STAT. The interrupt pulses are unaffected by EN_STAT and will always be shown. The INT output is identical to STAT and is used to interface with a low voltage host processor.

Table 1. STAT Pin Summary

CHARGE STATE	STAT AND INT BEHAVIOR
Charge in progress and EN_STAT=1	Low
Other normal conditions	High-Impedance
Status Changes: Supply Status Change (plug in or removal), safety timer fault, watchdog expiration, sleep mode, battery temperature fault (TS), battery fault (OVP or absent), thermal shutdown	128-µs pulse, then High Impedance

REGISTER DESCRIPTION

Status/Control Register (READ/WRITE)
Memory location: 00, Reset state: 0xxx 0xxx

BIT	NAME	Read/Write	FUNCTION
B7(MSB)	TMR_RST	Read/Write	Write: TMR_RST function, write “1” to reset the watchdog timer (auto clear) Read: Always 0
B6	STAT_2	Read only	000- No Valid Source Detected 001- IN Ready 010- NA 011- Charging 100- 101- Charge Done 110- NA 111- Fault
B5	STAT_1	Read only	
B4	STAT_0	Read only	
B3	NA	Read/Write	NA
B2	FAULT_2	Read only	000-Normal 001- Thermal Shutdown 010- Battery Temperature Fault 011- Watchdog Timer Expired 100- Safety Timer Expired 101- Supply Fault 110- NA 111- Battery Fault
B1	FAULT_1	Read only	

Battery/ Supply Status Register (READ/WRITE)
Memory location: 01, Reset state: xxxx 0xxx

BIT	NAME	Read/Write	FUNCTION
B7(MSB)	STAT1	Read Only	00-Normal 01-Supply OVP 10-Weak Source Connected (No Charging) 11- $V_{IN}<V_{UVLO}$
B6	STAT0	Read Only	
B5	NA	Read Only	NA
B4	NA	Read Only	NA
B3	NA	Read/Write	NA
B2	BATSTAT1	Read Only	00-Battery Present and Normal 01-Battery OVP 10-Battery Not Present 11- NA
B1	BATSTAT0	Read Only	
B0 (LSB)	EN_NOBATOP	Read/ Write	0-Normal Operation 1-Enables No Battery Operation when termination is disabled (default 0)

EN_NOBATOP (No Battery Operation with Termination Disabled)

The EN_NOBATOP bit is used to enable operation when termination is disabled and no battery is connected. This is useful for cases where the PA is connected to the BAT pin and it desired to do a GSM calibration in the factory. For this application, the TE bit (Bit 2 in Register 0x02h) should be set to a “0” to disable termination and the EN_NOBATOP should be set to a “1”. This feature should not be used during normal operation as it disables the BATOVP and the reverse boost protection circuits.

Control Register (READ/WRITE)
Memory location: 02, Reset state: 1000 1100

BIT	NAME	Read/Write	FUNCTION
B7(MSB)	RESET	Write Only	Write: 1-Reset all registers to default values 0-No effect Read: always get “1”
B6	NA	Read Only	NA
B5	NA	Read/Write	NA
B4	NA	Read/Write	NA
B3	EN_STAT	Read/Write	1-Enable STAT output to show charge status, 0-Disable STAT output for charge status. Fault interrupts are still show even when EN_STAT = 0. (default 1)
B2	TE	Read/Write	1-Enable charge current termination, 0-Disable charge current termination (default 1)
B1	$\overline{CE}$	Read/Write	1-Charger is disabled 0-Charger enabled (default 0)
B0 (LSB)	HZ_MODE	Read/Write	1-High impedance mode 0-Not high impedance mode (default 0)

RESET Bit

The RESET bit in the control register (0x02h) is used to reset all the charge parameters. Write “1” to RESET bit to reset all the registers to default values and place the bq24272 into DEFAULT mode and turn off the watchdog timer. The RESET bit is automatically cleared to zero once the bq24272 enters DEFAULT mode.

$\overline{CE}$ Bit (Charge Enable)

The $\overline{CE}$ bit in the control register (0x02h) is used to disable or enable the charge process. A low logic level (0) on this bit enables the charge and a high logic level (1) disables the charge. When charge is disabled, the SYS output regulates to VSYS(REG) and battery is disconnected from the SYS. Supplement mode is still available if the system load demands cannot be met by the supply. BGATE is high impedance when $\overline{CE}$ is high.

HZ_MODE Bit (High Impedance Mode Enable)

The HZ_MODE bit in the control register (0x02h) is used to disable or enable the high impedance mode. A low logic level (0) on this bit enables the IC and a high logic level (1) puts the IC in a low quiescent current state called high impedance mode. When in high impedance mode, the converter is off and the battery FET and BGATE are on. The load on SYS is supplied by the battery.

Control/Battery Voltage Register (READ/WRITE)
Memory location: 03, Reset state: 0001 0100

BIT	NAME	Read/Write	FUNCTION
B7(MSB)	V_{BREG5}	Read/Write	Battery Regulation Voltage: 640mV (default 0)
B6	V_{BREG4}	Read/Write	Battery Regulation Voltage: 320mV (default 0)
B5	V_{BREG3}	Read/Write	Battery Regulation Voltage: 160mV (default 0)
B4	V_{BREG2}	Read/Write	Battery Regulation Voltage: 80mV (default 1)
B3	V_{BREG1}	Read/Write	Battery Regulation Voltage: 40mV (default 0)
B2	V_{BREG0}	Read/Write	Battery Regulation Voltage: 20mV (default 1)
B1	$I_{INLIMIT\_IN}$	Read/Write	Input Limit for IN input 0 – 1.5A 1 – 2.5A (default 0)
B0(LSB)	NA	Read/Write	NA

- Charge voltage range is 3.5V–4.44V with the offset of 3.5V and step of 20mV (default 3.6V).

Vender/Part/Revision Register (READ only)
Memory location: 04, Reset state: 0100 0000

BIT	NAME	Read/Write	FUNCTION
B7(MSB)	Vender2	Read only	Vender Code: bit 2 (default 0)
B6	Vender1	Read only	Vender Code: bit 1 (default 1)
B5	Vender0	Read only	Vender Code: bit 0 (default 0)
B4	PN1	Read only	For I^2C Address 6Bh: 00: bq24272 01 – 11: Future product spins
B3	PN0	Read only	
B2	Revision2	Read only	000: Revision 1.0 001:Revision 1.1 010: Revision 2.0 011: Revision 2.1 100: Revision 2.2 101: Revision 2.3 110-111: Future Revisions
B1	Revision1	Read only	
B0(LSB)	Revision0	Read only	

Battery Termination/Fast Charge Current Register (READ/WRITE)
Memory location: 05, Reset state: 0011 0010

BIT	NAME	Read/Write	FUNCTION
B7(MSB)	I_{CHRG4}	Read/Write	Charge current: 1200 mA – (default 0)
B6	I_{CHRG3}	Read/Write	Charge current: 600 mA— (default 0)
B5	I_{CHRG2}	Read/Write	Charge current: 300 mA—(default 1)
B4	I_{CHRG1}	Read/Write	Charge current: 150 mA— (default 1)
B3	I_{CHRG0}	Read/Write	Charge current: 75 mA (default 0)
B2	I_{TERM2}	Read/Write	Termination current sense voltage: 200 mA (default 0)
B1	I_{TERM1}	Read/Write	Termination current sense voltage: 100 mA (default 1)
B0(LSB)	I_{TERM0}	Read/Write	Termination current sense voltage: 50 mA (default 0)

- Charge current sense offset is 550mA and default charge current is 1000mA
- Termination threshold offset is 50mA and default termination current is 150mA

V_{IN-DPM} Voltage/ DPPM Status Register
Memory location: 06, Reset state: xx00 0000

BIT	NAME	Read/Write	FUNCTION
B7(MSB)	MINSYS_STATUS	Read Only	1 – Minimum System Voltage mode is active (low battery condition) 0 – Minimum System Voltage mode is not active
B6	DPM_STATUS	Read Only	1 – V_{IN}-DPM mode is active 0 – V_{IN}-DPM mode is not active
B5	NA	Read/Write	NA
B4	NA	Read/Write	NA
B3	NA	Read/Write	NA
B2	V_{INDPM2}	Read/Write	IN input V_{IN-DPM} voltage: 320 mV (default 0)
B1	V_{INDPM1}	Read/Write	IN input V_{IN-DPM} voltage: 160 mV (default 0)
B0(LSB)	V_{INDPM0}	Read/Write	IN input V_{IN-DPM} voltage: 80 mV (default 0)

- V_{IN-DPM} voltage offset is 4.20 V and default V_{IN-DPM} threshold is 4.20 V.

Safety Timer/ NTC Monitor Register (READ/WRITE)
Memory location: 07, Reset state: 1001 1xxx

BIT	NAME	Read/Write	FUNCTION
B7(MSB)	2XTMR_EN	Read/Write	1 – Timer slowed by 2x when in thermal regulation, input current limit, V_{IN_DPM} or DPPM 0 – Timer not slowed at any time (default 0)
B6	TMR_1	Read/Write	Safety Timer Time Limit 00 – 27 minute fast charge 01 – 6 hour fast charge 10 – 9 hour fast charge 11 – Disable safety timers (default 00)
B5	TMR_2	Read/Write	
B4	NA	Read/Write	NA
B3	TS_EN	Read/Write	0 – TS function disabled 1 – TS function enabled (default 1)
B2	TS_FAULT1	Read Only	TS Fault Mode: 00 – Normal, No TS fault 01 – TS temp < T_{COLD} or TS temp > T_{HOT}(Charging suspended) 10 – T_{COOL} > TS temp > T_{COLD} (Charge current reduced by half) 11 – T_{WARM} < TS temp < T_{HOT} (Charge voltage reduced by 140mV)
B1	TS_FAULT0	Read Only	
B0(LSB)	LOW_CHG	Read/Write	0 – Charge current as programmed in Register 0x05 1 – Charge current half programmed value in Register 0x05 (default 0)

LOW_CHG Bit (Low Charge Mode Enable)

The LOW_CHG bit is used to reduce the charge current from the programmed value. This feature is used by systems where battery NTC is monitored by the host and requires a reduced charge current setting or by systems that need a “preconditioning” current for low battery voltages. Write a “1” to this bit to charge at half of the programmed charge. Write a “0” to this bit to charge at the programmed charge current.

APPLICATION INFORMATION

Output Inductor and Capacitor Selection Guidelines

When selecting an inductor, several attributes must be examined to find the right part for the application. First, the inductance value should be selected. The bq24272 is designed to work with 1.5µH to 2.2µH inductors. The chosen value will have an effect on efficiency and package size. Due to the smaller current ripple, some efficiency gain is reached using the 2.2µH inductor, however, due to the physical size of the inductor, this may not be a viable option. The 1.5µH inductor provides a good tradeoff between size and efficiency.

Once the inductance has been selected, the peak current must be calculated in order to choose the current rating of the inductor. Use equation 2 to calculate the peak current.

$$I_{PEAK} = I_{LOAD(MAX)} \times \left(1 + \frac{\%_{RIPPPLE}}{2}\right) \quad (3)$$

The inductor selected must have a saturation current rating less than or equal to the calculated I_{PEAK}. Due to the high currents possible with the bq24272, a thermal analysis must also be done for the inductor. Many inductors have 40°C temperature rise rating. This is the DC current that will cause a 40°C temperature rise above the ambient temperature in the inductor. For this analysis, the typical load current may be used adjusted for the duty cycle of the load transients. For example, if the application requires a 1.5A DC load with peaks at 2.5A 20% of the time, a Δ40°C temperature rise current must be greater than 1.7A:

$$I_{TEMPRISE} = I_{LOAD} + D \times (I_{PEAK} - I_{LOAD}) = 1.5A + 0.2 \times (2.5A - 1.5A) = 1.7A \quad (4)$$

The bq24272 provides internal loop compensation. Using this scheme, the bq24272 is stable with 10µF to 200µF of local capacitance. The capacitance on the BAT rail can be higher if distributed amongst the rail. To reduce the output voltage ripple, a ceramic capacitor with the capacitance between 10µF and 47µF is recommended for local bypass to SYS.

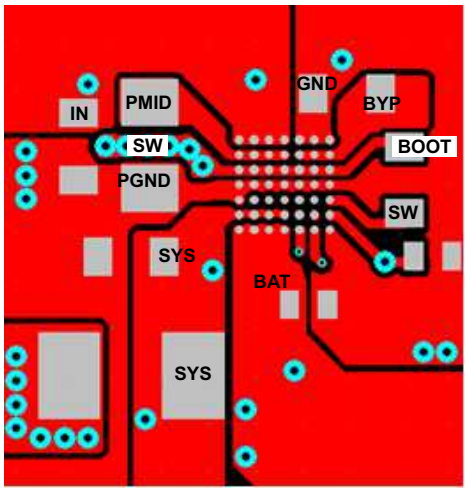
PCB Layout Guidelines

It is important to pay special attention to the PCB layout. The following provides some guidelines:

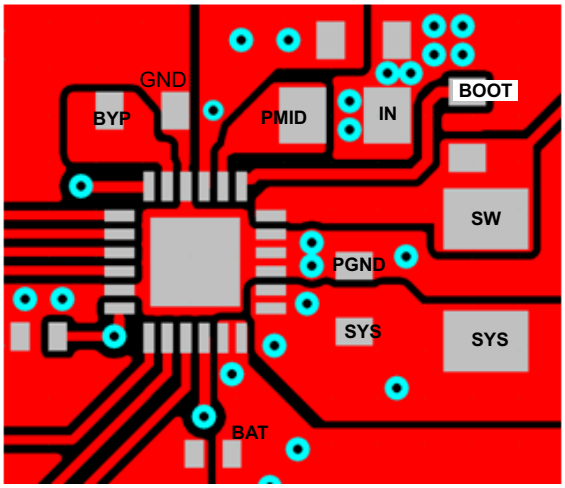
- To obtain optimal performance, the power input capacitors, connected from the PMID input to PGND, must be placed as close as possible to the bq24272
- Place 4.7µF input capacitor as close to PMID pin and PGND pin as possible to make high frequency current loop area as small as possible. Place 1µF input capacitor GNDs as close to the respective PMID cap GND and PGND pins as possible to minimize the ground difference between the input and PMID_.
- The local bypass capacitor from SYS to GND should be connected between the SYS pin and PGND of the IC. The intent is to minimize the current path loop area from the SW pin through the LC filter and back to the PGND pin.
- Place all decoupling capacitor close to their respective IC pin and as close as to PGND (do not place components such that routing interrupts power stage currents). All small control signals should be routed away from the high current paths.
- The PCB should have a ground plane (return) connected directly to the return of all components through vias (two vias per capacitor for power-stage capacitors, one via per capacitor for small-signal components). It is also recommended to put vias inside the PGND pads for the IC, if possible. A star ground design approach is typically used to keep circuit block currents isolated (high-power/low-power small-signal) which reduces noise-coupling and ground-bounce issues. A single ground plane for this design gives good results. With this small layout and a single ground plane, there is no ground-bounce issue, and having the components segregated minimizes coupling between signals.
- The high-current charge paths into IN, BAT, SYS and from the SW pins must be sized appropriately for the maximum charge current in order to avoid voltage drops in these traces. The PGND pins should be connected to the ground plane to return current through the internal low-side FET.
- For high-current applications, the balls for the power paths should be connected to as much copper in the board as possible. This allows better thermal performance as the board pulls heat away from the IC.

Sample Layout

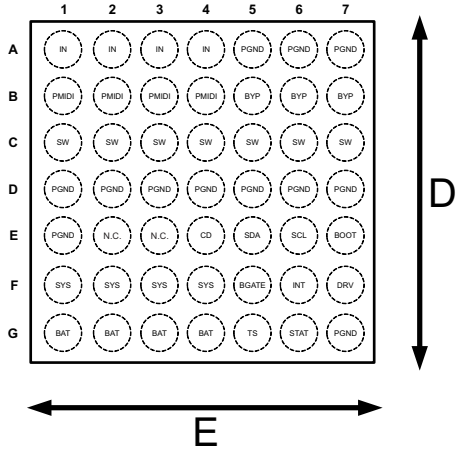
WCSP I2C PART

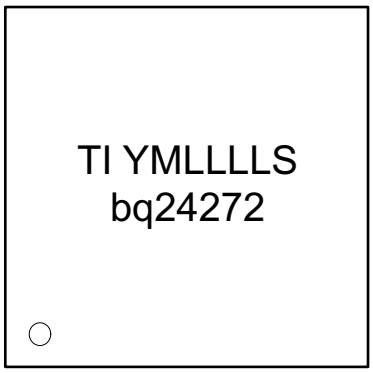


QFN I2C PART



Package Summary





0-Pin A1 Marker, TI-TI Letters, YM- Year Month Date Code, LLLL-Lot Trace Code, S-Assembly Site Code

CHIP SCALE PACKAGING DIMENSIONS

The bq2427x devices are available in a 49-bump chip scale package (YFF, NanoFree™). The package dimensions are:
D – 2.78 mm ± 0.05 mm
E – 2.78 mm ± 0.05 mm

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
BQ24272RGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ 24272	Samples
BQ24272RGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ 24272	Samples
BQ24272YFFR	ACTIVE	DSBGA	YFF	49	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ24272	Samples
BQ24272YFFT	ACTIVE	DSBGA	YFF	49	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ24272	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

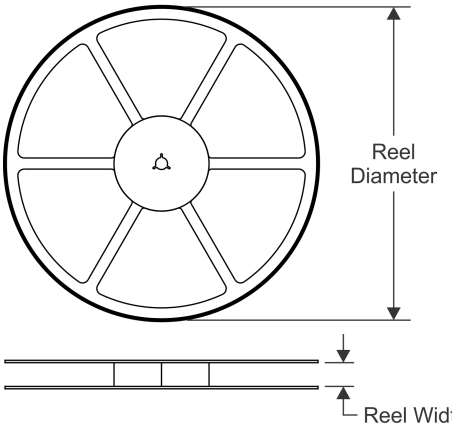
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

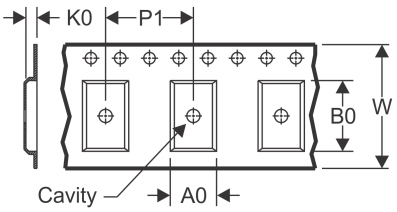
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

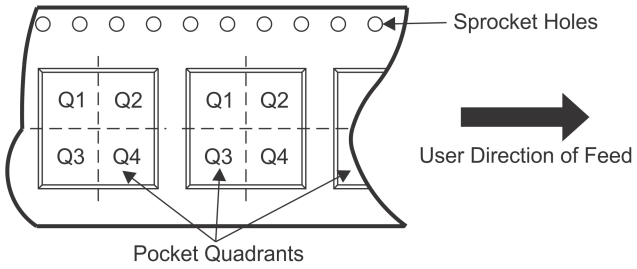


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

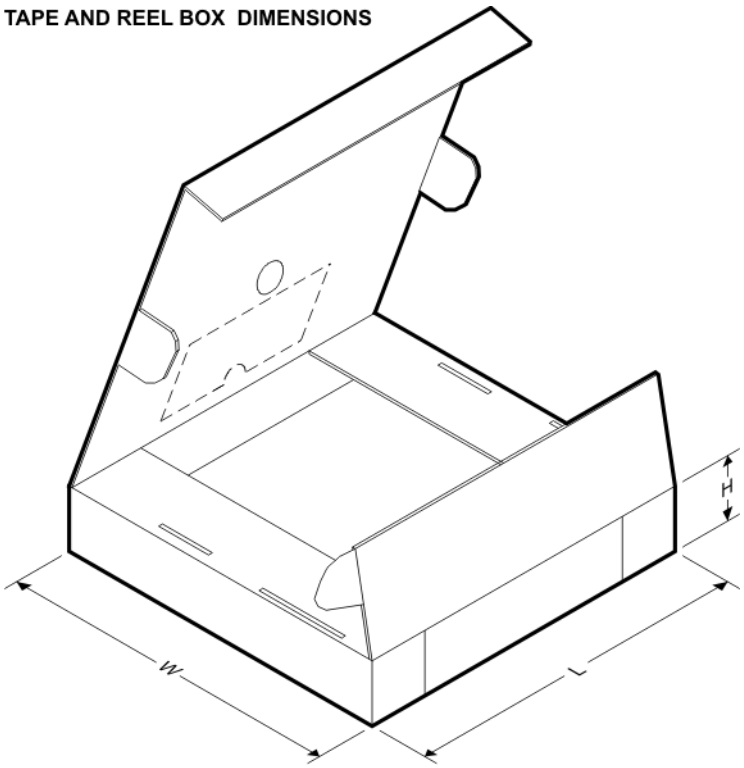
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24272RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ24272RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ24272YFFR	DSBGA	YFF	49	3000	180.0	8.4	2.93	2.93	0.81	4.0	8.0	Q1
BQ24272YFFT	DSBGA	YFF	49	250	180.0	8.4	2.93	2.93	0.81	4.0	8.0	Q1

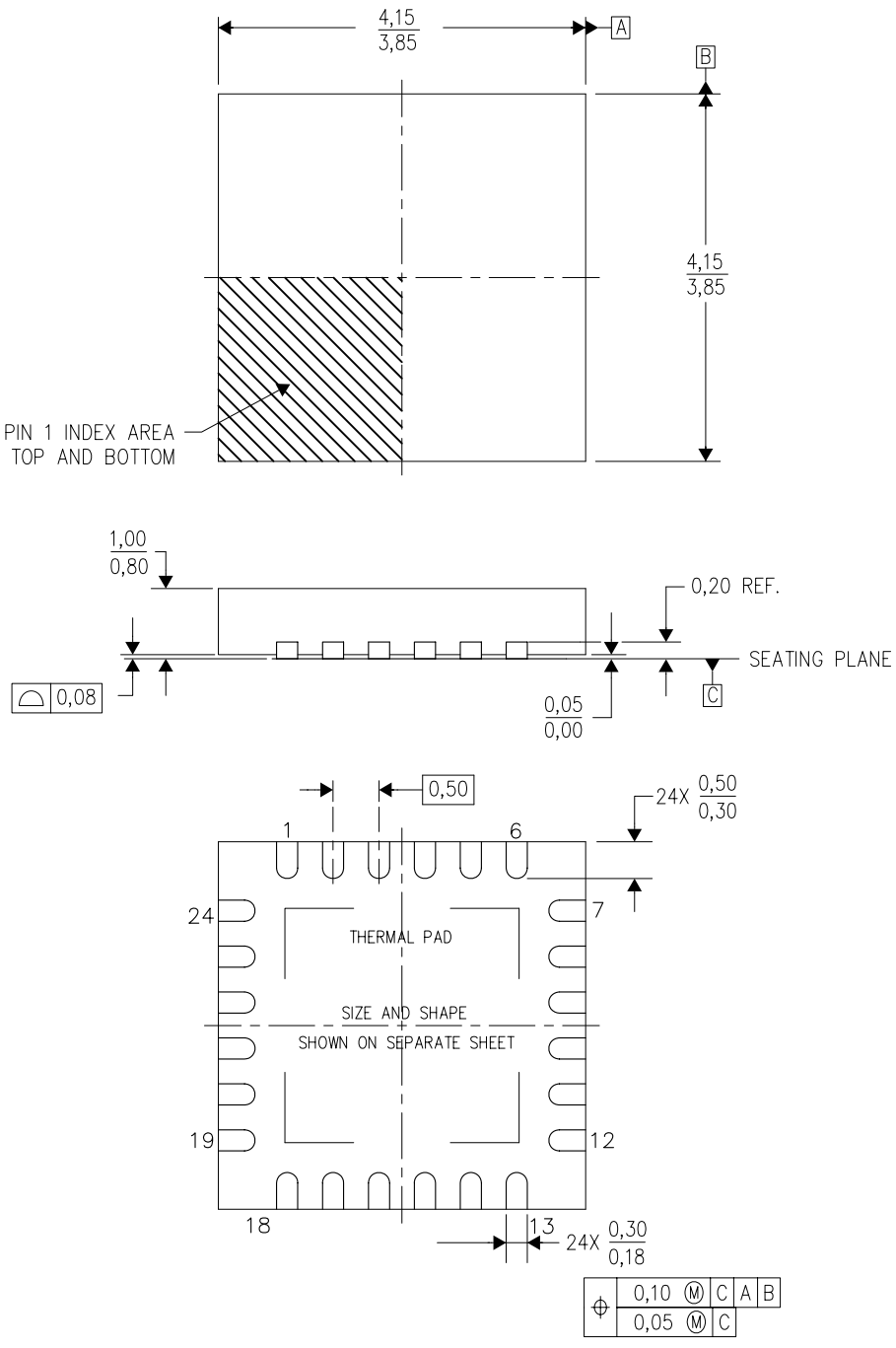
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24272RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
BQ24272RGET	VQFN	RGE	24	250	210.0	185.0	35.0
BQ24272YFFR	DSBGA	YFF	49	3000	210.0	185.0	35.0
BQ24272YFFT	DSBGA	YFF	49	250	210.0	185.0	35.0

RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

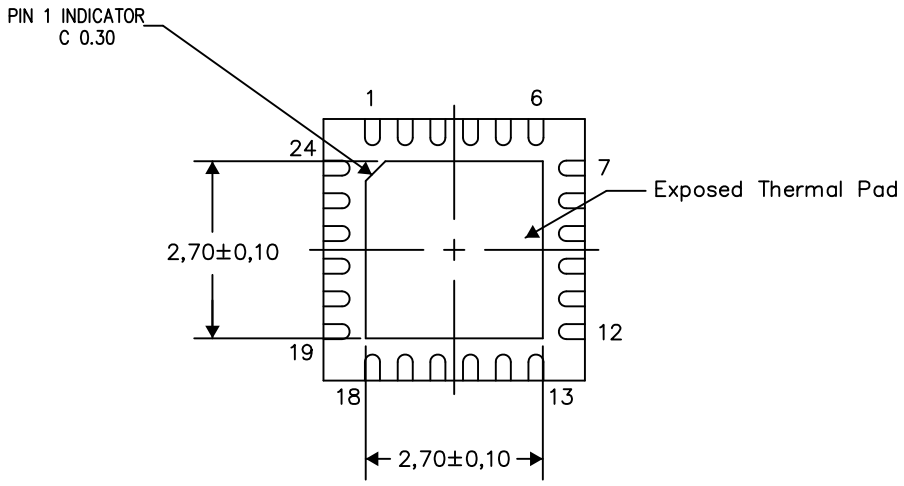
RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



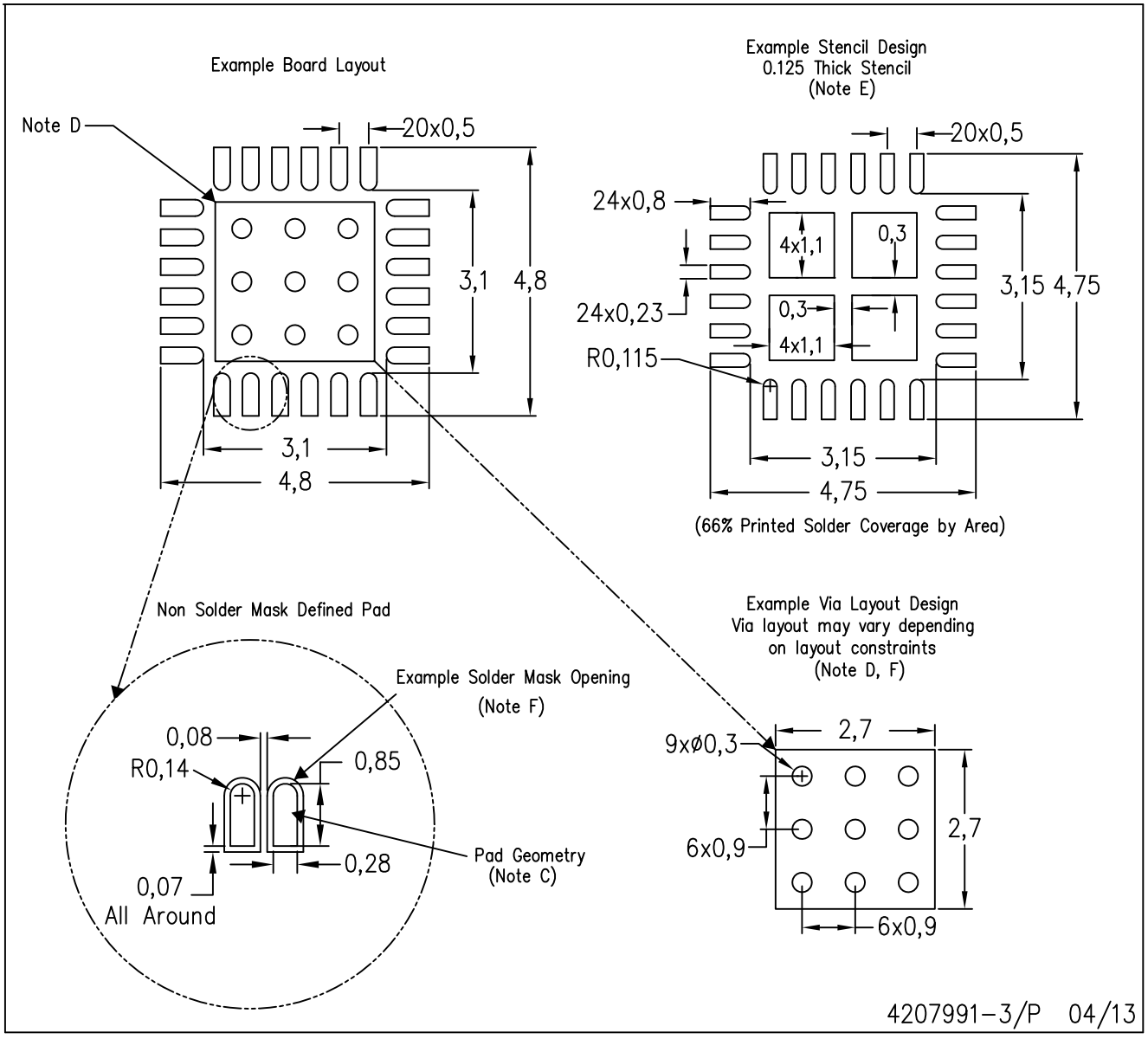
Bottom View

Exposed Thermal Pad Dimensions

4206344–4/AD 04/13

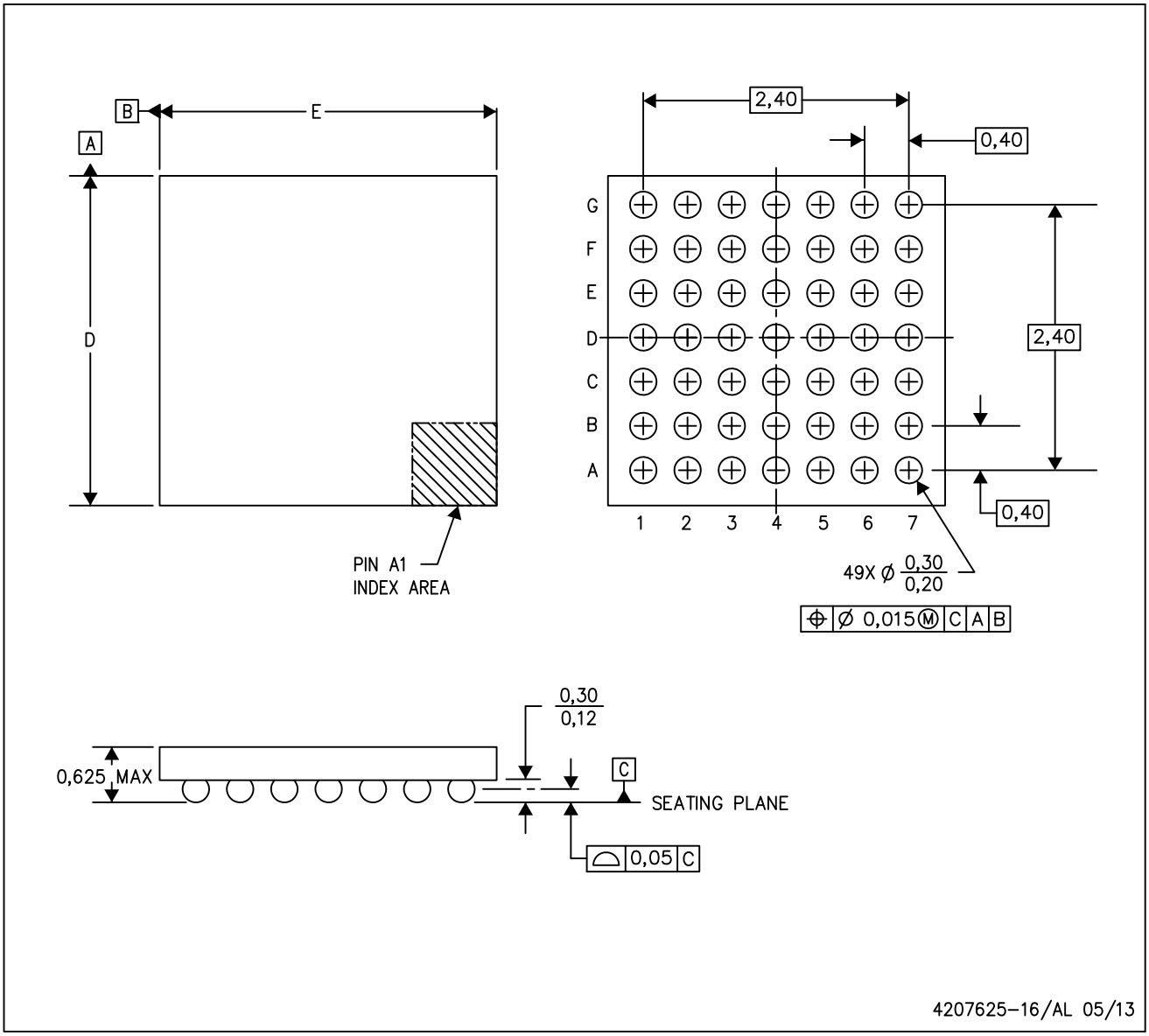
NOTES: A. All linear dimensions are in millimeters

RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

YFF (R–XBGA–N49) DIE–SIZE BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments

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