System-Side Impedance Track™ Fuel Gauge With Integrated Sense Resistor

Check for Samples: bq27421-G1

FEATURES

- **Single Series Cell Li-Ion Battery Fuel Gauge**
  - **Resides on System Board**
  - **Supports Embedded or Removable Batteries**
  - **Powered Directly from Battery with Integrated LDO**
  - **Low-value Integrated Sense Resistor (7 mΩ Typical)**
- **Easy to Configure Fuel Gauging Based on Patented Impedance Track™ Technology**
  - **Reports Remaining Capacity and State of Charge (SOC) with Smoothing Filter**
  - **Automatically Adjusts for Battery Aging, Self-discharge, Temperature, and Rate Changes**
  - **Battery State of Health (aging) Estimation**
- **Microcontroller Peripheral Supports:**
  - **400-kHz I²C™ Serial Interface**
  - **Configurable SOC Interrupt, or Battery Low Digital Output Warning**
  - **Internal Temperature Sensor, or Host Reported Temperature**
- **9-pin 1,62 mm × 1,58 mm × 0,5 mm Pitch CSP Package**

APPLICATIONS

- **Smartphones, Feature phones and Tablets**
- **Digital Still and Video Cameras**
- **Handheld Terminals**
- **MP3 or Multimedia Players**

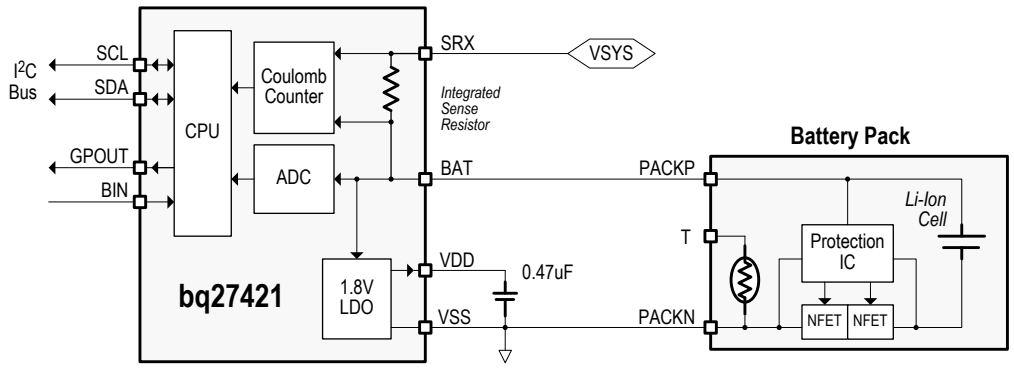
DESCRIPTION

The Texas Instruments bq27421-G1 is an easy to configure microcontroller peripheral that provides system-side fuel gauging for single-cell Li-Ion batteries. The device requires minimal user configuration and system microcontroller firmware development.

The bq27421-G1 uses the patented Impedance Track™ algorithm for fuel gauging, and provides information such as remaining battery capacity (mAh), state-of-charge (%), and battery voltage (mV).

Battery fuel gauging with the bq27421-G1 requires connections only to PACK+ (P+) and PACK– (P–) for a removable battery pack or embedded battery circuit. The tiny 9-pin 1,62 × 1,58 mm × 0,5 mm pitch CSP package is ideal for space constrained applications.

TYPICAL APPLICATION



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DEVICE INFORMATION

AVAILABLE OPTIONS

PART NUMBER	BATTERY TYPE	CHEM_ID (1)	FIRMWARE VERSION (2)	PACKAGE (3)	T_A	COMM. FORMAT	TAPE and REEL QUANTITY
bq27421YZFR-G1A	$LiCoO_2$ (4.2 V max charge)	0x128	1.08 (0x0108)	CSP-9	–40°C to 85°C	I^2C	3000
bq27421YZFT-G1A							250
bq27421YZFR-G1B	$LiMn_2O_4$ (4.3 - 4.35 V max charge)	0x312					3000
bq27421YZFT-G1B							250

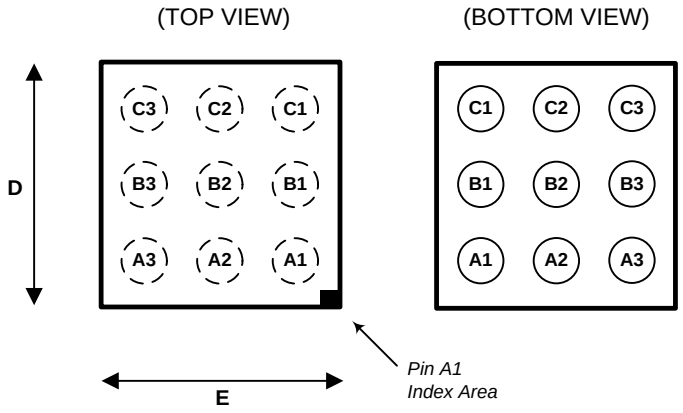
(1) See the CHEM_ID subcommand to confirm the battery chemistry type.
(2) See the FW_VERSION subcommand to confirm the firmware version.
(3) For the most current package and ordering information see the Package Option Addendum at the end of this document; or, see the TI website at www.ti.com.

THERMAL INFORMATION

THERMAL METRIC (1)		bq27421-G1 YZF(9 PINS)	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	107.8	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	0.7	
θ_{JB}	Junction-to-board thermal resistance	60.4	
ψ_{JT}	Junction-to-top characterization parameter	3.5	
ψ_{JB}	Junction-to-board characterization parameter	60.4	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	n/a	

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953

PIN DIAGRAM AND PACKAGE DIMENSIONS



DIM	MIN	TYP	MAX	UNITS
D	1550	1580	1610	µm
E	1590	1620	1650	

PIN FUNCTIONS

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
BAT	C3	PI, AI	LDO regulator input, battery voltage input, and coulomb counter input typically connected to the PACK+ terminal.
VDD	B3	PO	1.8V Regulator Output. Decouple with 0.47µF ceramic capacitor to Vss. This pin is not intended to provide power for other devices in the system.
VSS	B2, C1	PI	Ground pins. The center pin B2 is the actual device ground pin while pin C1 is floating internally and therefore C1 may be used as a bridge to connect to the board ground plane without requiring a via under the device package. Recommend routing the center pin B2 to the corner pin C1 using a top-layer metal trace on the board. Then route the corner pin C1 to the board ground plane.
SRX	C2	AI	Integrated high-side sense resistor and coulomb counter input typically connected to system power rail VSYS.
GPOUT	A1	DO	General Purpose open-drain output. May be configured as a Battery Low indicator or perform SOC interrupt (SOC_INT) function.
SDA	A2	DIO	Slave I^2C serial bus for communication with system (Master). Open-drain pins. Use with external 10kΩ pull-up resistors (typical) for each pin. If the external pull-up resistors will be disconnected from these pins during normal operation, recommend using external 1MΩ pull-down resistors to VSS at each pin to avoid floating inputs.
SCL	A3	DIO	
BIN	B1	DI	Battery-insertion detection input. A logic high to low transition is detected as a battery insertion event. Recommend using a pull-up resistor >1MΩ (1.8 MΩ typical) to V_{CC} for reduced power consumption. An internal pull-up resistor option is also available.

(1) I/O = Digital input/output, IA = Analog input, P = Power connection

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		VALUE	UNIT
V_{BAT}	BAT pin input voltage range	–0.3 to 6.0	V
V_{SRX}	SRX pin input voltage range(1)	V_{BAT} ± 0.03	V
V_{DD}	VDD pin supply voltage range (LDO ouptut)	–0.3 to 2.0	V
V_{IOD}	Open-drain I/O pins (SDA, SCL, GPOUT)	–0.3 to 6.0	V
V_{IOPP}	Push-Pull I/O pins (BIN)	–0.3 to V_{DD} + 0.3	V
T_A	Operating free-air temperature range	–40 to 85	°C
T_{STG}	Storage temperature range	–65 to 150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

T_A = 30°C and V_{REGIN} = V_{BAT} = 3.6V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{BAT}(1)	External input capacitor for internal LDO between BAT and V_{SS}	Nominal capacitor values specified. Recommend a 5% ceramic X5R type capacitor located close to the device.		0.1		µF
C_{LDO18} (1)	External output capacitor for internal LDO between V_{CC} and V_{SS}			0.47		µF
V_{PU} (1)	External pull-up voltage for open-drain pins (SDA, SCL, GPOUT)		1.62		3.6	V

(1) Specified by design. Not production tested.

SUPPLY CURRENT

T_A = 30°C and V_{REGIN} = V_{BAT} = 3.6V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC} (1)	NORMAL mode current	I_{LOAD} > ***Sleep Current*** (2)		93		µA
I_{SLP} (1)	SLEEP mode current	I_{LOAD} < ***Sleep Current*** (2)		21		µA
I_{HIB} (1)	HIBERNATE mode current	I_{LOAD} < ***Hibernate Current*** (2)		9		µA
I_{SD} (1)	SHUTDOWN mode current	Fuel gauge in host commanded SHUTDOWN mode. (LDO Regulator Output Disabled.)		0.6		µA

(1) Specified by design. Not production tested.
(2) Wake Comparator Disabled.

DIGITAL INPUT AND OUTPUT DC CHARACTERISTICS

T_A = –40°C to 85°C, typical values at T_A = 30°C and V_{REGIN} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IH(OD)}$	Input voltage, high (2)	External pullup resistor to V_{PU}	V_{PU} * 0.7			V
$V_{IH(PP)}$	Input voltage, high (3)		1.4			V
V_{IL}	Input voltage, low (2) (3)				0.6	V
V_{OL}	Output voltage, low (2)				0.6	V
I_{OH}	Output source current, high (2) (3)				0.5	mA
$I_{OL(OD)}$	Output sink current, low (2)				-3	mA
C_{IN} (1)	Input capacitance (2) (3)				5	pF
I_{lkg}	Input leakage current (I/O pins) (2) (3)				1	µA

(1) Specified by design. Not production tested.
(2) Open Drain pins: (SCL, SDA, GPOUT)
(3) Push Pull pin: (BIN)

LDO REGULATOR, WAKE-UP AND AUTO-SHUTDOWN DC CHARACTERISTICS

T_A = –40°C to 85°C, typical values at T_A = 30°C and V_{REGIN} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{BAT}	BAT pin regulator input		2.45		4.5	V
V_{DD}	Regulator output voltage			1.8		V
$UVLO_{IT+}$	V_{BAT} Under Voltage Lock Out LDO Wake-Up Rising Threshold(2)			2.0		V
$UVLO_{IT-}$	V_{BAT} Under Voltage Lock Out LDO Auto-Shutdown Falling Threshold(2)			1.95		V
V_{WU+} (1)	GPOUT (input) LDO Wake-Up rising edge threshold (2)	LDO Wake-up from SHUTDOWN mode	1.2			V

(1) Specified by design. Not production tested.
(2) If the device is commanded to SHUTDOWN via I2C with V_{BAT} > $UVLO_{IT+}$, a wake-up rising edge trigger is required on GPOUT .

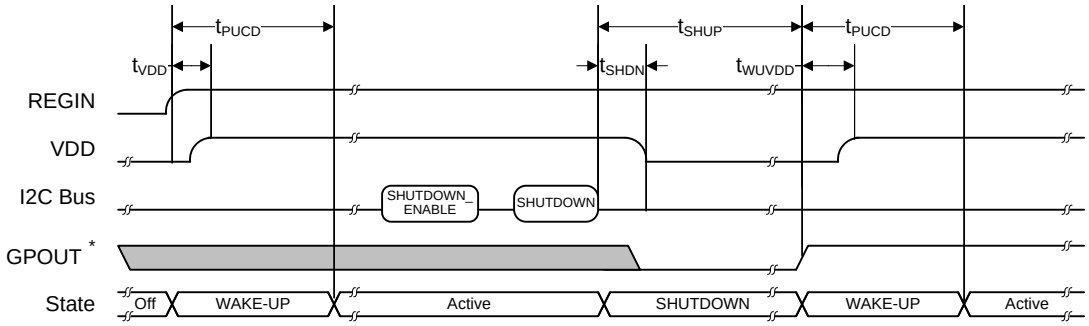
LDO REGULATOR, WAKE-UP AND AUTO-SHUTDOWN AC CHARACTERISTICS

T_A = –40°C to 85°C, typical values at T_A = 30°C and V_{REGIN} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{SHDN} (1)	SHUTDOWN Entry Time	Time delay from SHUTDOWN command to LDO output disable.			250	ms
t_{SHUP} (1)	SHUTDOWN GPOUT Low time	Minimum low time of GPOUT (input) in SHUTDOWN before WAKEUP	10			µs
t_{VDD} (1)	Initial V_{DD} Output delay			13		ms
t_{WUVDD} (1)	Wake-up V_{DD} Output delay	Time delay from rising edge of GPOUT (input) to nominal VDD output.		8		ms
t_{PUCD}	Power-up communication delay	Time delay from rising edge of REGIN to the Active state. Includes firmware initialization time.		250		ms

(1) Specified by design. Not production tested.

SHUTDOWN and WAKE-UP Timing



* GPOUT is configured as an input for wake-up signaling.

Figure 1. SHUTDOWN and WAKE-UP Timing Diagram

ADC (TEMPERATURE AND CELL MEASUREMENT) CHARACTERISTICS

T_A = –40°C to 85°C; typical values at T_A = 30°C and V_{REGIN} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IN(BAT)}$	BAT pin voltage measurement range.	Voltage divider enabled.	2.45		4.5	V
t_{ADC_CONV}	Conversion time			125		ms
	Effective Resolution			15		bits

(1) Specified by design. Not tested in production.

INTEGRATING ADC (COULOMB COUNTER) CHARACTERISTICS

T_A = –40°C to 85°C; typical values at T_A = 30°C and V_{REGIN} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{SR}	Input voltage range from BAT to SRX pins			BAT ± 25		mV
t_{SR_CONV}	Conversion time	Single conversion		1		s
	Effective Resolution	Single conversion		16		bits

(1) Assured by design. Not tested in production.

INTEGRATED SENSE RESISTOR CHARACTERISTICS

T_A = –40°C to 85°C; typical values at T_A = 30°C and V_{REGIN} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SRX_{RES} (2)	Resistance of Integrated Sense Resistor from SRX to VSS.	T_A = 30°C		7		mΩ
I_{SRX} (1)	Recommended Sense Resistor input current.	Long term RMS, average device utilization.			2000	mA
		Peak RMS current, 10% device utilization. (3)			2500	mA
		Peak pulsed current, 250mS max, 1% device utilization. (3)			3500	mA

(1) Specified by design. Not tested in production.
(2) Firmware compensation applied for temperature coefficient of resistor.
(3) Device utilization is the long term usage profile at a specific condition compared to the average condition.

I²C-COMPATIBLE INTERFACE COMMUNICATION TIMING CHARACTERISTICS

T_A = –40°C to 85°C; typical values at T_A = 30°C and V_{REGIN} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Standard Mode (100 kHz)						
$t_{d(STA)}$	Start to first falling edge of SCL		4.0			µs
$t_{w(L)}$	SCL pulse duration (low)		4.7			µs
$t_{w(H)}$	SCL pulse duration (high)		4.0			µs
$t_{su(STA)}$	Setup for repeated start		4.7			µs
$t_{su(DAT)}$	Data setup time	Host drives SDA	250			ns
$t_{h(DAT)}$	Data hold time	Host drives SDA	0			ns
$t_{su(STOP)}$	Setup time for stop		4.0			µs
$t_{(BUF)}$	Bus free time between stop and start	Includes Command Waiting Time	66			µs
t_f	SCL/SDA fall time (1)				300	ns
t_r	SCL/SDA rise time (1)				300	ns
f_{SCL}	Clock frequency (2)				100	kHz
Fast Mode (400 kHz)						
$t_{d(STA)}$	Start to first falling edge of SCL		600			ns
$t_{w(L)}$	SCL pulse duration (low)		1300			ns
$t_{w(H)}$	SCL pulse duration (high)		600			ns
$t_{su(STA)}$	Setup for repeated start		600			ns
$t_{su(DAT)}$	Data setup time	Host drives SDA	100			ns
$t_{h(DAT)}$	Data hold time	Host drives SDA	0			ns
$t_{su(STOP)}$	Setup time for stop		600			ns
$t_{(BUF)}$	Bus free time between stop and start	Includes Command Waiting Time	66			µs
t_f	SCL/SDA fall time (1)				300	ns
t_r	SCL/SDA rise time (1)				300	ns
f_{SCL}	Clock frequency (2)				400	kHz

(1) Specified by design. Not production tested.
(2) If the clock frequency (f_{SCL}) is > 100 kHz, use 1-byte write commands for proper operation. All other transactions types are supported at 400 kHz. (Refer to I²C INTERFACE and I²C Command Waiting Time)

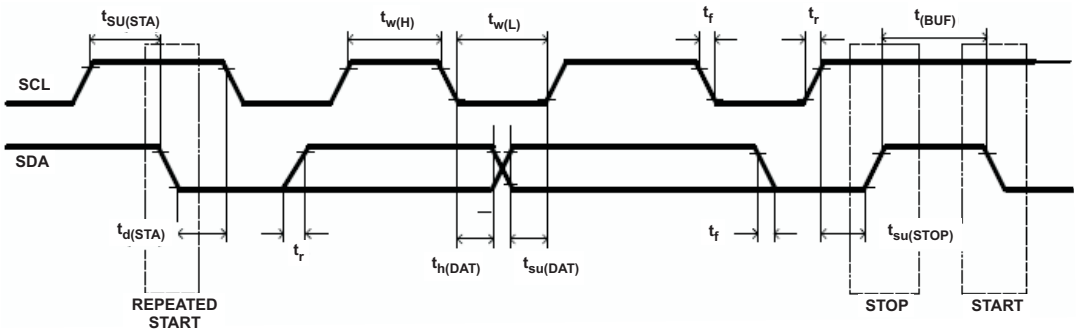


Figure 2. I²C-Compatible Interface Timing Diagrams

GENERAL DESCRIPTION

The bq27421-G1 accurately predicts the battery capacity and other operational characteristics of a single Li-based rechargeable cell. It can be interrogated by a system processor to provide cell information, such as state-of-charge (SOC).

Information is accessed through a series of commands, called *Standard Commands*. Further capabilities are provided by the additional *Extended Commands* set. Both sets of commands, indicated by the general format *Command( )*, are used to read and write information contained within the bq27421-G1 control and status registers, as well as its data locations. Commands are sent from system to gauge using the bq27421-G1's I^2C serial communications engine, and can be executed during application development, system manufacture, or end-equipment operation.

The key to the bq27421-G1's high-accuracy gas gauging prediction is Texas Instrument's proprietary Impedance Track™ algorithm. This algorithm uses cell measurements, characteristics, and properties to create state-of-charge predictions that can achieve high accuracy across a wide variety of operating conditions and over the lifetime of the battery.

The bq27421-G1 measures charge/discharge activity by monitoring the voltage across a small-value sense resistor. When a cell is attached to the bq27421-G1, cell impedance is computed, based on cell current, cell open-circuit voltage (OCV), and cell voltage under loading conditions.

The bq27421-G1 uses an integrated temperature sensor for estimating cell temperature. Alternatively, the host processor can provide temperature data for the bq27421-G1.

To minimize power consumption, the bq27421-G1 has several power modes: INITIALIZATION, NORMAL, SLEEP, HIBERNATE and SHUTDOWN. The bq27421-G1 passes automatically between these modes, depending upon the occurrence of specific events, though a system processor can initiate some of these modes directly. More details are found in the *bq27421-G1 Technical Reference Manual (SLUUAC5)*.

NOTE

Formatting Conventions in this Document:

Commands: *italics* with parentheses( ) and no breaking spaces, for example, *RemainingCapacity( ).*

Data Flash: *italics*, **bold**, and breaking spaces, for example, ***Design Capacity***.

Register bits and flags: *italics* with brackets [ ], for example, *[TDA]*

Data flash bits: *italics*, **bold**, and brackets [ ], for example, ***[LED1]***

Modes and states: ALL CAPITALS, for example, UNSEALED mode.

DATA COMMANDS

STANDARD DATA COMMANDS

The bq27421-G1 uses a series of 2-byte standard commands to enable system reading and writing of battery information. Each standard command has an associated command-code pair, as indicated in . Because each command consists of two bytes of data, two consecutive I2C transmissions must be executed both to initiate the command function, and to read or write the corresponding two bytes of data. Additional details are found in the *bq27421-G1 Technical Reference Manual (SLUUAC5)*.

Table 1. Standard Commands

NAME		COMMAND CODE	UNITS	SEALED ACCESS
Control( )	CNTL	0x00 / 0x01	N/A	R/W
Temperature( )	TEMP	0x02 / 0x03	0.1°K	R/W
Voltage( )	VOLT	0x04 / 0x05	mV	R
Flags( )	FLAGS	0x06 / 0x07	N/A	R
NominalAvailableCapacity( )		0x08 / 0x09	mAh	R
FullAvailableCapacity( )		0x0a / 0x0b	mAh	R
RemainingCapacity( )	RM	0x0c / 0x0d	mAh	R
FullChargeCapacity( )	FCC	0x0e / 0x0f	mAh	R
AverageCurrent( )		0x10 / 0x11	mA	R
StandbyCurrent( )		0x12 / 0x13	mA	R
MaxLoadCurrent( )		0x14 / 0x15	mA	R
AveragePower( )		0x18 / 0x19	mW	R
StateOfCharge( )	SOC	0x1c / 0x1d	%	R
IntTemperature( )		0x1e / 0x1f	0.1°K	R
StateOfHealth( )	SOH	0x20 / 0x21	num / %	R

Control( ): 0x00/0x01

Issuing a *Control( )* command requires a subsequent 2-byte subcommand. These additional bytes specify the particular control function desired. The *Control( )* command allows the system to control specific features of the bq27421-G1 during normal operation and additional features when the device is in different access modes, as described in . Additional details are found in the *bq27421-G1 Technical Reference Manual (SLUUAC5)*.

Table 2. *Control( )* Subcommands

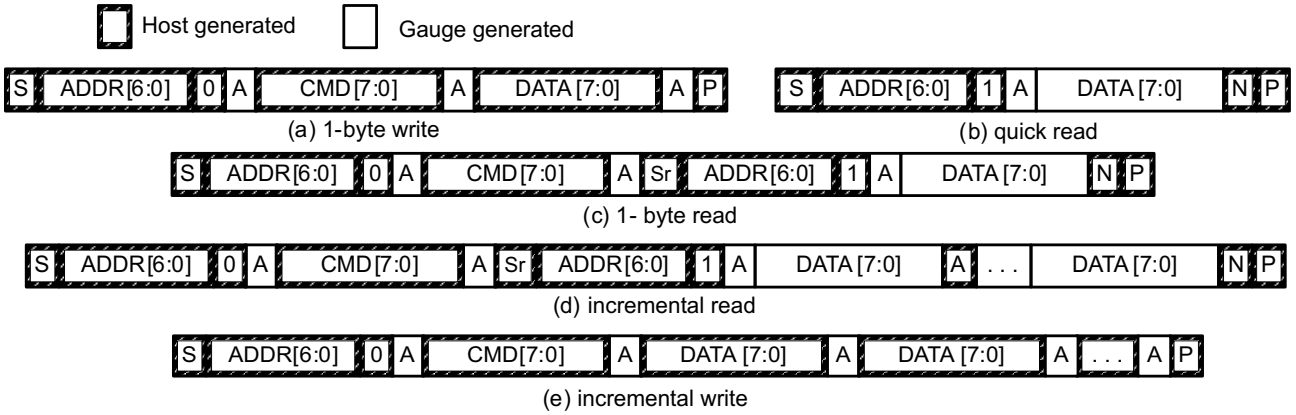
CNTL FUNCTION	CNTL DATA	SEALED ACCESS	DESCRIPTION
CONTROL_STATUS	0x0000	Yes	Reports the status of device.
DEVICE_TYPE	0x0001	Yes	Reports the device type (0x0421).
FW_VERSION	0x0002	Yes	Reports the firmware version of the device.
DM_CODE	0x0004	Yes	Reports the Data Memory Code number stored in NVM.
PREV_MACWRITE	0x0007	Yes	Returns previous MAC command code.
CHEM_ID	0x0008	Yes	Reports the chemical identifier of the Impedance Track™ configuration
BAT_INSERT	0x000c	Yes	Forces the *[BAT_DET]* bit set when the *[BIE]* bit is 0.
BAT_REMOVE	0x000d	Yes	Forces the *[BAT_DET]* bit clear when the *[BIE]* bit is 0.
SET_HIBERNATE	0x0011	Yes	Forces CONTROL_STATUS [*HIBERNATE*] to 1.
CLEAR_HIBERNATE	0x0012	Yes	Forces CONTROL_STATUS [*HIBERNATE*] to 0.
SET_CFGUPDATE	0x0013	No	Force CONTROL_STATUS [*CFGUPMODE*] to 1 and gauge enters CONFIG UPDATE mode.
SHUTDOWN_ENABLE	0x001b	No	Enables device SHUTDOWN mode.
SHUTDOWN	0x001c	No	Commands the device to enter SHUTDOWN mode.
TOGGLE_GPOUT	0x0023	Yes	Commands the device to toggle the GPOUT pin for 1ms.
SEALED	0x0020	No	Places the device in SEALED access mode.
RESET	0x0041	No	Performs a full device reset.
SOFT_RESET	0x0042	No	Gauge exits CONFIG UPDATE mode.

Refer to the bq27421-G1 Technical Reference Manual for detailed descriptions for the Standard Data Commands and *Control( )* subcommands.

FUNCTIONAL DESCRIPTION

I²C INTERFACE

The bq27421-G1 supports the standard I²C read, incremental read, quick read, one-byte write, and incremental write functions. The 7-bit device address (ADDR) is the most significant 7 bits of the hex address and is fixed as 1010101. The first 8 bits of the I²C protocol are, therefore, 0xAA or 0xAB for write or read, respectively.

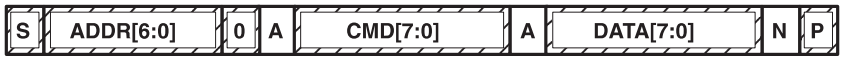


(S = Start, Sr = Repeated Start, A = Acknowledge, N = No Acknowledge, and P = Stop).

The quick read returns data at the address indicated by the address pointer. The address pointer, a register internal to the I²C communication engine, increments whenever data is acknowledged by the bq27421-G1 or the I²C master. “Quick writes” function in the same manner and are a convenient means of sending multiple bytes to consecutive command locations (such as two-byte commands that require two bytes of data).

The following command sequences are not supported:

Attempt to write a read-only address (NACK after data sent by master):



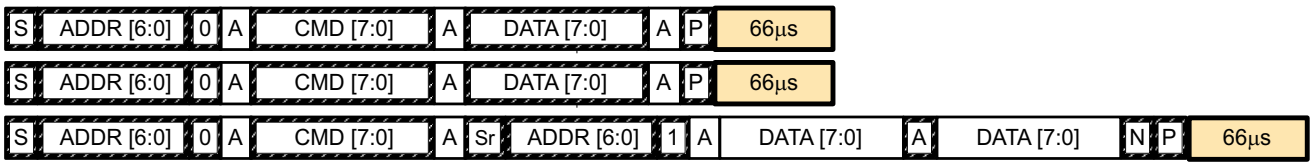
Attempt to read an address above 0x6B (NACK command):

I²C Time Out

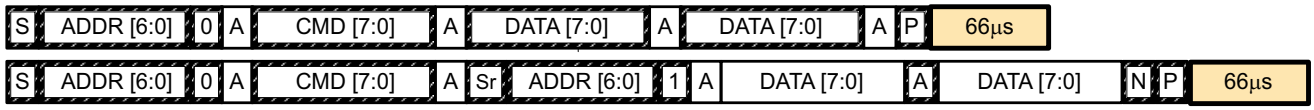
The I²C engine releases both SDA and SCL if the I²C bus is held low for 2 seconds. If the bq27421-G1 is holding the lines, releasing them frees them for the master to drive the lines. If an external condition is holding either of the lines low, the I²C engine enters the low-power sleep mode.

I²C Command Waiting Time

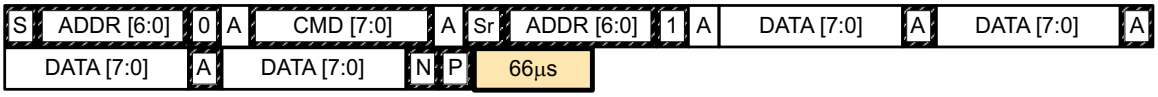
To ensure proper operation at 400 kHz, a $t_{(BUF)}$ ≥ 66 µs bus-free waiting time must be inserted between all packets addressed to the bq27421-G1. In addition, if the SCL clock frequency (f_{SCL}) is > 100 kHz, use individual 1-byte write commands for proper data flow control. The following diagram shows the standard waiting time required between issuing the control subcommand the reading the status result. For read-write standard command, a minimum of 2 seconds is required to get the result updated. For read-only standard commands, there is no waiting time required, but the host must not issue any standard command more than two times per second. Otherwise, the gauge could result in a reset issue due to the expiration of the watchdog timer.



Waiting time inserted between two 1-byte write packets for a subcommand and reading results
(required for 100 kHz < f_{SCL} ≤ 400 kHz)



Waiting time inserted between incremental 2-byte write packet for a subcommand and reading results
(acceptable for f_{SCL} ≤ 100 kHz)

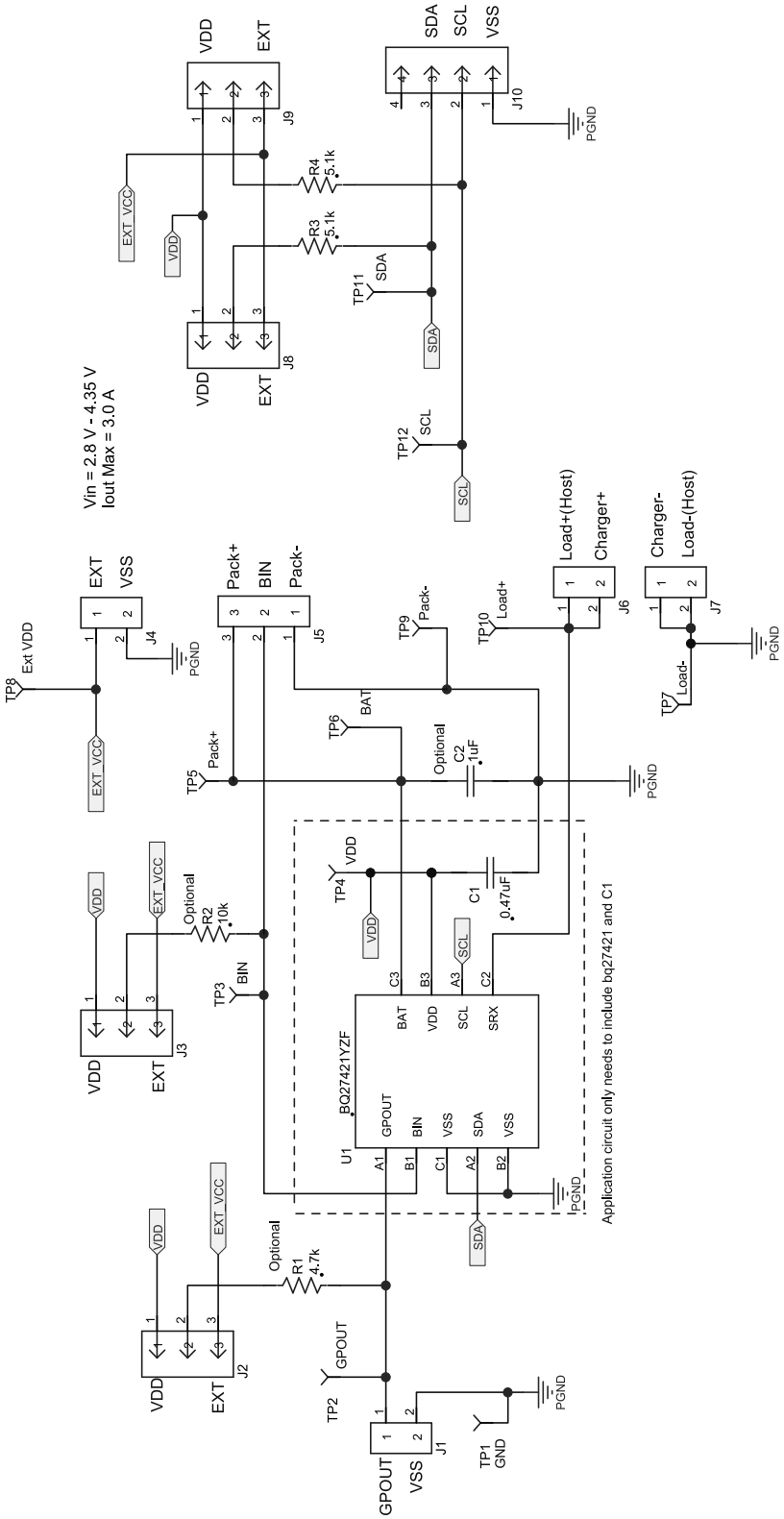


Waiting time inserted after incremental read

I²C Clock Stretching

A clock stretch can occur during all modes of fuel gauge operation. In SLEEP and HIBERNATE modes, a short ≤ 100 µs clock stretch occurs on all I²C traffic as the device must wake-up to process the packet. In the other modes (INITIALIZATION , NORMAL) a ≤ 4 ms clock stretching period may occur within packets addressed for the fuel gauge as the I²C interface performs normal data flow control.

REFERENCE (EVM) SCHEMATIC



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
BQ27421YZFR-G1A	ACTIVE	DSBGA	YZF	9	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ27421 G1A	Samples
BQ27421YZFR-G1B	ACTIVE	DSBGA	YZF	9	3000	TBD	Call TI	Call TI	-40 to 85	BQ27421 G1B	Samples
BQ27421YZFT-G1A	ACTIVE	DSBGA	YZF	9	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ27421 G1A	Samples
BQ27421YZFT-G1B	ACTIVE	DSBGA	YZF	9	250	TBD	Call TI	Call TI	-40 to 85	BQ27421 G1B	Samples

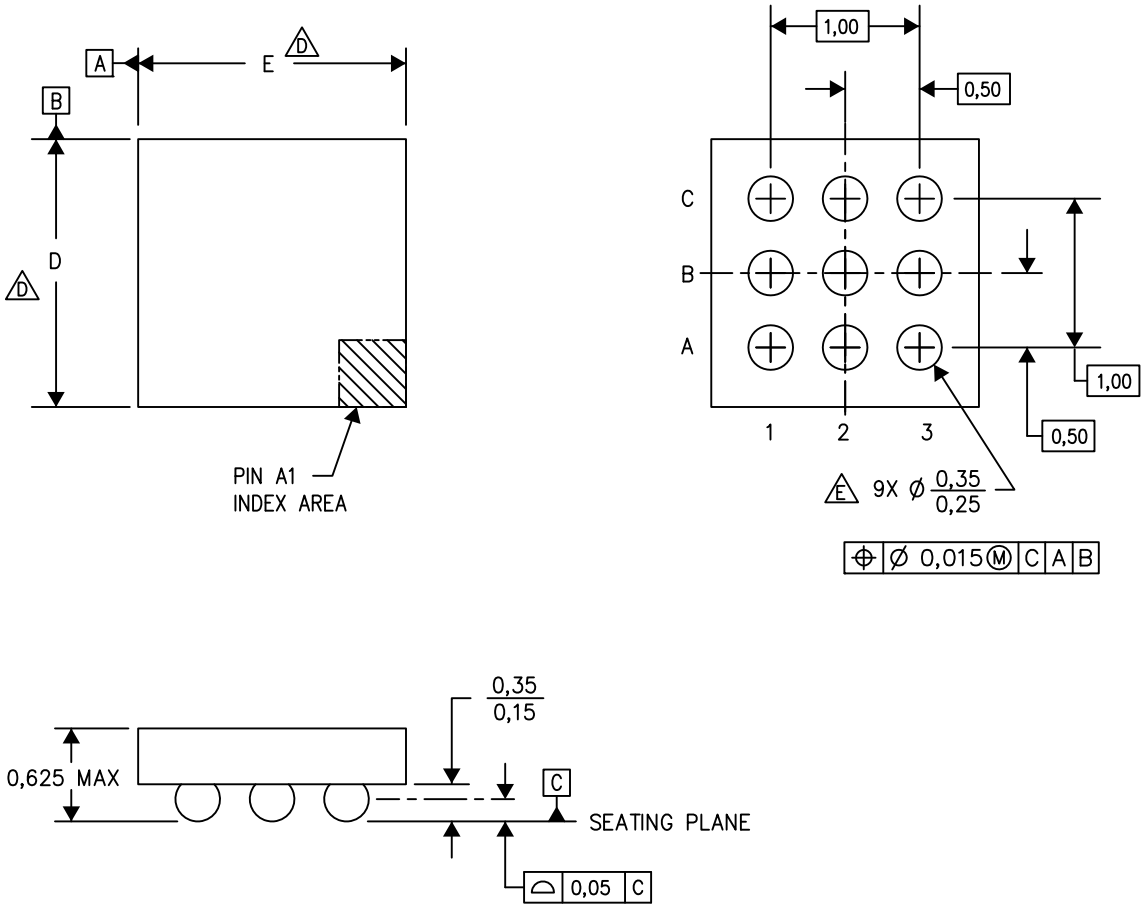
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

YZF (S–XBGA–N9) DIE–SIZE BALL GRID ARRAY



D: Max = 1.651 mm, Min = 1.59 mm

E: Max = 1.61 mm, Min = 1.55 mm

4205058–4/N 09/12

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative.
E. Reference Product Data Sheet for array population.
3 x 3 matrix pattern is shown for illustration only.
F. This package contains Pb–free balls.
Refer to YEF (Drawing #4204181) for tin–lead (SnPb) balls.

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