4-A and 6-A High-Speed 5-V Drive, Optimized Single-Gate Driver

Check for Samples: UCC27611

FEATURES

- **Enhancement Mode Gallium Nitride FETs (eGANFETs)**
- **4.0-V to 18-V Single Supply Range VDD Range**
- **Drive Voltage VREF Regulated to 5 V**
- **4-A Peak Source and 6-A Peak Sink Drive Current**
- **1-Ω and 0.35-Ω Pull-Up and Pull-Down Resistance (maximize high slew-rate dV and dt immunity)**
- **Split Output Configuration (allows turn-on and off optimization for individual FETs)**
- **Fast Propagation Delays (14-ns typical)**
- **Fast Rise and Fall Times (9-ns and 4-ns typical)**
- **TTL and CMOS Compatible Inputs (independent of supply voltage allow easy interface to digital and analog controllers)**
- **Dual Input Design offering Drive Flexibility (both inverting and non-inverting configurations)**
- **Output Held Low when Inputs are Floating**
- **VDD Under Voltage Lockout (UVLO)**
- **Optimized Pinout Compatible with eGANFET Footprint for Easy Layout**
- **2 mm x 2 mm WSON-6 Package with Exposed Thermal and Ground Pad, (minimized parasitic inductances to reduce gate ringing)**
- **Operating Temperature Range of -40°C to 140°C**

APPLICATIONS

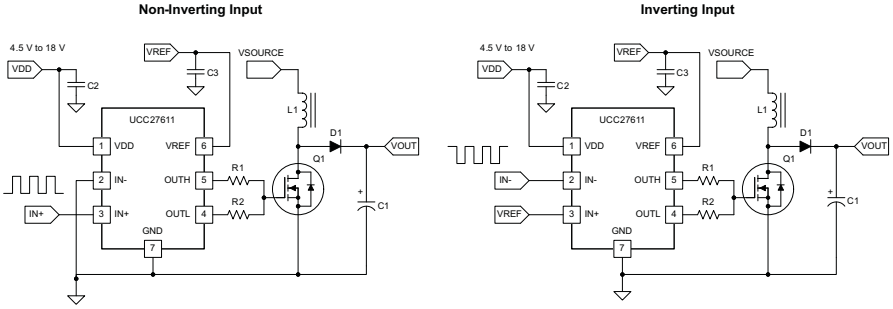
- **Switch-Mode Power Supplies**
- **DC-to-DC Converters**
- **Synchronous Rectification**
- **Solar Inverters, Motor Control, UPS**
- **Envelope Tracking Power Supplies**

DESCRIPTION

The UCC27611 is a single-channel, high-speed, gate driver optimized for 5-V drive, specifically addressing enhancement mode GaN FETs. The drive voltage VREF is precisely controlled by internal linear regulator to 5 V. The UCC27611 offers asymmetrical rail-to-rail peak current drive capability with 4-A source and 6-A sink. Split output configuration allows individual turn-on and off time optimization depending on FET. Package and pinout with minimum parasitic inductances reduce the rise and fall time and limit the ringing. Additionally, the short propagation delay with minimized tolerances and variations allows efficient operation at high frequencies. The 2-Ω and 0.3-Ω pull-up and pull-down resistance boosts immunity to hard switching with high slew rate dV and dt.

The independence from VDD input signal thresholds ensure TTL and CMOS low-voltage logic compatibility. For safety reason when the input pins are in a floating condition, the internal input pull-up and down resistors hold the output LOW. Internal circuitry on VREF pin provides an under voltage lockout function that holds output LOW until VREF supply voltage is within operating range. UCC27611 is offered in a small 2 mm x 2 mm WSON-6 package (DRV) with exposed thermal and ground pad which improves the package power handling capability. The UCC27611 operates over wide temperature range from -40°C to 140°C.

Typical Application Diagram



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

TEMPERATURE RANGE $T_A = T_J$	PACKAGED DEVICES (1)
	WSON-6 (DRV)
-40°C to +140°C	UCC27611DRV

(1)) For more information about traditional and new thermal metrics, see IC Package Thermal Metrics application report, SPRA953.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
V_{DD}	Supply voltage range	-0.3 to 20.0	V
	OUTH	-0.3 to VREF +0.3	
	OUTL	-0.3V to VREF +0.3	
	VREF	6	
I_{out_DC}	Continuous source current of OUTH/sink current of OUTL	0.3/0.6	A
I_{out_pulsed}	Continuous source current of OUTH/sink current of OUTL (0.5 µs),	4/8	
	IN+, IN-	-0.3V to 20	V
HBM	ESD, human body model	2000	
CDM	ESD, charged device model	500 (WSON)	
T_J	Operating virtual junction temperature range	-40 to 150	°C
T_{stg}	Storage temperature range	-65 to 150	
	Lead temperature, soldering, 10 sec.	300	
	Lead temperature, reflow	260	

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD	Supply voltage range,	4.0	12	18	V
T_J	Operating junction temperature range	-40		+140	°C
	IN+, IN- resistance range			100	kΩ
IN	Input voltage	0		18	V

THERMAL INFORMATION

THERMAL METRIC(1)		UCC27611 DRV 6 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	80.3	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	11.9	
θ_{JB}	Junction-to-board thermal resistance(4)	49.7	
ψ_{JT}	Junction-to-top characterization parameter(5)	5.5	
ψ_{JB}	Junction-to-board characterization parameter(6)	50.1	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	18.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

ELECTRICAL CHARACTERISTICS

VDD = 12 V, T_A = T_J = -40°C to 140°C, 2-µF capacitor from VDD to GND and from VREF to GND. Currents are positive into, negative out of the specified terminal. OUTH and OUTL are tied together. (unless otherwise noted) (1)

PARAMETER		CONDITION	MIN	TYP	MAX	UNITS
Bias Current						
$I_{DD(off)}$	Startup current	VDD = 3.0, IN+ = VDD, IN- = GND		100	180	µA
		IN+ = GND, IN- = VDD		75	160	
Under Voltage Lockout (UVLO)						
$V_{DD(on)}$	Supply start threshold		3.55	3.8	4.15	V
$V_{DD(off)}$	Minimum operating voltage after supply start		3.3	3.55	3.9	
V_{DD_H}	Supply voltage hysteresis			0.25		
Inputs (IN+, IN-)						
V_{IN_L}	Input signal low threshold	Output High for IN- pin, Output Low for IN+ pin	0.9	1.1	1.3	V
V_{IN_H}	Input signal high threshold	Output High for IN+ pin, Output Low for IN- pin	1.85	2.05	2.25	
V_{IN_HYS}	Input signal hysteresis		0.70	0.95	1.20	
V_{REF}						
V_{REF}	VREF regulator output range		4.75	5.0	5.15	V
V_{REF_line}	VREF line regulation	VDD from 6 V to 18 V			0.05	
V_{REF_liad}	VREF load regulation	I_R from 0 mA to 50 mA			0.075	
I_{SCC}	Short circuit current		-90	-75	-60	mA
Outputs (OUTH/OUTL AND OUT)						
$I_{SRC/SNK}$	Source peak current (OUTH) / sink peak current (OUTL) (2)	C_{LOAD} = 0.22 µF, F_{SW} = 1 kHz, (2)		-4/+8		A
V_{OH}	OUTH high voltage	I_{OUTH} = -10 mA	VDD - 0.05			V
V_{OL}	OUTL low voltage	I_{OUTL} = 10 mA			0.02	
R_{OH}	OUTH pull-up resistance	T_A = 25°C, I_{OUT} = -25 mA to -50 mA		1		Ω
		T_A = -40°C to 140°C, I_{OUT} = -50 mA			2	
R_{OL}	OUTH pull-down resistance	T_A = 25°C, I_{OUT} = 25 mA to 50 mA		0.35		
		TA = -40°C to 140°C, IOUT = 50 mA			1.5	
Switching Time						
t_R	Rise time (3)	C_{LOAD} = 1.0 nF		5		ns
t_F	Fall time (3)	C_{LOAD} = 1.0 nF		5		
t_{D1}	Turn-on propagation delay (3)	C_{LOAD} = 1.0 nF, IN = 0 V to 5 V		14	25	
t_{D2}	Turn-off propagation delay (3)	C_{LOAD} = 1.0 nF, IN = 5 V to 0 V		14	25	

(1) Device operational with output switching.
(2) Ensured by Design, Not tested in Production.
(3) See Figure 1 and Figure 2 timing diagrams.

Timing Diagrams (OUTH tied to OUTL)

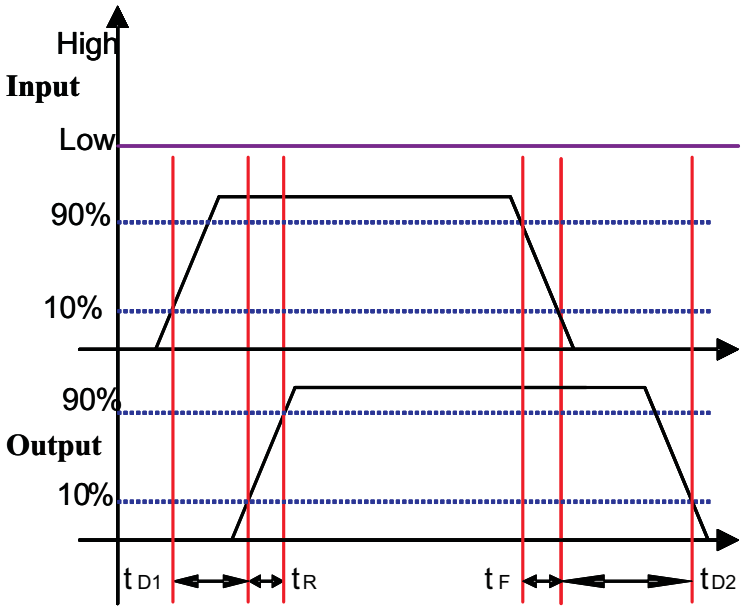


Figure 1. Non-Inverting Configuration
(input = IN+ and output = OUT (IN- = GND))

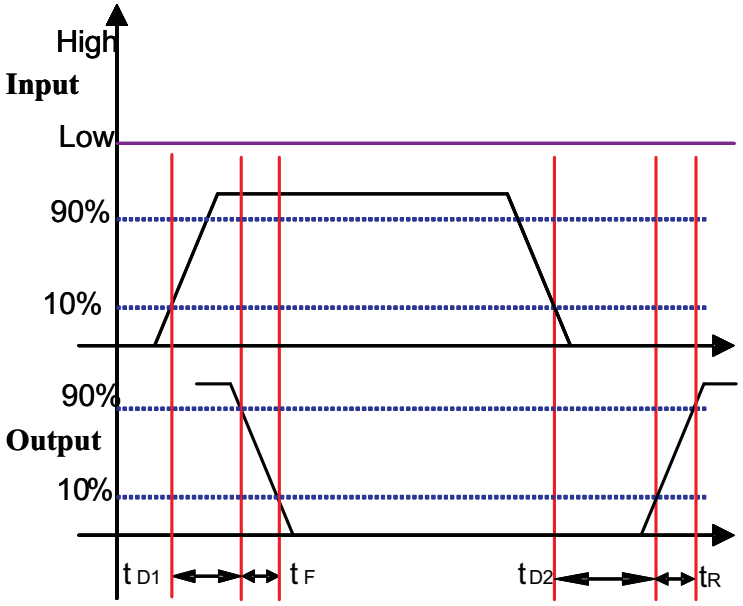


Figure 2. Inverting Configuration
(input = IN- and output = OUT (IN+ = VDD))

Typical Timing Waveforms

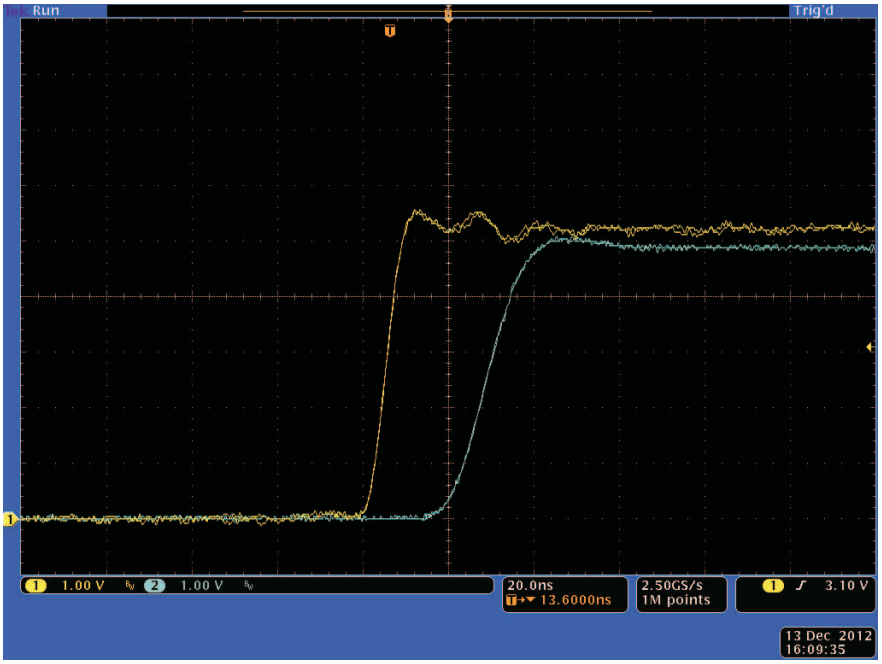


Figure 3. Output Rising
(Ch1 = IN+, Ch2 = OUTPUT)

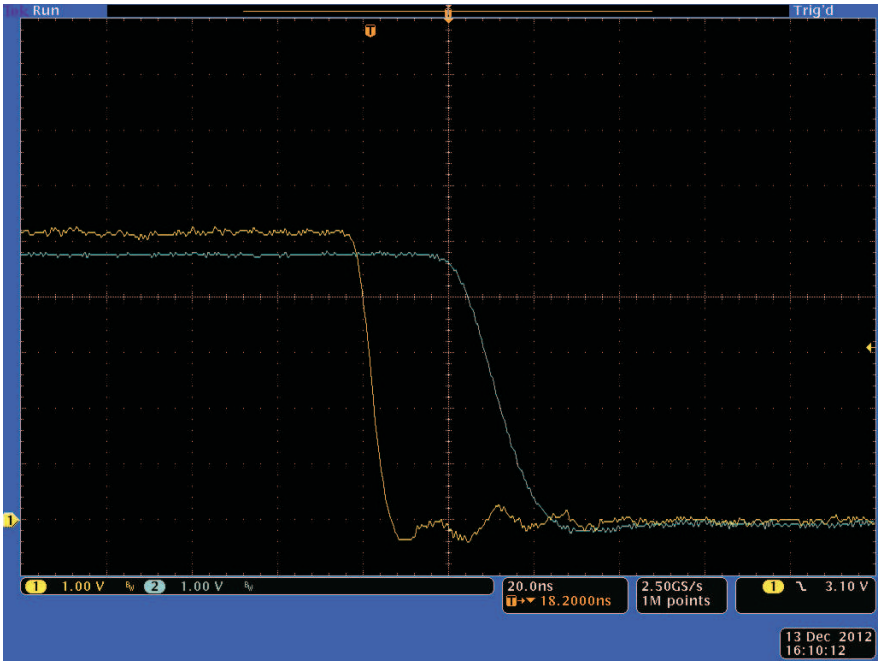
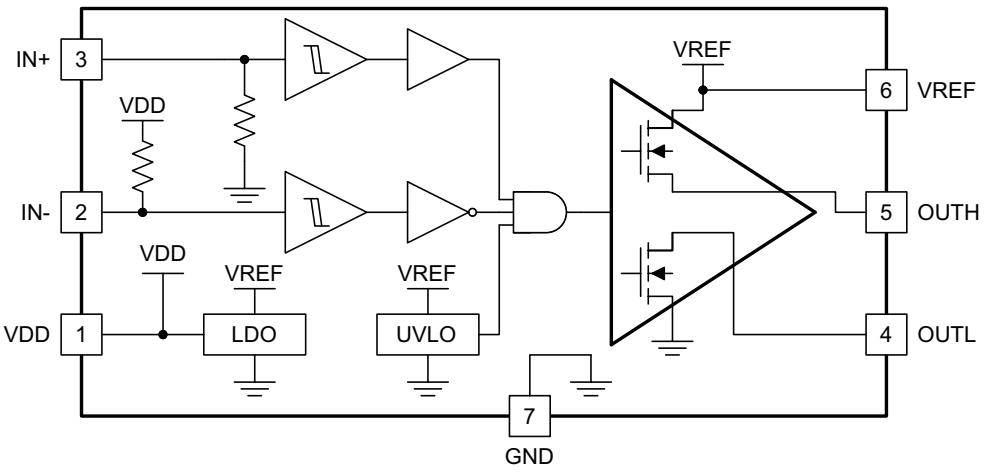


Figure 4. Output Falling
(Ch1 = IN+, Ch2 = OUTPUT)

DEVICE INFORMATION

Block Diagram



DRV Package
(Top view)

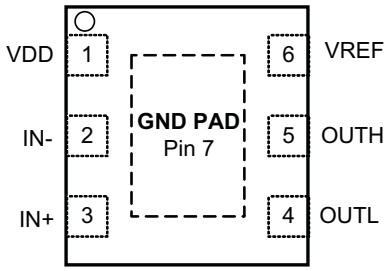


Figure 5.

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
VDD	1	I	Bias supply input. Connect a 2-µf ceramic capacitor minimum from this pin to the GND pin as close as possible to the device with the shortest trace lengths possible.
IN-	2	I	Inverting input. Pull IN+ to VDD in order to enable Output, when using the driver device in Inverting configuration.
IN+	3	I	Non-inverting input. Pull IN- to GND in order to enable output, when using the driver device in non-inverting configuration.
OUTL	4	O	8-A sink current output of driver.
OUTH	5	O	4-A source current output of driver.
VREF	6	O	Drive voltage, output of internal linear regulator. Connect a 2-µf ceramic capacitor minimum from this pin to the GND pin as close as possible to the device with the shortest trace lengths possible.
GND PAD	7	-	Ground. All signals are referenced to this node.

INPUT AND OUTPUT LOGIC TRUTH TABLE

IN+ PIN	IN- PIN	OUTH PIN	OUTL PIN	OUT (OUTH and OUTL pins tied together)
L	L	High-impedance	L	L
L	H	High-impedance	L	L
H	L	H	High-impedance	H
H	H	High-impedance	L	L

TYPICAL CHARACTERISTICS

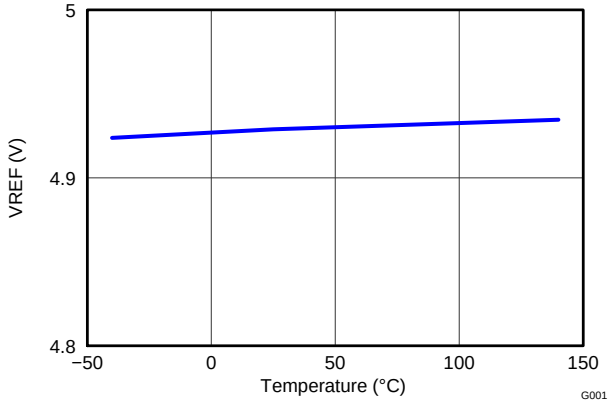


Figure 6. Reference Voltage vs. Temperature

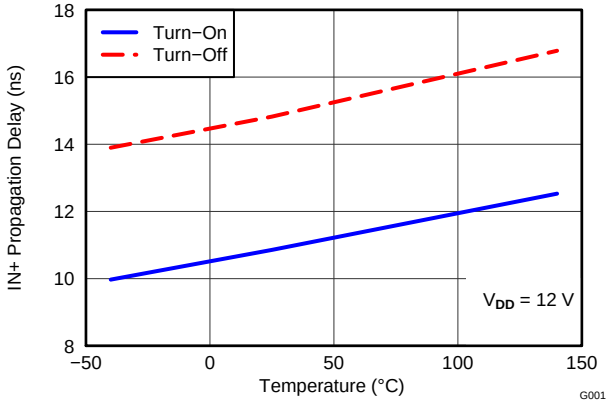


Figure 7. IN+ Propagation Delay

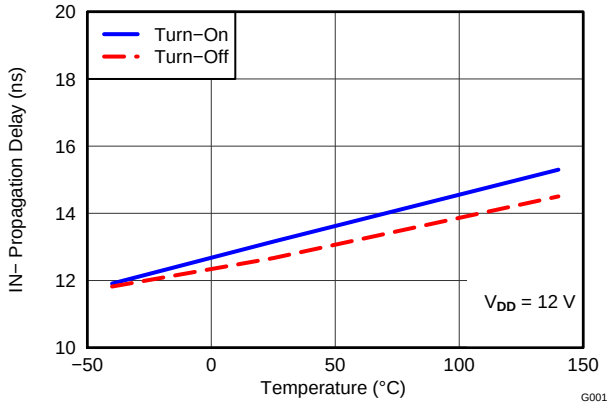


Figure 8. IN- Propagation Delay

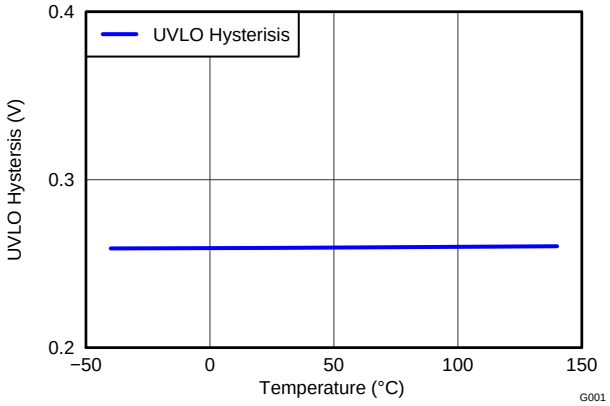


Figure 9. UVLO Hysteresis

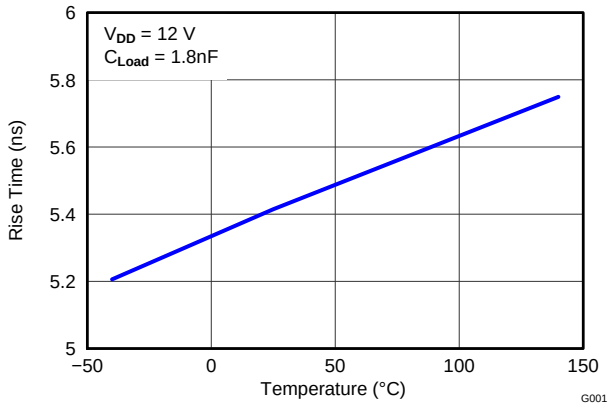


Figure 10. Rise Time

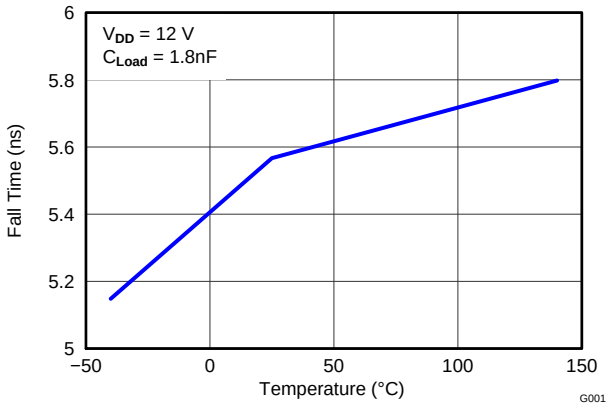


Figure 11. Fall Time

APPLICATION INFORMATION

Introduction

High-current gate driver devices are required in switching power applications for a variety of reasons. In order to effect fast switching of power devices and reduce associated switching power losses, a powerful gate driver can be employed between the PWM output of controllers and the gates of the power semiconductor devices. Further, gate drivers are indispensable when sometimes it is just not feasible to have the PWM controller directly drive the gates of the switching devices. With advent of digital power, this situation will be often encountered since the PWM signal from the digital controller is often a 3.3-V logic signal which is not capable of effectively turning on a power switch. A level shifting circuitry is needed to boost the 3.3-V signal to the gate-drive voltage (such as 12 V) in order to fully turn on the power device and minimize conduction losses. Traditional buffer drive circuits based on NPN and PNP bipolar transistors in totem-pole arrangement, being emitter follower configurations, prove inadequate with digital power since they lack level-shifting capability. Gate drivers effectively combine both the level-shifting and buffer-drive functions. Gate drivers also find other needs such as minimizing the effect of high-frequency switching noise by locating the high-current driver physically close to the power switch, driving gate-drive transformers and controlling floating power-device gates, reducing power dissipation and thermal stress in controllers by moving gate charge power losses into itself. Finally, emerging wide band-gap power device technologies such as GaN based switches, which are capable of supporting very high switching frequency operation, are driving very special requirements in terms of gate drive capability. These requirements include operation at low VDD voltages (5 V or lower), low propagation delays and availability in compact, low-inductance packages with good thermal capability. In summary gate-driver devices are extremely important components in switching power combining benefits of high-performance, low cost, component count and board space reduction and simplified system design.

VDD and Undervoltage Lockout

The UCC27611 devices have internal Under Voltage LockOut (UVLO) protection feature on the VDD pin supply circuit blocks. Whenever the driver is in UVLO condition (i.e. when VDD voltage less than VON during power up and when VDD voltage is less than VOFF during power down), this circuit holds all outputs LOW, regardless of the status of the inputs. The UVLO is typically 3.8 V with 250-mV typical hysteresis. This hysteresis helps prevent chatter when low VDD supply voltages have noise from the power supply and also when there are droops in the VDD bias voltage when the system commences switching and there is a sudden increase in IDD. The capability to operate at low voltage levels such as below 5 V, along with best-in-class switching characteristics, is especially suited for driving emerging GaN wide bandgap power semiconductor devices.

For example, at power up, the UCC27611 driver output remains LOW until the VDD voltage reaches the UVLO threshold. The magnitude of the OUT signal rises with VDD until steady-state VDD is reached. In the non-inverting operation (PWM signal applied to IN+ pin) shown below, the output remains LOW until the UVLO threshold is reached, and then the output is in-phase with the input. In the inverting operation (PWM signal applied to IN- pin) shown below the output remains LOW until the UVLO threshold is reached, and then the output is out-phase with the input. In both cases, the unused input pin must be properly biased to enable the output. It is worth noting that in these devices the output turns to high state only if IN+ pin is high and IN- pin is low after the UVLO threshold is reached.

Since the driver draws current from the VDD pin to bias all internal circuits, for the best high-speed circuit performance, two VDD bypass capacitors are recommended to prevent noise problems. The use of surface mount components is highly recommended. A 0.1-µF ceramic capacitor should be located as close as possible to the VDD to GND pins of the gate driver. In addition, a larger capacitor (such as 1 µF) with relatively low ESR should be connected in parallel and close proximity, in order to help deliver the high-current peaks required by the load. The parallel combination of capacitors should present a low impedance characteristic for the expected current levels and switching frequencies in the application.

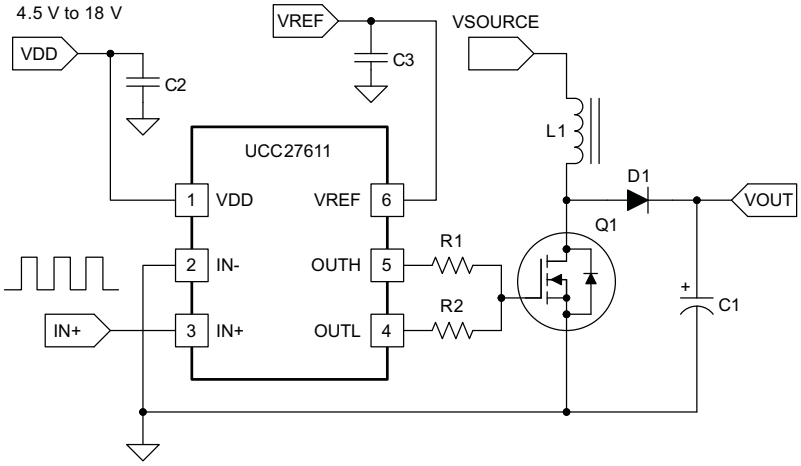


Figure 12. Power Up (non-inverting drive)

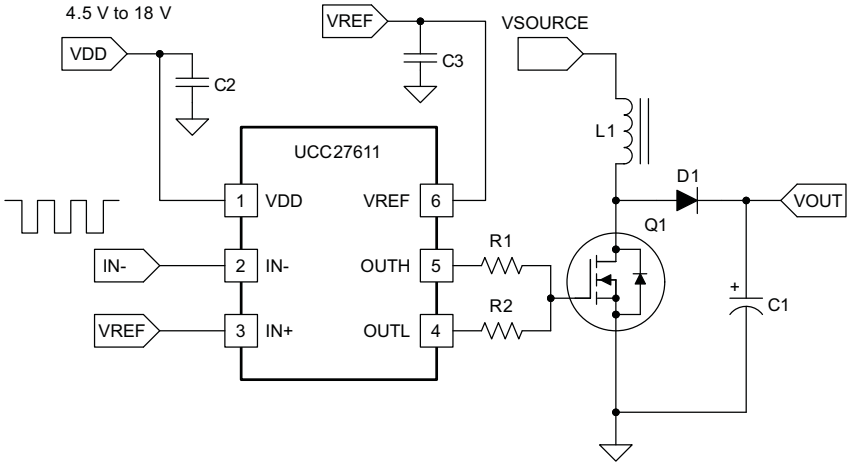


Figure 13. Power Up (inverting drive)

Operating Supply Current

The UCC27611 feature very low quiescent I_{DD} current. The total supply current is the sum of the quiescent IDD current, the average I_{OUT} current due to switching and finally any current related to pull-up resistors on the unused input pin. For example when the inverting input pin is pulled low additional current is drawn from VDD supply through the pull-up resistors (refer to DEVICE INFORMATION for the device Block Diagram). Knowing the operating frequency (f_{SW}) and the MOSFET gate (Q_G) charge at the drive voltage being used, the average I_{OUT} current can be calculated as product of Q_G and f_{SW}.

Input Stage

The input pins of the UCC27611 is based on a TTL and CMOS compatible input threshold logic that is independent of the VDD supply voltage. With typical high threshold = 1.95 V and typical low threshold = 1.3 V, the logic level thresholds can be conveniently driven with PWM control signals derived from 3.3-V and 5-V digital power controllers. Wider hysteresis (typ 1 V) offers enhanced noise immunity compared to traditional TTL logic implementations, where the hysteresis is typically less than 0.5 V. These devices also feature tight control of the input pin threshold voltage levels which eases system design considerations and ensures stable operation across temperature. The very low input capacitance on these pins reduces loading and increases switching speed.

The device features an important safety function wherein, whenever any of the input pins are in a floating condition, the output of the respective channel is held in the low state. This is achieved using VDD pull-up resistors on all the inverting inputs (IN- pin) or GND pull-down resistors on all the non-inverting input pins (IN+ pin), (refer to DEVICE INFORMATION for the device Block Diagram).

The device also features a dual input configuration with two input pins available to control the state of the output. The user has the flexibility to drive the device using either a non-inverting input pin (IN+) or an inverting input pin (IN-). The state of the output pin is dependent on the bias on both the IN+ and IN- pins. Refer to INPUT AND OUTPUT LOGIC TRUTH TABLE input and output logic truth table and the Typical Application Diagram, for additional clarification.

Once an input pin has been chosen for PWM drive, the other input pin (the unused input pin) must be properly biased in order to enable the output. As mentioned earlier, the unused input pin cannot remain in a floating condition because whenever any input pin is left in a floating condition the output is disabled for safety purposes. Alternatively, the unused input pin can effectively be used to implement an enable and disable function, as explained below.

- In order to drive the device in a non-inverting configuration, apply the PWM control input signal to IN+ pin. In this case, the unused input pin, IN-, must be biased low (tied to GND) in order to enable the output.
  - Alternately, the IN- pin can be used to implement the enable and disable function using an external logic signal. OUT is disabled when IN- is biased high and OUT is enabled when IN- is biased low.
- In order to drive the device in an inverting configuration, apply the PWM control input signal to IN- pin. In this case, the unused input pin, IN+, must be biased high (eg. tied to VDD) in order to enable the output.
  - Alternately, the IN+ pin can be used to implement the enable and disable function using an external logic signal. OUT is disabled when IN+ is biased low and OUT is enabled when IN+ is biased high.
- Finally, it is worth noting that the output pin can be driven into a high state ONLY when IN+ pin is biased high and IN- input is biased low.

The input stage of the driver should preferably be driven by a signal with a short rise or fall time. Caution must be exercised whenever the driver is used with slowly varying input signals, especially in situations where the device is located in a mechanical socket or PCB layout is not optimal:

- High dI and dt current from the driver output coupled with board layout parasitic can cause ground bounce. Since the device features just one GND pin which may be referenced to the power ground, this may modify the differential voltage between input pins and GND and trigger an unintended change of output state. Because of fast 13-ns propagation delay, this can ultimately result in high-frequency oscillations, which increases power dissipation and poses risk of damage.
- 1-V input threshold hysteresis boosts noise immunity compared to most other industry standard drivers.
- In the worst case, when a slow input signal is used and PCB layout is not optimal, it may be necessary to add a small capacitor (1 nF) between input pin and ground very close to the driver device. This helps to convert the differential mode noise with respect to the input logic circuitry into common mode noise and avoid unintended change of output state.

Enable Function

As mentioned earlier, an enable and disable function can be easily implemented in UCC27611 using the unused input pin. When IN+ is pulled down to GND or IN- is pulled down to VDD, the output is disabled. Thus IN+ pin can be used like an enable pin that is based on active high logic, while IN- can be used like an enable pin that is based on active low logic.

Output Stage

The output stage of the UCC27611 device is illustrated in Figure 14. OUTH and OUTL are externally connected and pinned out as OUTH and OUTL pins. The UCC27611 device features a unique architecture on the output stage which delivers the highest peak source current when it is most needed during the Miller plateau region of the power switch turn-on transition (when the power switch drain and collector voltage experiences dV and dt). The device output stage features a hybrid pull-up structure using a parallel arrangement of N-channel and P-channel MOSFET devices. By turning on the N-channel MOSFET during a narrow instant when the output changes state from low to high, the gate-driver device is able to deliver a brief boost in the peak-sourcing current enabling fast turn on.

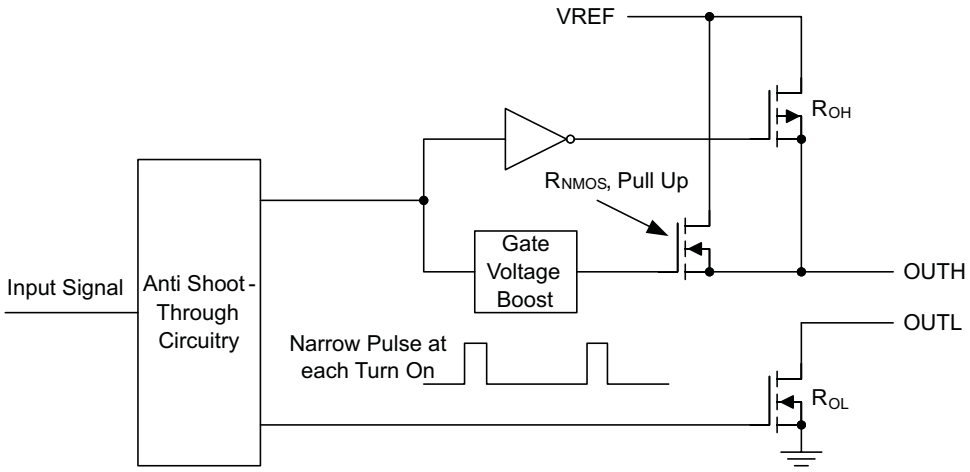


Figure 14. UCC27611 Gate Driver Output Structure

The R_{OH} parameter (see ELECTRICAL CHARACTERISTICS) is a DC measurement and it is representative of the on-resistance of the P-channel device only, since the N-channel device is turned on only during output change of state from low to high. Thus the effective resistance of the hybrid pull-up stage is much lower than what is represented by ROH parameter. The pull-down structure is composed of a N-channel MOSFET only. The R_{OL} parameter (see ELECTRICAL CHARACTERISTICS), which is also a DC measurement, is representative of true impedance of the pull-down stage in the device.

The UCC27611 is capable of delivering 4-A source, 6-A sink (asymmetrical drive) at VDD = 12 V. Strong sink capability in asymmetrical drive results in a very low pull-down impedance in the driver output stage which boosts immunity against parasitic, Miller turn on (C x dV/dt turn on) effect, especially where low gate-charge MOSFETs or emerging wide band-gap GaN power switches are used.

An example of a situation where Miller turn on is a concern is synchronous rectification (SR). In SR application, the dV and dt occurs on MOSFET drain when the MOSFET is already held in off state by the gate driver. The current discharging the C_{GD} Miller capacitance during this dV and dt is shunted by the pull-down stage of the driver. If the pull-down impedance is not low enough then a voltage spike can result in the V_{GS} of the MOSFET, which can result in spurious turn on. This phenomenon is illustrated in Figure 15. UCC27611 offers a best-in-class, 0.35-Ω (typ) pull-down impedance boosting immunity against Miller turn on.

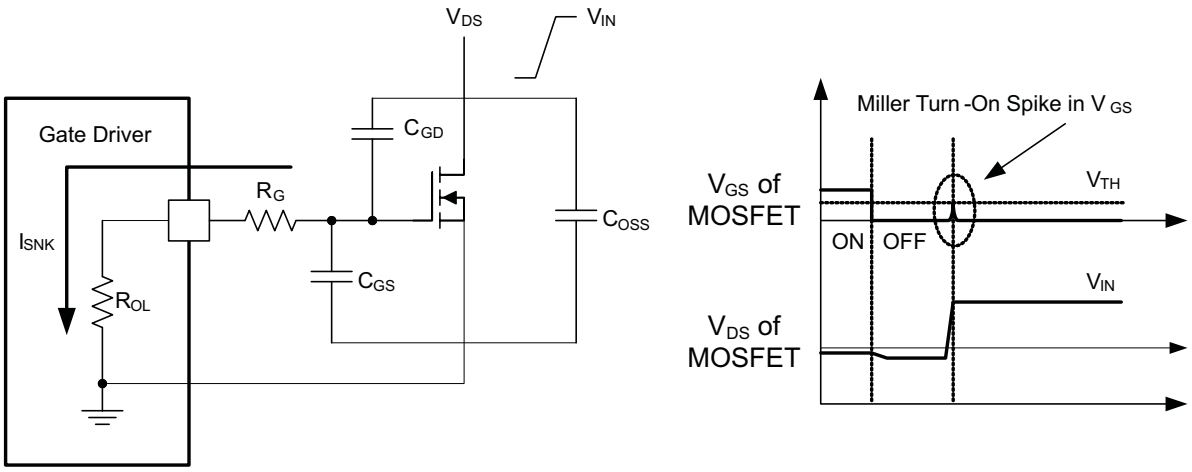


Figure 15. Low Pull-Down Impedance in UCC27611, 4-A and 6-A Asymmetrical Drive (output stage mitigates Miller turn-on effect)

The driver output voltage swings between VDD and GND providing rail-to-rail operation, thanks to the MOS output stage which delivers very low dropout. The presence of the MOSFET body diodes also offers low impedance to switching overshoots and undershoots. This means that in many cases, external Schottky diode clamps may be eliminated. The outputs of these drivers are designed to withstand 500-mA reverse current without either damage to the device or logic malfunction.

Power Dissipation

Power dissipation of the gate driver has two portions as shown in equation below:

$$P_{DISS} \times P_{DC} + P_{SW} \quad (1)$$

The DC portion of the power dissipation is $P_{DC} = I_Q \times V_{DD}$ where I_Q is the quiescent current for the driver. The quiescent current is the current consumed by the device to bias all internal circuits such as input stage, reference voltage, logic circuits, protections etc and also any current associated with switching of internal devices when the driver output changes state (such as charging and discharging of parasitic capacitances, parasitic shoot-through etc). The UCC27611 features very low quiescent currents (less than 1 mA, refer ELECTRICAL CHARACTERISTICS) and contains internal logic to eliminate any shoot-through in the output driver stage. Thus the effect of the P_{DC} on the total power dissipation within the gate driver can be safely assumed to be negligible.

The power dissipated in the gate-driver package during switching (P_{SW}) depends on the following factors:

- Gate charge required of the power device (usually a function of the drive voltage V_G, which is very close to input bias supply voltage V_{REF} due to low V_{OH} dropout).
- Switching frequency.
- Use of external gate resistors.

When a driver device is tested with a discrete, capacitive load it is a fairly simple matter to calculate the power that is required from the bias supply. The energy that must be transferred from the bias supply to charge the capacitor is given by:

$$EG = \frac{1}{2} \times C_{LOAD} \times V_{REF}^2$$

where

- Where C_{LOAD} is load capacitor and VDD is bias voltage feeding the driver. (2)

There is an equal amount of energy dissipated when the capacitor is charged. This leads to a total power loss given by the following:

$$P_G = C_{LOAD} \times V_{REF}^2 \times f_{SW}$$

where

- where f_{SW} is the switching frequency. (3)

The switching load presented by a power MOSFET and IGBT can be converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain voltage of the power device as it switches between the ON and OFF states. Most manufacturers provide specifications of typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge Q_g, one can determine the power that must be dissipated when charging a capacitor. This is done by using the equation, $Q_G = C_{LOAD} \times V_{DD}$, to provide the following equation for power:

$$P_G = C_{LOAD} \times V_{REF}^2 \times f_{SW} = Q_g \times V_{REF}^2 \times f_{SW} \quad (4)$$

This power P_G is dissipated in the resistive elements of the circuit when the MOSFET and IGBT is being turned on or off. Half of the total power is dissipated when the load capacitor is charged during turnon, and the other half is dissipated when the load capacitor is discharged during turnoff. When no external gate resistor is employed between the driver and MOSFET and IGBT, this power is completely dissipated inside the driver package. With the use of external gate-drive resistors, the power dissipation is shared between the internal resistance of driver and external gate resistor in accordance to the ratio of the resistances (more power dissipated in the higher resistance component). Based on this simplified analysis, the driver power dissipation during switching is calculated as follows:

$$P_{SW} = Q_g \times V_{REF} \times f_{SW} \left(\frac{R_{OFF}}{(R_{OFF} + R_{GATE})} \times \frac{R_{ON}}{(R_{ON} + R_{GATE})} \right)$$

where

- where $R_{OFF} = R_{OL}$ and R_{ON} (effective resistance of pull-up structure) = 2.7 x R_{OL} (5)

Low Propagation Delays

The UCC27611 driver devices feature best-in-class input-to-output propagation delay of 13 ns (typ) at VDD = 12 V. This promises the lowest level of pulse transmission distortion available from industry standard gate driver devices for high-frequency switching applications. As seen in Figure 7 and Figure 8, there is very little variation of the propagation delay with temperature and supply voltage as well, offering typically less than 20-ns propagation delays across the entire range of application conditions.

Reference Voltage (VREF)

The UCC27611 is a high-performance driver capable of fast rise and fall times at high-peak currents. Careful PCB layout to reduce parasitic inductances is critical to achieve maximum performance. When a less-than-optimal layout is unavoidable then the addition of a low capacitance schottky diode is recommended to prevent the energy ringing back from the gate and charging up the decoupling capacitor on VREF (see Figure 19).

The parasitic board inductance in conjunction with the Miller capacitance of the FET can cause excessive ringing on the gate drive waveform resulting in peaks higher that the regulated VREF drive voltage. With enough energy present the potential exists to charge the VREF decoupling capacitor higher than the 6-V maximum allowed on a Gallium Nitride transistor. To prevent this from happening, a low capacitance Schottky diode can be placed in the OUTH trace as shown below.

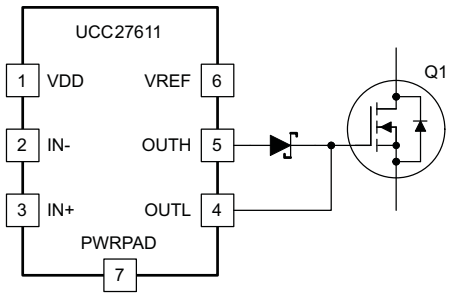


Figure 16. Low Capacitance Schottky Diode (see Figure 20)

The alternate method would be to add a loading resistor to VREF to bleed off the charge.

This method eliminates the additional voltage drop from the diode but, reduces the current available for additional circuits or gate drive if too small a value of resistor is used.

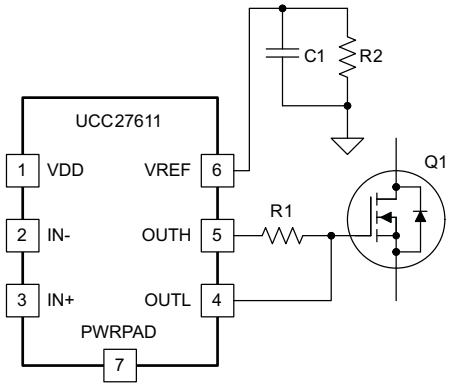


Figure 17. Loading Resistor to VREF (see Figure 21)

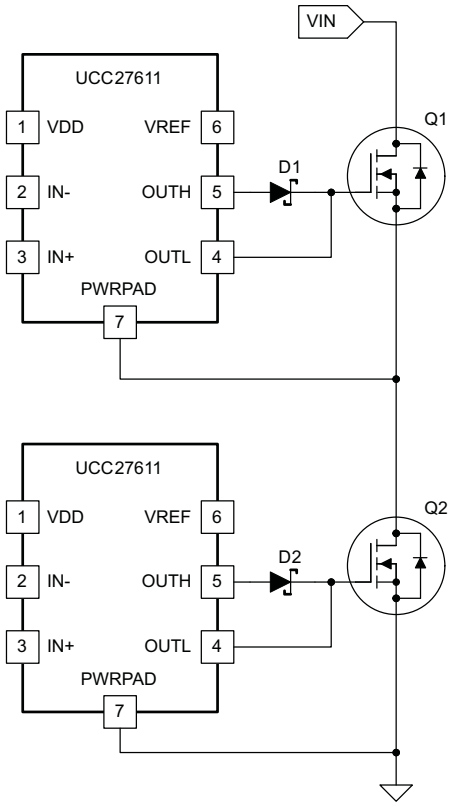


Figure 18. Typical Application

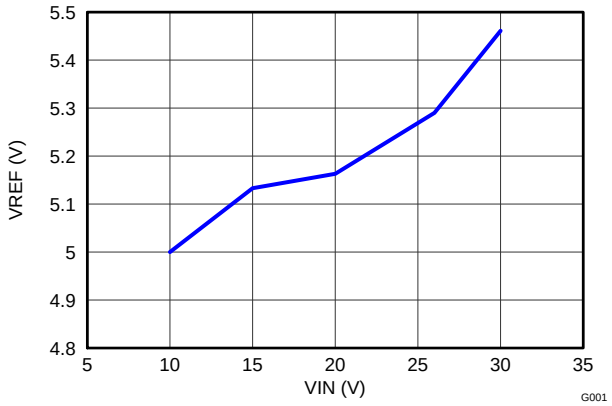


Figure 19. Reference Voltage vs. Input Voltage (VREF(cap) Charging)

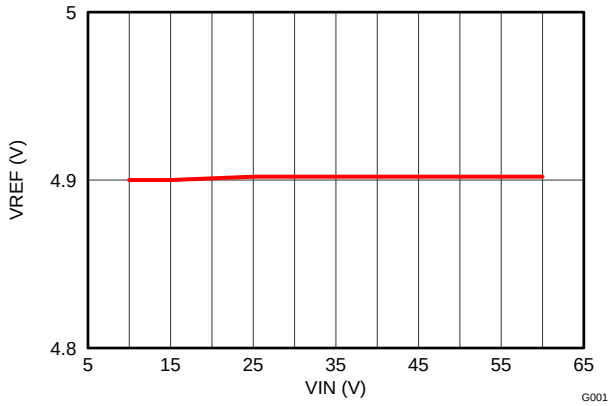


Figure 20. Reference Voltage vs. Input Voltage (VREF(cap) not charging, Schottky diode on OUTH)

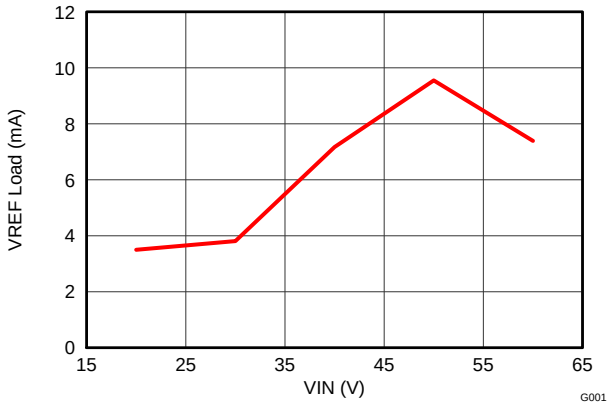


Figure 21. Reference Voltage Load Current vs. Input Voltage

Thermal Information

The useful range of a driver is greatly affected by the drive power requirements of the load and the thermal characteristics of the package. In order for a gate driver to be useful over a particular temperature range the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The thermal metrics for the driver package is summarized in the Thermal Information section of the datasheet. For detailed information regarding the thermal information table, please refer to the Application Note from Texas Instruments entitled IC Package Thermal Metrics (Texas Instruments Literature Number SPRA953A).

UCC27611 Offered in WSON, 7-Pin Package (DRV)

6-pin package with exposed thermal pad. The thermal information table summarizes the thermal performance metrics related to the two packages. θ_{JA} metric should be used for comparison of power dissipation between different packages. Under identical power dissipation conditions, the DRS package will maintain a lower die temperature than the D_{BV}. The ψ_{JT} and ψ_{JB} metrics should be used when estimating the die temperature during actual application measurements.

The DRV is a better thermal package overall because it has the exposed thermal pad and is able to sink heat to the PCB. The thermal pad in DRV package provides designers with an ability to create an excellent heat removal sub-system from the vicinity of the device, thus helping to maintain a lower junction temperature. This pad should be soldered to the copper on the printed circuit board directly underneath the device package. Then a printed circuit board designed with thermal lands and thermal vias completes a very efficient heat removal subsystem. In such a design, the heat is extracted from the semiconductor junction through the thermal pad, which is then efficiently conducted away from the location of the device on the PCB through the thermal network. This helps to maintain a lower board temperature near the vicinity of the device leading to an overall lower device junction temperature.

NOTE

The exposed pad in DRV package is directly connected to the GND of the internal circuitry. It is electrically and thermally connected to the device which is the ground of the device. It is required to externally connect the exposed pad to GND in PCB layout.

PCB Layout Recommendation

Proper PCB layout is extremely important in a high-current, fast-switching circuit to provide appropriate device operation and design robustness. The UCC27611 gate driver incorporates short-propagation delays and powerful output stages capable of delivering large current peaks with very fast rise and fall times at the gate of power switch to facilitate voltage transitions very quickly. At higher VDD voltages, the peak-current capability is even higher (4-A and 6-A peak current is at VDD = 12 V). Very high di and dt can cause unacceptable ringing if the trace lengths and impedances are not well controlled. The following circuit layout guidelines are strongly recommended when designing with these high-speed drivers.

- Locate the driver device as close as possible to power device in order to minimize the length of high-current traces between the output pins and the gate of the power device.
- Locate the VDD and VREF bypass capacitors between VDD, VREF and GND as close as possible to the driver with minimal trace length to improve the noise filtering. These capacitors support high-peak current being drawn from VDD during turn on of power MOSFET. The use of low inductance SMD components such as chip resistors and chip capacitors is highly recommended.
- The turn-on and turn-off current loop paths (driver device, power MOSFET and VDD, VREF bypass capacitors) should be minimized as much as possible in order to keep the stray inductance to a minimum. High dI and dt is established in these loops at two instances – during turn-on and turn-off transients, which will induce significant voltage transients on the output pin of the driver device and gate of the power switch.
- Wherever possible parallel the source and return traces, taking advantage of flux cancellation.
- Separate power traces and signal traces, such as output and input signals.
- Star-point grounding is a good way to minimize noise coupling from one current loop to another. The GND of the driver should be connected to the other circuit nodes such as source of power switch, ground of PWM controller etc at one, single point. The connected paths should be as short as possible to reduce inductance and be as wide as possible to reduce resistance.
- Use a ground plane to provide noise shielding. Fast rise and fall times at OUT may corrupt the input signals during transition. The ground plane must not be a conduction path for any current loop. Instead the ground plane must be connected to the star-point with one single trace to establish the ground potential. In addition to noise shielding, the ground plane can help in power dissipation as well.
- In noisy environments, it may be necessary to tie the unused Input pin of UCC27611 to VDD or VREF (in case of IN+) or GND (in case of IN-) using short traces in order to ensure that the output is enabled and to prevent noise from causing malfunction in the output.

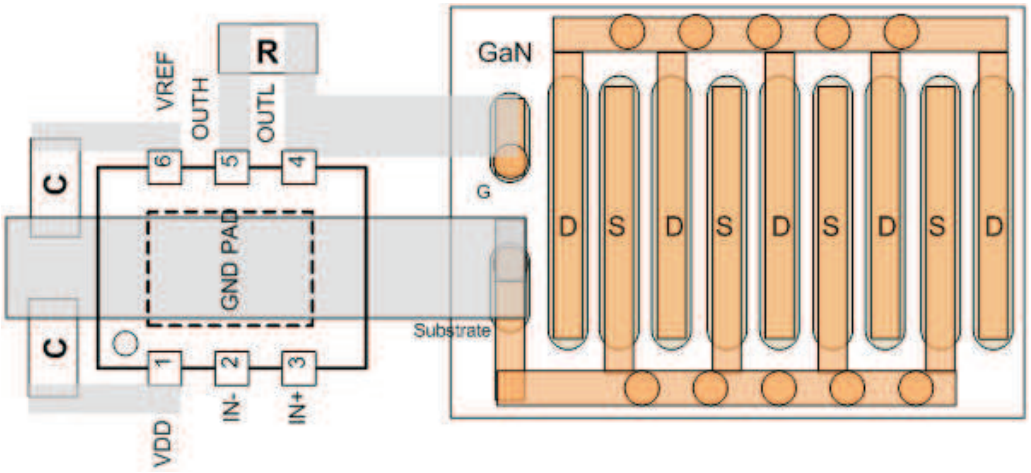


Figure 22. PCB Layout Recommendation

REVISION HISTORY

Changes from Original (December 2012) to Revision A	Page
• Changed marketing status from Product Preview to Production Data.	1

Changes from Revision A (December, 2012) to Revision B	Page
• Added ELECTRICAL CHARACTERISTICS Inputs (IN+, IN-) section values.	4

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC27611DRVR	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 140	7611	Samples
UCC27611DRVT	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 140	7611	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

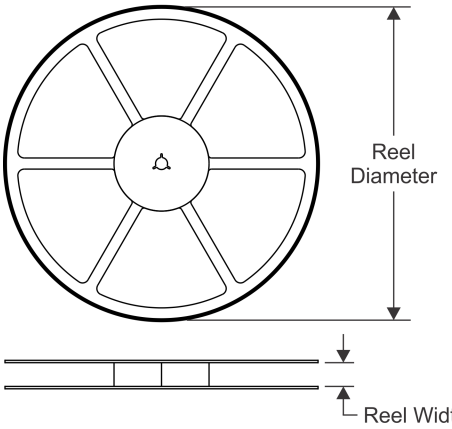
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

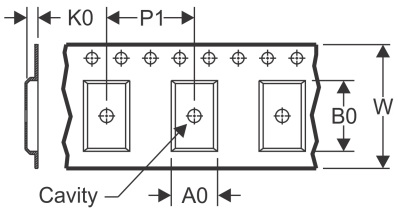
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

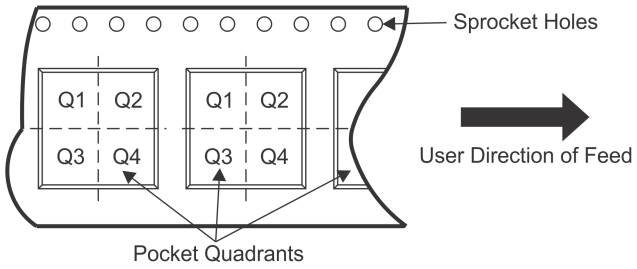


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

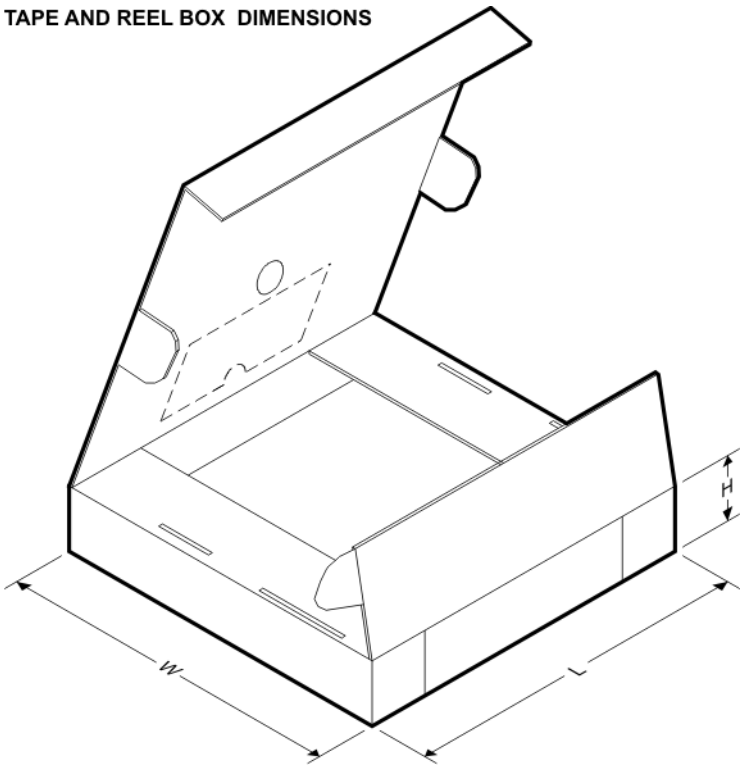
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC27611DRVR	SON	DRV	6	3000	330.0	24.4	2.3	2.3	1.15	4.0	8.0	Q2
UCC27611DRVT	SON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

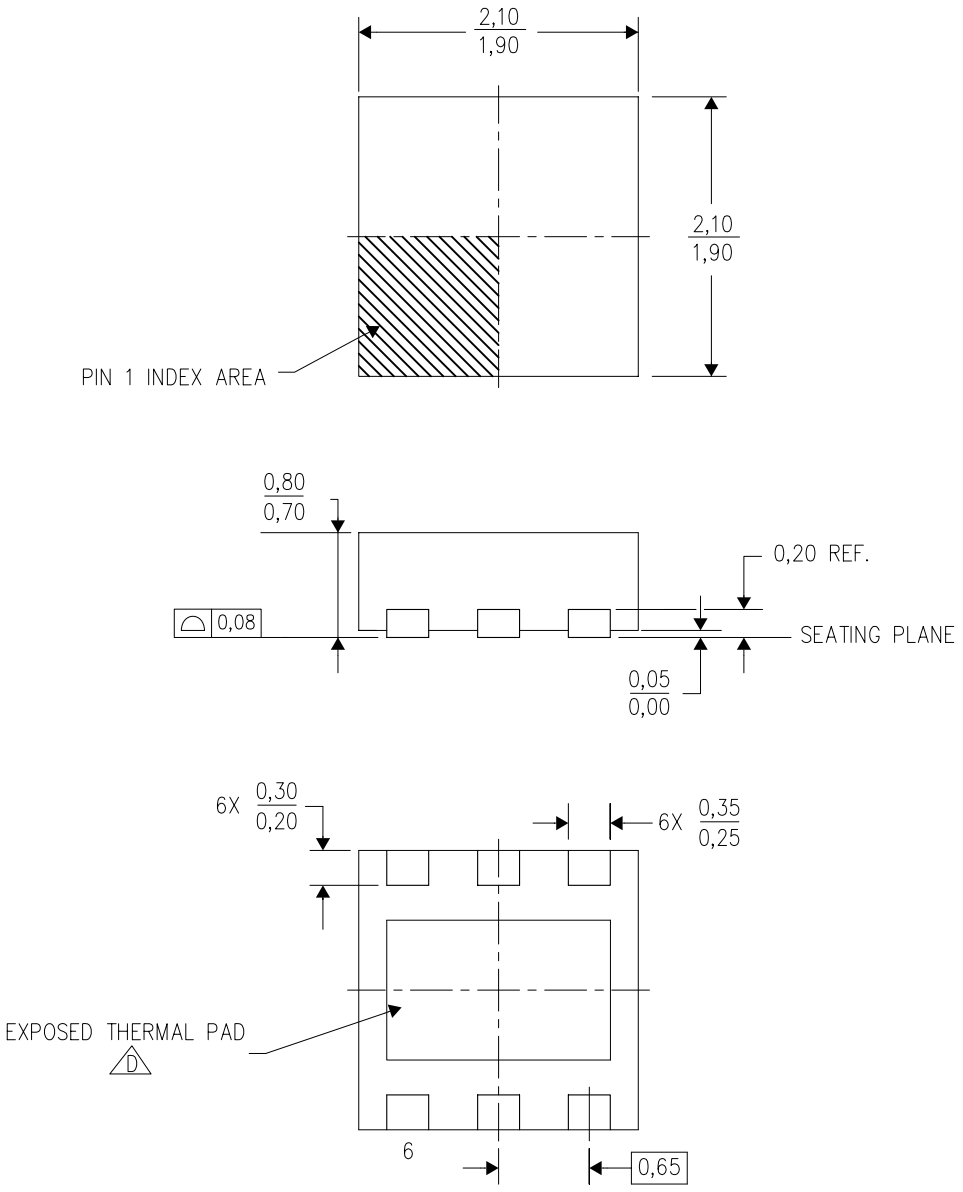
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC27611DRVR	SON	DRV	6	3000	367.0	367.0	35.0
UCC27611DRVT	SON	DRV	6	250	210.0	185.0	35.0

DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



4206925/E 10/10

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

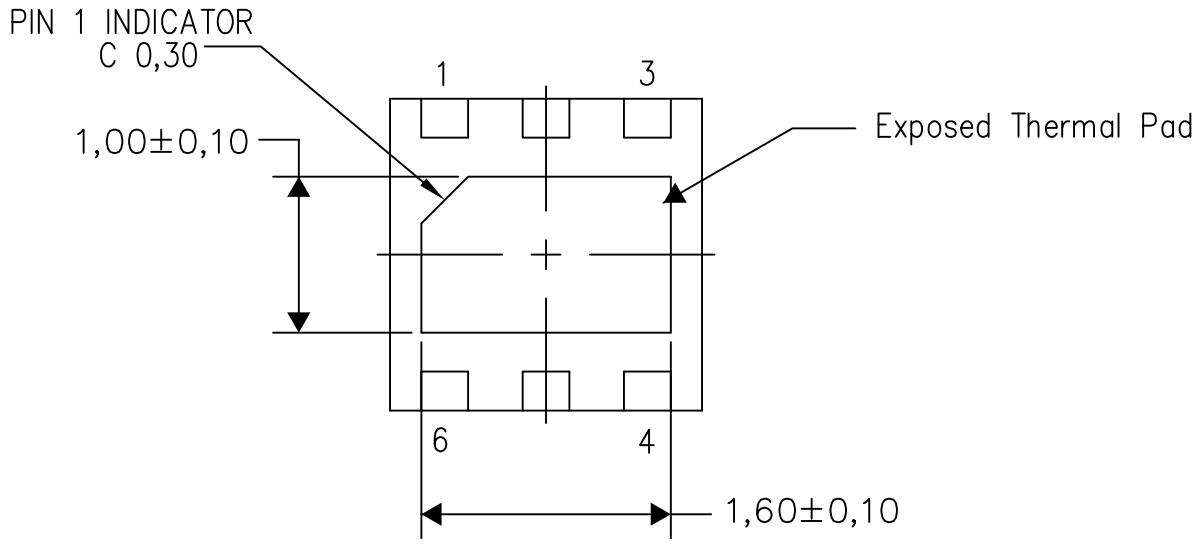
DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



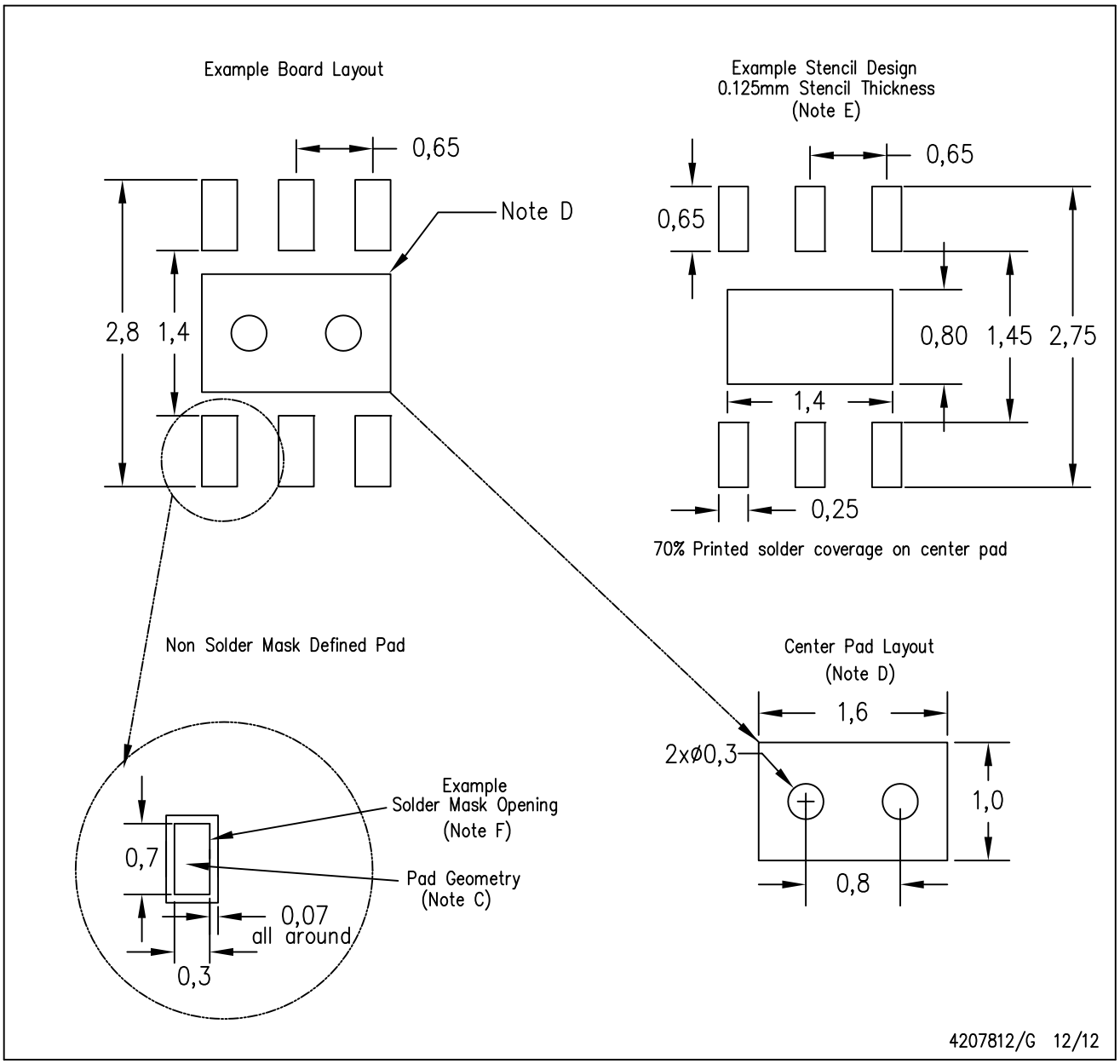
Bottom View

Exposed Thermal Pad Dimensions

4206926/N 03/13

NOTE: All linear dimensions are in millimeters

DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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