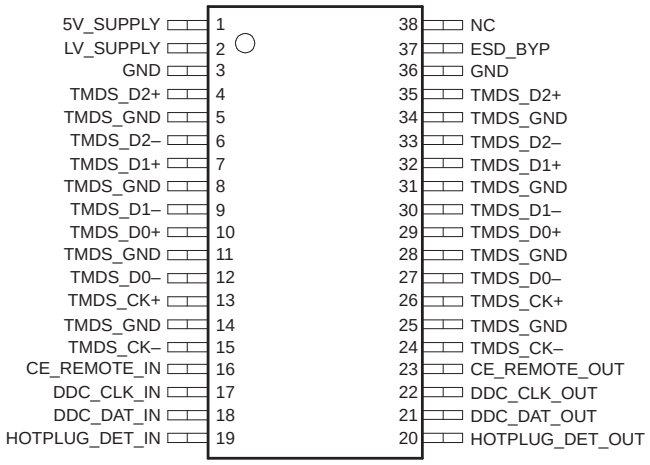
# SINGLE-CHIP HDMI RECEIVER PORT PROTECTION AND INTERFACE DEVICE

## FEATURES

- **Single-Chip ESD Solution for High-Definition Multmedia Interface (HDMI)**
- **Supports HDMI 1.3 Data Rate**
- **0.8-pF Capacitance for High-Speed Transition Minimized Directional Signaling (TMDS) Lines**
- **0.05-pF Matching Capacitance Between Differential Signal Pair**
- **Integrated Level Shifting for Control Lines**
- **±8-kV Contact Electrostatic Discharge (ESD) Protection on External Lines**
- **38-Pin Thin Shrink Small-Outline Package (TSSOP) Provides Seamless Layout Option With HDMI Connector**
- **Backdrive Protection**
- **Lead-Free Package**

**DBT PACKAGE**
**(TOP VIEW)**




## APPLICATIONS

- **Video Interfaces**
- **Consumer Electronics**
- **Displays and Digital Televisions**

## DESCRIPTION/ORDERING INFORMATION

The TPD12S520 is a single-chip electrostatic dischare (ESD) solution for the high-definition multmedia interface (HDMI) receiver port. In many cases, the core ICs, such as the scalar chipset, may not have robust ESD cells to sustain system-level ESD strikes. In these cases, the TPD12S520 provides the desired system-level ESD protection, such as the IEC61000-4-2 (Level 4) ESD, by absorbing the energy associated with the ESD strike.

While providing ESD protection, the TPD12S520 adds little or no additional glitch in the high-speed differential signals (see Figure 4 and Figure 5). High-speed transition minimized directional signaling (TMDS) lines add only 0.8-pF capacitance to the lines. In addition, monolithic integrated circuit technology ensures excellent matching between the two-signal pair of the differential line. This is a direct advantage over discrete ESD clamp solutions where variations between two different ESD clamps may significantly degrade the differential signal quality.

The low-speed control lines offer voltage level-shifting to eliminate the need for an external voltage-level shifter IC. Control-line ESD clamps add 3.5-pF capacitance to the control lines.

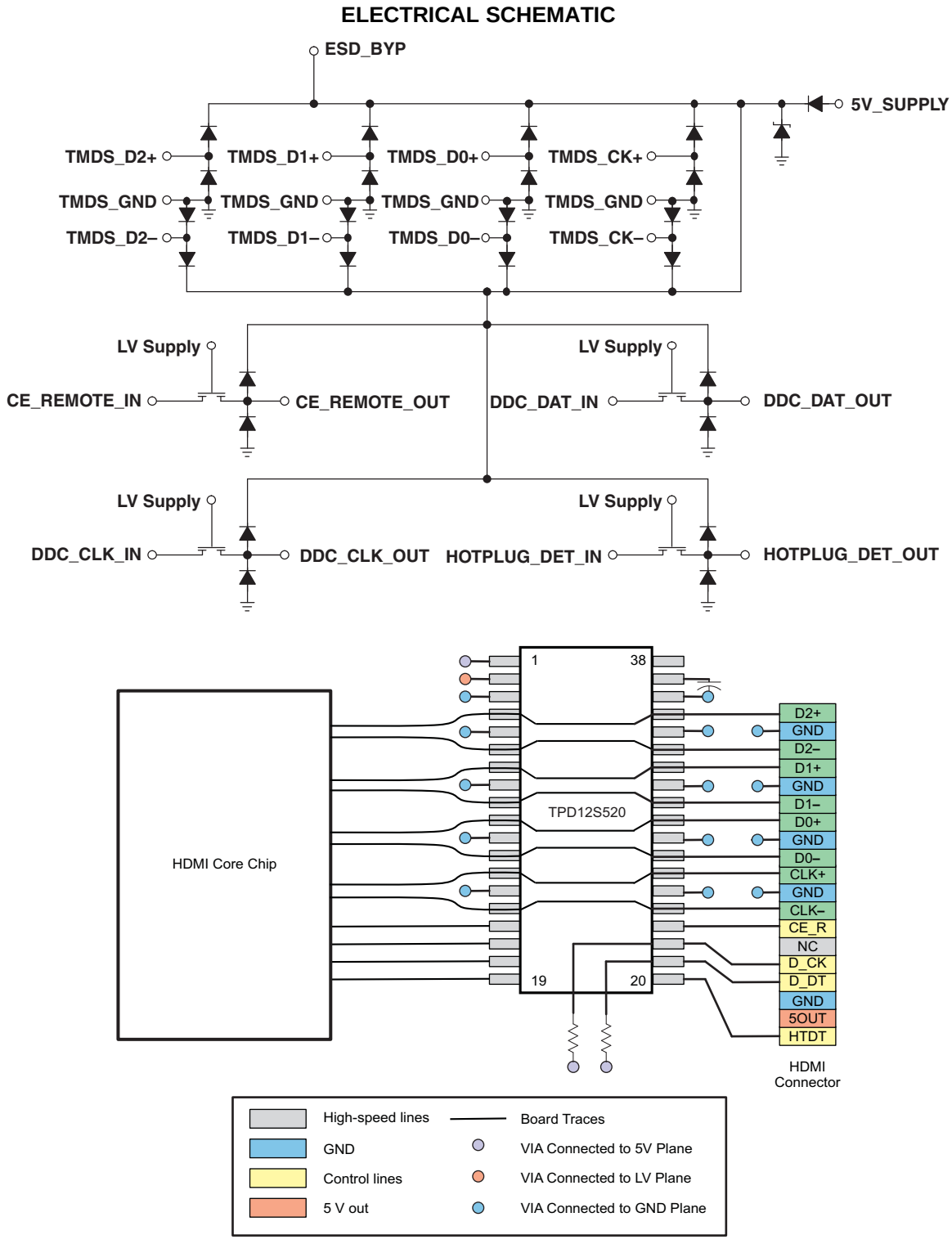
The 38-pin DBT package offers a seamless layout routing option (see Figure 1) to eliminate the routing glitch for the differential signal pair. DBT package pitch (0.5 mm) matches HDMI connector pitch. In addition, the pin mapping follows the same order as the HDMI connector pin mapping. This HDMI receiver port protection and interface device is designed specifically for next-generation HDMI receiver-interface protection.

**ORDERING INFORMATION**

| $T_A$ | PACKAGE(1)(2) | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| –40°C to 85°C | TSSOP-38 – DBT | Tape and reel | TPD12S520DBTR | PN520 |

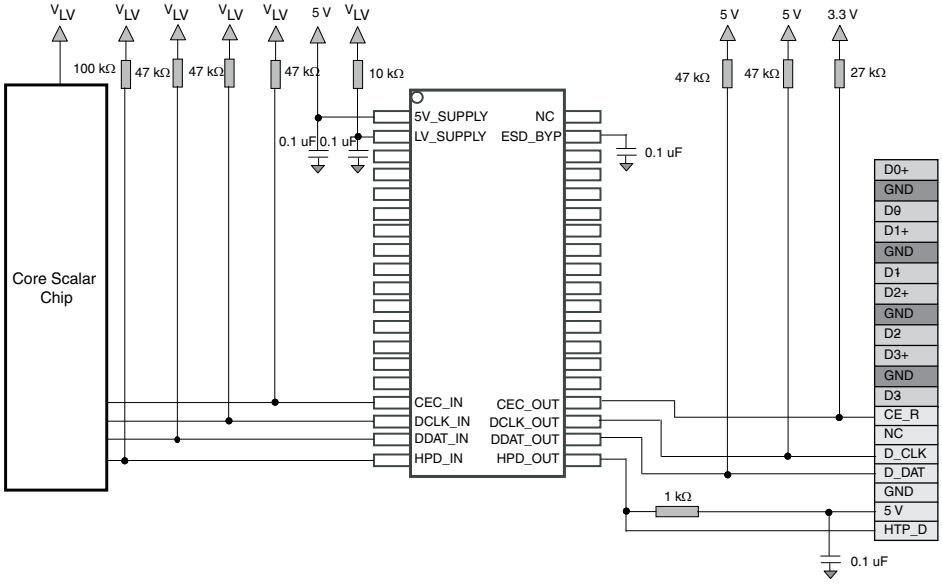
(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.




A. External bypass capacitors and resistor components not included

**Figure 1. Board Layout for HDMI Transmitter Using TPD12S520DBTR**




A. $V_{LV}$ = supply voltage of the core scalar chip

**Figure 2. Application Schematic Showing Pins Requiring External Components: HDMI Receiver Side**

## PIN DESCRIPTION

| NAME | PIN NO. | ESD LEVEL | DESCRIPTION |
|---|---|---|---|
| 5V_SUPPLY | 1 | 2 kV(1) | Current source for 5V_OUT |
| LV_SUPPLY | 2 | 2 kV(1) | Bias for CE/DDC/HOTPLUG level shifters |
| GND, TMDS_GND | 3, 5, 8, 11,14, 25, 28, 31, 34, 36 | NA | TMDS ESD and parasitic GND return(2) |
| TMDS_D2+ | 4, 35 | 8 kV(3) | TMDS 0.9-pF ESD protection(4) |
| TMDS_D2– | 6, 33 | 8 kV(3) | TMDS 0.9-pF ESD protection(4) |
| TMDS_D1+ | 7, 32 | 8 kV(3) | TMDS 0.9-pF ESD protection(4) |
| TMDS_D1– | 9, 30 | 8 kV(3) | TMDS 0.9-pF ESD protection(4) |
| TMDS_D0+ | 10, 29 | 8 kV(3) | TMDS 0.9-pF ESD protection(4) |
| TMDS_D0– | 12, 27 | 8 kV(3) | TMDS 0.9-pF ESD protection(4) |
| TMDS_CK+ | 13, 26 | 8 kV(3) | TMDS 0.9-pF ESD protection(4) |
| TMDS_CK– | 15, 24 | 8 kV(3) | TMDS 0.9-pF ESD protection(4) |
| CE_REMOTE_IN | 16 | 2 kV(1) | LV_SUPPLY referenced logic level into ASIC |
| DDC_CLK_IN | 17 | 2 kV(1) | LV_SUPPLY referenced logic level into ASIC |
| DDC_DAT_IN | 18 | 2 kV(1) | LV_SUPPLY referenced logic level into ASIC |
| HOTPLUG_DET_IN | 19 | 2 kV(1) | LV_SUPPLY referenced logic level into ASIC |
| HOTPLUG_DET_OUT | 20 | 8 kV(3) | 5 V_SUPPLY referenced logic level out, plus 3.5-pF ESD(5) to connector |
| DDC_DAT_OUT | 21 | 8 kV(3) | 5 V_SUPPLY referenced logic level out, plus 3.5-pF ESD to connector |
| DDC_CLK_OUT | 22 | 8 kV(3) | 5 V_SUPPLY referenced logic level out, plus 3.5-pF ESD to connector |
| CE_REMOTE_OUT | 23 | 8 kV(3) | 5 V_SUPPLY referenced logic level out, plus 3.5-pF ESD to connector |
| ESD_BYP | 37 | 2 kV(1) | ESD bypass. This pin must be connected to a 0.1-µF ceramic capacitor. |
| NC | 38 | NA | No connection |

(1) Human-Body Model (HBM) per MIL-STD-883, Method 3015, $C_{DISCHARGE}$ = 100 pF, $R_{DISCHARGE}$ = 1.5 kΩ, 5V_SUPPLY and LV_SUPPLY within recommended operating conditions, GND = 0 V, and ESD_BYP (pin 37) and HOTPLUG_DET_OUT (pin 20) each bypassed with a 0.1-µF ceramic capacitor connected to GND.
(2) These pins should be routed directly to the associated GND pins on the HDMI connector, with single-point ground vias at the connector.
(3) Standard IEC 61000-4-2, $C_{DISCHARGE}$ = 150 pF, $R_{DISCHARGE}$ = 330 Ω, 5V_SUPPLY and LV_SUPPLY within recommended operating conditions, GND = 0 V, and ESD_BYP (pin 37) and HOTPLUG_DET_OUT (pin 20) each bypassed with a 0.1-µF ceramic capacitor connected to GND.
(4) These two pins must be connected together inline on the PCB.
(5) This output can be connected to an external 0.1-µF ceramic capacitor, resulting in an increased ESD withstand voltage rating.

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{5V\_SUPPLY}$<br>$V_{LV\_SUPPLY}$ | Supply voltage | | 6 | V |
| $V_{IO}$ | DC voltage at any channel input | | 6 | V |
| $T_{stg}$ | Storage temperature range | –65 | 150 | °C |

## RECOMMENDED OPERATING CONDITIONS

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{5V\_SUPPLY}$ | Operating supply voltage | GND | 5 | 5.5 | V |
| $V_{LV\_SUPPLY}$ | Bias supply voltage | 1 | 3.3 | 5.5 | V |
| Operating temperature range | | –40 | | 85 | °C |

## ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{5V}$ | Operating supply current | 5V_SUPPLY = 5 V | | | 1 | 5 | µA |
| $I_{LV}$ | Bias supply current | LV_SUPPLY = 3.3 V | | | 1 | 2 | µA |
| $I_{OFF}$ | OFF-state leakage current, level-shifting NFET | LV_SUPPLY = 0 V | | | 0.1 | 1 | µA |
| $I_{BACKDRIVE}$ | Current conducted from output pins to V_SUPPLY rails when powered down | 5V_SUPPLY < $V_{CH\_OUT}$ | TMDS_[2:0]+/–, TMDS_CK+/–, CE_REMOTE_OUT, DDC_DAT_OUT, DDC_CLK_OUT, HOTPLUG_DET_OUT | | 0.1 | 5 | µA |
| $V_{ON}$ | Voltage drop across level-shifting NFET when ON | LV_SUPPLY = 2.5 V, $V_S$ = GND, $I_{DS}$ = 3 mA | | 75 | 95 | 140 | mV |
| $V_F$ | Diode forward voltage | $I_F$ = 8 mA, $T_A$ = 25°C (1) | Top diode | | 1 | | V |
| | | | Bottom diode | | 1 | | |
| $V_{ESD}$ | ESD withstand voltage | Pins 4, 7,10,13, 20–24, 27, 30, 33 (1)(2) | IEC | ±8 | | | kV |
| | | Pins 1, 2, 16–19, 37 (1)(3) | HBM | ±2 | | | |
| $V_{CL}$ | Channel clamp voltage at 8-kV HBM ESD | $T_A$ = 25°C (1)(3) | Positive transients | | 9 | | V |
| | | | Negative transients | | –9 | | |
| $R_{DYN}$ | Dynamic resistance | I = 1 A, $T_A$ = 25°C (4) | Positive transients | | 3 | | Ω |
| | | | Negative transients | | 1.5 | | |
| $I_{LEAK}$ | TMDS channel leakage current | $T_A$ = 25°C (1) | | | 0.01 | 1 | µA |
| $C_{IN}$, TMDS | TMDS channel input capacitance | 5V_SUPPLY = 5 V, Measured at 1 MHz, $V_{BIAS}$ = 2.5 V (1) | | | 0.8 | 1.0 | pF |
| $\Delta C_{IN}$, TMDS | TMDS channel input capacitance matching | 5V_SUPPLY = 5 V, Measured at 1 MHz, $V_{BIAS}$ = 2.5 V (1)(5) | | | 0.05 | | pF |
| $C_{MUTUAL}$ | Mutual capacitance between signal pin and adjacent signal pin | 5V_SUPPLY = 0 V, Measured at 1 MHz, $V_{BIAS}$ = 2.5 V (1) | | | 0.07 | | pF |
| $C_{IN}$ | Level-shifting input capacitance, capacitance to GND | 5V_SUPPLY = 0 V, Measured at 100 KHz, VBIAS = 2.5 V (1) | DDC | | 3.5 | 4 | pF |
| | | | CEC | | 3.5 | 4 | |
| | | | HP | | 3.5 | 4 | |

(1) This parameter is specified by design.
(2) Standard IEC 61000-4-2, $C_{DISCHARGE}$= 150 pF, $R_{DISCHARGE}$ = 330 Ω, 5V_SUPPLY and LV_SUPPLY within recommended operating conditions, GND = 0 V, and ESD_BYP (pin 37) and HOTPLUG_DET_OUT (pin 20) each bypassed with a 0.1-µF ceramic capacitor connected to GND.
(3) HBM per MIL-STD-883, Method 3015, $C_{DISCHARGE}$ = 100 pF, $R_{DISCHARGE}$ = 1.5 kΩ, 5V_SUPPLY and LV_SUPPLY within recommended operating conditions, GND = 0 V, and ESD_BYP (pin 37) and HOTPLUG_DET_OUT (pin 20) each bypassed with a 0.1-µF ceramic capacitor connected to GND.
(4) These measurements performed with no external capacitor on ESD_BYP.
(5) Intrapair matching, each TMDS pair (i.e., D+, D–)

## TYPICAL PERFORMANCE

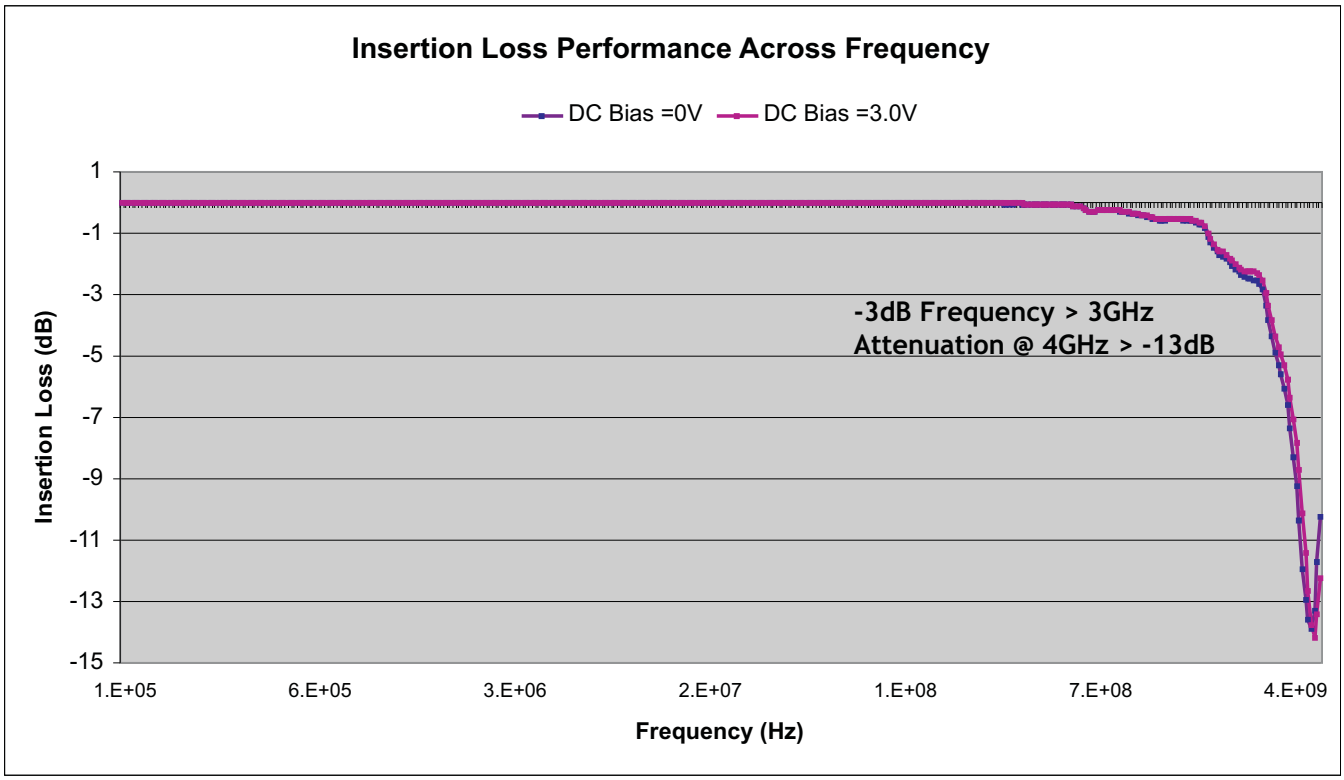



**Figure 3. Insertion Loss Performance Across Frequency**

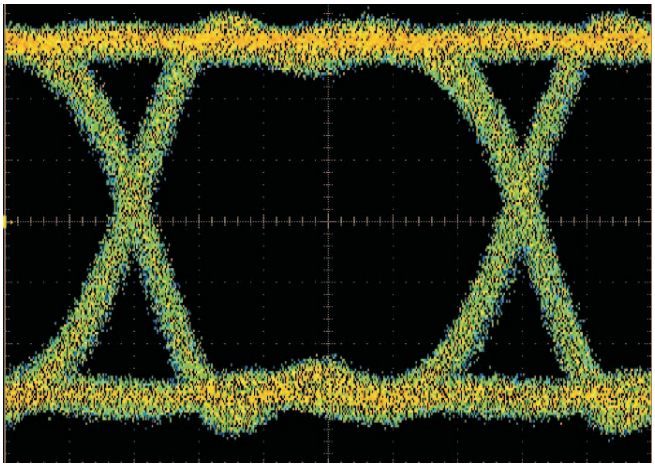


**Figure 4. Eye Diagram Without TPD12S520 in Test Socket (Across Differential Data Lines, Data Rate 1.6 Gbps)**

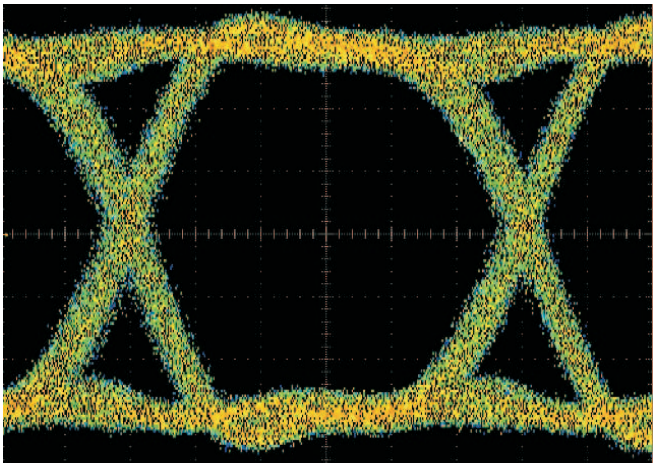


**Figure 5. Eye Diagram With TPD12S520 in Test Socket (Across Differential Data Lines, Data Rate 1.6 Gbps)**

## TYPICAL PERFORMANCE (continued)

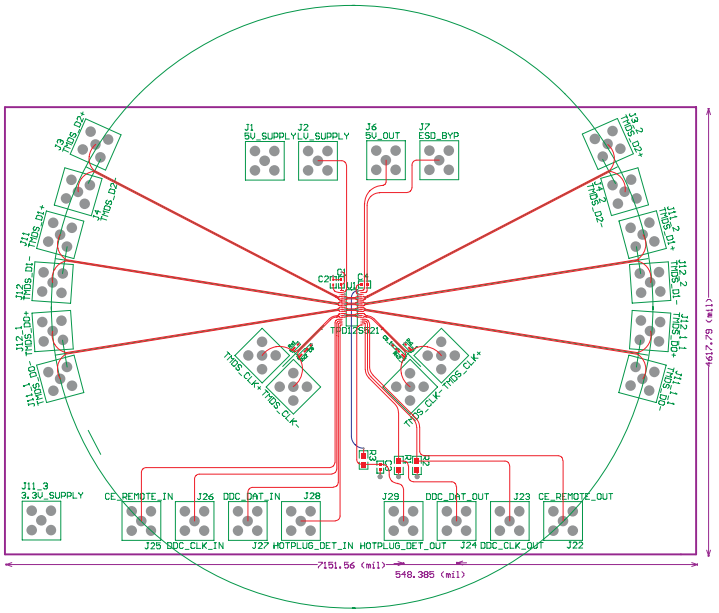



**Figure 6. Test Board to Measure Eye Diagram for TPD12S520 (See Eye Diagrams)**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPD12S520DBTR | ACTIVE | TSSOP | DBT | 38 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | PN520 | Samples |

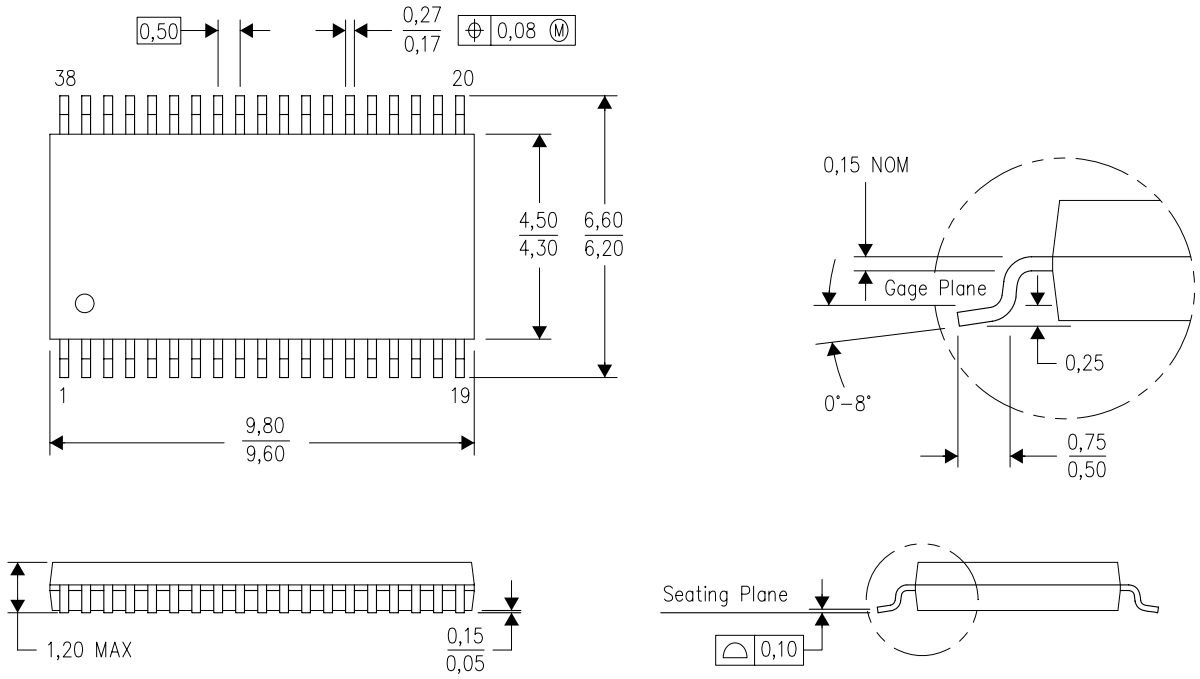
(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

DBT (R–PDSO–G38) PLASTIC SMALL OUTLINE




4073252-6/I 03/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–153.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

| **Products** | | **Applications** | |
|---|---|---|---|
| Audio | www.ti.com/audio | Automotive and Transportation | www.ti.com/automotive |
| Amplifiers | amplifier.ti.com | Communications and Telecom | www.ti.com/communications |
| Data Converters | dataconverter.ti.com | Computers and Peripherals | www.ti.com/computers |
| DLP® Products | www.dlp.com | Consumer Electronics | www.ti.com/consumer-apps |
| DSP | dsp.ti.com | Energy and Lighting | www.ti.com/energy |
| Clocks and Timers | www.ti.com/clocks | Industrial | www.ti.com/industrial |
| Interface | interface.ti.com | Medical | www.ti.com/medical |
| Logic | logic.ti.com | Security | www.ti.com/security |
| Power Mgmt | power.ti.com | Space, Avionics and Defense | www.ti.com/space-avionics-defense |
| Microcontrollers | microcontroller.ti.com | Video and Imaging | www.ti.com/video |
| RFID | www.ti-rfid.com | | |
| OMAP Applications Processors | www.ti.com/omap | **TI E2E Community** | e2e.ti.com |
| Wireless Connectivity | www.ti.com/wirelessconnectivity | | |

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265