8-CHANNEL CONSTANT-CURRENT LED SINK DRIVERS

Check for Samples: TLC5916, TLC5917

FEATURES

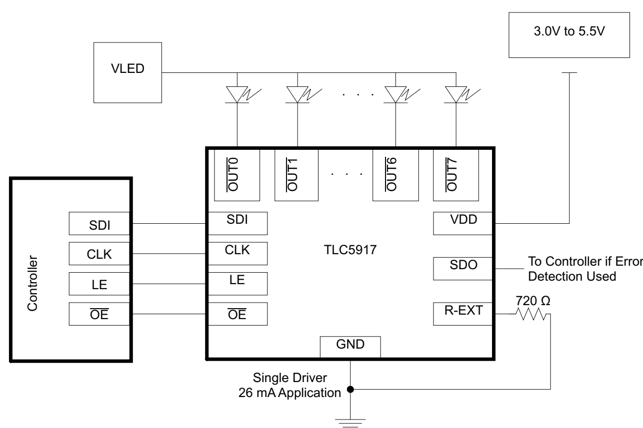
- **Eight Constant-Current Output Channels**
- **Output Current Adjusted Through Single External Resistor**
- **Constant Output Current Range: 3 mA to 120 mA per Channel**
- **Constant Output Current Invariant to Load Voltage Change**
- **Open Load, Short Load and Overtemperature Detection**
- **256-Step Programmable Global Current Gain**
- **Excellent Output Current Accuracy:**
  - **Between Channels: < ±3% (Max)**
  - **Between ICs: < ±6% (Max)**
- **Fast Response of Output Current**
- **30-MHz Clock Frequency**
- **Schmitt-Trigger Input**
- **3.3-V or 5-V Supply Voltage**
- **Maximum LED Voltage 20-V**
- **Thermal Shutdown for Overtemperature Protection**

APPLICATIONS

- **General LED Lighting Applications**
- **LED Display Systems**
- **LED Signage**
- **Automotive LED Lighting**
- **White Goods**
- **Gaming Machines/Entertainment**

ABSTRACT

The TLC5916 / TLC5917 Constant-Current LED Sink Drivers are designed to work alone or cascaded. Since each output is independently controlled, they can be programmed to be on or off by the user. The high LED voltage (VLED) allows for the use of a single LED per output or multiple LEDs on a single string. With independently controlled outputs supplied with constant current, the LEDs can be combined in parallel to create higher currents on a single string. The constant sink current for all channels is set through a single external resistor. This allows different LED drivers in the same application to sink various currents which provides optional implementation of multi-color LEDs. An additional advantage of the independent outputs is the ability to leave unused channels floating. The flexibility of the TLC5916 / TLC5917 LED drivers is ideal for applications such as (but not limited to): 7-segment displays, scrolling single color displays, gaming machines, white goods, video billboards and video panels.



Single Implementation of TLC5916/TLC5917 Device

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DESCRIPTION/ORDERING INFORMATION

The TLC5916/TLC5917 is designed for LED displays and LED lighting applications with constant-current control and open-load, shorted-load, and overtemperature detection. The TLC5916/TLC5917 contains an 8-bit shift register and data latches, which convert serial input data into parallel output format. At the output stage, eight regulated current ports are designed to provide uniform and constant current for driving LEDs within a wide range of LED Forward Voltage (VF) variations. Used in system design for LED display applications, e.g., LED panels, it provides great flexibility and device performance. Users can adjust the output current from 3 mA to 120 mA per channel through an external resistor, R_{ext}, which gives flexibility in controlling the light intensity of LEDs. The devices are designed for up to 20 V at the output port. The high clock frequency, 30 MHz, also satisfies the system requirements of high-volume data transmission.

The TLC5916/TLC5917 provides two operation modes: Normal Mode and Special Mode. Normal mode is used for shifting LED data into and out of the driver. Special Mode includes two functions: Error Detection and Current Gain Control. The two operation modes include three phases: Normal Mode phase, Mode Switching transition phase, and Special Mode phase. The signal on the multiple function pin $\overline{OE}$(ED2) is monitored to determine the mode. When a one-clock-wide pulse appears on $\overline{OE}$(ED2), the device enters the Mode Switching phase. At this time, the voltage level on LE(ED1) determines which mode the TLC5916/TLC5917 switches to.

In the Normal Mode phase, the serial data can be transferred into TLC5916/TLC5917 via the pin SDI, shifted in the shift register, and transferred out via the pin SDO. LE(ED1) can latch the serial data in the shift register to the output latch. $\overline{OE}$(ED2) enables the output drivers to sink current.

In the Special Mode phase, the low-voltage-level signal on $\overline{OE}$(ED2) can enable output channels and detect the status of the output current to determine if the driving current level is sufficient. The detected Error Status is loaded into the 8-bit shift register and shifted out via the pin SDO, synchronous to the CLK signal. The system controller can read the error status and determine if the LEDs are properly lit.

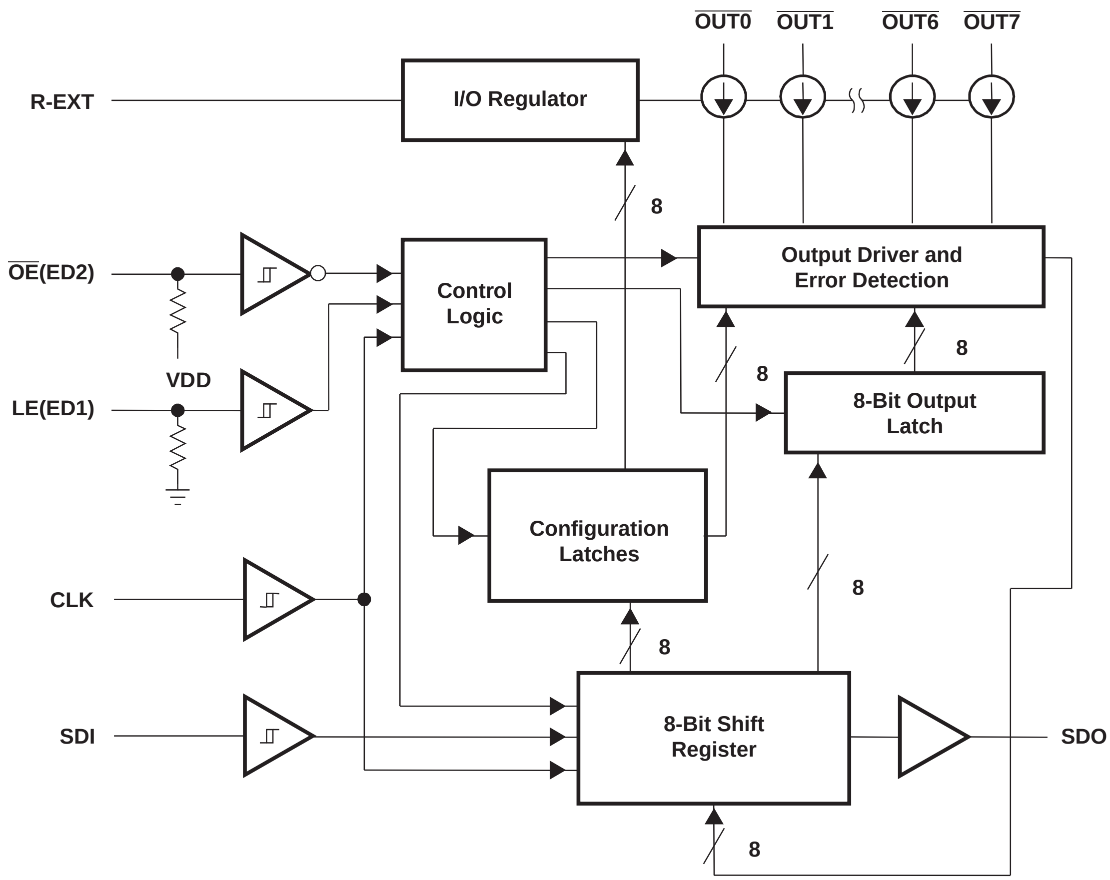
In the Special Mode phase, the TLC5916/TLC5917 allows users to adjust the output current level by setting a runtime-programmable Configuration Code. The code is sent into the TLC5916/TLC5917 via SDI. The positive pulse of LE(ED1) latches the code in the shift register into a built-in 8-bit configuration latch, instead of the output latch. The code affects the voltage at the terminal R-EXT and controls the output-current regulator. The output current can be finely adjusted by a gain ranging from 1/12 to 127/128 in 256 steps. Therefore, the current skew between ICs can be compensated within less than 1%. This feature is suitable for white balancing in LED color display panels.

Table 1. ORDERING INFORMATION(1)

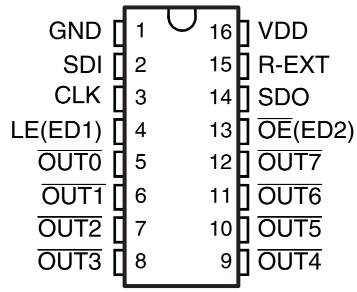
T_A	SHORT TO V_{LED} DETECTION	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	No	PDIP – N	Tube of 25	TLC5916IN	TLC5916IN
		SOIC – D	Tube of 40	TLC5916ID	TLC5916I
			Reel of 2500	TLC5916IDR	
		TSSOP – PW	Tube of 90	TLC5916IPW	Y5916
			Reel of 2000	TLC5916IPWR	
	Yes	PDIP – N	Tube of 25	TLC5917IN	TLC5917IN
		SOIC – D	Tube of 40	TLC5917ID	TLC5917I
			Reel of 2500	TLC5917IDR	
		TSSOP – PW	Tube of 90	TLC5917IPW	Y5917
			Reel of 2000	TLC5917IPWR	

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

BLOCK DIAGRAM



D, N, OR PW PACKAGE
(TOP VIEW)



Terminal Descriptions

TERMINAL NAME	DESCRIPTION
CLK	Clock input for data shift on rising edge
GND	Ground for control logic and current sink
LE(ED1)	Data strobe input Serial data is transferred to the respective latch when LE(ED1) is high. The data is latched when LE(ED1) goes low. Also, a control signal input for an Error Detection Mode and Current Adjust Mode (see Timing Diagram). LE(ED1) has an internal pulldown.
$\overline{\text{OE}}$(ED2)	Output enable. When $\overline{\text{OE}}$(ED2) is active (low), the output drivers are enabled; when $\overline{\text{OE}}$(ED2) is high, all output drivers are turned OFF (blanked). Also, a control signal input for an Error Detection Mode and Current Adjust Mode (see Figure 1). $\overline{\text{OE}}$(ED2) has an internal pullup.
$\overline{\text{OUT0}}$–$\overline{\text{OUT7}}$	Constant-current outputs
R-EXT	External Resistor - Connect an external resistor to ground to set the current for all outputs
SDI	Serial-data input to the Shift register
SDO	Serial-data output to the following SDI of next driver IC or to the microcontroller
VDD	Supply voltage

Table 2. Diagnostic Features

DEVICE(1)	OVERTEMPERATURE DETECTION	OPEN-LOAD DETECTION	SHORT TO GND DETECTION	SHORT TO V_{LED} DETECTION
TLC5916	X	X	X	
TLC5917	X	X	X	X

(1) The device has one single error register for all these conditions (one error bit per channel).

Timing Diagram

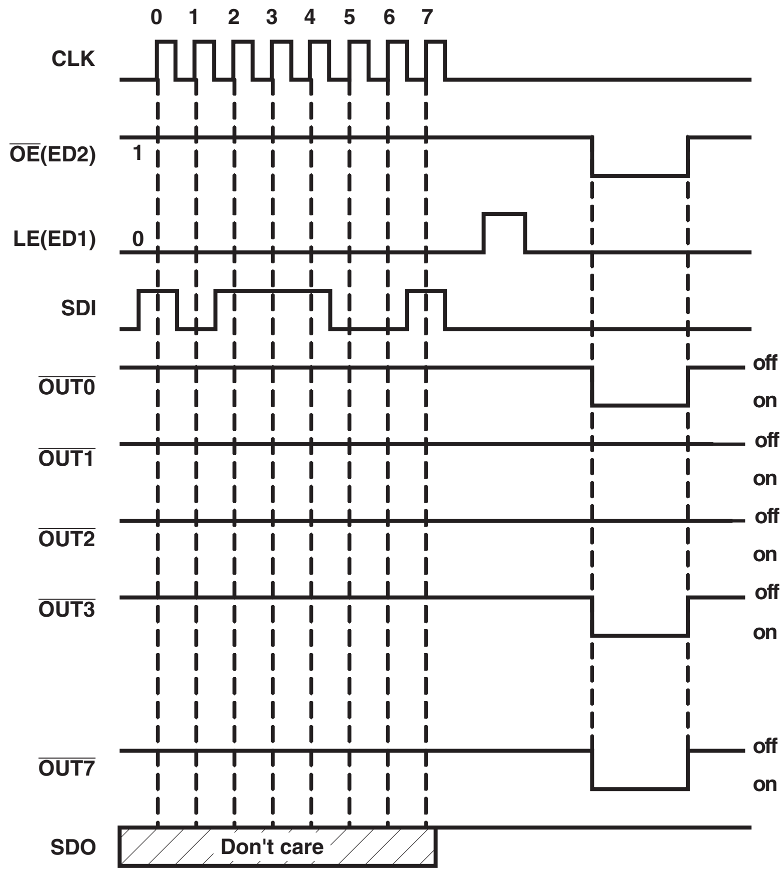


Figure 1. Normal Mode

Table 3. Truth Table in Normal Mode

CLK	LE(ED1)	$\overline{OE}$(ED2)	SDI	$\overline{OUT0}$...$\overline{OUT7}$	SDO
↑	H	L	Dn	Dn...Dn – 7	Dn – 7
↑	L	L	Dn + 1	No change	Dn – 6
↑	H	L	Dn + 2	Dn + 2...Dn – 5	Dn – 5
↓	X	L	Dn + 3	Dn + 2...Dn – 5	Dn – 5
↓	X	H	Dn + 3	Off	Dn – 5

The signal sequence shown in Figure 2 makes the TLC5916/TLC5917 enter Current Adjust and Error Detection Mode.

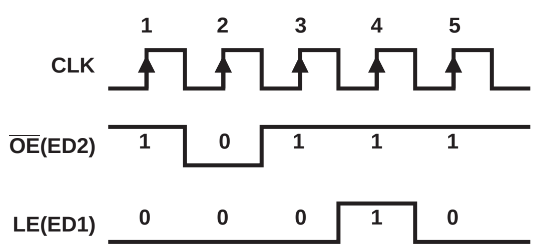


Figure 2. Switching to Special Mode

In the Current Adjust Mode, sending the positive pulse of LE(ED1), the content of the shift register (a current adjust code) is written to the 8-bit configuration latch (see Figure 3).

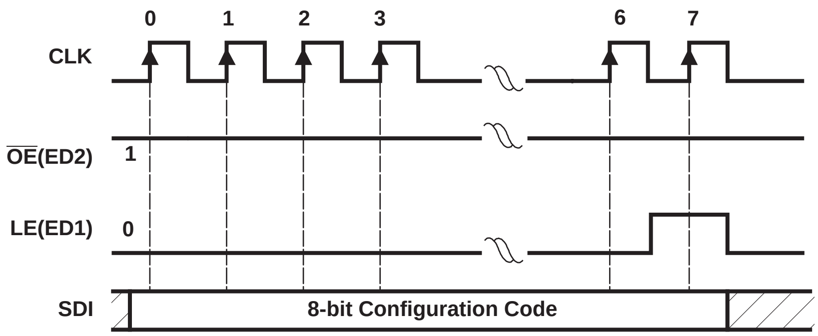


Figure 3. Writing Configuration Code

When the TLC5916/TLC5917 is in the Error Detection Mode, the signal sequence shown in Figure 4 enables a system controller to read error status codes through SDO.

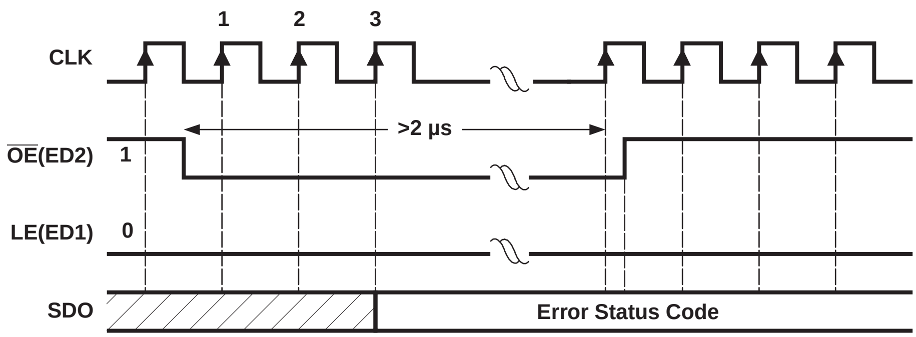


Figure 4. Reading Error Status Code

The signal sequence shown in Figure 5 makes TLC5916/TLC5917 resume the Normal Mode. Switching to Normal Mode resets all internal Error Status registers. OE(ED2) always enables the output port, whether the TLC5916/TLC5917 enters Current Adjust Mode or not.

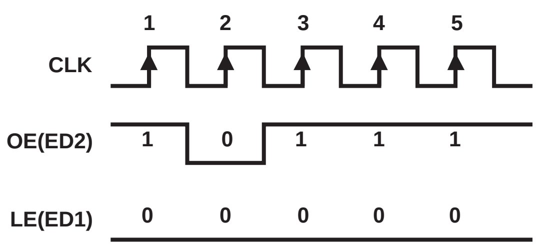


Figure 5. Switching to Normal Mode

Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{DD}	Supply voltage range		0	7	V
V_I	Input voltage range		–0.4	V_{DD} + 0.4	V
V_O	Output voltage range		–0.5	20	V
f_{clk}	Clock frequency			25	MHz
I_{OUT}	Output current			120	mA
I_{GND}	GND terminal current			960	mA
T_A	Operating free-air temperature range		–40	125	°C
T_J	Operating junction temperature range		–40	150	°C
T_{stg}	Storage temperature range		–55	150	°C
ESD	Electrostatic discharge capability, $V_{(HBMESD)}$	100 pF, 1.5 kΩ		1.5	kV

THERMAL INFORMATION

THERMAL METRIC[(1)]		TLC5916			TLC5917			UNITS
		16 PINS			16 PINS			
		D	N	PW	D	N	PW	
θ_{JA}	Junction-to-ambient thermal resistance	87.4	51.8	113.9	87.4	51.8	114.8	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	48.1	39.1	35.2	48.1	39.1	35.9	
θ_{JB}	Junction-to-board thermal resistance	44.4	31.8	59.2	44.4	31.8	59.8	
ψ_{JT}	Junction-to-top characterization parameter	12.5	23.9	1.3	12.5	23.9	1.3	
ψ_{JB}	Junction-to-board characterization parameter	44.2	31.7	58.5	44.2	31.7	59.2	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	n/a	n/a	n.a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

Recommended Operating Conditions

		CONDITIONS		MIN	MAX	UNIT
V_{DD}	Supply voltage			3	5.5	V
V_O	Supply voltage to output pins	$\overline{OUT0}$–$\overline{OUT7}$			20	V
I_O	Output current	DC test circuit	$V_O \geq 0.6$ V	3		mA
			$V_O \geq 1$ V		120	
I_{OH}	High-level output current source	SDO shorted to GND		–1		mA
I_{OL}	Low-level output current sink	SDO shorted to V_{CC}		1		mA
V_{IH}	High-level input voltage	CLK, $\overline{OE}$(ED2), LE(ED1), and SDI		$0.7 \times V_{DD}$	V_{DD}	V
V_{IL}	Low-level input voltage	CLK, $\overline{OE}$(ED2), LE(ED1), and SDI		0	$0.3 \times V_{DD}$	V

Recommended Timing

V_{DD} = 3 V to 5.5 V (unless otherwise noted)

		CONDITIONS	MIN	MAX	UNIT
$t_{w(L)}$	LE(ED1) pulse duration	Normal Mode	20		ns
$t_{w(CLK)}$	CLK pulse duration	Normal Mode	20		ns
$t_{w(OE)}$	$\overline{OE}$(ED2) pulse duration	Normal Mode, I_{OUT} < 60 mA	500		ns
		Normal Mode, I_{OUT} > 60 mA	700		
$t_{su(D)}$	Setup time for SDI	Normal Mode	3		ns
$t_{h(D)}$	Hold time for SDI	Normal Mode	2		ns
$t_{su(L)}$	Setup time for LE(ED1)	Normal Mode	15		ns
$t_{h(L)}$	Hold time for LE(ED1)	Normal Mode	15		ns
$t_{w(CLK)}$	CLK pulse duration	Error Detection Mode	20		ns
$t_{w(ED2)}$	$\overline{OE}$(ED2) pulse duration	Error Detection Mode	2000		ns
$t_{su(ED1)}$	Setup time for LE(ED1)	Error Detection Mode	4		ns
$t_{h(ED1)}$	Hold time for LE(ED1)	Error Detection Mode	10		ns
$t_{su(ED2)}$	Setup time for $\overline{OE}$(ED2)	Error Detection Mode	6		ns
$t_{h(ED2)}$	Hold time for $\overline{OE}$(ED2)	Error Detection Mode	10		ns
f_{CLK}	Clock frequency	Cascade operation		30	MHz

Electrical Characteristics

V_{DD} = 3 V, T_J = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{DD}	Input voltage			3		5.5	V
V_O	Supply voltage to the output pins					20	V
I_O	Output current	V_O ≥ 0.6 V		3			mA
		V_O ≥ 1 V				120	
I_{OH}	High-level output current, source			–1			mA
I_{OL}	Low-level output current, sink			1			mA
V_{IH}	High-level input voltage			0.7 × V_{DD}		V_{DD}	V
V_{IL}	Low-level input voltage			GND		0.3 × V_{DD}	V
I_{leak}	Output leakage current	V_{OH} = 17 V	T_J = 25°C			0.5	µA
			T_J = 125°C			2	
V_{OH}	High-level output voltage	SDO, I_{OL} = –1 mA		V_{DD} – 0.4			V
V_{OL}	Low-level output voltage	SDO, I_{OH} = 1 mA				0.4	V
$I_{O(1)}$	Output current 1	V_{OUT} = 0.6 V, R_{ext} = 720 Ω, CG = 0.992			26		mA
	Output current error, die-die	I_{OL} = 26 mA, V_O = 0.6 V, R_{ext} = 720 Ω, T_J = 25°C			±3	±6	%
	Output current skew, channel-to-channel	I_{OL} = 26 mA, V_O = 0.6 V, R_{ext} = 720 Ω, T_J = 25°C			±1.5	±3	%
$I_{O(2)}$	Output current 2	V_O = 0.8 V, R_{ext} = 360 Ω, CG = 0.992			52		mA
	Output current error, die-die	I_{OL} = 52 mA, V_O = 0.8 V, R_{ext} = 360 Ω, T_J = 25°C			±2	±6	%
	Output current skew, channel-to-channel	I_{OL} = 52 mA, V_O = 0.8 V, R_{ext} = 360 Ω, T_J = 25°C			±1.5	±3	%
I_{OUT} vs V_{OUT}	Output current vs output voltage regulation	V_O = 1 V to 3 V, I_O = 26 mA			±0.1		%/V
		V_{DD} = 3.0 V to 5.5 V, I_O = 26 mA/120 mA			±1		
	Pullup resistance	$\overline{OE}$(ED2)			500		kΩ
	Pulldown resistance	LE(ED1)			500		kΩ
T_{sd}	Overtemperature shutdown(2)			150	175	200	°C
T_{hys}	Restart temperature hysteresis(2)				15		°C
$I_{OUT,Th}$	Threshold current for open error detection	$I_{OUT,target}$ = 3 mA to 120 mA			0.5 × I_{target}		%
$V_{OUT,TTh}$	Trigger threshold voltage for short-error detection (TLC5917 only)	$I_{OUT,target}$ = 3 mA to 120 mA		2.5	2.7	3.1	V
$V_{OUT,RTh}$	Return threshold voltage for short-error detection (TLC5917 only)	$I_{OUT,target}$ = 3 mA to 120 mA		2.2			V
I_{DD}	Supply current	R_{ext} = Open			5	10	mA
		R_{ext} = 720 Ω			8	14	
		R_{ext} = 360 Ω			11	18	
		R_{ext} = 180 Ω			16	22	

(1) Typical values represent the likely parametric nominal values determined at the time of characterization. Typical values depend on the application and configuration and may vary over time. Typical values are not ensured on production material.
(2) Specified by design.

Electrical Characteristics

V_{DD} = 5.5 V, T_J = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{DD}	Input voltage			3		5.5	V
V_O	Supply voltage to the output pins					20	V
I_O	Output current	$V_O \geq 0.6$ V		3			mA
		$V_O \geq 1$ V				120	
I_{OH}	High-level output current, source			–1			mA
I_{OL}	Low-level output current, sink			1			mA
V_{IH}	High-level input voltage			$0.7 \times V_{DD}$		V_{DD}	V
V_{IL}	Low-level input voltage			GND		$0.3 \times V_{DD}$	V
I_{leak}	Output leakage current	V_{OH} = 17 V	T_J = 25°C			0.5	µA
			T_J = 125°C			2	
V_{OH}	High-level output voltage	SDO, I_{OL} = –1 mA		V_{DD} – 0.4			V
V_{OL}	Low-level output voltage	SDO, I_{OH} = 1 mA				0.4	V
$I_{O(1)}$	Output current 1	V_{OUT} = 0.6 V, R_{ext} = 720 Ω, CG = 0.992			26		mA
	Output current error, die-die	I_{OL} = 26 mA, V_O = 0.6 V, R_{ext} = 720 Ω, T_J = 25°C			±3	±6	%
	Output current skew, channel-to-channel	I_{OL} = 26 mA, V_O = 0.6 V, R_{ext} = 720 Ω, T_J = 25°C			±1.5	±3	%
$I_{O(2)}$	Output current 2	V_O = 0.8 V, R_{ext} = 360 Ω, CG = 0.992			52		mA
	Output current error, die-die	I_{OL} = 52 mA, V_O = 0.8 V, R_{ext} = 360 Ω, T_J = 25°C			±2	±6	%
	Output current skew, channel-to-channel	I_{OL} = 52 mA, V_O = 0.8 V, R_{ext} = 360 Ω, T_J = 25°C			±1.5	±3	%
I_{OUT} vs V_{OUT}	Output current vs output voltage regulation	V_O = 1 V to 3 V , I_O = 26 mA			±0.1		%/V
		V_{DD} = 3.0 V to 5.5 V, I_O = 26 mA/120 mA			±1		
	Pullup resistance	$\overline{OE}$(ED2),			500		kΩ
	Pulldown resistance	LE(ED1),			500		kΩ
T_{sd}	Overtemperature shutdown(2)			150	175	200	°C
T_{hys}	Restart temperature hysteresis(2)				15		°C
$I_{OUT,Th}$	Threshold current for open error detection	$I_{OUT,target}$ = 3 mA to 120 mA			$0.5 \times I_{target}$		%
$V_{OUT,TTh}$	Trigger threshold voltage for short-error detection (TLC5917 only)	$I_{OUT,target}$ = 3 mA to 120 mA		2.5	2.7	3.1	V
$V_{OUT,RTh}$	Return threshold voltage for short-error detection (TLC5917 only)	$I_{OUT,target}$ = 3 mA to 120 mA		2.2			V
I_{DD}	Supply current	R_{ext} = Open			6	10	mA
		R_{ext} = 720 Ω			11	14	
		R_{ext} = 360 Ω			13	18	
		R_{ext} = 180 Ω			19	24	

(1) Typical values represent the likely parametric nominal values determined at the time of characterization. Typical values depend on the application and configuration and may vary over time. Typical values are not ensured on production material.
(2) Specified by design.

Switching Characteristics

V_{DD} = 3 V, T_J = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PLH1}	Low-to-high propagation delay time, CLK to $\overline{OUTn}$	V_{IH} = V_{DD}, V_{IL} = GND, R_{ext} = 360 Ω, V_L = 4 V, R_L = 44 Ω, C_L = 10 pF, CG = 0.992	40	65	95	ns
t_{PLH2}	Low-to-high propagation delay time, LE(ED1) to $\overline{OUTn}$		40	65	95	ns
t_{PLH3}	Low-to-high propagation delay time, $\overline{OE}$(ED2) to $\overline{OUTn}$		40	65	95	ns
t_{PLH4}	Low-to-high propagation delay time, CLK to SDO		12	20	30	ns
t_{PHL1}	High-to-low propagation delay time, CLK to $\overline{OUTn}$			300	365	ns
t_{PHL2}	High-to-low propagation delay time, LE(ED1) to $\overline{OUTn}$			300	365	ns
t_{PHL3}	High-to-low propagation delay time, $\overline{OE}$(ED2) to $\overline{OUTn}$			300	365	ns
t_{PHL4}	High-to-low propagation delay time, CLK to SDO		12	20	30	ns
$t_{w(CLK)}$	Pulse duration, CLK		20			ns
$t_{w(L)}$	Pulse duration, LE(ED1)		20			ns
$t_{w(OE)}$	Pulse duration, $\overline{OE}$(ED2)		500			ns
$t_{w(ED2)}$	Pulse duration, $\overline{OE}$(ED2) in Error Detection Mode		2			μs
$t_{h(ED1,ED2)}$	Hold time, LE(ED1) and $\overline{OE}$(ED2)		10			ns
$t_{h(D)}$	Hold time, SDI		2			ns
$t_{su(D,ED1)}$	Setup time, SDI, LE(ED1)		3			ns
$t_{su(ED2)}$	Setup time, $\overline{OE}$(ED2)		8.5			ns
$t_{h(L)}$	Hold time, LE(ED1), Normal Mode		15			ns
$t_{su(L)}$	Setup time, LE(ED1), Normal Mode		15			ns
t_r	Rise time, CLK(2)				500	ns
t_f	Fall time, CLK(2)				500	ns
t_{or}	Rise time, outputs (off)		40	85	105	ns
t_{or}	Rise time, outputs (off), T_J = 25°C			83	100	ns
t_{of}	Rise time, outputs (on)		100	280	370	ns
t_{of}	Rise time, outputs (on), T_J = 25°C			170	225	ns
f_{CLK}	Clock frequency	Cascade operation			30	MHz

(1) Typical values represent the likely parametric nominal values determined at the time of characterization. Typical values depend on the application and configuration and may vary over time. Typical values are not ensured on production material.
(2) If the devices are connected in cascade and t_r or t_f is large, it may be critical to achieve the timing required for data transfer between two cascaded devices.

Switching Characteristics

V_{DD} = 5.5 V, T_J = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PLH1}	Low-to-high propagation delay time, CLK to $\overline{\text{OUTn}}$	$V_{IH} = V_{DD}$, V_{IL} = GND, R_{ext} = 360 Ω, V_L = 4 V, R_L = 44 Ω, C_L = 10 pF, CG = 0.992	40	65	95	ns
t_{PLH2}	Low-to-high propagation delay time, LE(ED1) to $\overline{\text{OUTn}}$		40	65	95	ns
t_{PLH3}	Low-to-high propagation delay time, $\overline{\text{OE}}$(ED2) to $\overline{\text{OUTn}}$		40	65	95	ns
t_{PLH4}	Low-to-high propagation delay time, CLK to SDO		8	20	30	ns
t_{PHL1}	High-to-low propagation delay time, CLK to $\overline{\text{OUTn}}$			300	365	ns
t_{PHL2}	High-to-low propagation delay time, LE(ED1) to $\overline{\text{OUTn}}$			300	365	ns
t_{PHL3}	High-to-low propagation delay time, $\overline{\text{OE}}$(ED2) to $\overline{\text{OUTn}}$			300	365	ns
t_{PHL4}	High-to-low propagation delay time, CLK to SDO		8	20	30	ns
$t_{w(CLK)}$	Pulse duration, CLK		20			ns
$t_{w(L)}$	Pulse duration, LE(ED1)		20			ns
$t_{w(OE)}$	Pulse duration, $\overline{\text{OE}}$(ED2)		500			ns
$t_{w(ED2)}$	Pulse duration, $\overline{\text{OE}}$(ED2) in Error Detection Mode		2			μs
$t_{h(D,ED1,ED2)}$	Hold time, SDI, LE(ED1), and $\overline{\text{OE}}$(ED2)		10			ns
$t_{h(D)}$	Hold time, SDI		2			ns
$t_{su(D,ED1)}$	Setup time, SDI, LE(ED1)		3			ns
$t_{su(ED2)}$	Setup time, $\overline{\text{OE}}$(ED2)		8.5			ns
$t_{h(L)}$	Hold time, LE(ED1), Normal Mode		15			ns
$t_{su(L)}$	Setup time, LE(ED1), Normal Mode		15			ns
t_r	Rise time, CLK(2)				500	ns
t_f	Fall time, CLK(2)				500	ns
t_{or}	Rise time, outputs (off)		40	85	105	ns
t_{or}	Rise time, outputs (off), T_J = 25°C			83	100	ns
t_{of}	Rise time, outputs (on)		100	280	370	ns
t_{of}	Rise time, outputs (on), T_J = 25°C			170	225	ns
f_{CLK}	Clock frequency	Cascade operation			30	MHz

(1) Typical values represent the likely parametric nominal values determined at the time of characterization. Typical values depend on the application and configuration and may vary over time. Typical values are not ensured on production material.
(2) If the devices are connected in cascade and t_r or t_f is large, it may be critical to achieve the timing required for data transfer between two cascaded devices.

PARAMETER MEASUREMENT INFORMATION

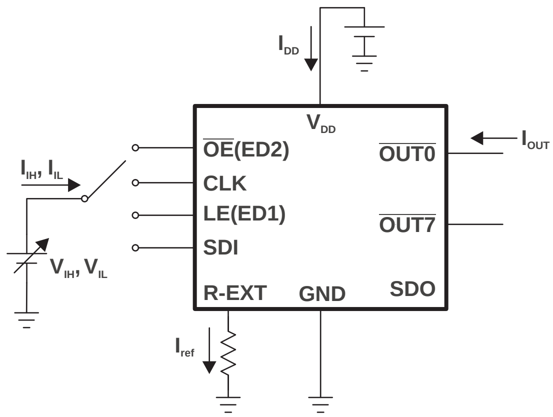


Figure 6. Test Circuit for Electrical Characteristics

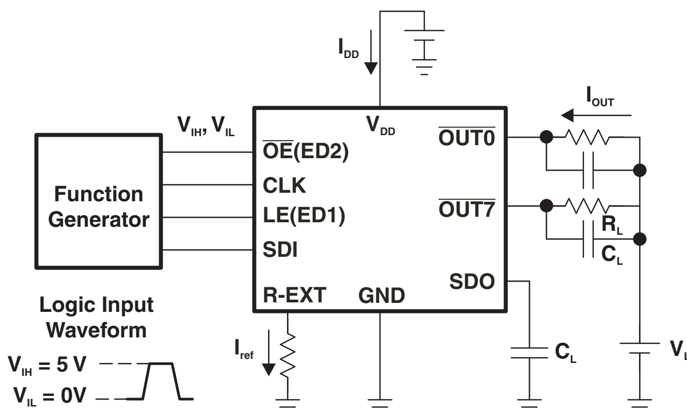


Figure 7. Test Circuit for Switching Characteristics

PARAMETER MEASUREMENT INFORMATION (continued)

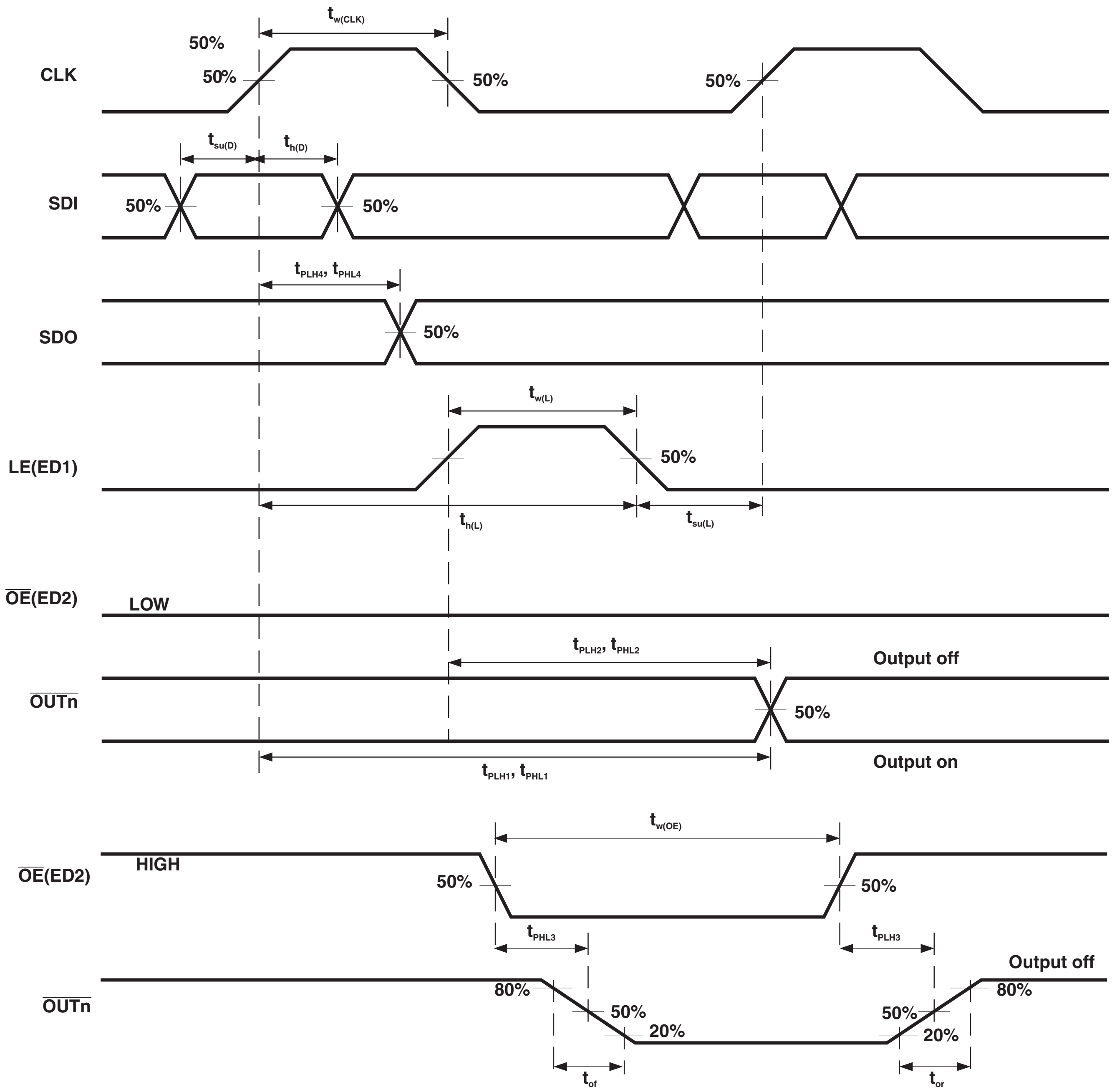


Figure 8. Normal Mode Timing Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

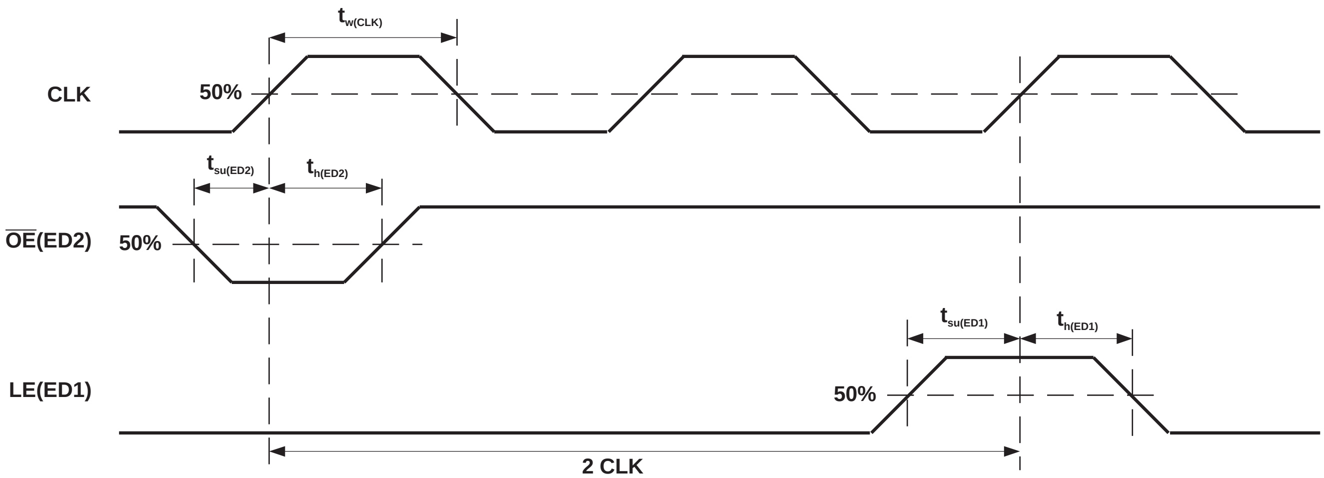


Figure 9. Switching to Special Mode Timing Waveforms

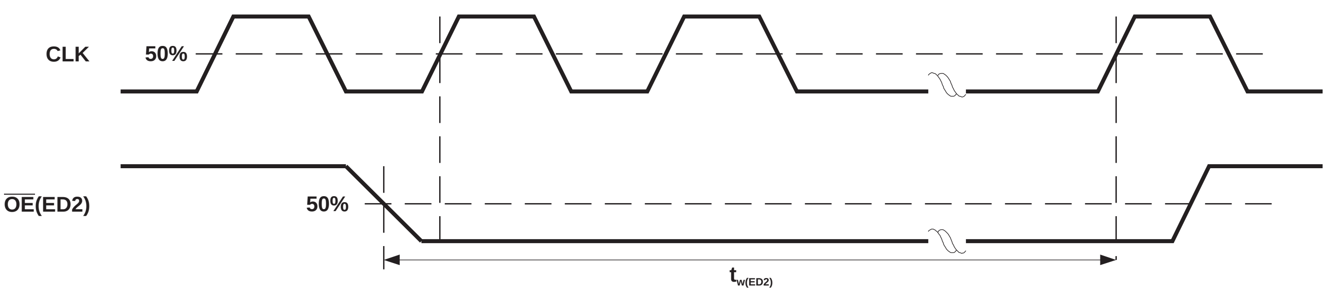


Figure 10. Reading Error Status Code Timing Waveforms

TYPICAL CHARACTERISTICS

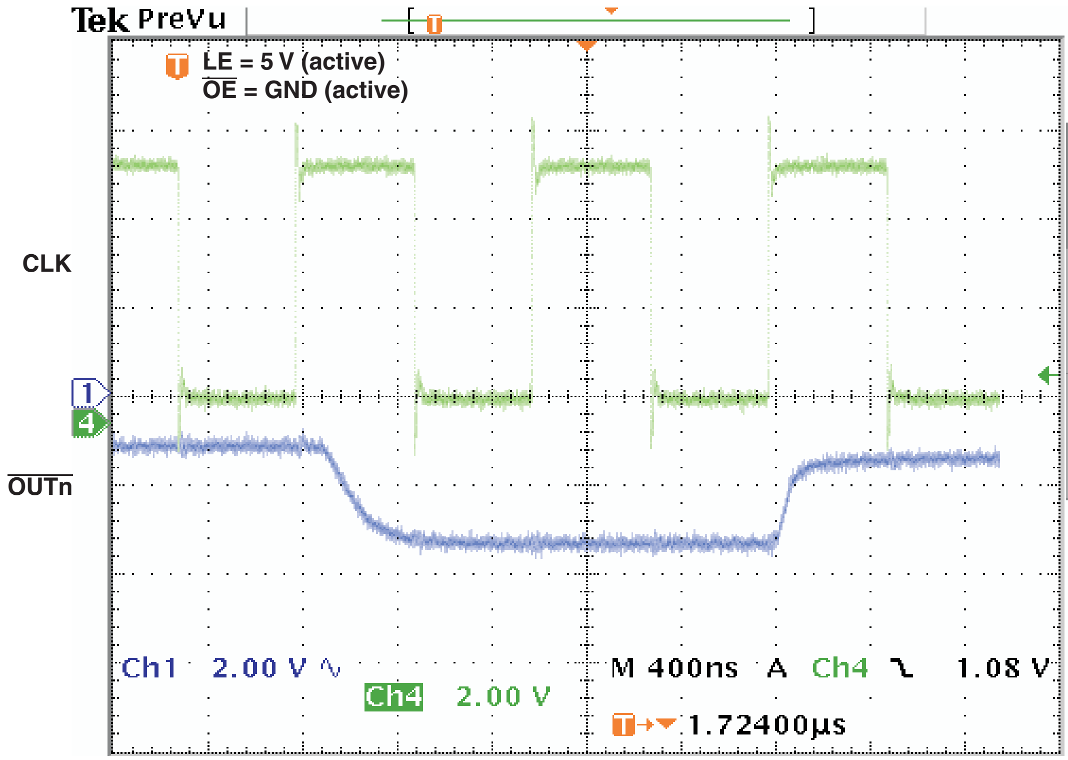


Figure 11. Response Time, CLK to OUTn

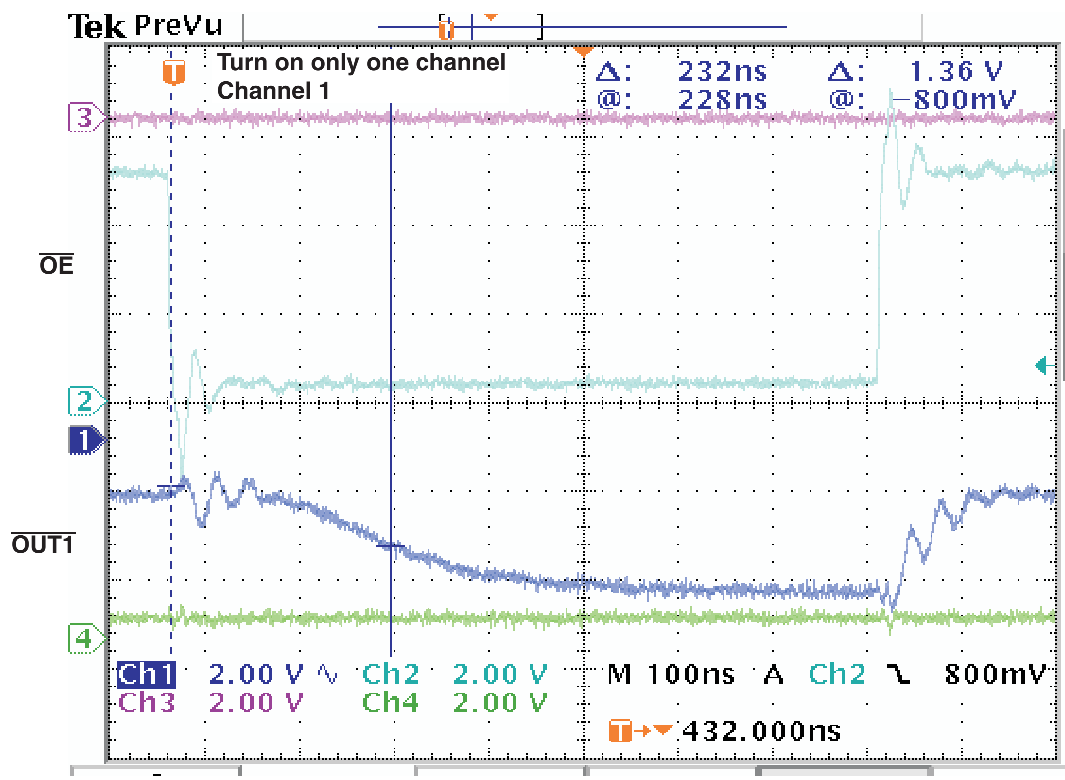


Figure 12. Response Time, OE to OUT1

TYPICAL CHARACTERISTICS (continued)

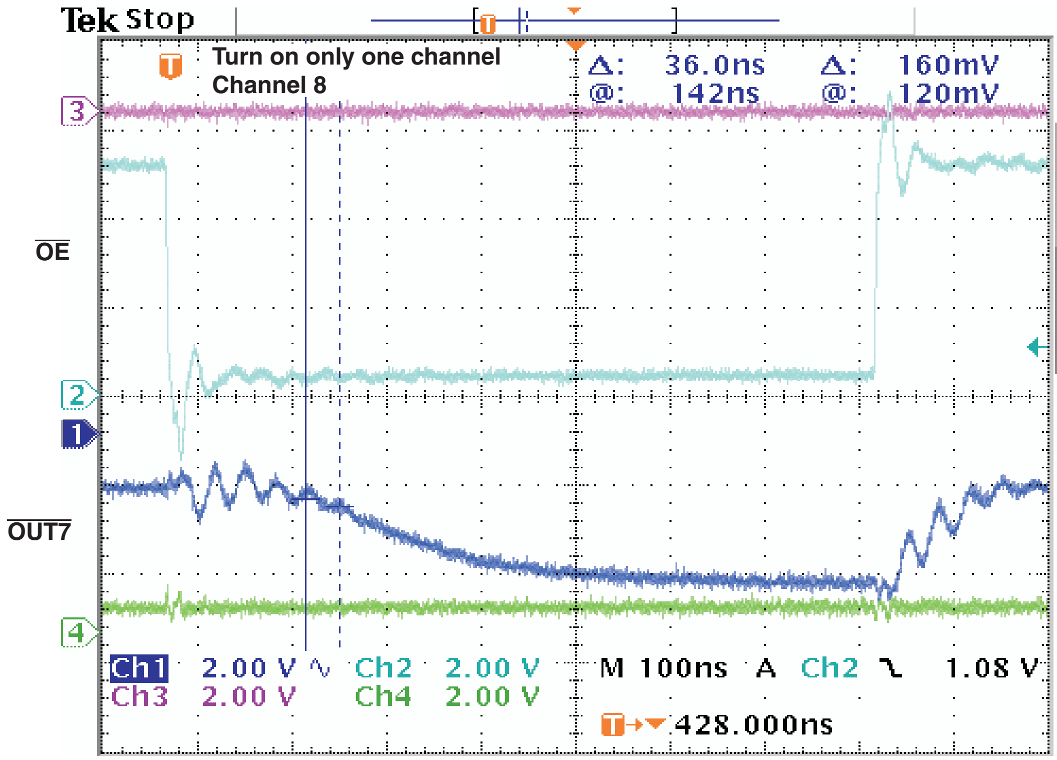


Figure 13. Response Time, $\overline{OE}$ to $\overline{OUT7}$

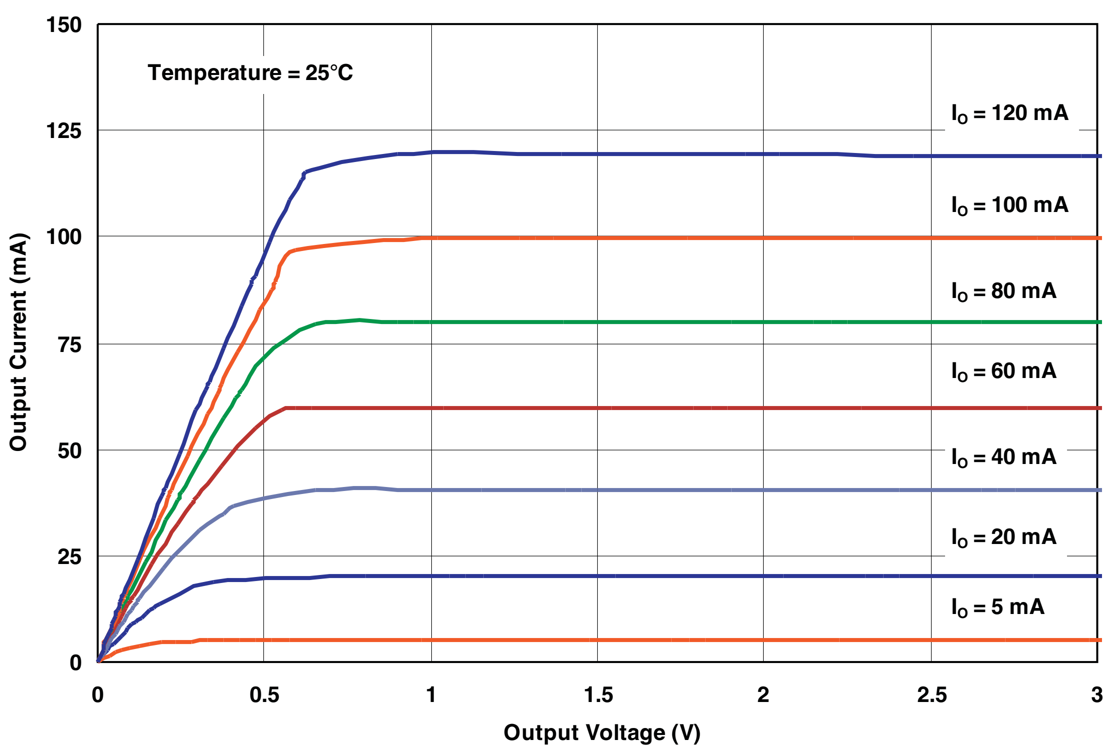


Figure 14. Output Current vs Output Voltage

APPLICATION INFORMATION

Operating Principles

Constant Current

In LED display applications, TLC5916/TLC5917 provides nearly no current variations from channel to channel and from IC to IC. While 5 mA ≤ I_{OUT} ≤ 100 mA, the maximum current skew between channels is less than ±3% and between ICs is less than ±6%.

Adjusting Output Current

TLC5916/TLC5917 scales up the reference current, I_{ref}, set by the external resistor R_{ext} to sink a current, I_{out}, at each output port. Users can follow the below formulas to calculate the target output current $I_{OUT,target}$ in the saturation region. In the equations,

R_{ext} is the resistance of the external resistor connected between the R-EXT terminal and ground and $V_{R\text{-}EXT}$ is the voltage of R-EXT, which is controlled by the programmable voltage gain (VG). VG is defined by the Configuration Code.

$V_{R\text{-}EXT} = 1.26\ V \times VG$

$I_{ref} = V_{R\text{-}EXT}/R_{ext}$,

$I_{OUT,target} = I_{ref} \times 15 \times 3^{CM-1}$

The Current Multiplier (CM) determines that the ratio $I_{OUT,target}/I_{ref}$ is 15 or 5. After power on, the default value of VG is 127/128 = 0.992, and the default value of CM is 1, so that the ratio $I_{OUT,target}/I_{ref}$ = 15. Based on the default VG and CM:

$V_{R\text{-}EXT} = 1.26\ V \times 127/128 = 1.25\ V$

$I_{OUT,target} = (1.25\ V/R_{ext}) \times 15$

Therefore, the default current is approximately 52 mA at 360 Ω and 26 mA at 720 Ω. The default relationship after power on between $I_{OUT,target}$ and R_{ext} is shown in Figure 15.

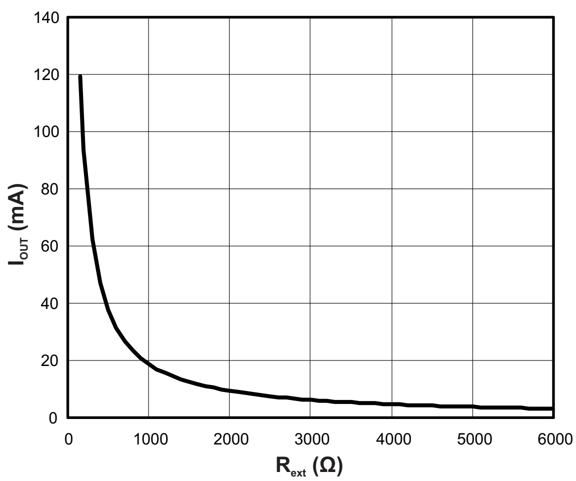


Figure 15. Default Relationship Curve Between $I_{OUT,target}$ and R_{ext} After Power Up

Typical Applications

Figure 16 shows implementation of a single TLC5916/TLC5917 device. Figure 17 shows a cascaded driver implementation.

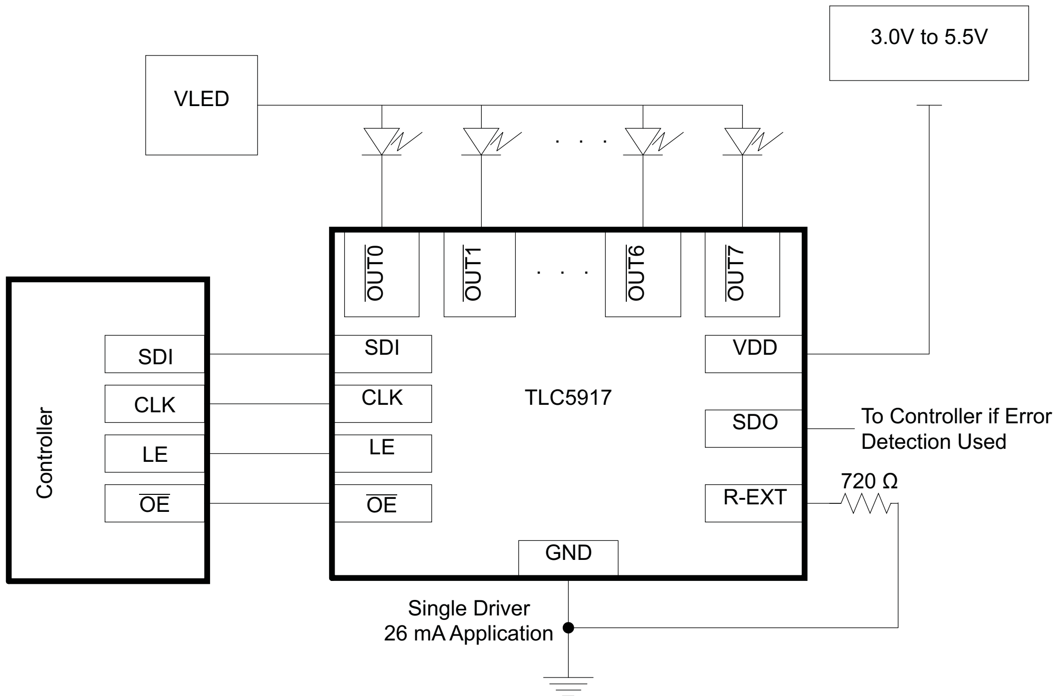


Figure 16. Single Implementation of TLC5916/TLC5917 Device

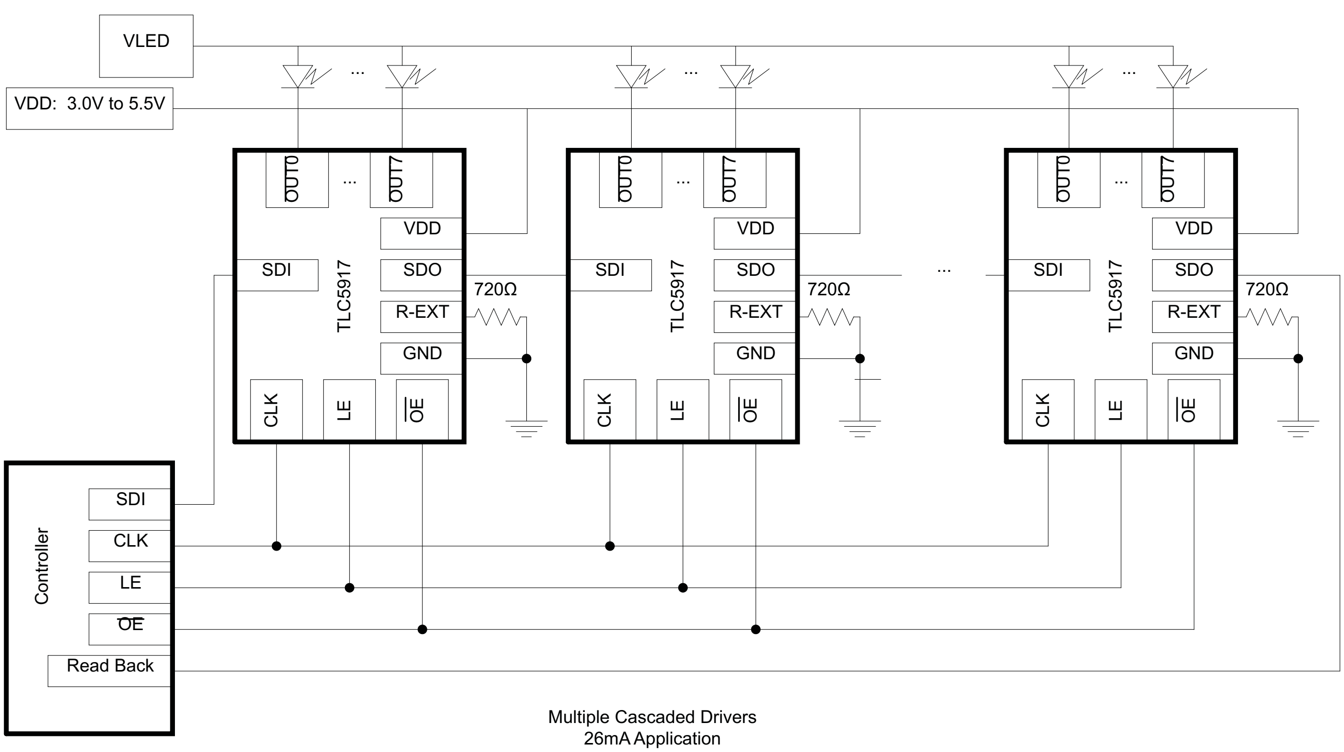


Figure 17. Cascading Implementation of TLC5916/TLC5917 Device

Operation Phases

Operation Mode Switching

To switch between its two modes, TLC5916/TLC5917 monitors the signal $\overline{OE}$(ED2). When an one-clock-wide pulse of $\overline{OE}$(ED2) appears, TLC5916/TLC5917 enters the two-clock-period transition phase, the Mode Switching phase. After power on, the default operation mode is the Normal Mode (see Figure 18).

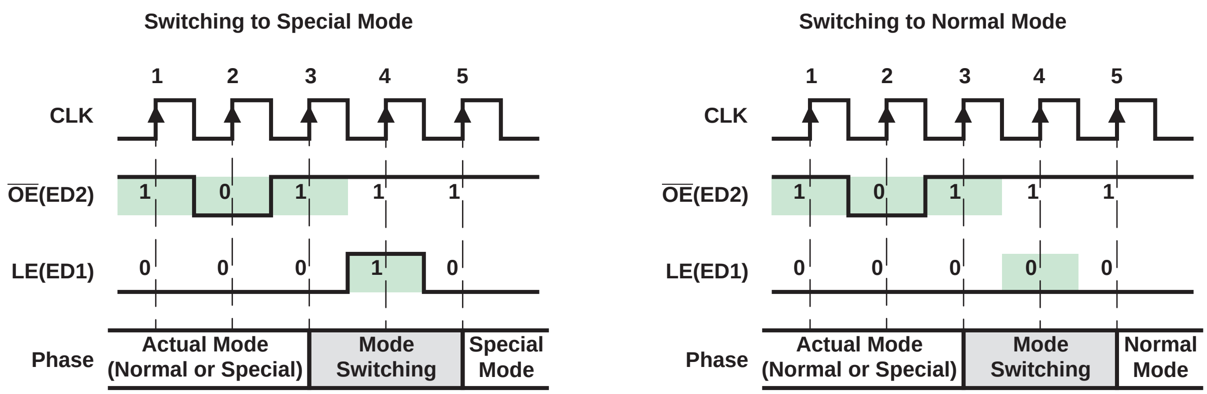


Figure 18. Mode Switching

As shown in Figure 18, once a one-clock-wide short pulse (101) of $\overline{OE}$(ED2) appears, TLC5916/TLC5917 enters the Mode Switching phase. At the fourth rising edge of CLK, if LE(ED1) is sampled as voltage high, TLC5916/TLC5917 switches to Special Mode; otherwise, it switches to Normal Mode. The signal LE(ED1) between the third and the fifth rising edges of CLK cannot latch any data. Its level is used only to determine into which mode to switch. However, the short pulse of $\overline{OE}$(ED2) can still enable the output ports. During mode switching, the serial data can still be transferred through SDI and shifted out from SDO.

NOTES:

1. The signal sequence for the mode switching may be used frequently to ensure that TLC5916/TLC5917 is in the proper mode.
2. The 1 and 0 on the LE(ED1) signal are sampled at the rising edge of CLK. The X means its level does not affect the result of mode switching mechanism.
3. After power on, the default operation mode is Normal Mode.

Normal Mode Phase

Serial data is transferred into TLC5916/TLC5917 via SDI, shifted in the Shift Register, and output via SDO. LE(ED1) can latch the serial data in the Shift Register to the Output Latch. $\overline{OE}$(ED2) enables the output drivers to sink current. These functions differ only as described in Operation Mode Switching, in which case, a short pulse triggers TLC5916/TLC5917 to switch the operation mode. However, as long as LE(ED1) is high in the Mode Switching phase, TLC5916/TLC5917 remains in the Normal Mode, as if no mode switching occurred.

Special Mode Phase

In the Special Mode, as long as $\overline{OE}$(ED2) is not low, the serial data is shifted to the Shift Register via SDI and shifted out via SDO, as in the Normal Mode. However, there are two differences between the Special Mode and the Normal Mode, as shown in the following sections.

Reading Error Status Code in Special Mode

When $\overline{OE}$(ED2) is pulled low while in Special Mode, error detection and load error status codes are loaded into the Shift Register, in addition to enabling output ports to sink current. Figure 19 shows the timing sequence for error detection. The 0 and 1 signal levels are sampled at the rising edge of each CLK. At least three zeros must be sampled at the voltage low signal $\overline{OE}$(ED2). Immediately after the second zero is sampled, the data input source of the Shift Register changes to the 8-bit parallel Error Status Code register, instead of from the serial data on SDI. Normally, the error status codes are generated at least 2 µs after the falling edge of $\overline{OE}$(ED2). The occurrence of the third or later zero saves the detected error status codes into the Shift Register. Therefore, when $\overline{OE}$(ED2) is low, the serial data cannot be shifted into TLC5916/TLC5917 via SDI. When $\overline{OE}$(ED2) is pulled high, the data input source of the Shift Register is changed back to SDI. At the same time, the output ports are disabled and the error detection is completed. Then, the error status codes saved in the Shift Register can be shifted out via SDO bit by bit along with CLK, as well as the new serial data can be shifted into TLC5916/TLC5917 via SDI.

While in Special Mode, the TLC5916/TLC5917 cannot simultaneously transfer serial data and detect LED load error status.

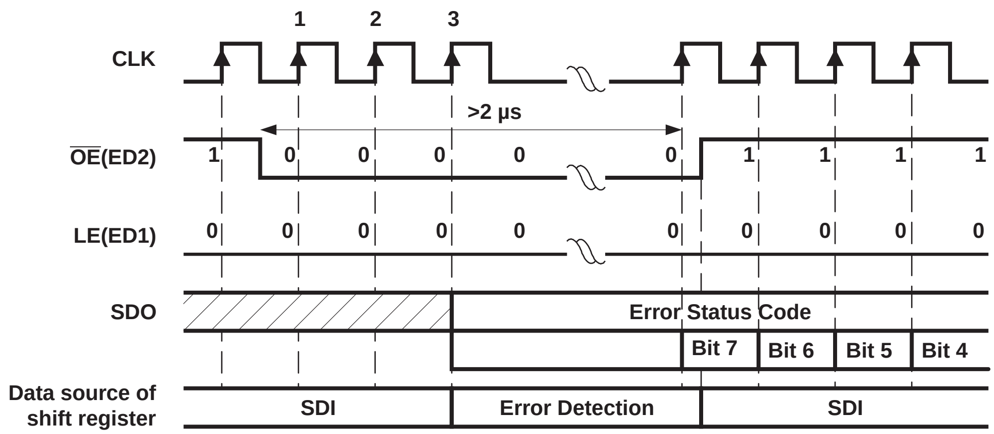


Figure 19. Reading Error Status Code

Writing Configuration Code in Special Mode

When in Special Mode, the active high signal LE(ED1) latches the serial data in the Shift Register to the Configuration Latch, instead of the Output Latch. The latched serial data is used as the Configuration Code.

The code is stored until power off or the Configuration Latch is rewritten. As shown in Figure 20, the timing for writing the Configuration Code is the same as the timing in the Normal Mode to latching output channel data. Both the Configuration Code and Error Status Code are transferred in the common 8-bit Shift Register. Users must pay attention to the sequence of error detection and current adjustment to avoid the Configuration Code being overwritten by Error Status Code.

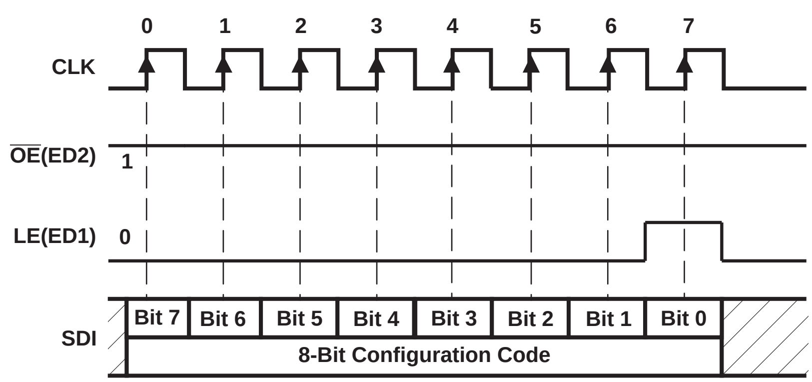


Figure 20. Writing Configuration Code

Open-Circuit Detection Principle

The LED Open-Circuit Detection compares the effective current level I_{out} with the open load detection threshold current $I_{OUT,Th}$. If I_{OUT} is below the $I_{OUT,Th}$ threshold, the TLC5916/TLC5917 detects an open-load condition. This error status can be read as an error status code in the Special Mode. For open-circuit error detection, a channel must be on.

Table 4. Open-Circuit Detection

STATE OF OUTPUT PORT	CONDITION OF OUTPUT CURRENT	ERROR STATUS CODE	MEANING
Off	I_{OUT} = 0 mA	0	Detection not possible
On	$I_{OUT} < I_{OUT,Th}$ (1)	0	Open circuit
	$I_{OUT} \geq I_{OUT,Th}$ (1)	Channel n error status bit 1	Normal

(1) $I_{OUT,Th} = 0.5 \times I_{OUT,target}$ (typical)

Short-Circuit Detection Principle (TLC5917 Only)

The LED short-circuit detection compares the effective voltage level (V_{OUT}) with the shorted-load detection threshold voltages $V_{OUT,TTh}$ and $V_{OUT,RTh}$. If V_{OUT} is above the $V_{OUT,TTh}$ threshold, the TLC5917 detects an shorted-load condition. If V_{OUT} is below the $V_{OUT,RTh}$ threshold, no error is detected/error bit is reset. This error status can be read as an error status code in the Special Mode. For short-circuit error detection, a channel must be on.

Table 5. Shorted-Load Detection

STATE OF OUTPUT PORT	CONDITION OF OUTPUT VOLTAGE	ERROR STATUS CODE	MEANING
Off	I_{OUT} = 0 mA	0	Detection not possible
On	$V_{OUT} \geq V_{OUT,TTh}$	0	Short circuit
	$V_{OUT} < V_{OUT,RTh}$	1	Normal

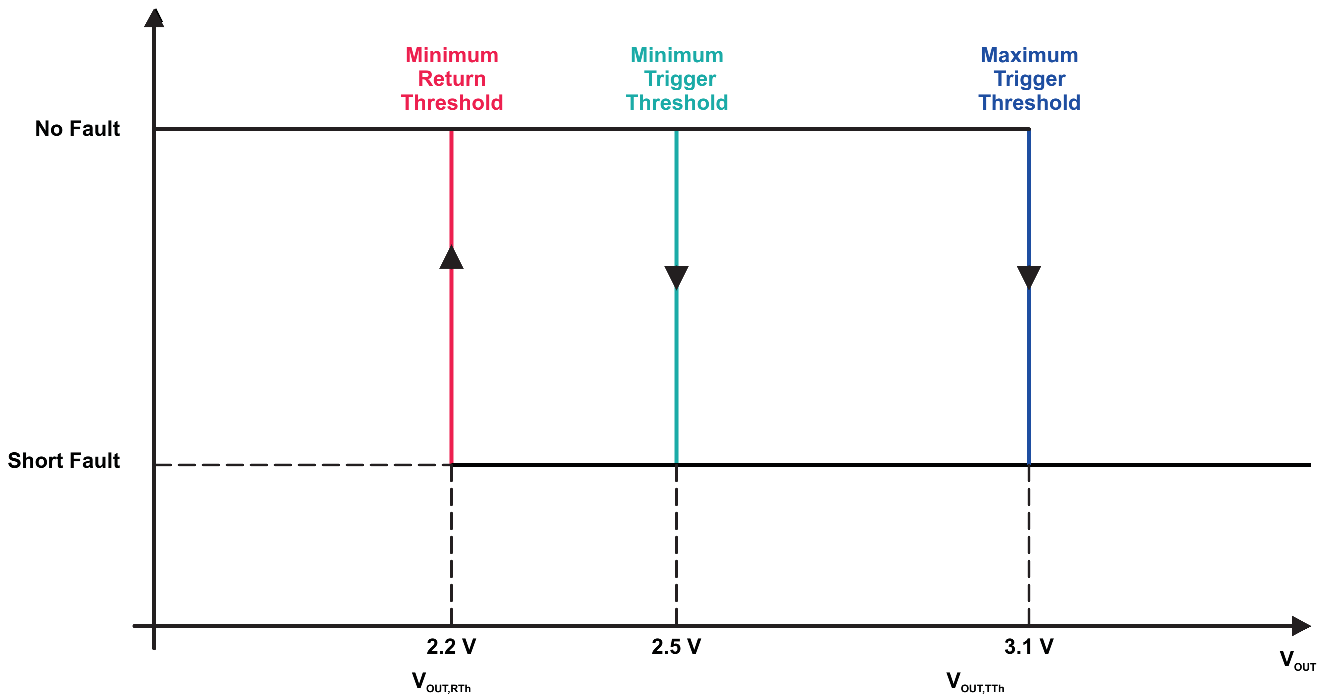


Figure 21. Short-Circuit Detection Principle

Overtemperature Detection and Shutdown

TLC5916/TLC5917 is equipped with a global overtemperature sensor and eight individual, channel-specific, overtemperature sensors.

- When the global sensor reaches the trip temperature, all output channels are shut down, and the error status is stored in the internal Error Status register of every channel. After shutdown, the channels automatically restart after cooling down, if the control signal (output latch) remains on. The stored error status is not reset after cooling down and can be read out as the error status code in the Special Mode.
- When one of the channel-specific sensors reaches trip temperature, only the affected output channel is shut down, and the error status is stored only in the internal Error Status register of the affected channel. After shutdown, the channel automatically restarts after cooling down, if the control signal (output latch) remains on. The stored error status is not reset after cooling down and can be read out as error status code in the Special Mode.

For channel-specific overtemperature error detection, a channel must be on.

The error status code is reset when TLC5916/TLC5917 returns to Normal Mode.

Table 6. Overtemperature Detection(1)

STATE OF OUTPUT PORT	CONDITION	ERROR STATUS CODE	MEANING
Off	I_{OUT} = 0 mA	0	
On On → all channels Off	$T_j < T_{j,trip}$ global	1	Normal
	$T_j > T_{j,trip}$ global	All error status bits = 0	Global overtemperature
On On → Off	$T_j < T_{j,trip}$ channel n	1	Normal
	$T_j > T_{j,trip}$ channel n	Channel n error status bit = 0	Channel n overtemperature

(1) The global shutdown threshold temperature is approximately 170°C.

8-Bit Configuration Code and Current Gain

Bit definition of the Configuration Code in the Configuration Latch is shown in Table 7.

Table 7. Bit Definition of 8-Bit Configuration Code

	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Meaning	CM	HC	CC0	CC1	CC2	CC3	CC4	CC5
Default	1	1	1	1	1	1	1	1

Bit 7 is first sent into TLC5916/TLC5917 via SDI. Bits 1 to 7 {HC, CC[0:5]} determine the voltage gain (VG) that affects the voltage at R-EXT and indirectly affects the reference current, I_{ref}, flowing through the external resistor at R-EXT. Bit 0 is the Current Multiplier (CM) that determines the ratio $I_{OUT,target}/I_{ref}$. Each combination of VG and CM gives a specific Current Gain (CG).

- VG: the relationship between {HC,CC[0:5]} and the voltage gain is calculated as shown below:

  $VG = (1 + HC) \times (1 + D/64) / 4$

  $D = CC0 \times 2^5 + CC1 \times 2^4 + CC2 \times 2^3 + CC3 \times 2^2 + CC4 \times 2^1 + CC5 \times 2^0$

  Where HC is 1 or 0, and D is the binary value of CC[0:5]. So, the VG could be regarded as a floating-point number with 1-bit exponent HC and 6-bit mantissa CC[0:5]. {HC,CC[0:5]} divides the programmable voltage gain VG into 128 steps and two sub-bands:

  Low voltage sub-band (HC = 0): VG = 1/4 ~ 127/256, linearly divided into 64 steps

  High voltage sub-band (HC = 1): VG = 1/2 ~ 127/128, linearly divided into 64 steps
- CM: In addition to determining the ratio $I_{OUT,target}/I_{ref}$, CM limits the output current range.

  High Current Multiplier (CM = 1): $I_{OUT,target}/I_{ref} = 15$, suitable for output current range I_{OUT} = 10 mA to 120 mA.

  Low Current Multiplier (CM = 0): $I_{OUT,target}/I_{ref} = 5$, suitable for output current range I_{OUT} = 3 mA to 40 mA
- CG: The total Current Gain is defined as the following.

  $V_{R\text{-}EXT} = 1.26\ V \times VG$

  $I_{ref} = V_{R\text{-}EXT}/R_{ext}$, if the external resistor, R_{ext}, is connected to ground.

  $I_{OUT,target} = I_{ref} \times 15 \times 3^{CM-1} = 1.26\ V/R_{ext} \times VG \times 15 \times 3^{CM-1} = (1.26\ V/R_{ext} \times 15) \times CG$

  $CG = VG \times 3^{CM-1}$

  Therefore, CG = (1/12) to (127/128), and it is divided into 256 steps. If CG = 127/128 = 0.992, the $I_{OUT,target}$-R_{ext}.

Examples

- Configuration Code {CM, HC, CC[0:5]} = {1,1,111111}

  VG = 127/128 = 0.992 and CG = VG × 3^0 = VG = 0.992
- Configuration Code = {1,1,000000}

  VG = (1 + 1) × (1 + 0/64)/4 = 1/2 = 0.5, and CG = 0.5
- Configuration Code = {0,0,000000}

  VG = (1 + 0) × (1 + 0/64)/4 = 1/4, and CG = (1/4) × 3^{-1} = 1/12

After power on, the default value of the Configuration Code {CM, HC, CC[0:5]} is {1,1,111111}. Therefore, VG = CG = 0.992. The relationship between the Configuration Code and the Current Gain is shown in Figure 22.

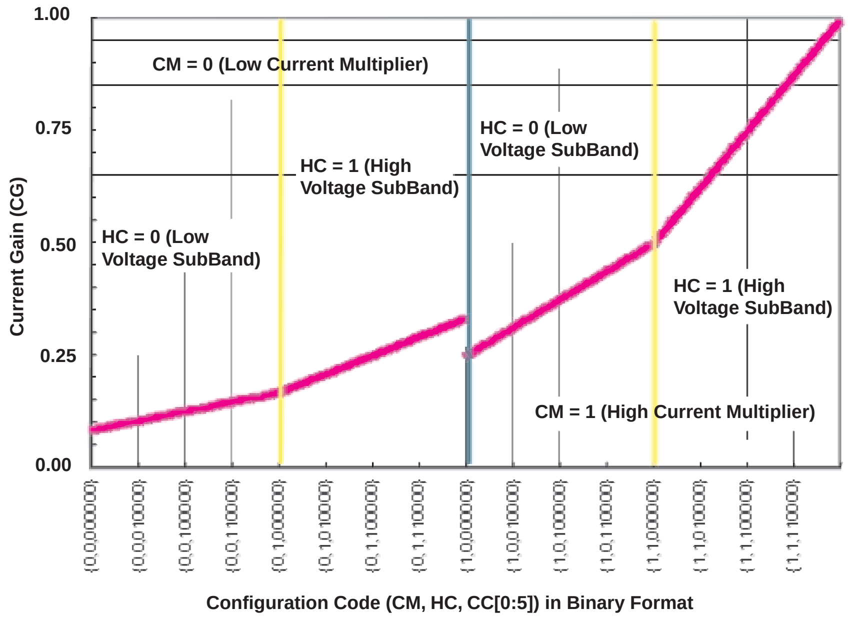


Figure 22. Current Gain vs Configuration Code

REVISION HISTORY

Changes from Revision A (November 2010) to Revision B	Page
• Added Maximum LED Voltage 20-V to Features.	1
• Added Abstract section.	1
• Changed resistor value in Single Implementation diagram from 840Ω to 720Ω.	1
• Changed Default Relationship Curve to reflect correct data.	18
• Changed resistor value in Single Implementation diagram from 840Ω to 720Ω.	19
• Changed resistor value in Cascading Implementation diagram from 840Ω to 720Ω.	19

Changes from Revision B (February 2011) to Revision C	Page
• Replaced the Power Dissipation and Thermal Impedance table with the Thermal Information tables	7

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TLC5916ID	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC5916IDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC5916IDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC5916IDRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC5916IN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TLC5916INE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TLC5916IPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC5916IPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC5916IPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC5916IPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC5917ID	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC5917IDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC5917IDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC5917IDRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC5917IN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TLC5917INE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TLC5917IPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC5917IPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TLC5917IPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC5917IPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF TLC5916, TLC5917 :

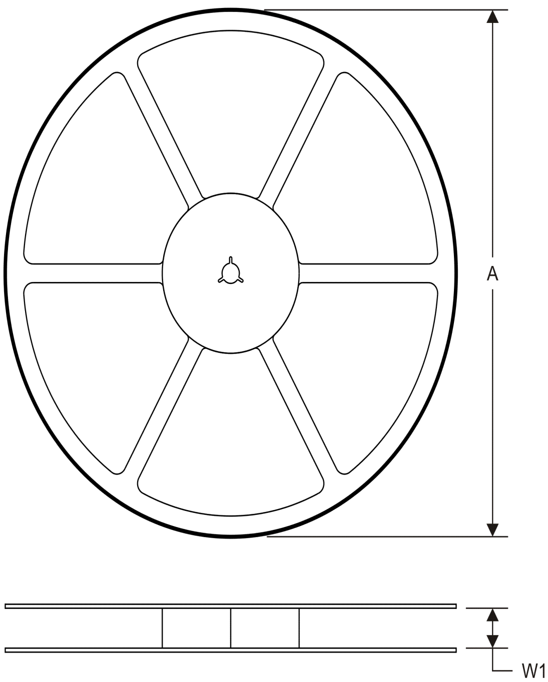
- Automotive: TLC5916-Q1, TLC5917-Q1

NOTE: Qualified Version Definitions:

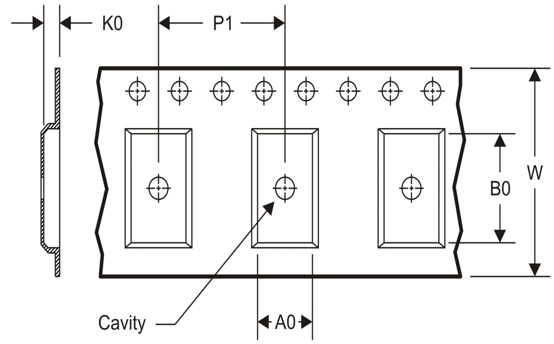
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



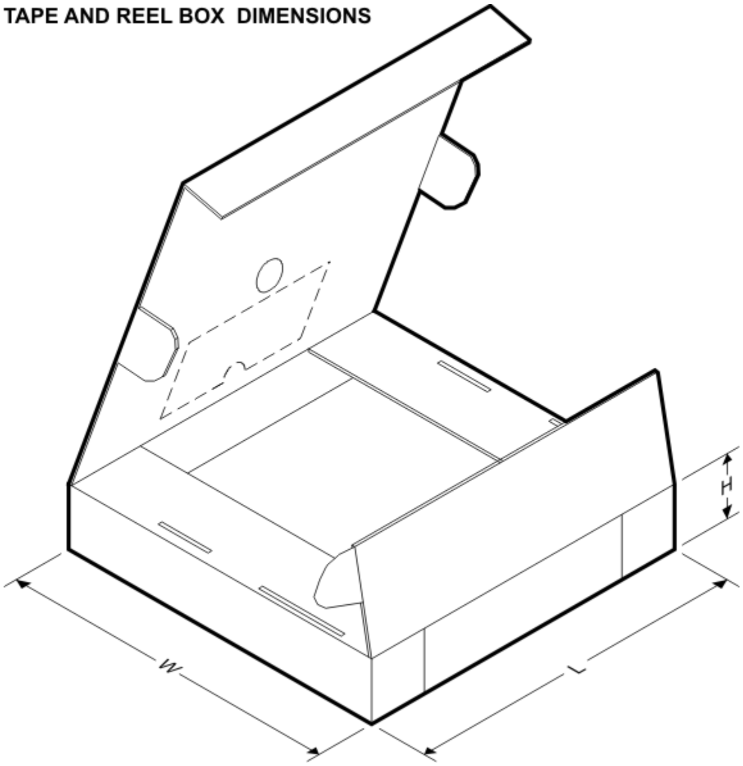
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC5916IDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TLC5916IPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLC5917IDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TLC5917IPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

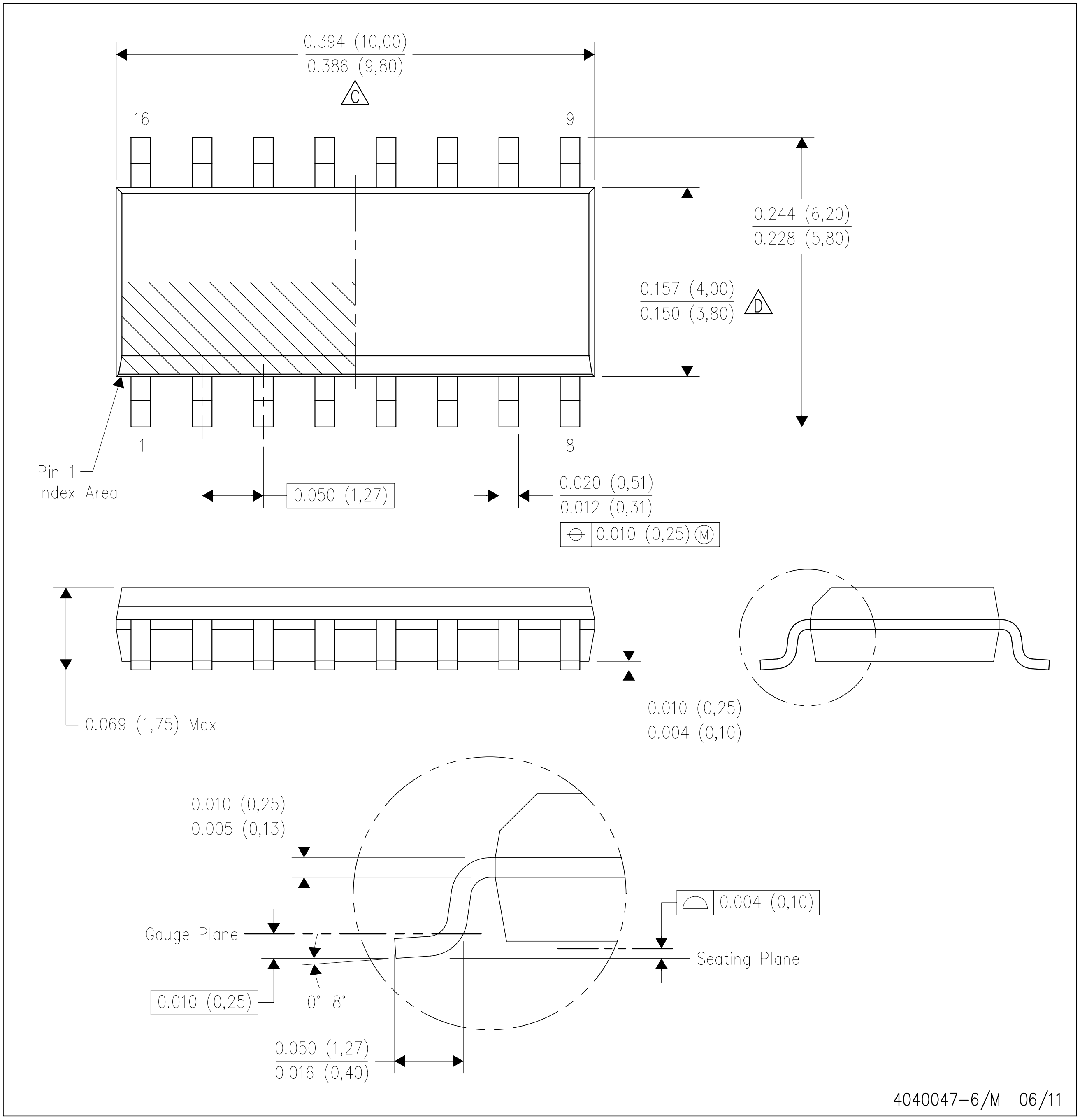
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

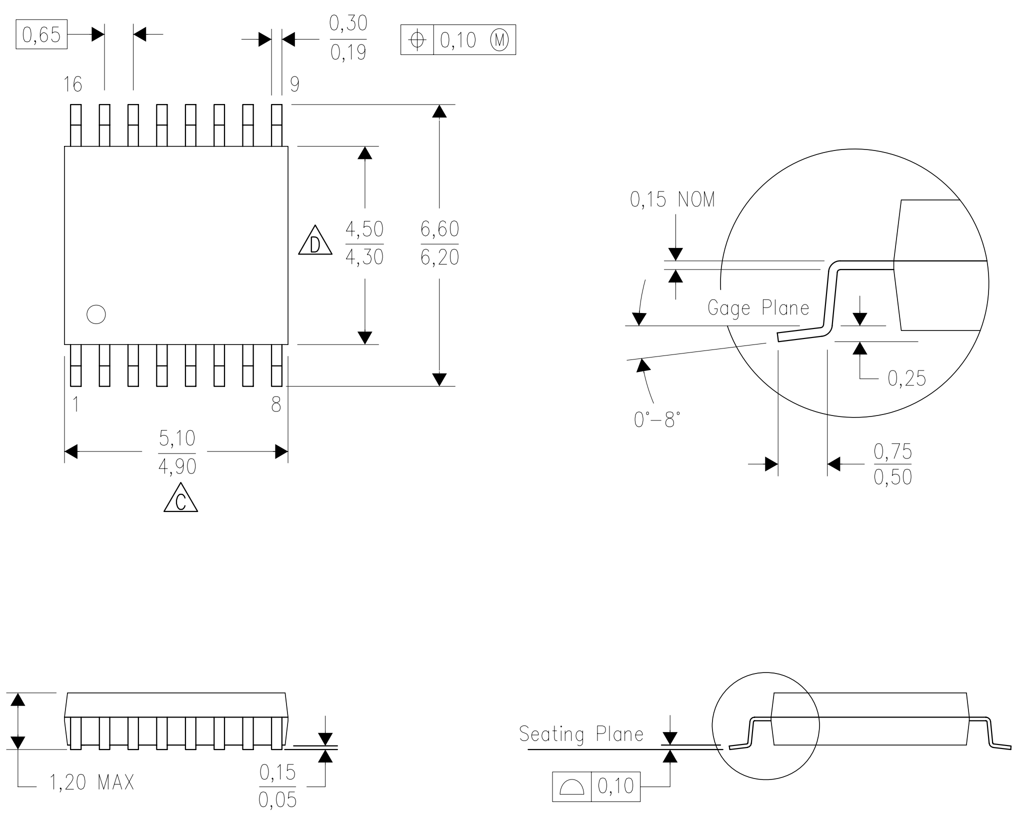
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC5916IDR	SOIC	D	16	2500	333.2	345.9	28.6
TLC5916IPWR	TSSOP	PW	16	2000	367.0	367.0	35.0
TLC5917IDR	SOIC	D	16	2500	333.2	345.9	28.6
TLC5917IPWR	TSSOP	PW	16	2000	367.0	367.0	35.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



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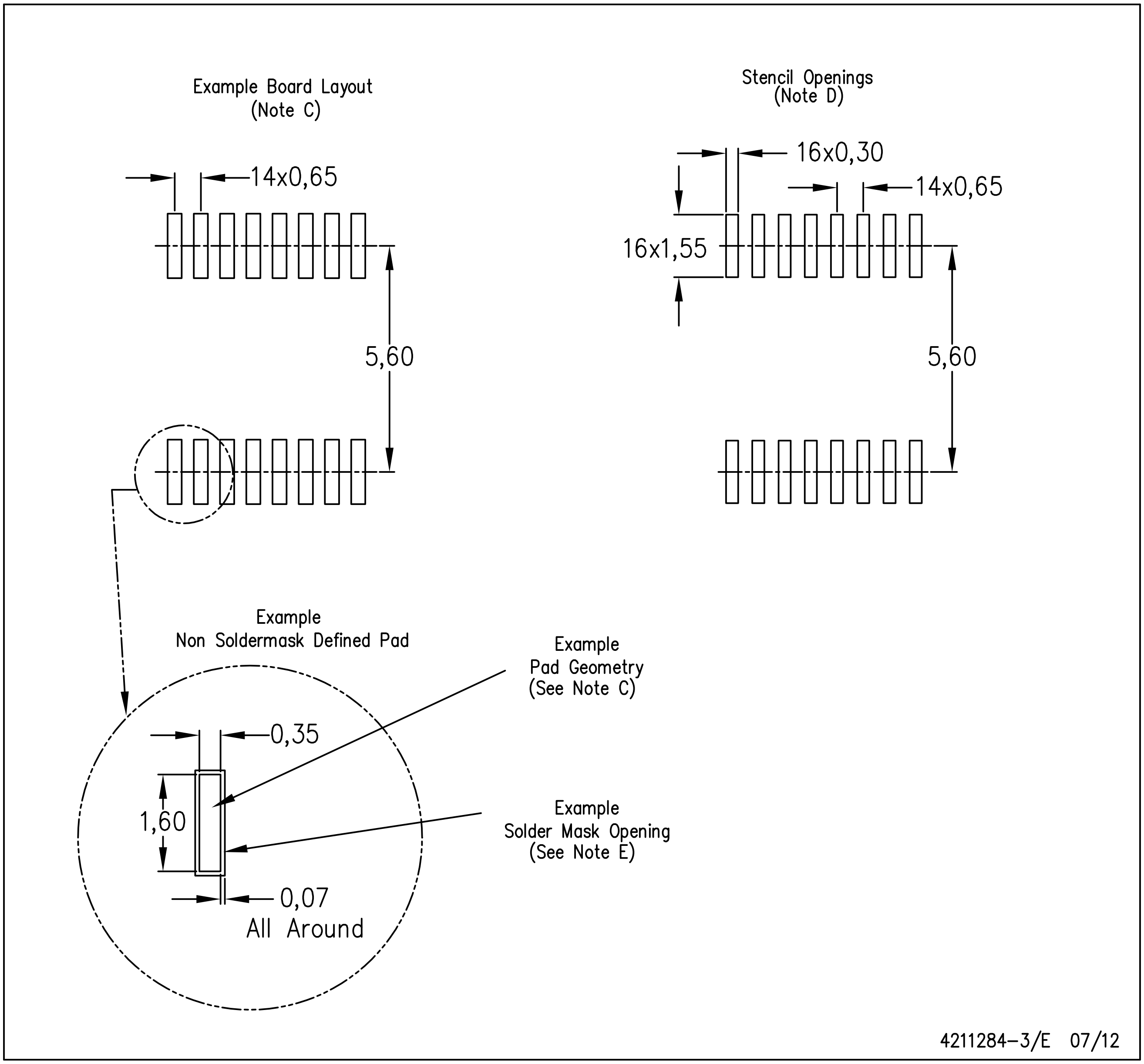
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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