2-CHANNEL ESD-PROTECTION ARRAY FOR AC-COUPLED/NEGATIVE-RAIL DATA INTERFACES

Check for Samples: TPD2E007

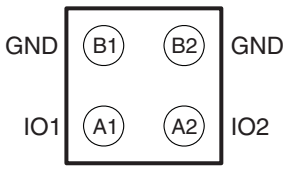
FEATURES

- **ESD Protection Exceeds IEC61000-4-2 (Level 4)**
  - **±15-kV Human-Body Model (HBM)**
  - **±8-kV IEC 61000-4-2 Contact Discharge**
  - **±15-kV IEC 61000-4-2 Air-Gap Discharge**
- **4.5-A Peak Pulse Current (8/20 ms Pulse)**
- **15-pF Line to GND Capacitance**
- **Low 50-nA Leakage Current**
- **2-Channel Device**
- **Space-Saving PicoStar™ and DCK Package**

APPLICATIONS

- **Cell Phones, PDAs**
- **Audio Interface Connections**
- **Consumer Electronics (DVR, Set-Top Box, TV)**
- **Industrial Interface (RS-232, RS-485, RS-422, LVDS)**

YFMG4 PACKAGE (BOTTOM VIEW)

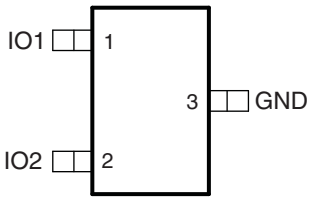


0.8 mm × 0.8 mm (0.4 mm pitch)

YFMG4 PIN DESCRIPTIONS

TERMINAL		DESCRIPTION
NAME	NO.	
IO	A1, A2	ESD-protection channel
GND	B1, B2	Ground

DCK PACKAGE (TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

This device is an application-specific integrated parts (ASIP) designed to offer system level ESD solutions for wide range of portable and industrial applications. The back-to-back diode array allows AC-coupled or negative-going data transmission (audio interface, LVDS, RS-485, RS-232, etc.) without compromising signal integrity. The PicoStar™ package is intended to be embedded inside the printed circuit board which saves board space in portable applications. This device exceeds the IEC61000-4-2 (Level 4) ESD protection and suitable to provide system level ESD protection for the valuable internal ICs while placed near the connector.

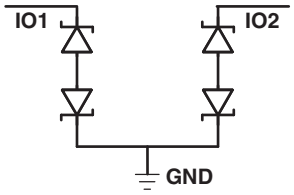
The TPD2E007 is offered in a 4-bump PicoStar™ and 3-pin DCK packages. The PicoStar™ package (YFMG4), with only 0.15 mm (Max) package height, is recommended for ultra space saving application where the package height is a key concern. The PicoStar™ package can be used in either embedded PCB board applications or in surface mount applications. The industry standard DCK package offers straightforward board layout option in legacy designs.

ORDERING INFORMATION

T_A	PACKAGE(1) (2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	DSLGA – YFM	Tape and reel	TPD2E007YFMRG4	45 T
–40°C to 85°C	3-DCK	Tape and reel	TPD2E007DCKR	45U

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

EQUIVALENT SCHEMATIC REPRESENTATION



ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{IO}			–13.5	13.5	V
	Continuous power dissipation (T_A = 70°C)	YFM package		270	mW
		DCK package		218	
	Operating temperature range		–40	85	°C
T_{stg}	Storage temperature range		–65	150	°C
T_J	Junction temperature			150	°C
	Bump temperature (soldering)	Infrared (15 s)		220	°C
		Vapor phase (60 s)		215	
	Lead temperature (soldering, 10 s)			300	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{BR}	Break-down voltage	I_{IO} = 10 mA	±14			V
I_{IO}	Channel leakage current			20	50	nA
R_d	Dynamic resistance			3.5		Ω
C_{IN}	Channel input capacitance	V_{IO} = 2.5 V		10	15	pF

(1) Typical values are at V_{CC} = 5 V and T_A = 25°C.

ESD Protection

PARAMETER	TYP	UNIT
HBM	±15	kV
IEC 61000-4-2 Contact Discharge	±8	kV
IEC 61000-4-2 Air-Gap Discharge	±15	kV

TYPICAL OPERATING CHARACTERISTICS

IEC Clamping Waveforms (20 ns/div)

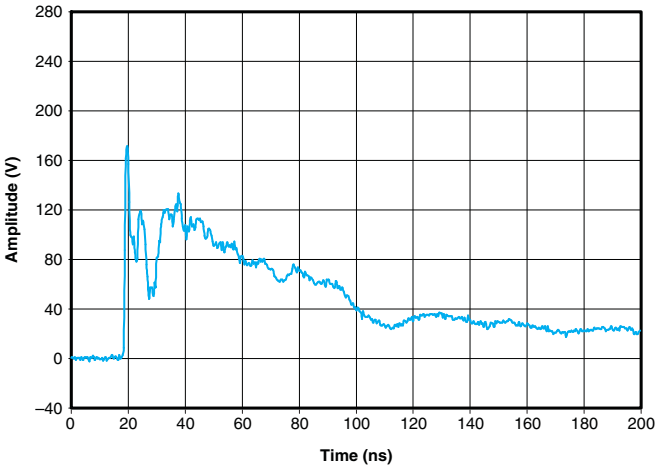


Figure 1. 8-kV Contact

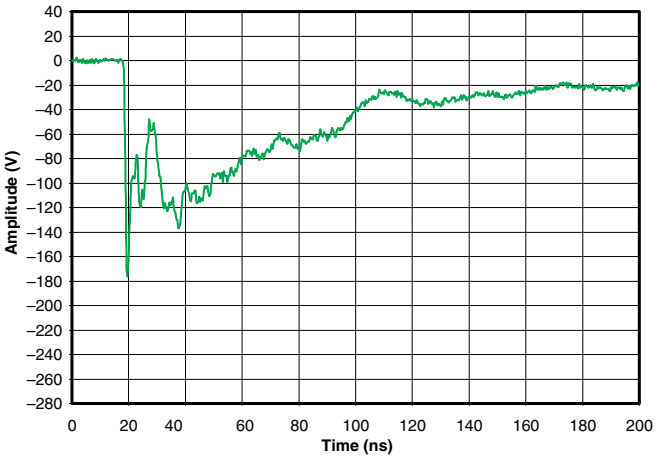


Figure 2. –8-kV Contact

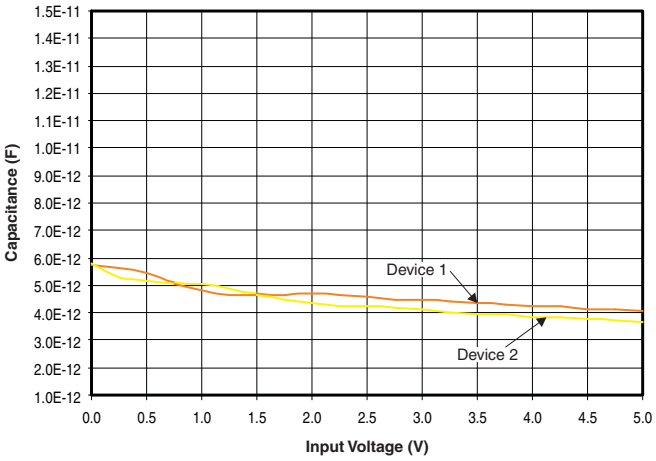


Figure 3. Capacitance vs Input Voltage at T_A = 27°C

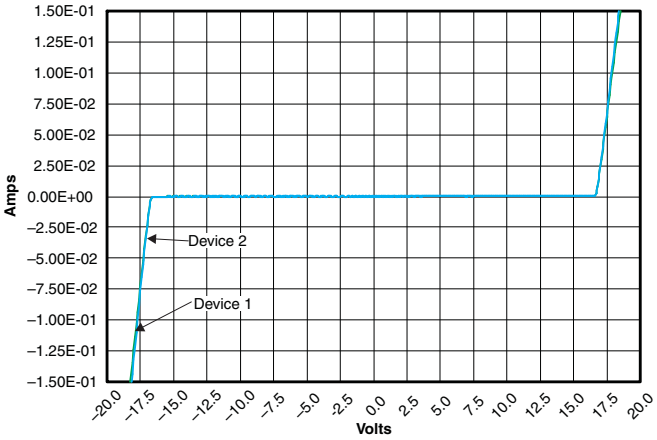


Figure 4. Diode Breakdown Voltage Data at T_A = 27°C

REVISION HISTORY

Changes from Revision D (October 2009) to Revision E	Page
• Added max continuous power dissipation value for DCK package	2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD2E007DCKR	ACTIVE	SC70	DCK	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	45U	Samples
TPD2E007YFMR	PREVIEW	DSLGA	YFM	4		TBD	Call TI	Call TI	-40 to 85		
TPD2E007YFMRG4	ACTIVE	DSLGA	YFM	4	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 85	45 T	Samples
TPD2E007YFMTG4	ACTIVE	DSLGA	YFM	4	250	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 85	45 T	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

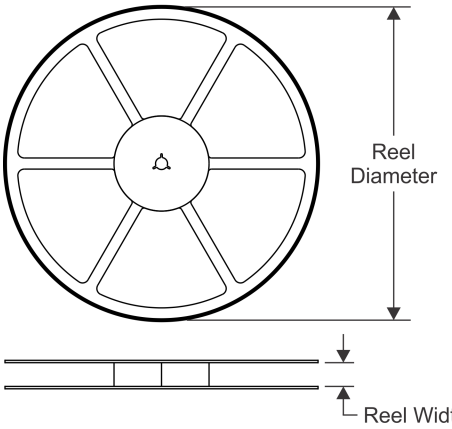
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

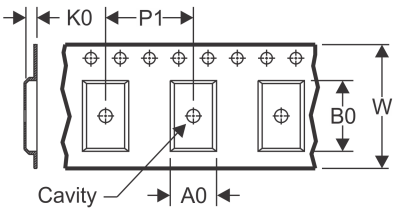
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

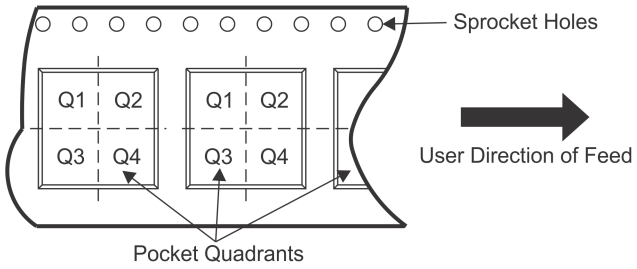


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

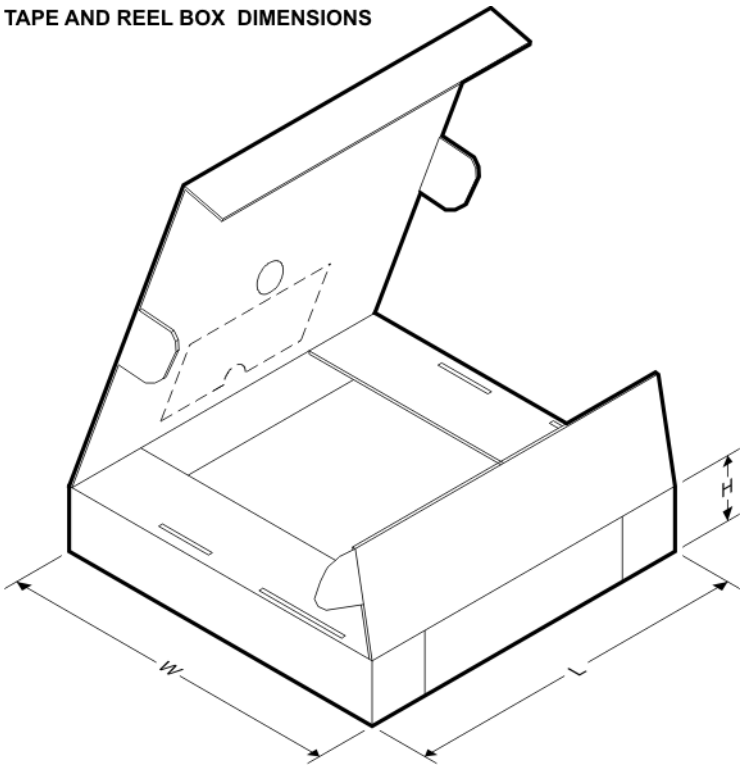
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD2E007DCKR	SC70	DCK	3	3000	179.0	8.4	2.4	2.4	1.19	4.0	8.0	Q3
TPD2E007YFMRG4	DSLGA	YFM	4	3000	178.0	9.2	0.83	0.83	0.19	4.0	8.0	Q1
TPD2E007YFMTG4	DSLGA	YFM	4	250	178.0	9.2	0.83	0.83	0.19	4.0	8.0	Q1

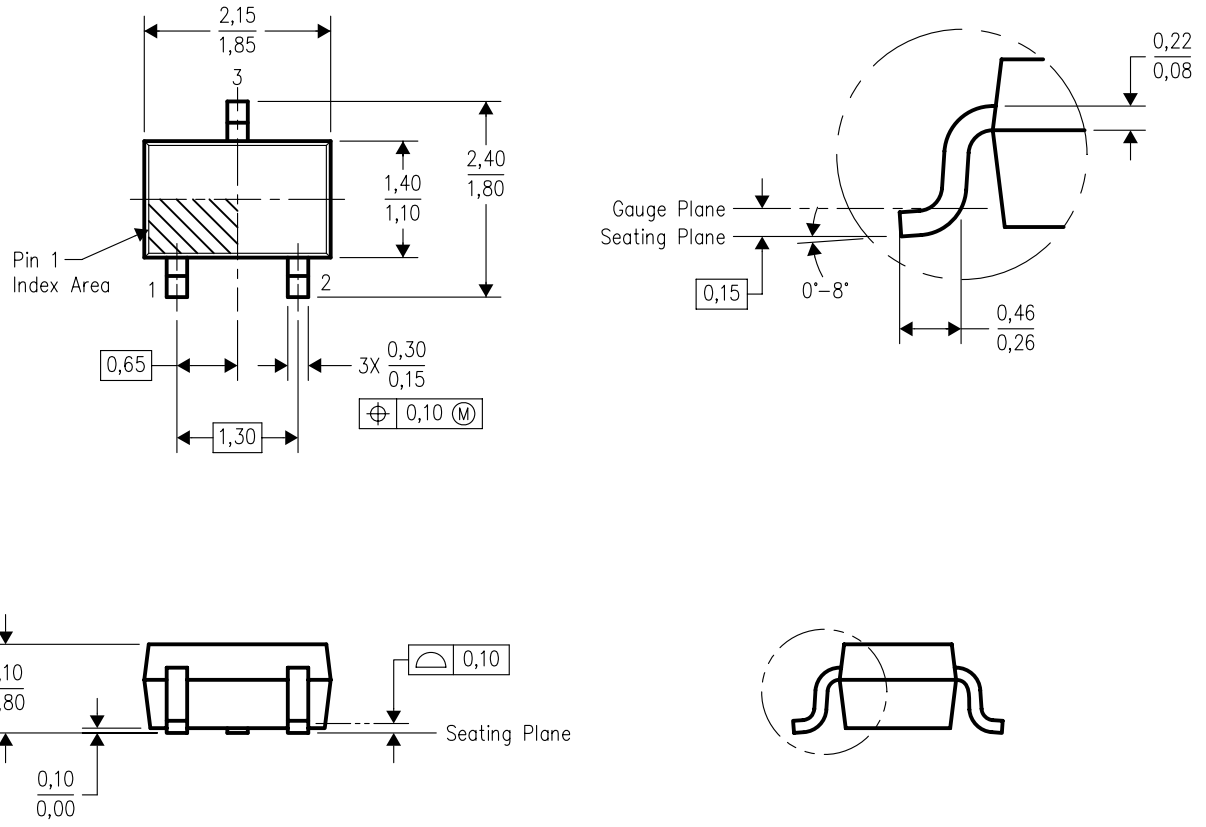
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD2E007DCKR	SC70	DCK	3	3000	195.0	200.0	45.0
TPD2E007YFMRG4	DSLGA	YFM	4	3000	220.0	220.0	35.0
TPD2E007YFMTG4	DSLGA	YFM	4	250	220.0	220.0	35.0

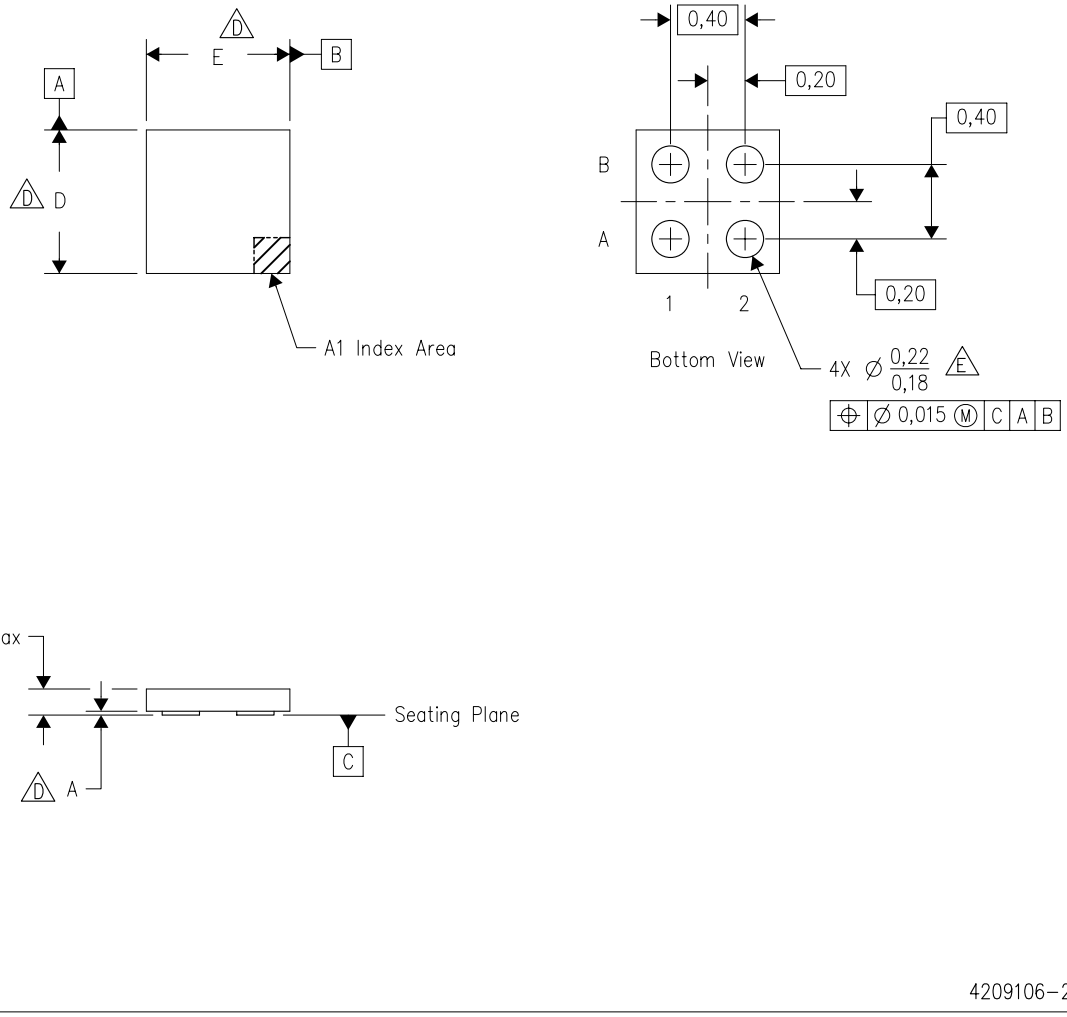
DCK (R–PDSO–G3) PLASTIC SMALL–OUTLINE PACKAGE



4093553–2/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.

YFM (S–pSTAR–N4) PicoStar™



4209106–2/K 11/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. PicoStar™ package configuration.
D. The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative.
E. Reference Product Data Sheet for array population. 2 x 2 matrix pattern is shown for illustration only.
F. This package is a Pb–free solder land design.

PicoStar is a trademark of Texas Instruments.

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