
CSP-9

800-mA, 6-MHz HIGH-EFFICIENCY STEP-DOWN CONVERTER WITH I^2C^{TM} COMPATIBLE INTERFACE IN CHIP SCALE PACKAGING

Check for Samples: TPS62650, TPS62651

FEATURES

- **86% Efficiency at 6 MHz Operation**
- **38μA Quiescent Current**
- **Wide V_{IN} Range From 2.3 V to 5.5 V**
- **6MHz Regulated Frequency Operation**
- ***Best-In-Class* Load and Line Transient**
- **±2% PWM DC Voltage Accuracy**
- **Automatic PFM/PWM Mode Switching**
- **Low Ripple Light-Load PFM**
- **I^2C Compatible Interface up to 3.4 Mbps**
- **Pin-Selectable Output Voltage (VSEL)**
- **Internal Soft-Start, <150-μs Start-Up Time**
- **Current Overload and Thermal Shutdown Protection**
- **Three Surface-Mount External Components Required (One MLCC Inductor, Two Ceramic Capacitors)**
- **Complete Sub 1-mm Component Profile Solution**
- **Total Solution Size <13mm^2**
- **Available in a 9-Pin NanoFree™ (CSP) Packaging**

APPLICATIONS

- **SmartReflex™ Compliant Power Supply**
- **OMAP™ Application Processor Core Supply**
- **Cell Phones, Smart-Phones**
- **Micro DC-DC Converter Modules**

DESCRIPTION

The TPS6265x device is a high-frequency synchronous step-down dc-dc converter optimized for battery-powered portable applications. Intended for low-power applications, the TPS6265x supports up to 800mA load current and allows the use of small, low cost inductors and capacitors.

The device is ideal for mobile phones and similar portable applications powered by a single-cell Li-Ion battery. With an output voltage range adjustable via I^2C interface down to 0.75V, the device supports low-voltage DSPs and processors core power supplies in smart-phones and handheld computers.

The TPS6265x operates at a regulated 6MHz switching frequency and enters the efficiency optimized power-save mode operation at light load currents to maintain high efficiency over the entire load current range. In the shutdown mode, the current consumption is reduced to less than 3.5μA.

The serial interface is compatible with Standard, Fast/Fast Plus and High-Speed mode I^2C specification allowing transfers at up to 3.4 Mbps. This communication interface is used for dynamic voltage scaling with voltage steps down to 12.5mV, for setting the output voltage or reprogramming the mode of operation (PFM/PWM or Forced PWM) for instance.

The TPS6265x is available in an 9-pin chip-scale package (CSP).

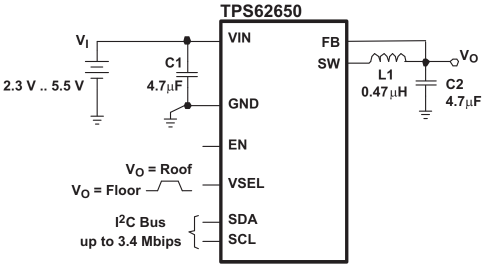

Figure 1. Typical Application

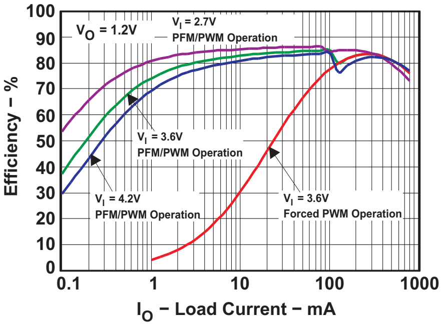

Figure 2. Efficiency vs Load Control

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

PART NUMBER(1)	OUTPUT VOLTAGE RANGE(2)	DEFAULT OUTPUT VOLTAGE(2)		I^2C ADDRESS BITS(2)		PACKAGE(3)	ORDERING	PACKAGE MARKING (CC)
		VSEL0	VSEL1	A2	A1			
TPS62650(4)	0.75 V to 1.4375 V	1.05 V	1.2 V	0	1	YFF-9	TPS62650YFF	GJ
TPS62651(4)	0.75 V to 1.4375 V	0.95 V	1.1 V	1	1	YFF-9	TPS62651YFF	GK

(1) All devices are specified for operation in the commercial temperature range, –40°C to 85°C.
(2) For customized output voltage limits (within a 0.75 V to 1.5375 V range), default output voltage and I^2C address, contact the factory. Internal tap points are available to facilitate default output voltage settings in multiples of 50 mV.
(3) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(4) The following registers bits are set by internal hardware logic and not user programmable through I^2C:
  (a) VSEL0[7] = 1
  (b) VSEL1[7] = 1
  (c) CONTROL1[3:2] = 00

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE		UNIT
		MIN	MAX	
Input Voltage	at VIN, SW(2)	–0.3	7	V
	at FB (2)	–0.3	3.6	V
	at EN, VSEL, SCL, SDA (2)	–0.3	$V_I + 0.3$	V
Power dissipation		Internally limited		
Operating junction temperature, T_A (3)		–40	85	°C
Maximum operating junction Temperature, T_J			150	°C
Storage temperature range, T_{stg}		–65	150	°C
ESD rating(4)	Human body model		2	kV
	Charge device model		1	kV
	Machine model		200	V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A(max)}$) is dependent on the maximum operating junction temperature ($T_{J(max)}$), the maximum power dissipation of the device in the application ($P_{D(max)}$), and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A(max)} = T_{J(max)} - (\theta_{JA} \times P_{D(max)})$. To achieve optimum performance, it is recommended to operate the device with a maximum junction temperature of 105°C.
(4) The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin. The machine model is a 200-pF capacitor discharged directly into each pin.

DISSIPATION RATINGS(1)

PACKAGE	$R_{\theta JA}$ (2)	$R_{\theta JB}$ (2)	POWER RATING $T_A \leq 25°C$	DERATING FACTOR ABOVE $T_A = 25°C$
YFF	105°C/W	35°C/W	950 mW	8 mW/°C

(1) Maximum power dissipation is a function of $T_J(max)$, θ_{JA} and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = [T_J(max) - T_A] / \theta_{JA}$.
(2) This thermal data is measured with high-K board (4 layers board according to JESD51-7 JEDEC standard).

ELECTRICAL CHARACTERISTICS

Minimum and maximum values are at V_I = 2.3V to 5.5V, V_O = 1.2 V, EN = 1.8V, EN_DCDC bit = 1, AUTO mode and T_A = -40°C to 85°C; Circuit of Parameter Measurement Information section (unless otherwise noted). Typical values are at V_I = 3.6V, V_O = 1.2 V, EN = 1.8V, EN_DCDC bit = 1, AUTO mode and T_A = 25°C (unless otherwise noted).

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
V_I	Input voltage range			2.3		5.5	V
I_Q	Operating quiescent current		V_I = 3.6 V, I_O = 0 mA, -40°C ≤ T_J≤ 85°C. Device not switching		38	58	µA
			V_I = 3.6 V, I_O = 0 mA. PWM mode		5.35		mA
$I_{(SD)}$	Shutdown current		V_I = 3.6 V, EN = GND, EN_DCDC bit = X, -40°C ≤ T_J≤ 85°C		0.5	3.5	µA
			V_I = 3.6 V, EN = V_I, EN_DCDC bit = 0, -40°C ≤ T_J≤ 85°C		0.5	3.5	µA
UVLO	Undervoltage lockout threshold				2.05	2.15	V
ENABLE, VSEL, SDA, SCL							
V_{IH}	High-level input voltage			0.9			V
V_{IL}	Low-level input voltage					0.4	V
I_{lkg}	Input leakage current		Input tied to GND or V_I, -40°C ≤ T_J≤ 85°C		0.01	0.7	µA
POWER SWITCH							
$r_{DS(on)}$	P-channel MOSFET on resistance		V_I = $V_{(GS)}$ = 3.6 V		255		mΩ
			V_I = $V_{(GS)}$ = 2.5 V		335		
I_{lkg}	P-channel leakage current, PMOS		$V_{(DS)}$ = 5.5 V, -40°C ≤ T_J≤ 85°C			1	µA
$r_{DS(on)}$	N-channel MOSFET on resistance		V_I = $V_{(GS)}$ = 3.6 V		140		mΩ
			V_I = $V_{(GS)}$ = 2.5 V		200		
I_{lkg}	N-channel leakage current, NMOS		$V_{(DS)}$ = 5.5 V, -40°C ≤ T_J≤ 85°C			1	µA
r_{DIS}	Discharge resistor for power-down sequence				15	50	Ω
	P-MOS current limit		2.3 V ≤ V_I ≤ 4.8 V. Open loop	1350	1500	1700	mA
	Input current limit under short-circuit conditions		V_O = 0 V		11		mA
	Thermal shutdown				140		°C
	Thermal shutdown hysteresis				15		°C
OSCILLATOR							
f_{SW}	Oscillator frequency		I_O = 0 mA. PWM mode	5.4	6	6.6	MHz
OUTPUT							
V_O	Regulated DC output voltage accuracy	TPS62650/1	2.3 V ≤ V_I ≤ 5.5 V, 0 mA ≤ $I_{O(DC)}$ ≤ 800 mA V_O = 0.75 V, 1.05 V, 1.20 V, 1.4375 V (TPS62650) V_O = 0.75 V, 0.95 V, 1.10 V, 1.4375 V (TPS62651) PWM operation	–2%		2%	
			2.3 V ≤ V_I ≤ 5.5 V, 0 mA ≤ $I_{O(DC)}$ ≤ 800 mA V_O = 0.75 V, 1.05 V, 1.20 V, 1.4375 V (TPS62650) V_O = 0.75 V, 0.95 V, 1.10 V, 1.4375 V (TPS62651) PFM/PWM Operation	–2%		3%	
	Regulated DC output voltage temperature drift		V_I = 3.6 V, V_O = 1.20 V, $I_{O(DC)}$ = 50 mA -40°C ≤ T_J ≤ 105°C. PWM operation	-0.5%		+0.5%	
	Line regulation		V_I = V_O + 0.5 V (min 2.3 V) to 5.5 V, $I_{O(DC)}$ = 200 mA		0.13		%/V
	Load regulation		$I_{O(DC)}$ = 0 mA to 800 mA		–0.00046		%/mA
	Feedback input resistance				480		kΩ
ΔV_O	Power-save mode ripple voltage		V_O = 1.05 V, VSEL = GND, $I_{O(DC)}$ = 1 mA PFM operation		16		mV_{PP}
			V_O = 1.20 V, VSEL = V_I, $I_{O(DC)}$ = 1 mA PFM operation		16		mV_{PP}
DAC							
	Resolution	TPS62650 TPS62651		6			Bits
	Differential nonlinearity		Specified monotonic by design			±0.4	LSB

ELECTRICAL CHARACTERISTICS (continued)

Minimum and maximum values are at V_I = 2.3V to 5.5V, V_O = 1.2 V, EN = 1.8V, EN_DCDC bit = 1, AUTO mode and T_A = -40°C to 85°C; Circuit of Parameter Measurement Information section (unless otherwise noted). Typical values are at V_I = 3.6V, V_O = 1.2 V, EN = 1.8V, EN_DCDC bit = 1, AUTO mode and T_A = 25°C (unless otherwise noted).

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
TIMING							
	Setup Time Between Rising EN and Start of I^2C Stream	TPS62650/1		50			μs
V_O	Output voltage settling time	TPS62650/1	From min to max output voltage, $I_{O(DC)}$ = 500 mA, VSEL = V_I, PWM operation		12		μs
	Start-up time	TPS62650/1	Time from active EN to V_O V_O = 1.2 V, I_O = 0 mA, PWM operation		125		μs
			Time from active EN to V_O V_O = 1.05 V, I_O = 0 mA, PFM operation		120		

I^2C INTERFACE TIMING CHARACTERISTICS(1)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$f_{(SCL)}$	SCL Clock Frequency	Standard mode		100	kHz
		Fast mode		400	kHz
		Fast mode plus		1	MHz
		High-speed mode (write operation), C_B – 100 pF max		3.4	MHz
		High-speed mode (read operation), C_B – 100 pF max		3.4	MHz
		High-speed mode (write operation), C_B – 400 pF max		1.7	MHz
		High-speed mode (read operation), C_B – 400 pF max		1.7	MHz
t_{BUF}	Bus Free Time Between a STOP and START Condition	Standard mode	4.7		μs
		Fast mode	1.3		μs
		Fast mode plus	0.5		μs
t_{HD}, t_{STA}	Hold Time (Repeated) START Condition	Standard mode	4		μs
		Fast mode	600		ns
		Fast mode plus	260		ns
		High-speed mode	160		ns
t_{LOW}	LOW Period of the SCL Clock	Standard mode	4.7		μs
		Fast mode	1.3		μs
		Fast mode plus	0.5		μs
		High-speed mode, C_B – 100 pF max	160		ns
		High-speed mode, C_B – 400 pF max	320		ns
t_{HIGH}	HIGH Period of the SCL Clock	Standard mode	4		μs
		Fast mode	600		ns
		Fast mode plus	260		ns
		High-speed mode, C_B – 100 pF max	60		ns
		High-speed mode, C_B – 400 pF max	120		ns
t_{SU}, t_{STA}	Setup Time for a Repeated START Condition	Standard mode	4.7		μs
		Fast mode	600		ns
		Fast mode plus	260		ns
		High-speed mode	160		ns
t_{SU}, t_{DAT}	Data Setup Time	Standard mode	250		ns
		Fast mode	100		ns
		Fast mode plus	50		ns
		High-speed mode	10		ns

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(1) Specified by design. Not tested in production.

I^2C INTERFACE TIMING CHARACTERISTICS[(1)] (continued)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{HD}, t_{DAT}	Data Hold Time	Standard mode	0	3.45	µs
		Fast mode	0	0.9	µs
		Fast mode plus	0		µs
		High-speed mode, C_B – 100 pF max	0	70	ns
		High-speed mode, C_B – 400 pF max	0	150	ns
t_{RCL}	Rise Time of SCL Signal	Standard mode	20 + 0.1 C_B	1000	ns
		Fast mode	20 + 0.1 C_B	300	ns
		Fast mode plus		120	ns
		High-speed mode, C_B – 100 pF max	10	40	ns
		High-speed mode, C_B – 400 pF max	20	80	ns
t_{RCL1}	Rise Time of SCL Signal After a Repeated START Condition and After an Acknowledge BIT	Standard mode	20 + 0.1 C_B	1000	ns
		Fast mode	20 + 0.1 C_B	300	ns
		Fast mode plus		120	ns
		High-speed mode, C_B – 100 pF max	10	80	ns
		High-speed mode, C_B – 400 pF max	20	160	ns
t_{FCL}	Fall Time of SCL Signal	Standard mode	20 + 0.1 C_B	300	ns
		Fast mode	20 + 0.1 C_B	300	ns
		Fast mode plus		120	ns
		High-speed mode, C_B – 100 pF max	10	40	ns
		High-speed mode, C_B – 400 pF max	20	80	ns
t_{RDA}	Rise Time of SDA Signal	Standard mode	20 + 0.1 C_B	1000	ns
		Fast mode	20 + 0.1 C_B	300	ns
		Fast mode plus		120	ns
		High-speed mode, C_B – 100 pF max	10	80	ns
		High-speed mode, C_B – 400 pF max	20	160	ns
t_{FDA}	Fall Time of SDA Signal	Standard mode	20 + 0.1 C_B	300	ns
		Fast mode	20 + 0.1 C_B	300	ns
		Fast mode plus		120	ns
		High-speed mode, C_B – 100 pF max	10	80	ns
		High-speed mode, C_B – 400 pF max	20	160	ns
$t_{SU,}$ t_{STO}	Setup Time of STOP Condition	Standard mode	4		µs
		Fast mode	600		ns
		Fast mode plus	260		ns
		High-Speed mode	160		ns
C_B	Capacitive Load for SDA and SCL	Standard mode		400	pF
		Fast mode		400	pF
		Fast mode plus		550	pF
		High-Speed mode		400	pF

I^{2}C TIMING DIAGRAMS

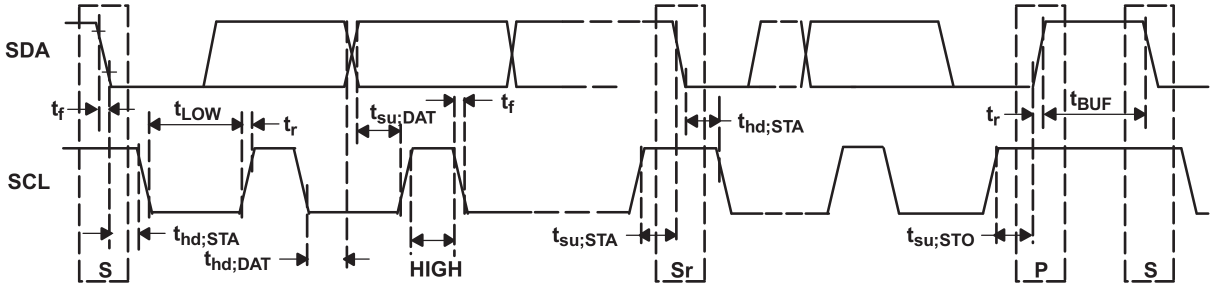
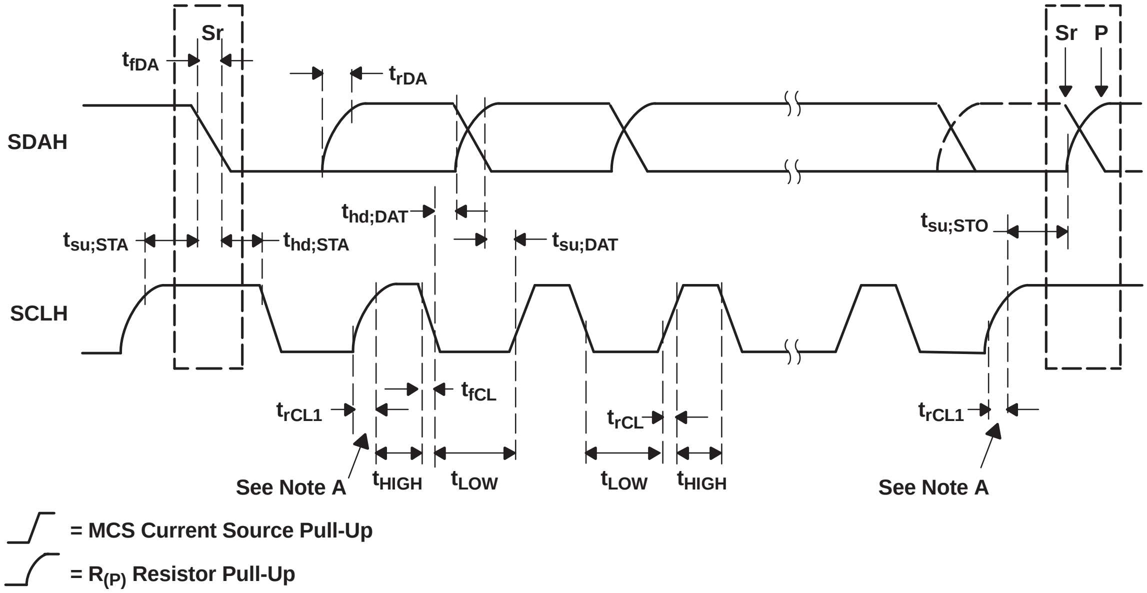


Figure 3. Serial Interface Timing Diagram for Standard-, Fast-, Fast-Mode Plus

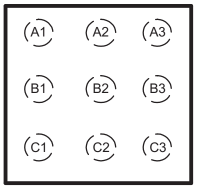


Note A: First rising edge of the SCLH signal after Sr and after each acknowledge bit.

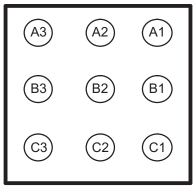
Figure 4. Serial Interface Timing Diagram for HS-Mode

PIN ASSIGNMENTS

TPS6265x
CSP−9
(TOP VIEW)



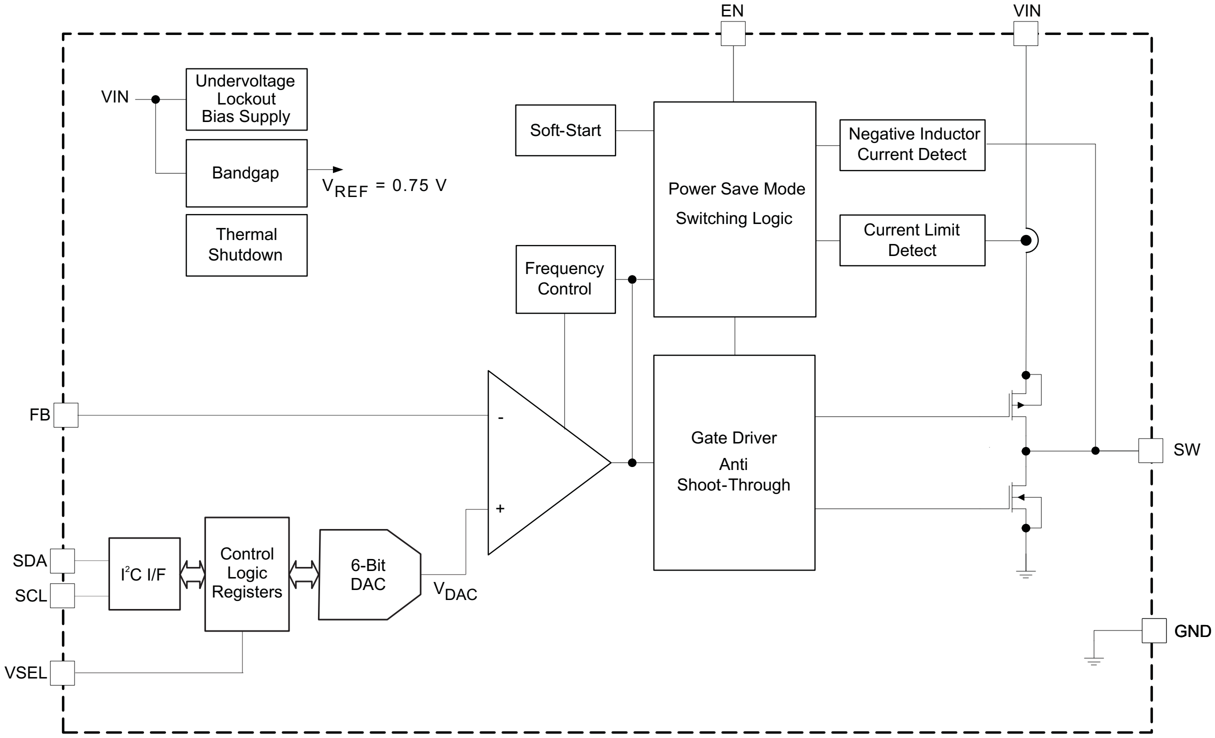
TPS6265x
CSP−9
(BOTTOM VIEW)



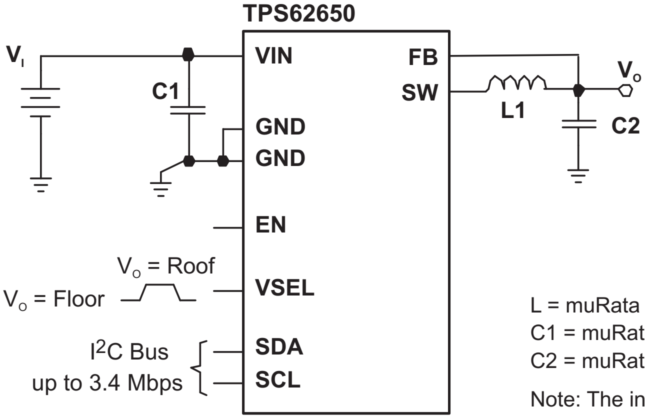
TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
VIN	A2	I	This is the input voltage pin of the device. Connect directly to the input bypass capacitor.
EN	B3	I	This is the enable pin of the device. Connect this pin to ground forces the device into shutdown mode. Pulling this pin to V_I enables the device. On the rising edge of the enable pin, all the registers are reset with their default values. This pin must not be left floating and must be terminated.
VSEL	A1	I	VSEL signal is primarily used to scale the output voltage and to set the TPS6265x operation between active mode (VSEL=HIGH) and sleep mode (VSEL=LOW). The mode of operation can also be adapted by I^2C settings. This pin must not be left floating and must be terminated.
SDA	A3	I/O	Serial interface address/data line.
SCL	B2	I	Serial interface clock line.
FB	C1	I	Output feedback sense input. Connect FB to the converter output.
GND	C2, C3		Ground.
SW	B1	I/O	This is the switch pin of the converter and connected to the drain of the internal power MOSFETs.

FUNCTIONAL BLOCK DIAGRAM



PARAMETER MEASUREMENT INFORMATION



L = muRata LQM21PN1R0NGR
C1 = muRata GRM155R60J475M (4.7µF, 6.3V, 0402, X5R)
C2 = muRata GRM155R60J475M (4.7µF, 6.3V, 0402, X5R)

Note: The internal registers are set to their default values

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
η	Efficiency	vs Output current	5, 6, 7, 8
		vs Input voltage	9
	Peak-to-peak output ripple voltage	vs Output Current	10, 11, 12, 13
V_O	DC output voltage	vs Output current	14, 15, 16, 17
		vs Ambient temperature	18, 19
	Measured output voltage	vs DAC target output voltage	20
	PFM/PWM Boundaries		21
I_Q	Quiescent current	vs Input voltage	22
I_{SD}	Shutdown current	vs Input voltage	23
f_S	Switching frequency	vs Input voltage	24
$r_{DS(on)}$	P-channel MOSFET $r_{DS(on)}$	vs Input voltage	25
	N-channel MOSFET $r_{DS(on)}$	vs Input voltage	26
	Load transient response		27 - 38
	Line transient PWM operation		39
	Combined line and load transient response		40
	PWM operation		41
	Power-save mode operation		42
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	Output voltage ramp control		45
	Start-up		46, 47

TYPICAL CHARACTERISTICS (continued)

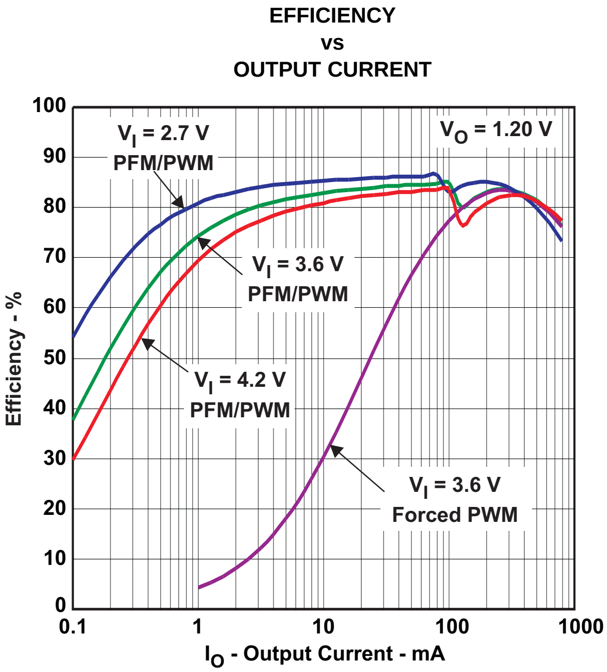


Figure 5.

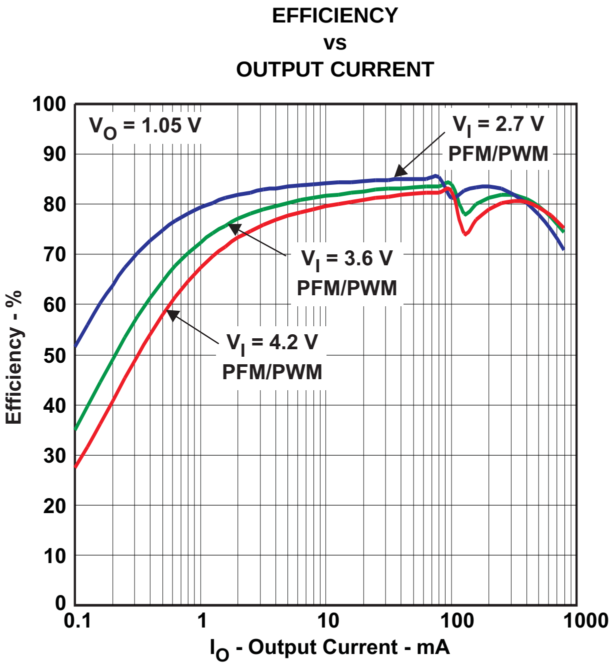


Figure 6.

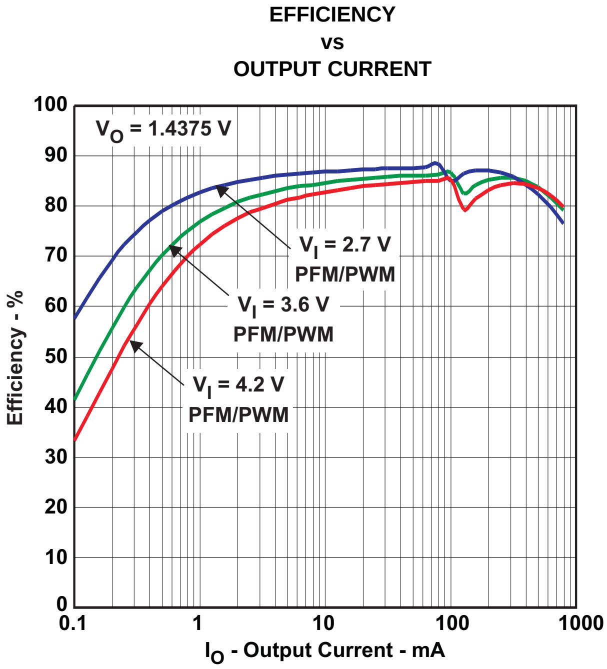


Figure 7.

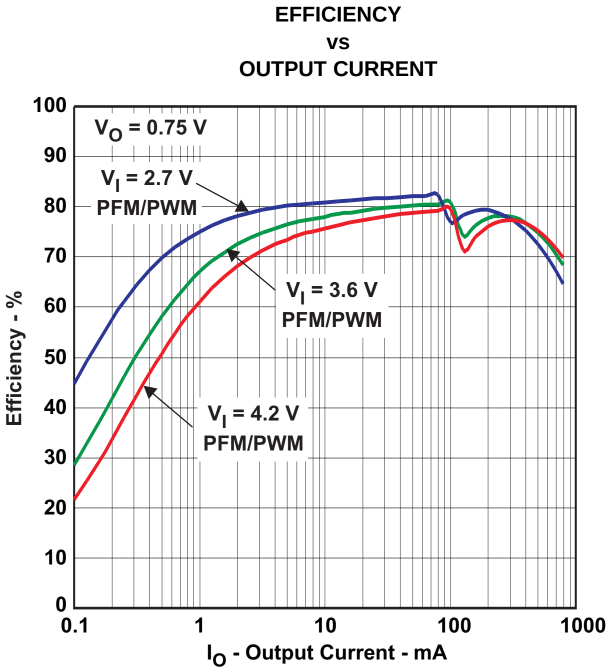


Figure 8.

TYPICAL CHARACTERISTICS (continued)

EFFICIENCY
vs
INPUT VOLTAGE

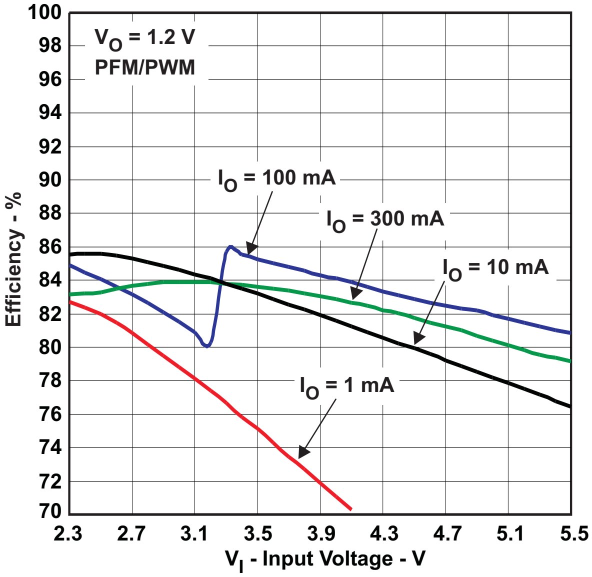


Figure 9.

PEAK-TO-PEAK OUTPUT RIPPLE VOLTAGE
vs
OUTPUT CURRENT

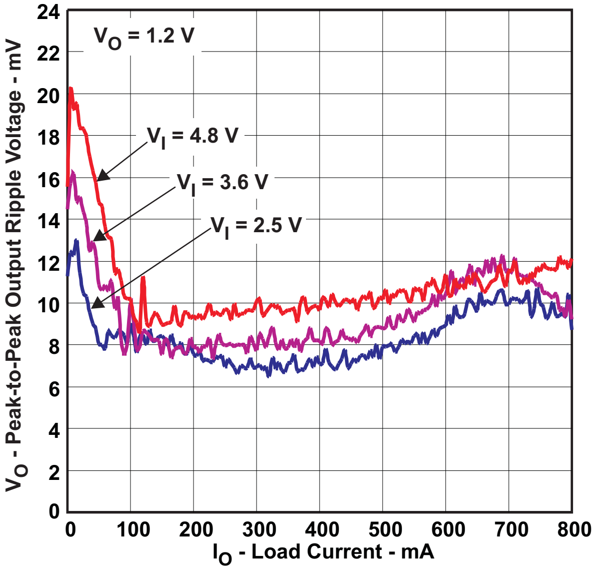


Figure 10.

PEAK-TO-PEAK OUTPUT RIPPLE VOLTAGE
vs
OUTPUT CURRENT

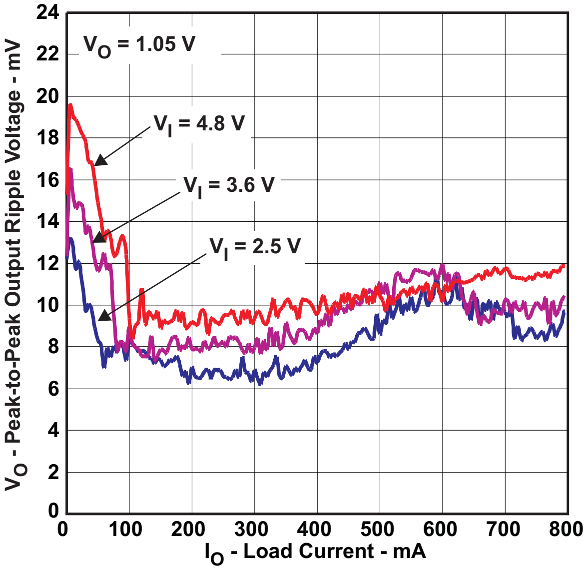


Figure 11.

PEAK-TO-PEAK OUTPUT RIPPLE VOLTAGE
vs
OUTPUT CURRENT

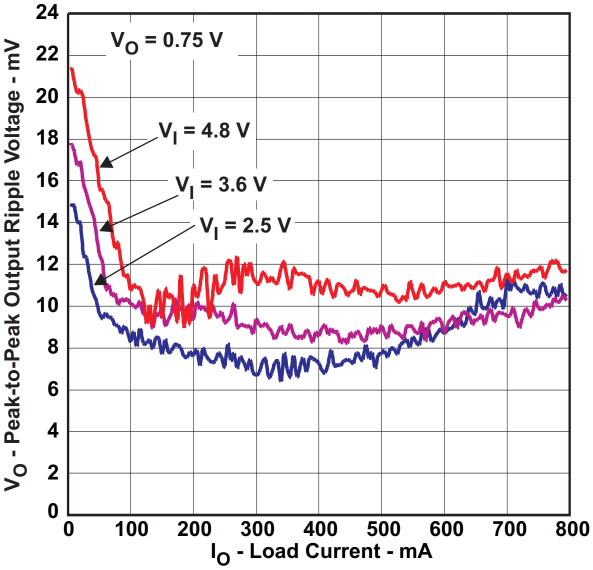


Figure 12.

TYPICAL CHARACTERISTICS (continued)

PEAK-TO-PEAK OUTPUT RIPPLE VOLTAGE
vs
OUTPUT CURRENT

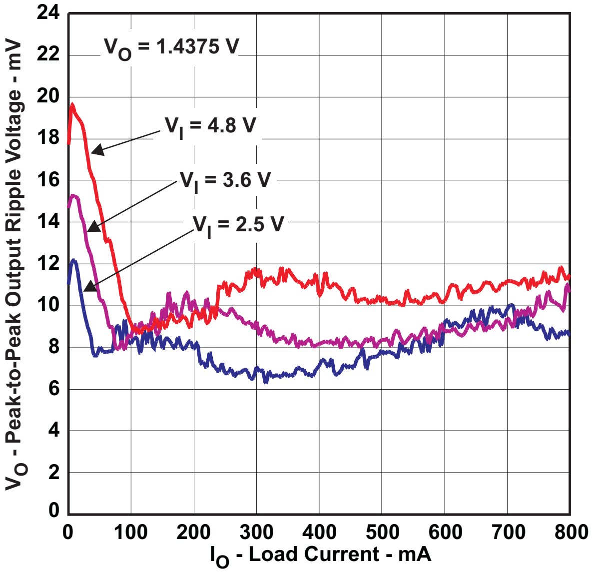


Figure 13.

DC OUTPUT VOLTAGE
vs
OUTPUT CURRENT

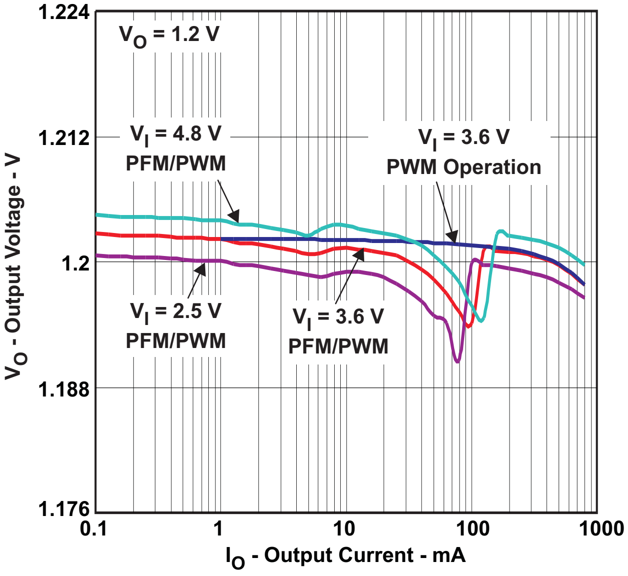


Figure 14.

DC OUTPUT VOLTAGE
vs
OUTPUT CURRENT

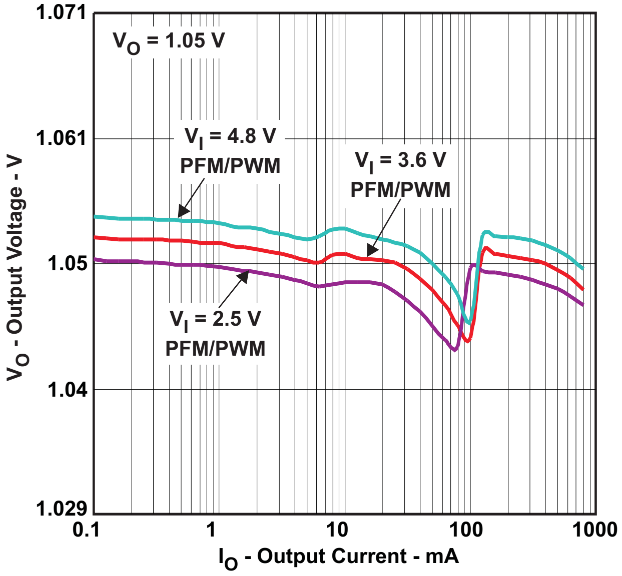


Figure 15.

DC OUTPUT VOLTAGE
vs
OUTPUT CURRENT

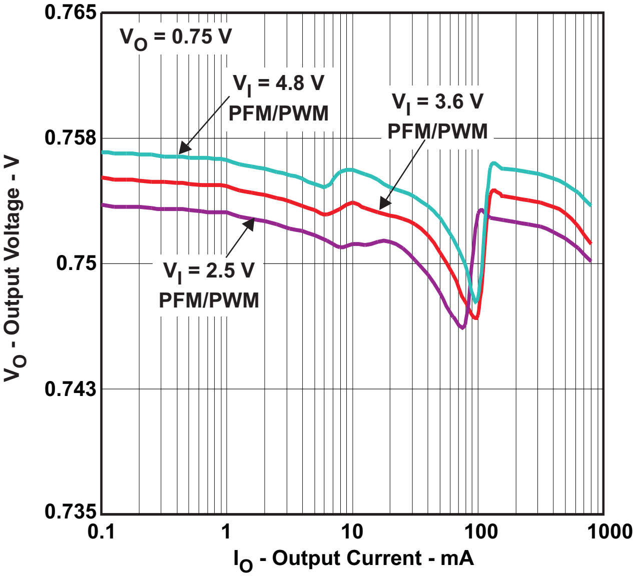


Figure 16.

TYPICAL CHARACTERISTICS (continued)

DC OUTPUT VOLTAGE
vs
OUTPUT CURRENT

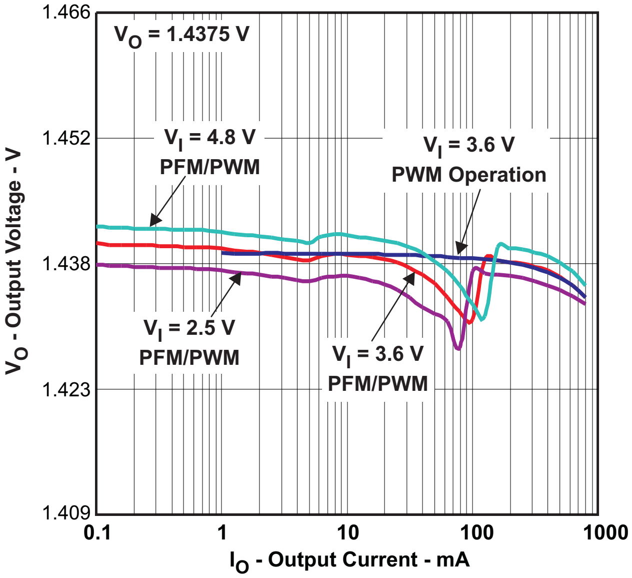


Figure 17.

DC OUTPUT VOLTAGE
vs
AMBIENT TEMPERATURE

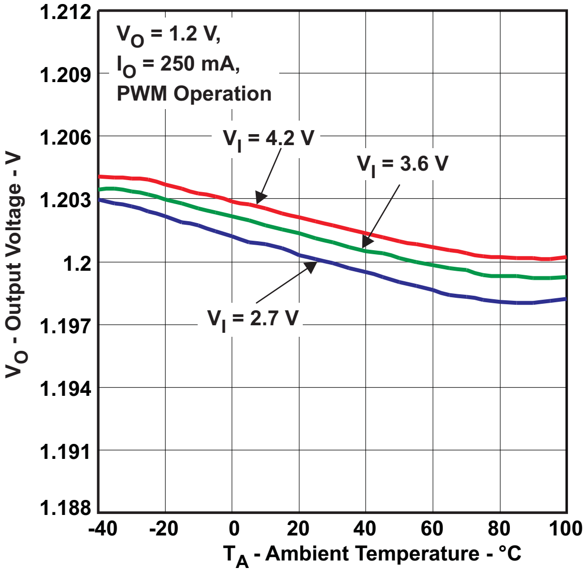


Figure 18.

DC OUTPUT VOLTAGE
vs
AMBIENT TEMPERATURE

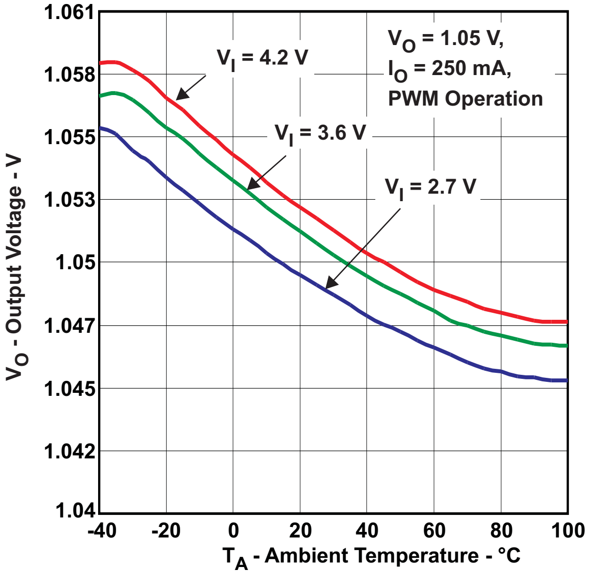


Figure 19.

MEASURED OUTPUT VOLTAGE
vs
DAC TARGET OUTPUT VOLTAGE

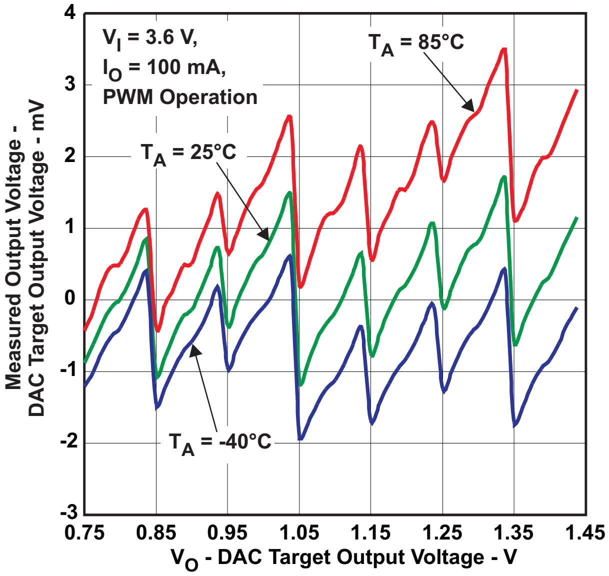


Figure 20.

TYPICAL CHARACTERISTICS (continued)

PFM/PWM BOUNDARIES

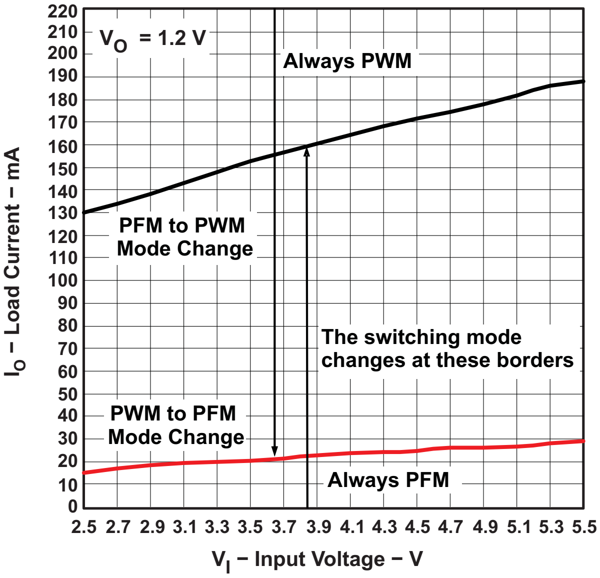


Figure 21.

QUIESCENT CURRENT vs INPUT VOLTAGE

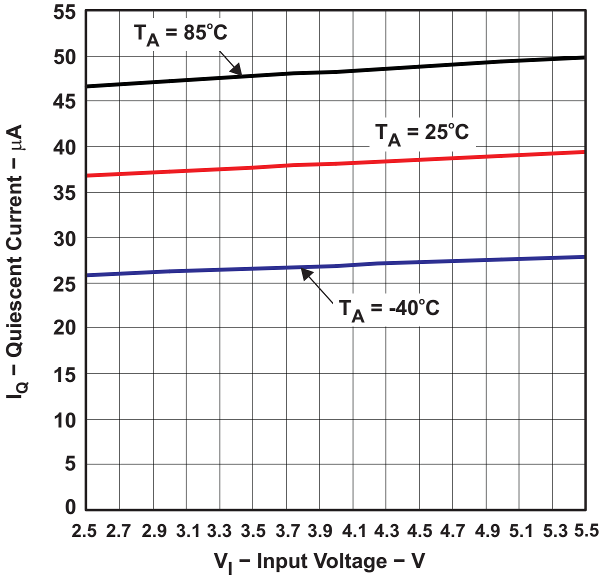


Figure 22.

SHUTDOWN CURRENT vs INPUT VOLTAGE

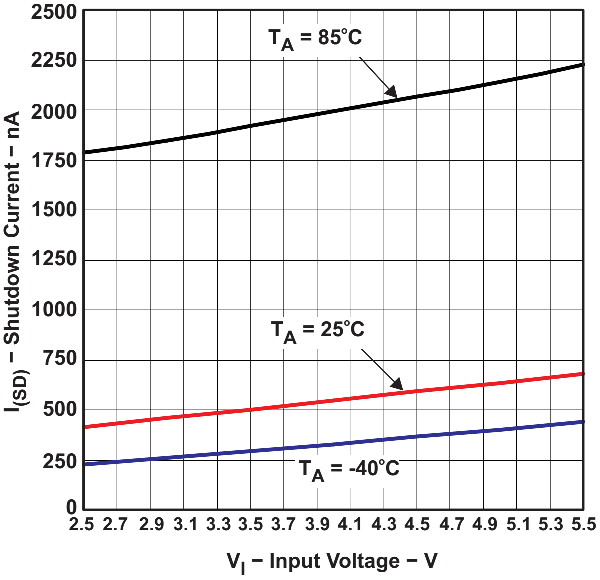


Figure 23.

SWITCHING FREQUENCY vs INPUT VOLTAGE

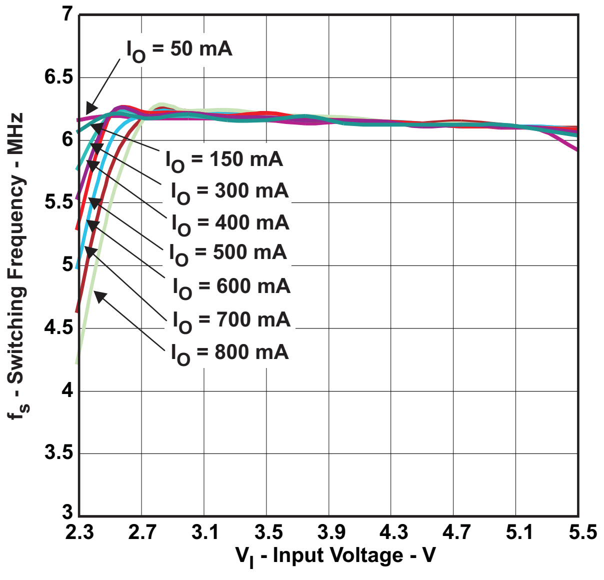


Figure 24.

TYPICAL CHARACTERISTICS (continued)

$r_{DS(on)}$ P-MOSFET vs INPUT VOLTAGE

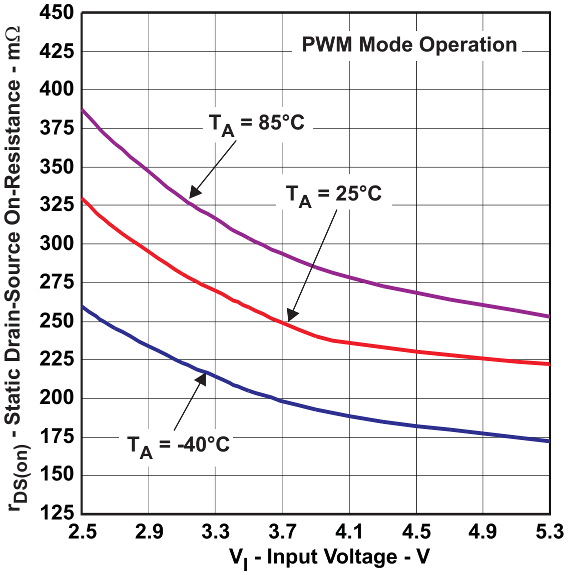


Figure 25.

$r_{DS(on)}$ N-MOSFET vs INPUT VOLTAGE

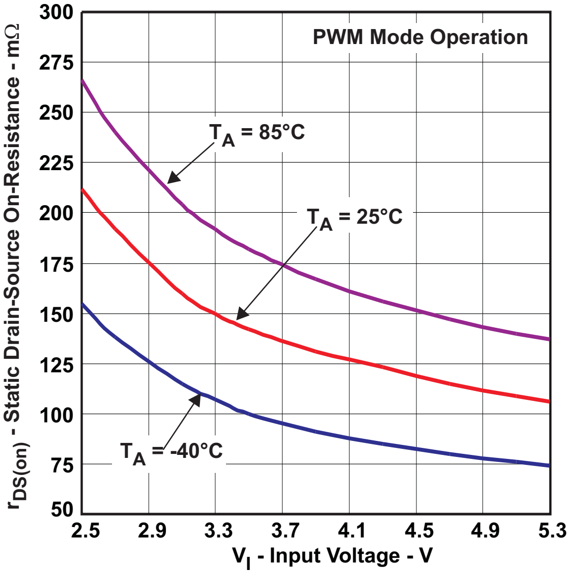


Figure 26.

LOAD TRANSIENT: 50 mA / 400 mA / 50 mA PWM OPERATION

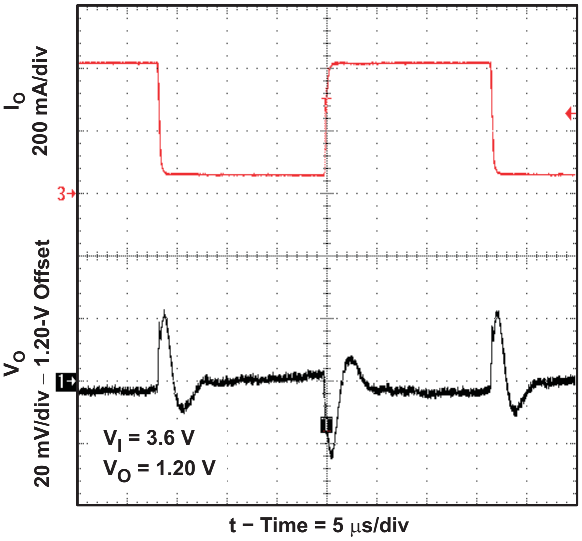


Figure 27.

LOAD TRANSIENT: 50 mA / 400 mA PWM OPERATION

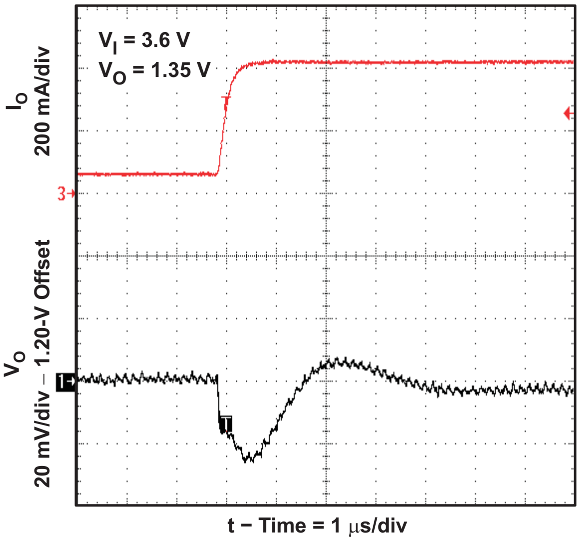


Figure 28.

TYPICAL CHARACTERISTICS (continued)

LOAD TRANSIENT: 400 mA / 50 mA PWM OPERATION

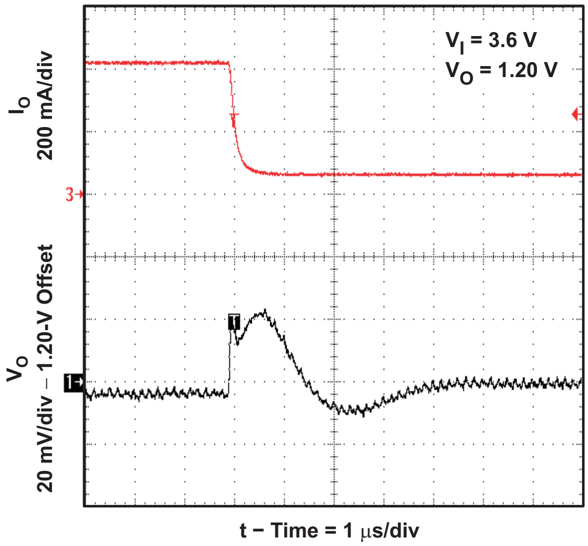


Figure 29.

LOAD TRANSIENT: 50 mA / 400 mA / 50 mA PFM/PWM OPERATION

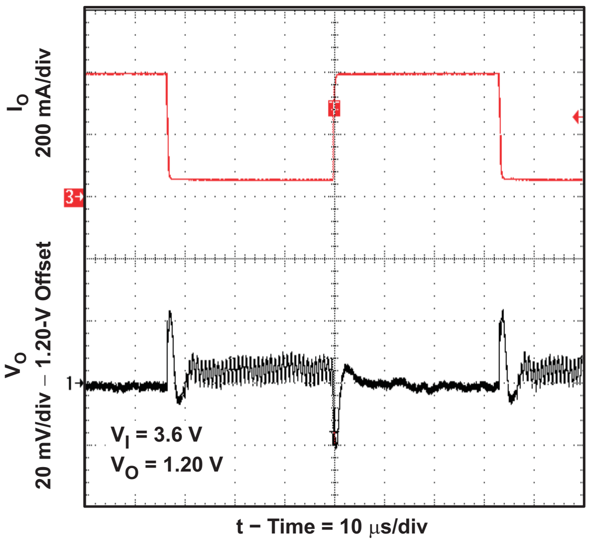


Figure 30.

LOAD TRANSIENT: 50 mA / 400 mA PFM/PWM OPERATION

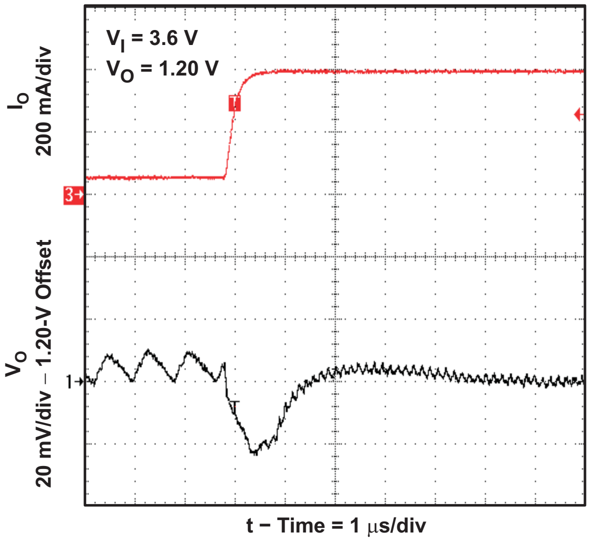


Figure 31.

LOAD TRANSIENT: 400 mA / 50 mA PFM/PWM OPERATION

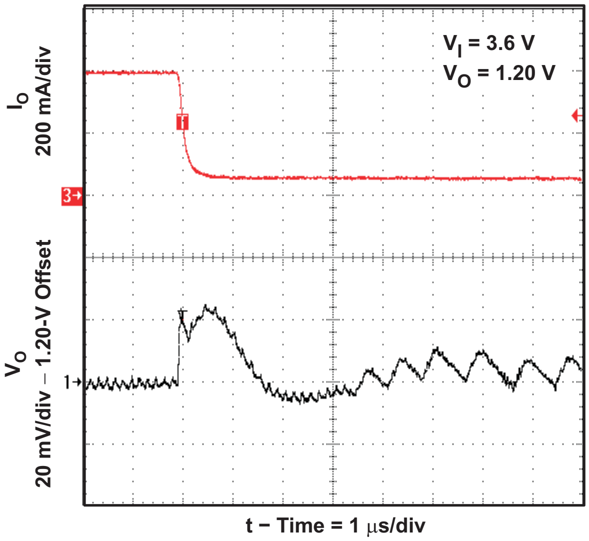


Figure 32.

TYPICAL CHARACTERISTICS (continued)

LOAD TRANSIENT: 400 mA / 750 mA / 400 mA
PWM OPERATION

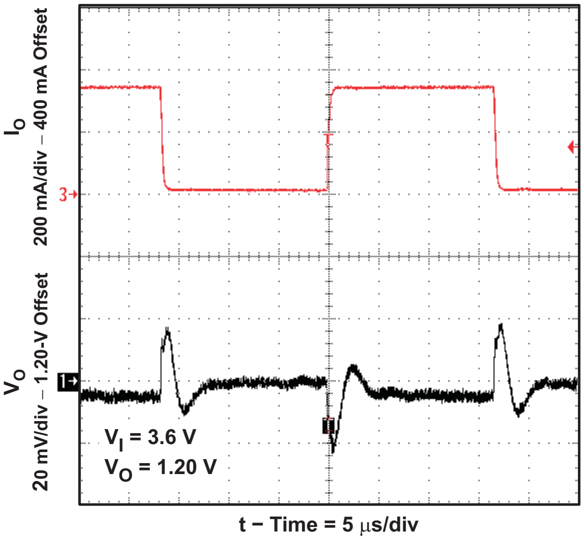


Figure 33.

LOAD TRANSIENT: 400 mA / 750 mA
PWM OPERATION

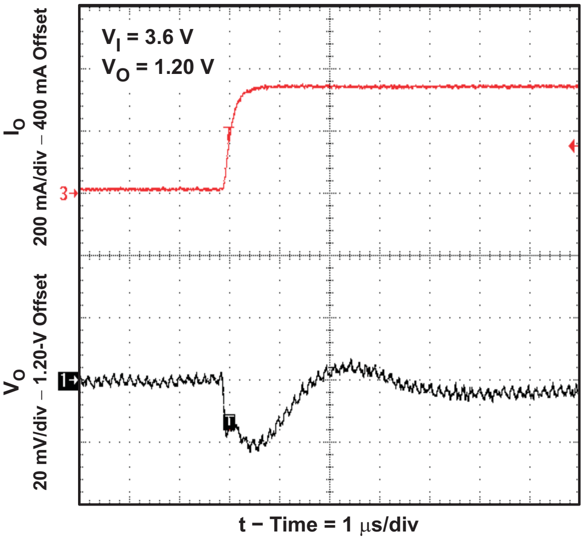


Figure 34.

LOAD TRANSIENT: 750 mA / 400 mA
PWM OPERATION

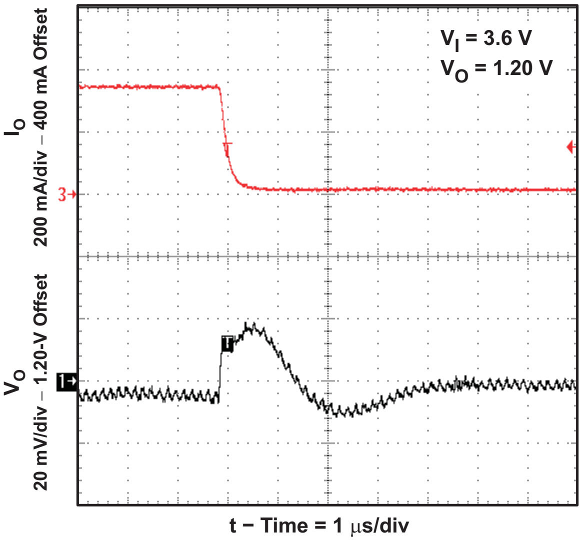


Figure 35.

LOAD TRANSIENT: 5 mA / 100 mA / 5 mA
PFM/PWM OPERATION

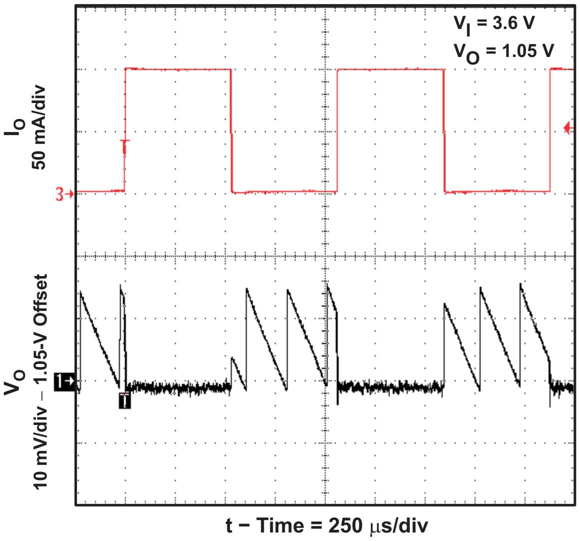


Figure 36.

TYPICAL CHARACTERISTICS (continued)

LOAD TRANSIENT: 5 mA / 100 mA
PFM/PWM OPERATION

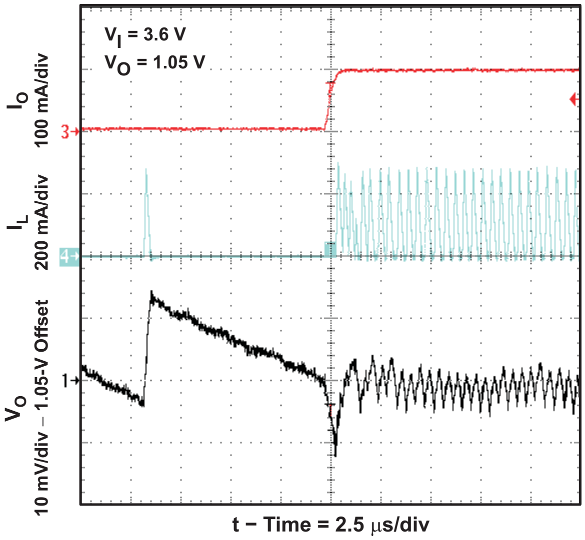


Figure 37.

LOAD TRANSIENT: 100 mA / 5 mA
PFM/PWM OPERATION

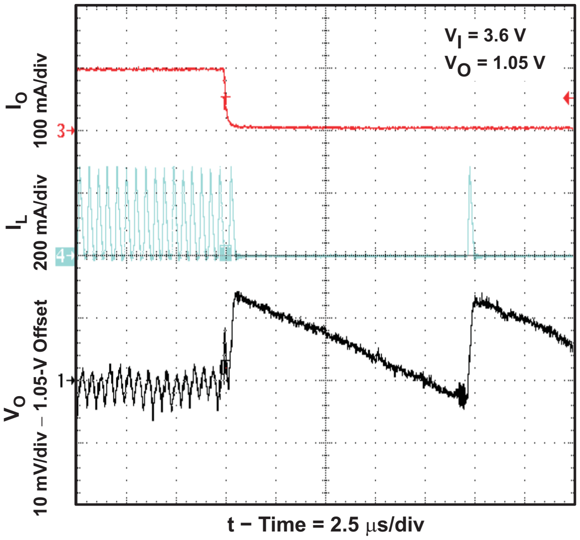


Figure 38.

LINE TRANSIENT
PWM OPERATION

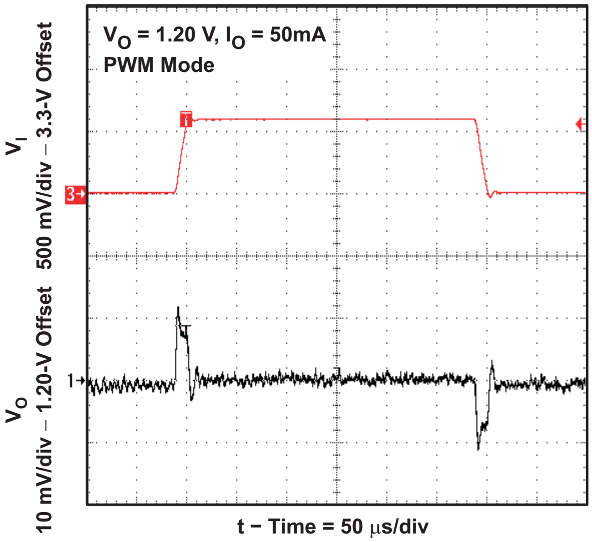


Figure 39.

COMBINED LINE/LOAD TRANSIENT
(3.3 V TO 3.9 V, 400 mA TO 800 mA)
PWM OPERATION

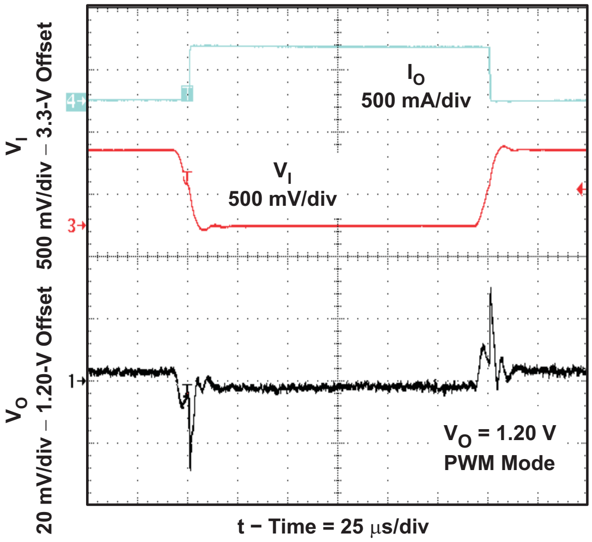


Figure 40.

TYPICAL CHARACTERISTICS (continued)

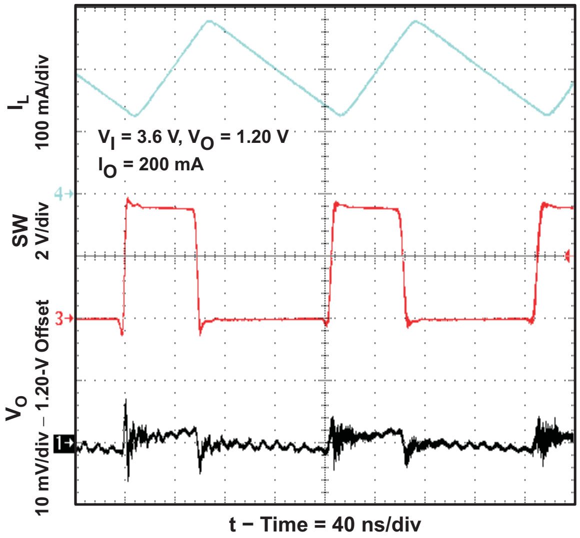

PWM OPERATION

Figure 41.

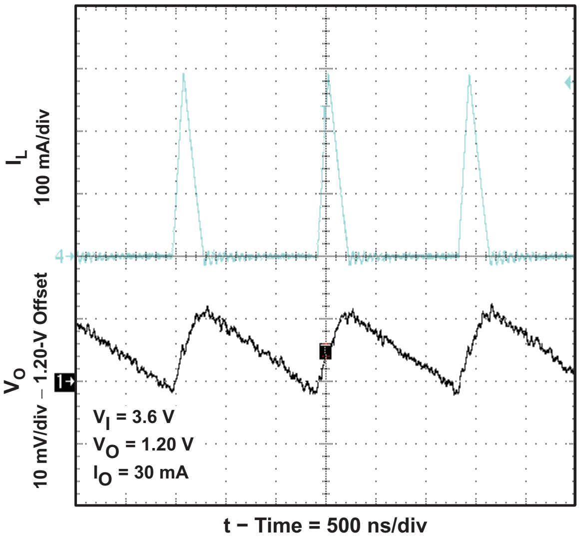

POWER SAVE MODE OPERATION

Figure 42.

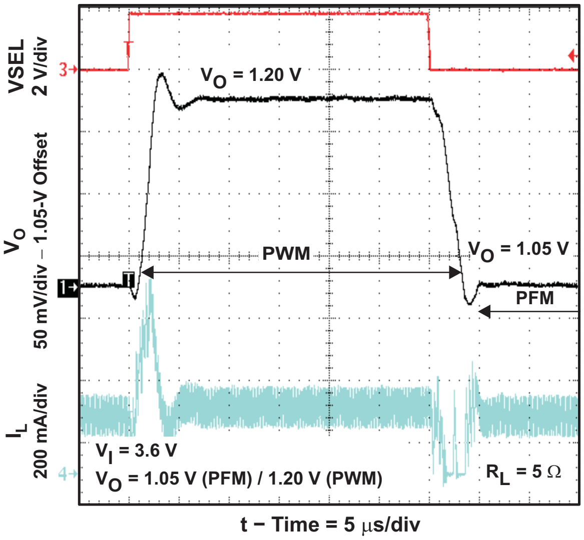

DYNAMIC VOLTAGE MANAGEMENT

Figure 43.

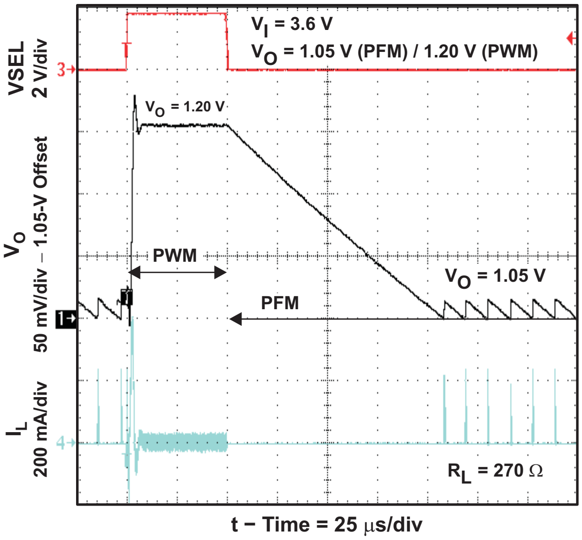

DYNAMIC VOLTAGE MANAGEMENT

Figure 44.

TYPICAL CHARACTERISTICS (continued)

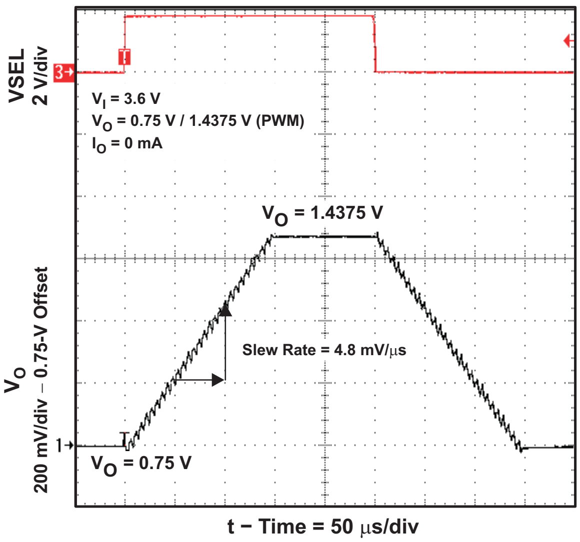

OUTPUT VOLTAGE RAMP CONTROL

Figure 45.

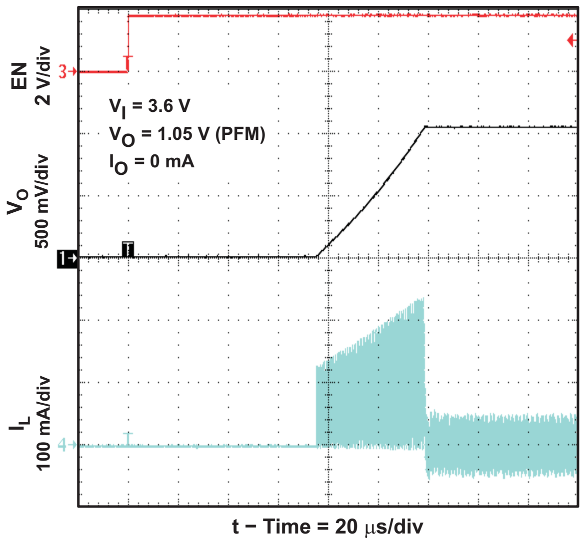

START UP

Figure 46.

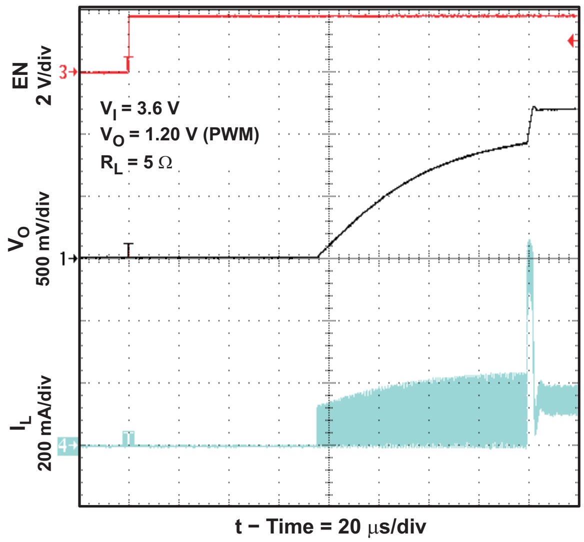

START UP

Figure 47.

DETAILED DESCRIPTION

Operation

The TPS6265x is a synchronous step-down converter typically operates at a regulated 6-MHz frequency pulse width modulation (PWM) at moderate to heavy load currents. At light load currents, the TPS6265x converter operates in power-save mode with pulse frequency modulation (PFM) and automatic transition into PWM operation when the load current increases.

The TPS6265x integrates an I^2C compatible interface allowing transfers up to 3.4 Mbps. This communication interface can be used for dynamic voltage scaling with voltage steps down to 12.5 mV, for reprogramming the mode of operation (PFM or forced PWM) or disable/enabling the output voltage for instance. For more details, see the I^2C interface and register description section.

The converter uses a unique frequency locked ring oscillating modulator to achieve *best-in-class* load and line response and allows the use of tiny inductors and small ceramic input and output capacitors. At the beginning of each switching cycle, the P-channel MOSFET switch is turned on and the inductor current ramps up rising the output voltage until the main comparator trips, then the control logic turns off the switch.

One key advantage of the non-linear architecture is that there is no traditional feed-back loop. The loop response to change in V_O is essentially instantaneous, which explains its extraordinary transient response. The absence of a traditional, high-gain compensated linear loop means that the TPS6265x is inherently stable over a range of small L and C_O.

Although this type of operation normally results in a switching frequency that varies with input voltage and load current, an internal frequency lock loop (FLL) holds the switching frequency constant over a large range of operating conditions.

Combined with *best in class* load and line transient response characteristics, the low quiescent current of the device (ca. 38µA) allows to maintain high efficiency at light load, while preserving fast transient response for applications requiring tight output regulation.

SWITCHING FREQUENCY

The magnitude of the internal ramp, which is generated from the duty cycle, reduces for duty cycles either set of 50%. Thus, there is less overdrive on the main comparator inputs which tends to slow the conversion down. The intrinsic maximum operating frequency of the converter is about 10MHz to 12MHz, which is controlled to circa. 6MHz by a frequency locked loop.

When high or low duty cycles are encountered, the loop runs out of range and the conversion frequency falls below 6MHz. The tendency is for the converter to operate more towards a "constant inductor peak current" rather than a "constant frequency". In addition to this behavior which is observed at high duty cycles, it is also noted at low duty cycles.

When the converter is required to operate towards the 6MHz nominal at extreme duty cycles, the application can be assisted by decreasing the ratio of inductance (L) to the output capacitor's equivalent serial inductance (ESL). This increases the *ESL step* seen at the main comparator's feed-back input thus decreasing its propagation delay, hence increasing the switching frequency.

POWER-SAVE MODE

If the load current decreases, the converter will enter Power Save Mode operation automatically. During power-save mode the converter operates in discontinous current (DCM) single-pulse PFM mode, which produces low output ripple compared with other PFM architectures.

When in power-save mode, the converter resumes its operation when the output voltage trips below the nominal voltage. It ramps up the output voltage with a minimum of one pulse and goes into power-save mode when the inductor current has returned to a zero steady state. The PFN on-time varies inversely proportional to the input voltage and proportional to the output voltage giving the regulated switching frequency when is steady-state.

PFM mode is left and PWM operation is entered as the output current can no longer be supported in PFM mode. As a consequence, the DC output voltage is typically positioned ca 0.5% above the nominal output voltage and the transition between PFM and PWM is seamless.

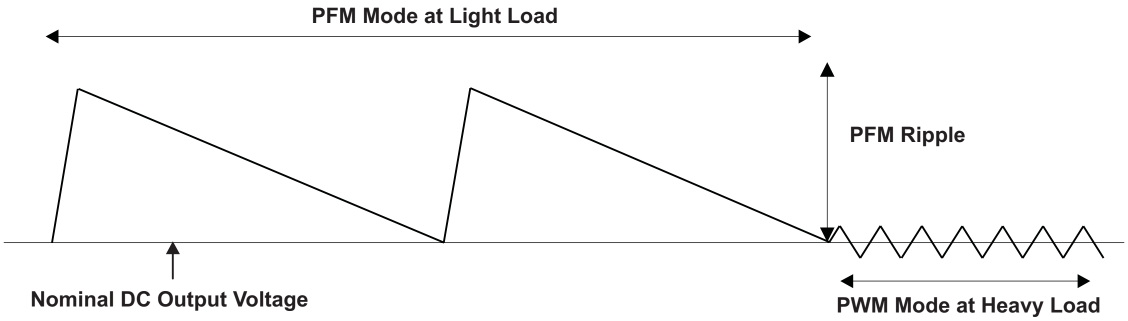


Figure 48. Operation in PFM Mode and Transfer to PWM Mode

MODE SELECTION

Depending on the settings of CONTROL1 register the device can be operated in either the regulated frequency PWM mode or in the automatic PWM and power-save mode. In this mode, the converter operates in a regulated frequency PWM mode at moderate to heavy loads and in the PFM mode during light loads, which maintains high efficiency over a wide load current range. For more details, see the CONTROL1 register description.

The regulated frequency PWM mode has the tightest regulation and the best line/load transient performance. Furthermore, this mode of operation allows simple filtering of the switching frequency for noise-sensitive applications. In forced PWM mode, the efficiency is lower compared to the power-save mode during light loads.

It is possible to switch from power-save mode (PFM) to forced PWM mode during operation either via the VSEL signal or by re-programming the CONTROL1 register. This allows adjustments to the converters operation to match the specific system requirements leading to more efficient and flexible power management.

ENABLE

The device starts operation when EN pin is set high and starts up with the soft start. This signal is gated by the EN_DCDC bit defined in register VSEL0 and VSEL1. On rising edge of the EN pin, all the registers are reset with their default values. Enabling the converter's operation via the EN_DCDC bit does not affect internal register settings. This allows the output voltage to be programmed to other values than the default voltage before starting up the converter. For more details, see the *VSEL0/1* register description.

Pulling the EN pin, VSEL0[6] bit or VSEL1[6] bit low forces the device into shutdown, with a shutdown current as defined in the electrical characteristics table. In this mode, the P and N-channel MOSFETs are turned off, the internal resistor feedback divider is disconnected, and the entire internal-control circuitry is switched off. For proper operation, the EN pin must be terminated and must not be left floating.

In addition, depending on the setting of CONTROL2[6] bit, the device can actively discharge the output capacitor when it turns off. The integrated discharge resistor has a typical resistance of 15 Ω. The required time to discharge the output capacitor at V_O depends on load current and the output capacitance value.

SOFT START

The TPS6265x has an internal soft-start circuit that limits the inrush current during start-up. This limits input voltage drops when a battery or a high-impedance power source is connected to the input of the converter.

The soft-start system progressively increases the on-time from a minimum pulse-width of 35ns as a function of the output voltage. This mode of operation continues for c.a. 100μs after enable. Should the output voltage not have reached its target value by this time, such as in the case of heavy load, the soft-start transitions to a second mode of operation.

The converter will then operate in a current limit mode, specifically the P-MOS current limit is set to half the nominal limit and the N-channel MOSET remains on until the inductor current has reset. After a further 100 μs, the device ramps up to full current limit operation providing that the output voltage has risen above 0.5V (approximately). Therefore, the start-up time depends on the output capacitor and load current.

UNDERVOLTAGE LOCKOUT

The undervoltage lockout circuit prevents the device from misoperation at low input voltages. It prevents the converter from turning on the switch or rectifier MOSFET under undefined conditions. The TPS6265x device have a UVLO threshold set to 2.05V (typical). Fully functional operation is permitted down to 2.15 V input voltage.

SHORT-CIRCUIT PROTECTION

The TPS6265x integrates a P-channel MOSFET current limit to protect the device against heavy load or short circuits. When the current in the P-channel MOSFET reaches its current limit, the P-channel MOSFET is turned off and the N-channel MOSFET is turned on. The regulator continues to limit the current on a cycle-by-cycle basis.

As soon as the output voltage falls below ca. 0.4V, the converter current limit is reduced to half of the nominal value and the PWROK bit is reset. Because the short-circuit protection is enabled during start-up, the device does not deliver more than half of its nominal current limit until the output voltage exceeds approximately 0.5V. This needs to be considered when a load acting as a current sink is connected to the output of the converter.

THERMAL SHUTDOWN

As soon as the junction temperature, T_J, exceeds typically 140°C, the device goes into thermal shutdown. In this mode, the P- and N-channel MOSFETs are turned off. The device continues its operation when the junction temperature again falls below typically 130°C.

VOLTAGE AND MODE SELECTION

The TPS6265x features a pin-selectable output voltage. VSEL is primarily used to scale the output voltage between active (VSEL = HIGH) and sleep mode (VSEL = LOW). For maximum flexibility, it is possible to reprogram the operating mode of the converter (e.g. forced PWM, or auto transition PFM/PWM) associated with VSEL signal via the I^2C interface

VSEL output voltage and mode selection is defined as following:

VSEL = LOW: — DC/DC output voltage determined by VSEL0 register value. DC/DC mode of operation is determined by MODE0 bit in CONTROL1 register.

VSEL = HIGH: — DC/DC output voltage determined by VSEL1 register value. DC/DC mode of operation is determined by MODE1 bit in CONTROL1 register.

The application processor programs via I^2C the output voltages associated with the two states of VSEL signal: floor (VSEL0) and roof (VSEL1) values. The application processor also writes the DEFSLEW value in the CONTROL2 register to control the output voltage ramp rate.

These two registers can be continuously updated via I^2C to provide the appropriate output voltage according to the VSEL input. The voltage changes with the selected ramp rate immediately after writing to the VSEL0 or VSEL1 register.

Table 1 shows the output voltage states depending on VSEL0, VSEL1 registers, and VSEL signal.

Table 1. Dynamic Voltage Scaling Functional Overview

VSEL PIN	VSEL0 REGISTER	VSEL1 REGISTER	OUTPUT VOLTAGE
Low	No action	No action	Floor
Low	Write new value	No action	Change to new value
Low	No action	Write	No change stays at floor voltage
High	No action	No action	Roof
High	Write new value	No action	No change stays at roof voltage
High	No action	Write new value	Change to new value

In PFM mode, when the output voltage is programmed to a lower value by toggling VSEL signal from high to low, PWROK is defined as low, while the output capacitor is discharged by the load until the converter starts pulsing to maintain the voltage within regulation. In multiple-step mode, PWROK is defined as low while the output voltage is ramping up or down.

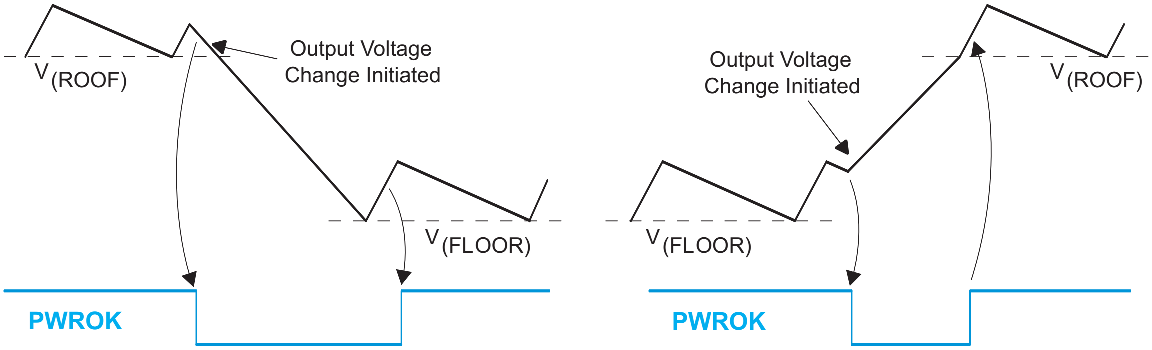


Figure 49. PWROK Functional Behavior

VOLTAGE RAMP CONTROL

The TPS6265x offers a voltage ramp rate control that can operate in two different modes:

- Multiple-Step Mode
- Single-Step Mode

The mode is selected via DEFSLEW control bits in the CONTROL2 register.

Single-Step Voltage Scaling Mode (default), DEFSLEW[2:0] = [111]

In single-step mode, the TPS6265x ramps the output voltage with maximum slew-rate when transitioning between the floor and the roof voltages (switch to a higher voltage).

When switching between the roof and the floor voltages (transition to a lower voltage), the ramp rate control is dependent on the mode selection (see CONTROL1 register) associated with the target register (Forced PWM or auto transition PFM/PWM).

Table 2 shows the ramp rate control when transitioning to a lower voltage with DEFSLEW set to immediate transition.

Table 2. Ramp Rate Control vs. Target Mode

Mode Associated with Target Voltage	Output Voltage Ramp Rate
Forced PWM	Immediate
PFM/PWM	DC/DC converter stops switching. Time to ramp down depends on output capacitance and load current

For instance, when the output is programmed to transition to a lower voltage with PFM operation enabled, the TPS6265x ramps down the output voltage without controlling the ramp rate or having intermediate micro-steps. The required time to ramp down the voltage depends on the capacitance present at the output of the TPS6265x and on the load current. From an overall system perspective, this is the most efficient way to perform dynamic voltage scaling.

Multiple-Step Voltage Scaling Mode, DEFSLEW[2:0] = [000] to [110]

In multiple-step mode the TPS6265x controls the output voltage ramp rate regardless of the load current and mode of operation (e.g. Forced PWM or PFM/PWM). The voltage ramp control is done by adjusting the time between the voltage micro-steps.

THEORY OF OPERATION

Serial Interface Description

I^2C is a 2-wire serial interface developed by Philips Semiconductor (see I^2C-Bus Specification, Version 2.1, January 2000). The bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I^2C compatible devices connect to the I^2C bus through open drain I/O pins, SDA and SCL. A master device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A slave device receives and/or transmits data on the bus under control of the master device.

The TPS6265x device works as a slave and supports the following data transfer modes, as defined in the I^2C-Bus Specification: standard mode (100 kbps), fast mode (400 kbps), fast mode plus (1 Mbps) and high-speed mode (up to 3.4 Mbps). The interface adds flexibility to the power supply solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements. Register contents remain intact as long as supply voltage remains above 2.1 V (typical).

The data transfer protocol for standard, fast and fast plus modes is exactly the same, therefore, they are referred to as F/S-mode in this document. The protocol for high-speed mode is different from the F/S-mode, and it is referred to as HS-mode. The TPS6265x device supports 7-bit addressing; 10-bit addressing and general call address are not supported.

The TPS6265x device has a 7-bit address with two bits factory programmable allowing up to four dc/dc converters to be connected to the same bus. The 4 MSBs are *1001* and the LSB is *0*.

Standard-, Fast- and Fast-Mode Plus Protocol

The *master* initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, see Figure 50. All I^2C-compatible devices should recognize a start condition.

The master then generates the SCL pulses, and transmits the 7-bit address and the read/write direction bit R/W on the SDA line. During all transmissions, the master ensures that data is *valid*. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse, see Figure 51. All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an *acknowledge*, see Figure 52, by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge, the master knows that the communication link with a slave has been established.

The master generates further SCL cycles to either transmit data to the slave (R/W bit 1) or receive data from the slave (R/W bit 0). In either case, the receiver needs to acknowledge the data sent by the transmitter. An acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary.

To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low to high while the SCL line is high, see Figure 50. This releases the bus and stops the communication link with the addressed slave. All I^2C compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released, and they wait for a start condition followed by a matching address

Attempting to read data from register addresses not listed in this section results in 00h being read out.

H/S-Mode Protocol

When the bus is idle, both SDA and SCL lines are pulled high by the pull-up devices.

The master generates a start condition followed by a valid serial byte containing HS master code 00001XXX. This transmission is made in F/S-mode at no more than 400 Kbps. No device is allowed to acknowledge the HS master code, but all devices must recognize it and switch their internal setting to support 3.4-Mbps operation.

The master then generates a repeated start condition (a repeated start condition has the same timing as the start condition). After this repeated start condition, the protocol is the same as F/S-mode, except that transmission speeds up to 3.4 Mbps are allowed. A stop condition ends the HS-mode and switches all the internal settings of the slave devices to support the F/S-mode. Instead of using a stop condition, repeated start conditions are used to secure the bus in HS-mode.

Attempting to read data from register addresses not listed in this section results in FFh being read out.

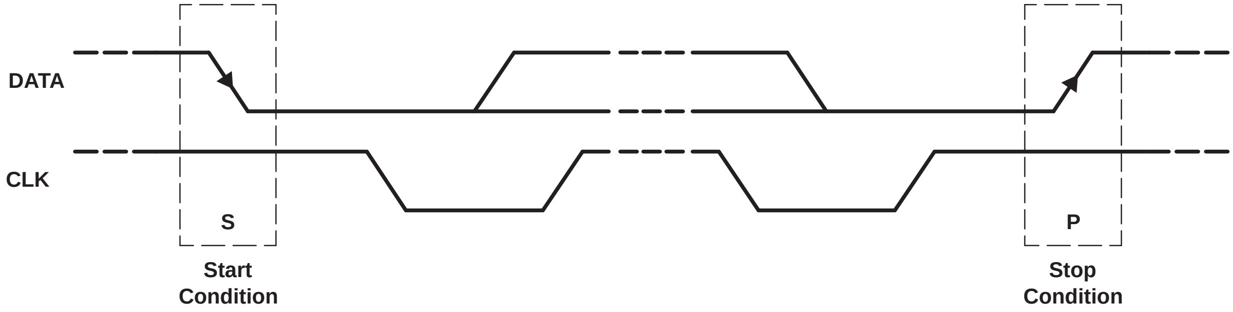


Figure 50. START and STOP Conditions

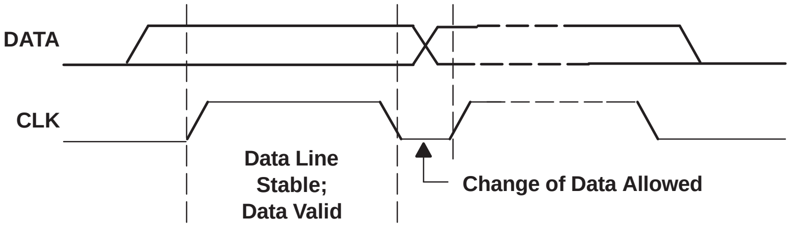


Figure 51. Bit Transfer on the Serial Interface

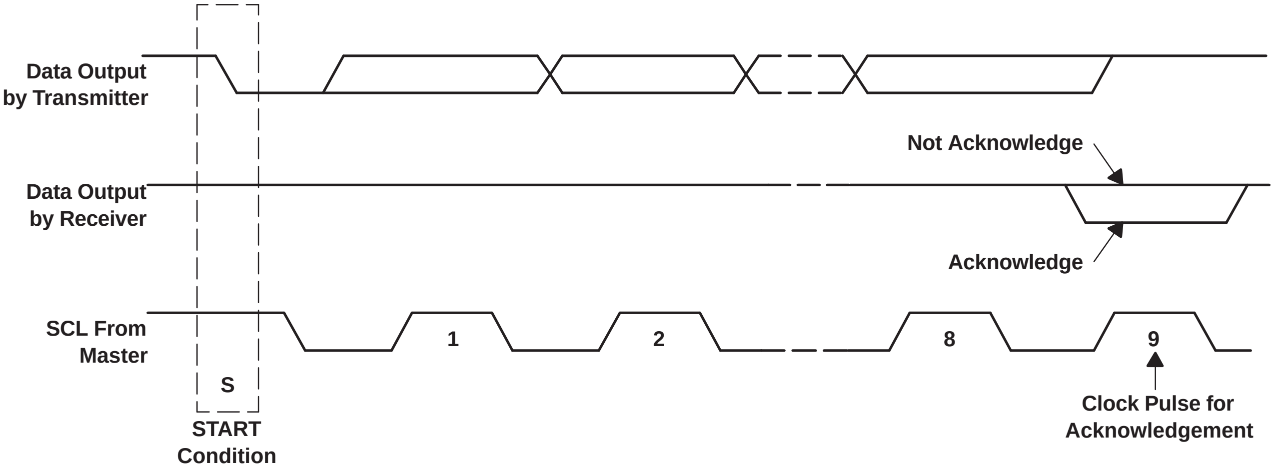


Figure 52. Acknowledge on the I^2C Bus

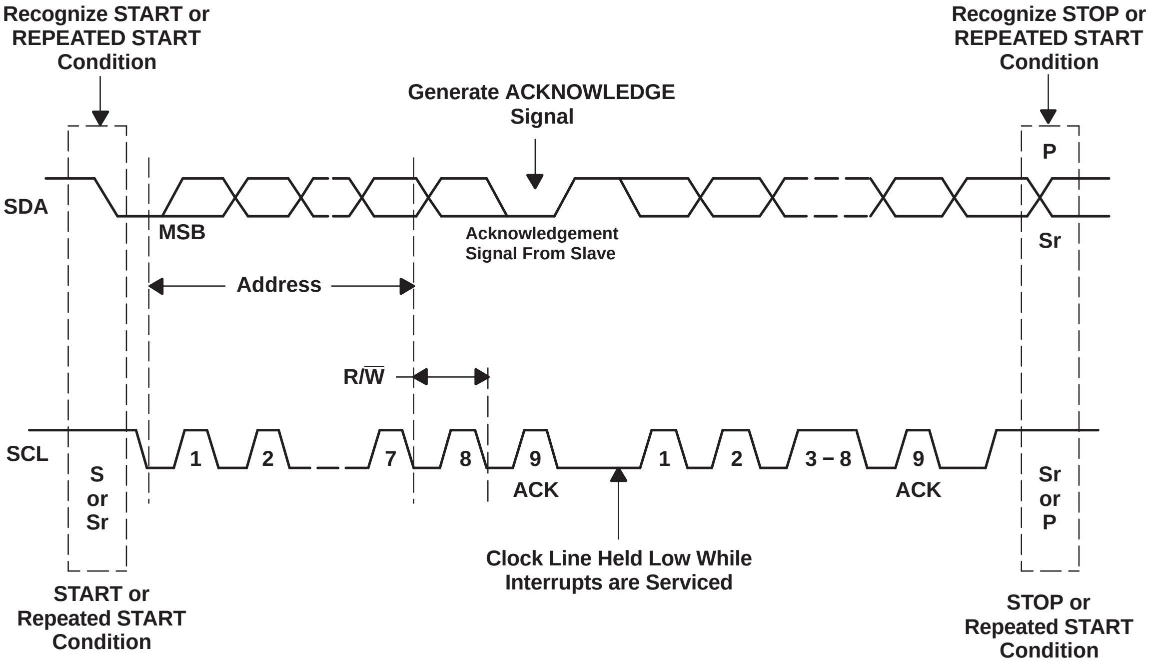


Figure 53. Bus Protocol

TPS6265X I^{2}C Update Sequence

The TPS6265x requires a start condition, a valid I^{2}C address, a register address byte, and a data byte for a single update. After the receipt of each byte, TPS6265x device acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I^{2}C address selects the TPS6265x. TPS6265x performs an update on the falling edge of the LSB byte.

When the TPS6265x is in hardware shutdown (EN pin tied to ground) the device can not be updated via the I^{2}C interface. Conversely, the I^{2}C interface is fully functional during software shutdown (EN_DCDC bit = 0).

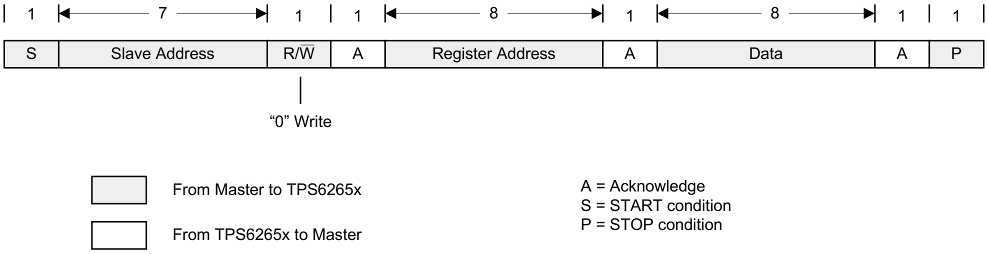


Figure 54. "Write" Data Transfer Format in Standard, Fast- and Fast-Plus Modes

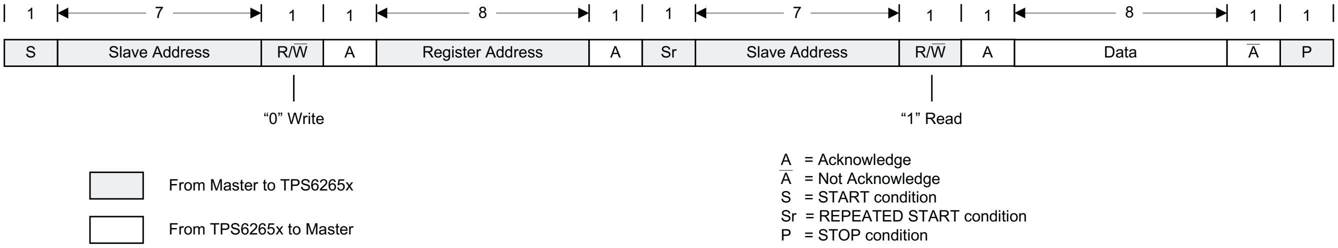


Figure 55. "Read" Data Transfer Format in Standard, Fast- and Fast-Plus Modes

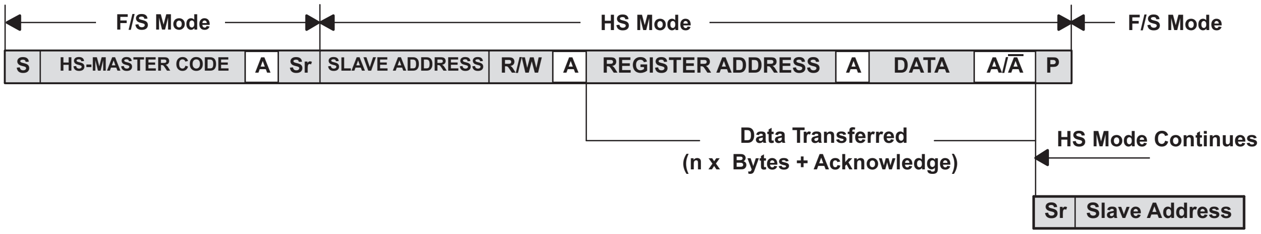


Figure 56. Data Transfer Format in H/S-Mode

Slave Address Byte

MSB							LSB
X	1	0	0	1	A2	A1	0

The slave address byte is the first byte received following the START condition from the master device. The first four bits (MSBs) of the address are factory preset to 1001. The next two bits (A2, A1) of the address are device option dependent. The LSB bit (A0) is also factory preset to 0. Up to 4 TPS6265x type of devices can be connected to the same I^{2}C-Bus. See the ordering information table for more details.

Register Address Byte

MSB							LSB
0	0	0	0	0	0	D1	D0

Following the successful acknowledgment of the slave address, the bus master sends a byte to the TPS6265x, which contains the address of the register to be accessed. The TPS6265x contains four 8-bit registers accessible via a bidirectional I^{2}C-bus interface. All internal registers have read and write access.

REGISTER DESCRIPTION

VSEL0 REGISTER DESCRIPTION

Memory location: 0x00

Description	EN_DCDC	FREE	VSM0[5:0]					
Bits	D7	D6	D5	D4	D3	D2	D1	D0
Memory type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default value	1	0	X	X	X	X	X	X

Bit	Description
EN_DCDC	**Enable/Disable DC/DC operation.** This bit gates the external EN pin control signal. This bit is mirrored in VSEL1 register. 0: Device in shutdown regardless of the EN signal. 1: Device enabled when EN is high, disabled when EN is low.
VSM0[5:0]	**Output voltage selection bits (floor voltage).**(1) 6-bit unsigned binary linear coding. Output voltage = Minimum output voltage + (VSM0[5:0] x 12.5 mV)

(1) Register value is set according to the default output voltage, see ordering information table.

VSEL1 REGISTER DESCRIPTION

Memory location: 0x01

Description	EN_DCDC	FREE	VSM1[5:0]					
Bits	D7	D6	D5	D4	D3	D2	D1	D0
Memory type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default value	1	0	X	X	X	X	X	X

Bit	Description
EN_DCDC	**Enable/Disable DC/DC operation.** This bit gates the external EN pin control signal. This bit is mirrored in VSEL0 register. 0: Device in shutdown regardless of the EN signal. 1: Device enabled when EN is high, disabled when EN is low.
VSM1[5:0]	**Output voltage selection bits (roof voltage).**(1) 6-bit unsigned binary linear coding. Output voltage = Minimum output voltage + (VSM1[5:0] x 12.5 mV)

(1) Register value is set according to the default output voltage, see ordering information table.

CONTROL1 REGISTER DESCRIPTION

Memory location: 0x02

Description	RESERVED	RESERVED	FREE	FREE	MODE_CTRL[1:0]		MODE1	MODE0
Bits	D7	D6	D5	D4	D3	D2	D1	D0
Memory type	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Default value	0	0	0	0	0	0	0	0

Bit	Description
MODE_CTRL[1:0]	**Mode control bits.**[1] 00: Operation follows MODE0, MODE1. 01: PFM/PWM operation independent of VSEL signal. 10: Forced PWM operation independent of VSEL signal. 11: PFM/PWM operation independent of VSEL signal.
MODE1	**VSEL high (roof voltage) operating mode selection bit.** 0: Forced PWM. 1: PFM/PWM automatic transition.
MODE0	**VSEL low (floor voltage) operating mode selection bit.** 0,1: PFM/PWM automatic transition (no effect).

(1) See the ordering information table to verify the validity of this option.

CONTROL2 REGISTER DESCRIPTION

Memory location: 0x03

Description	FREE	OUTPUT_DISCHARGE	PWROK	FREE	FREE	DEFSLEW		
Bits	D7	D6	D5	D4	D3	D2	D1	D0
Memory type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default value	0	1	0	0	0	1	1	1

Bit	Description
OUTPUT_ DISCHARGE	**Output capacitor auto-discharge control bit.** 0: The output capacitor is not actively discharged when the converter is disabled. 1: The output capacitor is discharged through an internal resistor when the converter is disabled.
PWROK	**Power good bit.** 0: The output voltage is not within its regulation limits. 1: The output voltage is in regulation.
DEFSLEW	**Output voltage slew-rate control bits.** 000: 0.15mV/μs 001: 0.3mV/μs 010: 0.6mV/μs 011: 1.2mV/μs 100: 2.4mV/μs 101: 4.8mV/μs 110: 9.6mV/μs 111: Immediate

APPLICATION INFORMATION

INDUCTOR SELECTION

The TPS6265x series of step-down converters have been optimized to operate with an effective inductance value in the range of 0.3µH to 1.3µH and with output capacitors in the range of 4.7µF to 10µF. The internal compensation is optimized to operate with an output filter of L = 0.47µH and C_O = 4.7µF. Larger or smaller inductor values can be used to optimize the performance of the device for specific operation conditions. For more details, refer to the section "checking loop stability".

The inductor value affects its peak-to-peak ripple current, the PWM-to-PFM transition point, the output voltage ripple and the efficiency. The selected inductor has to be rated for its dc resistance and saturation current. The inductor ripple current (ΔI_L) decreases with higher inductance and increases with higher V_I or V_O.

$$\Delta I_L = \frac{V_O}{V_I} \times \frac{V_I - V_O}{L \times f_{SW}} \qquad \Delta I_{L(MAX)} = I_{O(MAX)} + \frac{\Delta I_L}{2}$$

with: f_{SW} = switching frequency (6 MHz typical)

L = inductor value

ΔI_L = peak-to-peak inductor ripple current

$I_{L(MAX)}$ = maximum inductor current (1)

In high-frequency converter applications, the efficiency is essentially affected by the inductor AC resistance (i.e. quality factor) and to a smaller extent by the inductor DCR value. To achieve high efficiency operation, care should be taken in selecting inductors featuring a quality factor above 25 at the switching frequency. Increasing the inductor value produces lower RMS currents, but degrades transient response. For a given physical inductor size, increased inductance usually results in an inductor with lower saturation current.

The total losses of the coil consist of both the losses in the DC resistance ($R_{(DC)}$) and the following frequency-dependent components:

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic field losses of the neighboring windings (proximity effect)
- Radiation losses

The following inductor series from different suppliers have been used with the TPS6265x converters.

Table 3. List of Inductors

MANUFACTURER	SERIES	DIMENSIONS
MURATA	LQM21PN1R0NGR	2.0 x 1.2 x 1.0 max. height
	LQM21PNR54MG0	2.0 x 1.2 x 1.0 max. height
	LQM21PNR47MG0	2.0 x 1.2 x 1.0 max. height
	LQM2MPN1R0NG0	2.0 x 1.6 x 1.0 max. height
TOKO	MDT2012-CX1R0A	2.0 x 1.2 x 1.0 max. height
FDK	MIPS2012D1R0-X2	2.0 x 1.2 x 1.0 max. height

OUTPUT CAPACITOR SELECTION

The advanced fast-response voltage mode control scheme of the TPS6265x allows the use of tiny ceramic capacitors. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. For best performance, the device should be operated with a minimum effective output capacitance of 1.6µF. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies.

At nominal load current, the device operates in PWM mode and the overall output voltage ripple is the sum of the voltage step caused by the output capacitor ESL and the ripple current flowing through the output capacitor impedance.

At light loads, the output capacitor limits the output ripple voltage and provides holdup during large load transitions. A 4.7µF capacitor typically provides sufficient bulk capacitance to stabilize the output during large load transitions. The typical output voltage ripple is 1.5% of the nominal output voltage V_O.

The output voltage ripple during PFM mode operation can be kept small. The PFM pulse is time controlled, which allows to modify the charge transferred to the output capacitor by the value of the inductor. The resulting PFM output voltage ripple and PFM frequency depend in first order on the size of the output capacitor and the inductor value. The PFM frequency decreases with smaller inductor values and increases with larger once. Increasing the output capacitor value and the effective inductance will minimize the output ripple voltage.

INPUT CAPACITOR SELECTION

Because of the nature of the buck converter having a pulsating input current, a low ESR input capacitor is required to prevent large voltage transients that can cause misbehavior of the device or interferences with other circuits in the system. For most applications, a 2.2µF or 4.7µF capacitor is sufficient. If the application exhibits a noisy or erratic switching frequency, the remedy will probably be found by experimenting with the value of the input capacitor.

Take care when using only ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output can induce ringing at the VIN pin. This ringing can couple to the output and be mistaken as loop instability or could even damage the part. Additional "bulk" capacitance (electrolytic or tantalum) should in this circumstance be placed between C_I and the power source lead to reduce ringing than can occur between the inductance of the power source leads and C_I.

CHECKING LOOP STABILITY

The first step of circuit and stability evaluation is to look from a steady-state perspective at the following signals:

- Switching node, SW
- Inductor current, I_L
- Output ripple voltage, $V_{O(AC)}$

These are the basic signals that need to be measured when evaluating a switching converter. When the switching waveform shows large duty cycle jitter or the output voltage or inductor current shows oscillations, the regulation loop may be unstable. This is often a result of board layout and/or L-C combination.

As a next step in the evaluation of the regulation loop, the load transient response is tested. The time between the application of the load transient and the turn on of the P-channel MOSFET, the output capacitor must supply all of the current required by the load. V_O immediately shifts by an amount equal to $\Delta I_{(LOAD)}$ x ESR, where ESR is the effective series resistance of C_O. $\Delta I_{(LOAD)}$ begins to charge or discharge C_O generating a feedback error signal used by the regulator to return V_O to its steady-state value. The results are most easily interpreted when the device operates in PWM mode.

During this recovery time, V_O can be monitored for settling time, overshoot or ringing that helps judge the converter’s stability. Without any ringing, the loop has usually more than 45° of phase margin.

Because the damping factor of the circuitry is directly related to several resistive parameters (e.g., MOSFET $r_{DS(on)}$) that are temperature dependant, the loop stability analysis has to be done over the input voltage range, load current range, and temperature range.

LAYOUT CONSIDERATIONS

As for all switching power supplies, the layout is an important step in the design. High-speed operation of the TPS6265x devices demand careful attention to PCB layout. Care must be taken in board layout to get the specified performance. If the layout is not carefully done, the regulator could show poor line and/or load regulation, stability and switching frequency issues as well as EMI problems. It is critical to provide a low inductance, impedance ground path. Therefore, use wide and short traces for the main current paths.

The input capacitor should be placed as close as possible to the IC pins as well as the inductor and output capacitor. In order to get an optimum *ESL step*, the output voltage feedback point (FB) should be taken in the output capacitor path, approximately 1mm away for it. The feed-back line should be routed away from noisy components and traces (e.g. SW line).

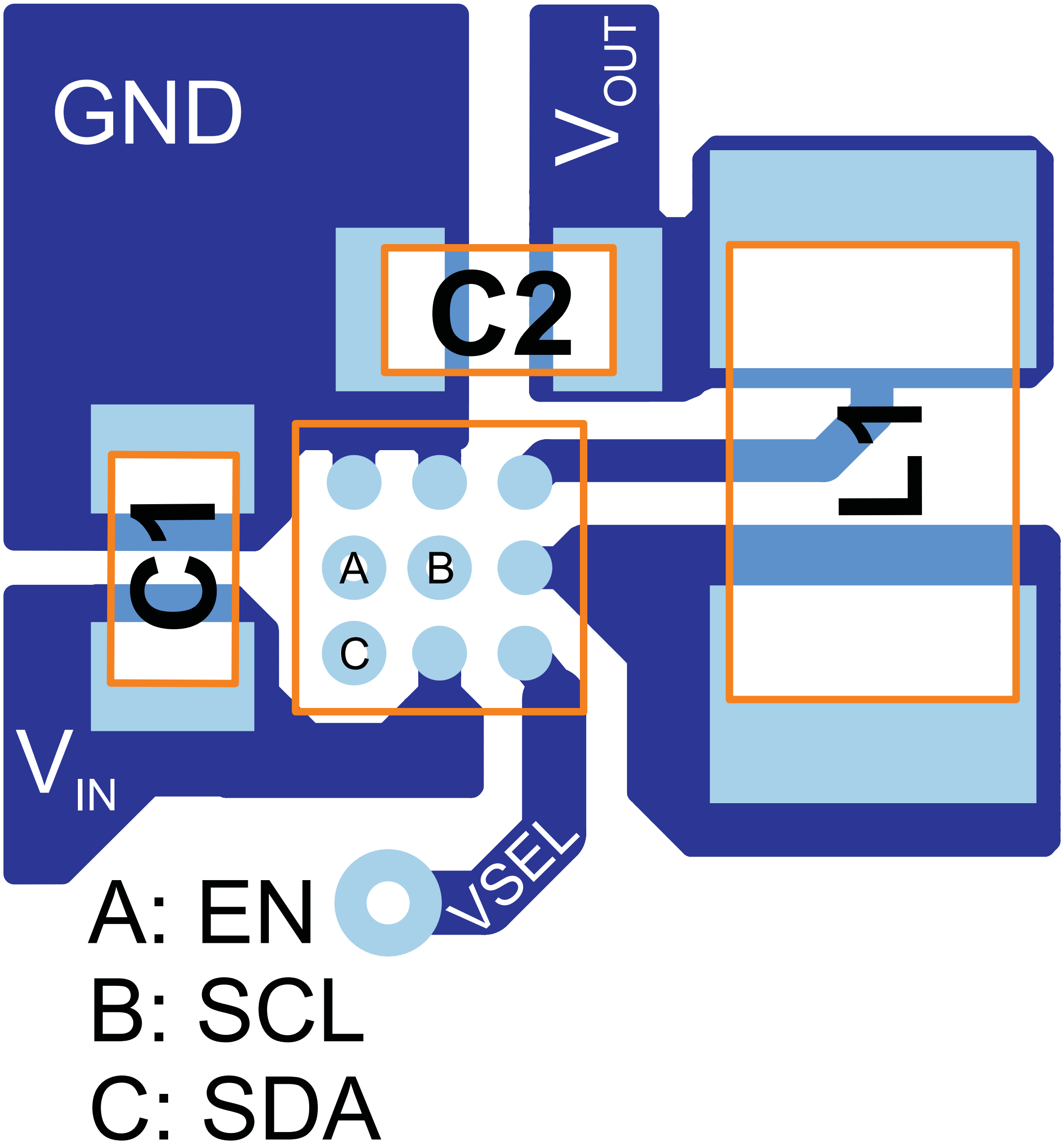


Figure 57. Suggested Layout (Top)

Thermal Information

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependant issues such as thermal coupling, airflow, added heat sinks, and convection surfaces, and the presence of other heat-generating components, affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below:

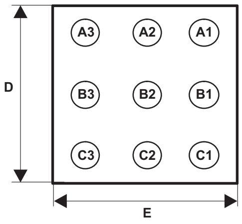
- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB
- Introducing airflow in the system

The maximum recommended junction temperature (T_J) of the TPS6265x device is 105°C. The thermal resistance of the 9-pin CSP package (YFF) is $R_{\theta JA}$ = 105°C/W. The regulator operation is specified to a maximum ambient temperature T_A of 85°C. Therefore, the maximum power dissipation is about 200mW.

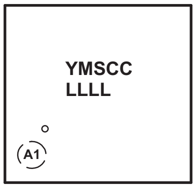
$$P_D MAX = \frac{T_J MAX - T_A}{R_{\theta JA}} = \frac{105°C - 85°C}{105°C/W} = 190\ mW \tag{2}$$

PACKAGE SUMMARY

CHIP SCALE PACKAGE
(BOTTOM VIEW)



CHIP SCALE PACKAGE
(TOP VIEW)



Code:

- YM - Year Month date code
- S - assembly site code
- CC - Chip code
- LLLL - Lot trace code

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS62650YFFR	ACTIVE	DSBGA	YFF	9	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	GJ	Samples
TPS62650YFFT	ACTIVE	DSBGA	YFF	9	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	GJ	Samples
TPS62651YFFR	ACTIVE	DSBGA	YFF	9	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	GK	Samples
TPS62651YFFT	ACTIVE	DSBGA	YFF	9	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	GK	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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OTHER QUALIFIED VERSIONS OF TPS62650 :

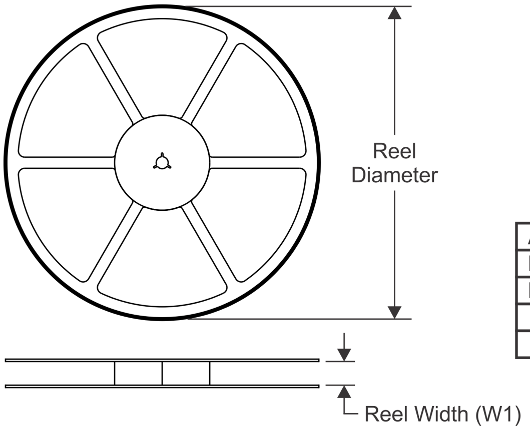
- Automotive: TPS62650-Q1

NOTE: Qualified Version Definitions:

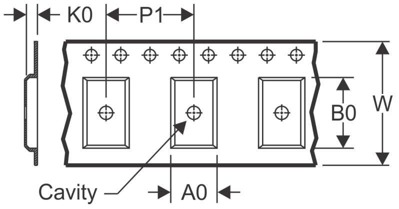
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

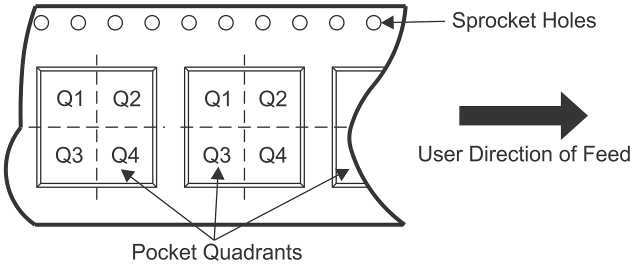


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

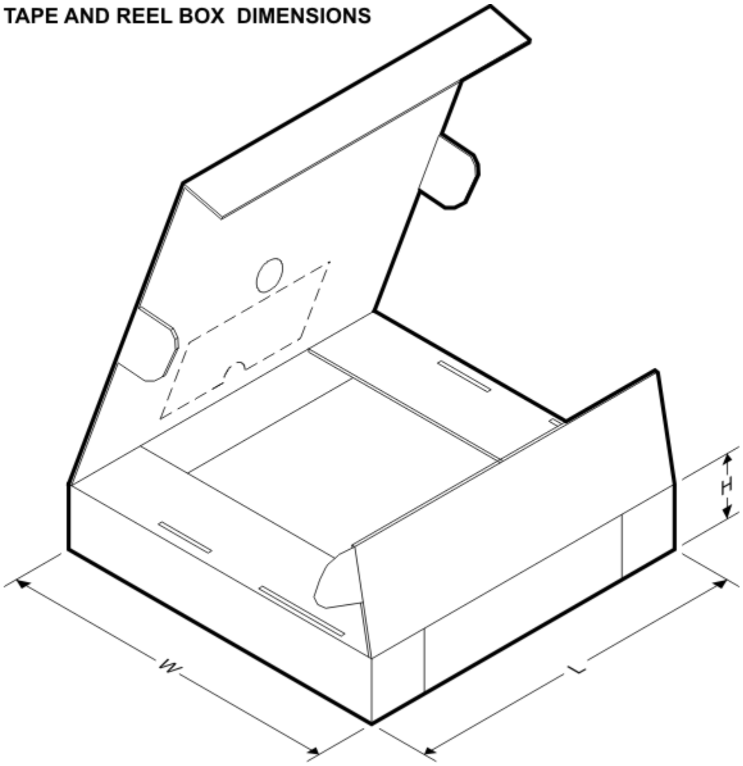
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62650YFFR	DSBGA	YFF	9	3000	180.0	8.4	1.45	1.45	0.8	4.0	8.0	Q1
TPS62651YFFR	DSBGA	YFF	9	3000	180.0	8.4	1.45	1.45	0.8	4.0	8.0	Q1
TPS62651YFFT	DSBGA	YFF	9	250	180.0	8.4	1.45	1.45	0.8	4.0	8.0	Q1

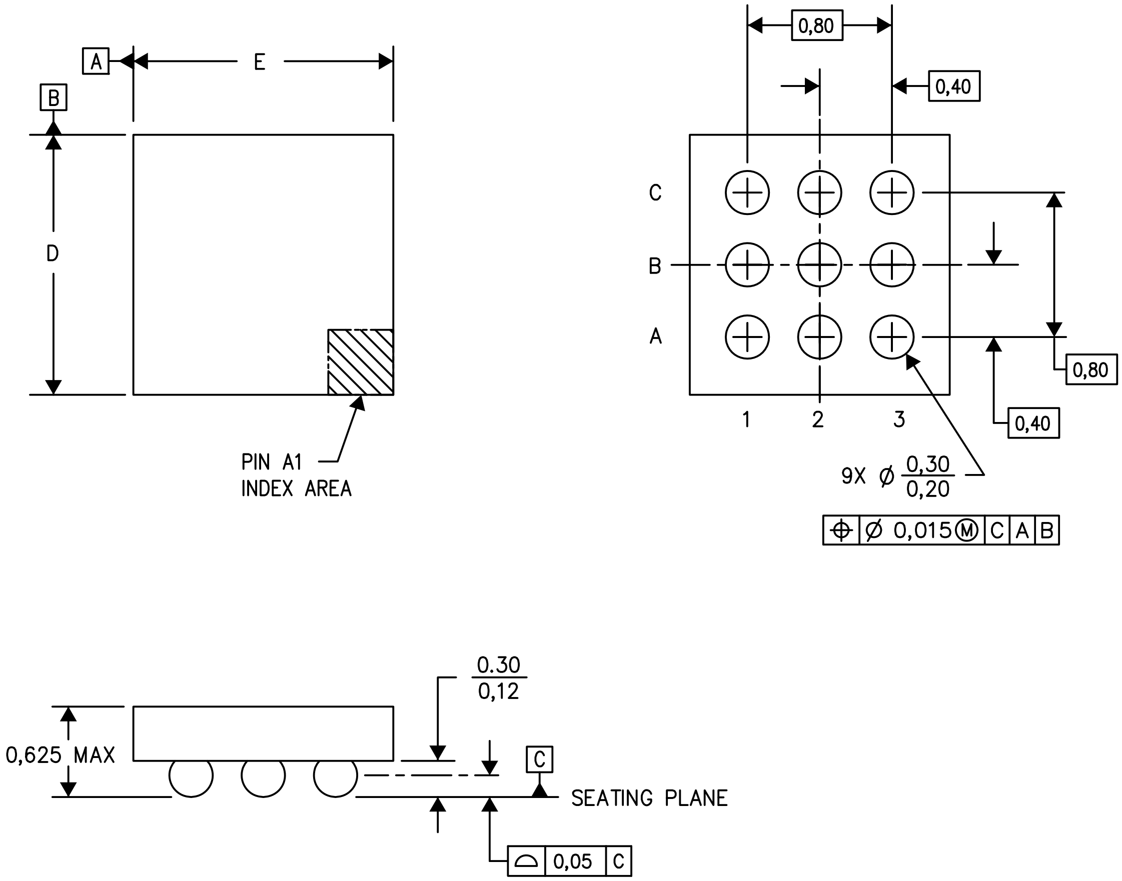
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62650YFFR	DSBGA	YFF	9	3000	210.0	185.0	35.0
TPS62651YFFR	DSBGA	YFF	9	3000	210.0	185.0	35.0
TPS62651YFFT	DSBGA	YFF	9	250	210.0	185.0	35.0

YFF (S–XBGA–N9) DIE–SIZE BALL GRID ARRAY



D: Max = 1.352 mm, Min =1.292 mm

E: Max = 1.326 mm, Min =1.266 mm

4207625–6/AM 06/13

NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments

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