

FEATURES

- Qualified for Automotive Applications
- Eight Constant-Current Output Channels
- Output Current Adjusted Through External Resistor
- Constant Output Current Range:
5 mA to 120 mA
- Constant Output Current Invariant to Load Voltage Change
- Open Load, Short Load, and Overtemperature Detection
- 256-Step Programmable Global Current Gain
- Excellent Output Current Accuracy:
 - Between Channels: < $\pm 3\%$ (Max)
 - Between ICs: < $\pm 6\%$ (Max)
- Fast Response of Output Current
- 30-MHz Clock Frequency
- Schmitt-Trigger Input
- 3.3-V or 5-V Supply Voltage
- Thermal Shutdown for Overtemperature Protection

APPLICATIONS

- General LED Lighting Applications
- LED Display Systems
- LED Signage
- Automotive LED Lighting
- White Goods
- Gaming Machines/Entertainment

DESCRIPTION/ORDERING INFORMATION

The TLC5916/TLC5917 is designed for LED displays and LED lighting applications with constant-current control and open-load, shorted-load, and overtemperature detection. The TLC5916/TLC5917 contains an 8-bit shift register and data latches, which convert serial input data into parallel output format. At the output stage, eight regulated current ports are designed to provide uniform and constant current for driving LEDs within a wide range of VF variations. Used in system design for LED display applications, e.g., LED panels, it provides great flexibility and device performance. Users can adjust the output current from 5 mA to 120 mA through an external resistor, R_{ext} , which gives flexibility in controlling the light intensity of LEDs. The devices are designed for up to 17 V at the output port. The high clock frequency, 30 MHz, also satisfies the system requirements of high-volume data transmission.

The TLC5916/TLC5917 provides a Special Mode in which two functions are included, Error Detection and Current Gain Control. There are two operation modes and three phases: Normal Mode phase, Mode Switching transition phase, and Special Mode phase. The signal on the multiple function pin $\overline{OE}(ED2)$ is monitored to determine the mode. When an one-clock-wide pulse appears on $\overline{OE}(ED2)$, the device enters the Mode Switching phase. At this time, the voltage level on LE(ED1) determines the mode to which the TLC5916/TLC5917 switches.

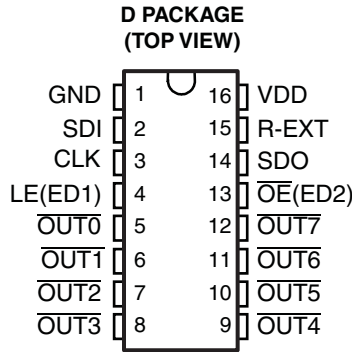
In the Normal Mode phase, the serial data can be transferred into TLC5916/TLC5917 via the pin SDI, shifted in the shift register, and transferred out via the pin SDO. LE(ED1) can latch the serial data in the shift register to the output latch. $\overline{OE}(ED2)$ enables the output drivers to sink current.

In the Special Mode phase, the low-voltage-level signal $\overline{OE}(ED2)$ can enable output channels and detect the status of the output current, to determine if the driving current level is sufficient. The detected Error Status is loaded into the 8-bit shift register and shifted out via the pin SDO, synchronous to the CLK signal. The system controller can read the error status and determine whether or not the LEDs are properly lit.

In the Special Mode phase, the TLC5916/TLC5917 allows users to adjust the output current level by setting a runtime-programmable Configuration Code. The code is sent into the TLC5916/TLC5917 via SDI. The positive pulse of LE(ED1) latches the code in the shift register into a built-in 8-bit configuration latch, instead of the output latch. The code affects the voltage at the terminal R-EXT and controls the output-current regulator. The output current can be finely adjusted by a gain ranging from 1/12 to 127/128 in 256 steps. Therefore, the current skew between ICs can be compensated within less than 1%. This feature is suitable for white balancing in LED color display panels.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



Terminal Descriptions

TERMINAL NAME	DESCRIPTION
CLK	Clock input for data shift on rising edge
GND	Ground for control logic and current sink
LE(ED1)	Data strobe input. Serial data is transferred to the respective latch when LE(ED1) is high. The data is latched when LE(ED1) goes low. Also, LE(ED1) is a control signal input for an Error Detection mode and Current Adjust mode (See Timing Diagram). LE(ED1) has an internal pull-down.
$\overline{\text{OE}}(\text{ED2})$	Output enable. When $\overline{\text{OE}}(\text{ED2})$ is active (low), the output drivers are enabled; when $\overline{\text{OE}}(\text{ED2})$ is high, all output drivers are turned OFF (blanked). Also, $\overline{\text{OE}}(\text{ED2})$ is a control signal input for an Error Detection mode and Current Adjust mode (See Timing Diagram). $\overline{\text{OE}}(\text{ED2})$ has an internal pullup.
$\overline{\text{OUT0}}\text{--}\overline{\text{OUT7}}$	Constant-current outputs
R-EXT	Input used to connect an external resistor for setting up all output currents
SDI	Serial-data input to the Shift register
SDO	Serial-data output to the following SDI of next driver IC or to the microcontroller
VDD	Supply voltage

Diagnostic Features

DEVICE ⁽¹⁾	OVERTEMPERATURE DETECTION	OPEN-LOAD DETECTION	SHORT TO GND DETECTION	SHORT TO V_{LED} DETECTION
TLC5916	X	X	X	
TLC5917	X	X	X	X

(1) The device has one single error register for all these conditions (one error bit per channel).

Timing Diagrams

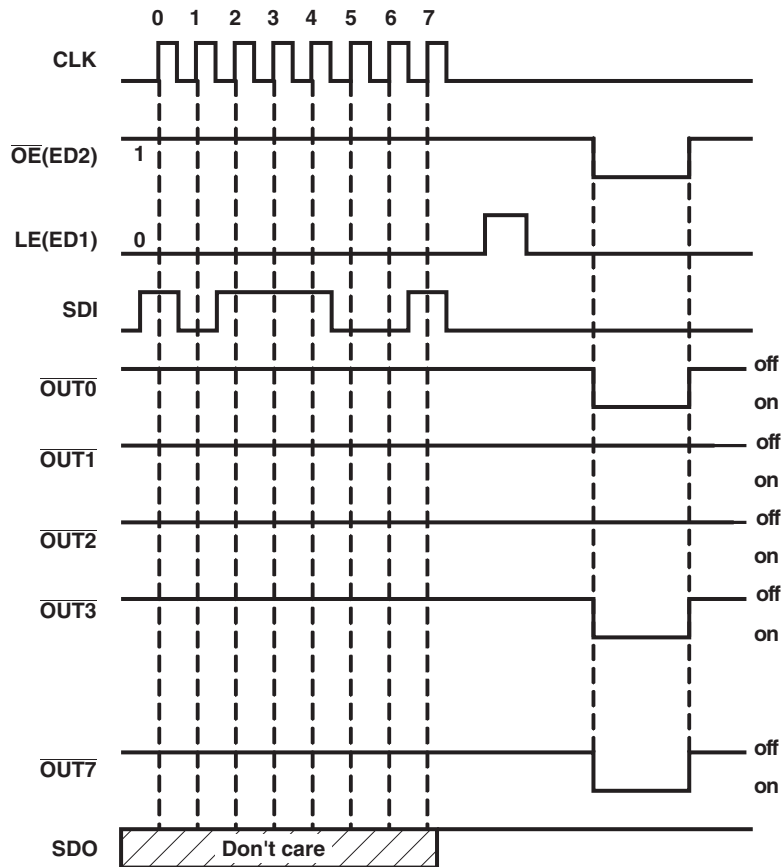


Figure 1. Normal Mode

Truth Table in Normal Mode

CLK	LE(ED1)	OE(ED2)	SDI	OUT0...OUT7	SDO
↑	H	L	Dn	Dn...Dn – 7	Dn – 7
↑	L	L	Dn + 1	No change	Dn – 6
↑	H	L	Dn + 2	Dn + 2...Dn – 5	Dn – 5
↓	X	L	Dn + 3	Dn + 2...Dn – 5	Dn – 5
↓	X	H	Dn + 3	Off	Dn – 5

The signal sequence shown in Figure 2 makes the TLC5916/TLC5917 enter Current Adjust and Error Detection mode.

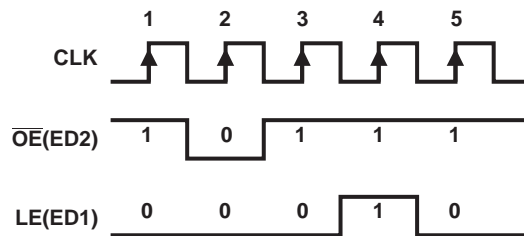


Figure 2. Switching to Special Mode

In the Current Adjust mode, sending the positive pulse of LE(ED1), the content of the Shift register (a current adjust code) is written to the 8-bit configuration latch (see [Figure 3](#)).

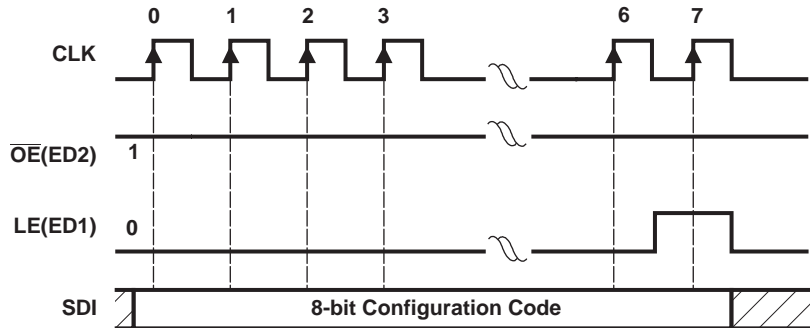


Figure 3. Writing Configuration Code

When the TLC5916/TLC5917 is in the Error Detection mode, the signal sequence shown in [Figure 4](#) enables a system controller to read error status codes through SDO.

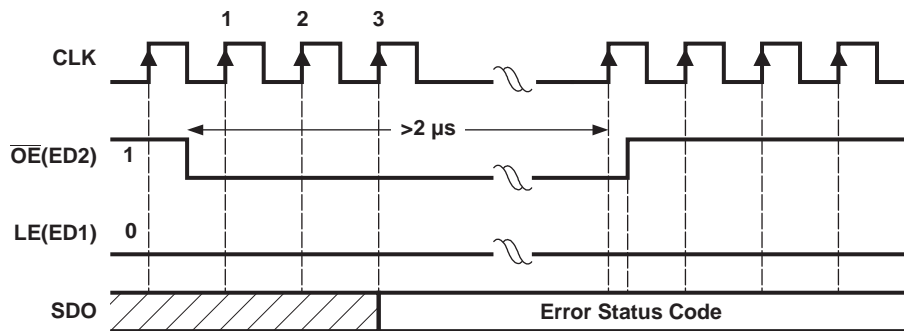


Figure 4. Reading Error Status Code

The signal sequence shown in [Figure 5](#) makes TLC5916/TLC5917 resume the Normal mode. Switching to Normal mode resets all internal Error Status registers. OE(ED2) always enables the output port, whether the TLC5916/TLC5917 enters Current Adjust mode or not.

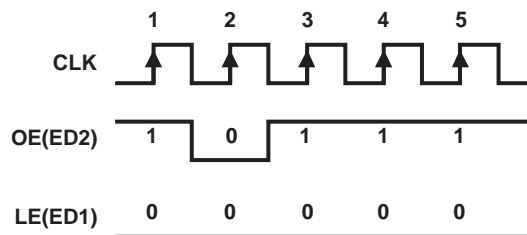


Figure 5. Switching to Normal Mode

TLC5916-Q1, TLC5917-Q1 8-BIT CONSTANT-CURRENT LED SINK DRIVERS

SLVS814–JANUARY 2008

Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{DD}	Supply voltage range	0	7	V
V_I	Input voltage range	-0.4	$V_{DD} + 0.4$	V
V_O	Output voltage range	-0.5	20	V
f_{clk}	Clock frequency		25	MHz
I_{OUT}	Output current		120	mA
I_{GND}	GND terminal current		960	mA
T_A	Operating free-air temperature range	-40	125	°C
T_J	Operating junction temperature range	-40	150	°C
T_{stg}	Storage temperature range	-55	150	°C
ESD	Electrostatic discharge capability	Human-Body Model	1500	V
		Machine Model	150	
		Charged-Device Model	1000	

Power Dissipation and Thermal Impedance

		MIN	MAX	UNIT	
P_D	Power dissipation	Mounted on JEDEC 4-layer board (JESD 51-7), No airflow, $T_A = 85^\circ\text{C}$, $T_J = 125^\circ\text{C}$		0.6	W
θ_{JA}	Thermal impedance, junction to free air	Mounted on JEDEC 1-layer board (JESD 51-3), No airflow		103	°C/W
		Mounted on JEDEC 4-layer board (JESD 51-7), No airflow		66	

Recommended Operating Conditions

		MIN	MAX	UNIT		
V_{DD}	Supply voltage	3	5.5	V		
V_O	Supply voltage to output pins	$\overline{OUT0}$ – $\overline{OUT7}$		17	V	
I_O	Output current	DC test circuit	$V_O \geq 0.6\text{ V}$	5	mA	
			$V_O \geq 1\text{ V}$	120		
I_{OH}	High-level output current source	SDO shorted to GND		-1	mA	
I_{OL}	Low-level output current sink	SDO shorted to V_{CC}		1	mA	
V_{IH}	High-level input voltage	CLK, \overline{OE} (ED2), LE(ED1), and SDI		$0.7 \times V_{DD}$	V_{DD}	V
V_{IL}	Low-level input voltage	CLK, \overline{OE} (ED2), LE(ED1), and SDI		0	$0.3 \times V_{DD}$	V

Recommended Timing

$V_{DD} = 3\text{ V to }5.5\text{ V}$ (unless otherwise noted)

			MIN	MAX	UNIT
$t_{w(L)}$	LE(ED1) pulse duration	Normal mode	20		ns
$t_{w(CLK)}$	CLK pulse duration	Normal mode	20		ns
$t_{w(OE)}$	\overline{OE} (ED2) pulse duration	Normal mode, $I_{OUT} < 60\text{ mA}$	675		ns
		Normal mode, $I_{OUT} > 60\text{ mA}$	800		
$t_{su(D)}$	Setup time for SDI	Normal mode	3		ns
$t_{h(D)}$	Hold time for SDI	Normal mode	2		ns
$t_{su(L)}$	Setup time for LE(ED1)	Normal mode	15		ns
$t_{h(L)}$	Hold time for LE(ED1)	Normal mode	15		ns
$t_{w(CLK)}$	CLK pulse duration	Error Detection mode	20		ns
$t_{w(ED2)}$	\overline{OE} (ED2) pulse duration	Error Detection mode	2000		ns
$t_{su(ED1)}$	Setup time for LE(ED1)	Error Detection mode	4		ns
$t_{h(ED1)}$	Hold time for LE(ED1)	Error Detection mode	10		ns
$t_{su(ED2)}$	Setup time for \overline{OE} (ED2)	Error Detection mode	8.5		ns
$t_{h(ED2)}$	Hold time for \overline{OE} (ED2)	Error Detection mode	10		ns
f_{CLK}	Clock frequency	Cascade operation		30	MHz

TLC5916-Q1, TLC5917-Q1 8-BIT CONSTANT-CURRENT LED SINK DRIVERS

SLVS814–JANUARY 2008

Electrical Characteristics

 $V_{DD} = 3\text{ V}$, $T_J = -40^\circ\text{C}$ to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
V_{DD}	Input voltage		3		5.5	V
V_O	Supply voltage to the output pins				17	V
I_O	Output current	$V_O \geq 0.6\text{ V}$	5			mA
		$V_O \geq 1\text{ V}$			120	
I_{OH}	High-level output current, source		-1			mA
I_{OL}	Low-level output current, sink		1			mA
V_{IH}	High-level input voltage		$0.7 \times V_{DD}$		V_{DD}	V
V_{IL}	Low-level input voltage		GND		$0.3 \times V_{DD}$	V
I_{leak}	Output leakage current	$V_{OH} = 17\text{ V}$	$T_J = 25^\circ\text{C}$		0.5	μA
			$T_J = 125^\circ\text{C}$		2	
V_{OH}	High-level output voltage	SDO, $I_{OL} = -1\text{ mA}$	$V_{DD} - 0.4$			V
V_{OL}	Low-level output voltage	SDO, $I_{OH} = 1\text{ mA}$			0.4	V
$I_{O(1)}$	Output current 1	$V_{OUT} = 0.6\text{ V}$, $R_{ext} = 720\ \Omega$, CG = 0.992		26		mA
	Output current error, die-die	$I_{OL} = 26\text{ mA}$, $V_O = 0.6\text{ V}$, $R_{ext} = 720\ \Omega$, $T_J = 25^\circ\text{C}$		± 3	± 6	%
	Output current skew, channel-to-channel	$I_{OL} = 26\text{ mA}$, $V_O = 0.6\text{ V}$, $R_{ext} = 720\ \Omega$, $T_J = 25^\circ\text{C}$		± 1.5	± 3	%
$I_{O(2)}$	Output current 2	$V_O = 0.8\text{ V}$, $R_{ext} = 360\ \Omega$, CG = 0.992		52		mA
	Output current error, die-die	$I_{OL} = 52\text{ mA}$, $V_O = 0.8\text{ V}$, $R_{ext} = 360\ \Omega$, $T_J = 25^\circ\text{C}$		± 2	± 6	%
	Output current skew, channel-to-channel	$I_{OL} = 52\text{ mA}$, $V_O = 0.8\text{ V}$, $R_{ext} = 360\ \Omega$, $T_J = 25^\circ\text{C}$		± 1.5	± 3	%
$I_{OUT\text{ vs }V_{OUT}}$	Output current vs output voltage regulation	$V_O = 1\text{ V}$ to 3 V , $I_O = 26\text{ mA}$		± 0.1		%V
		$V_{DD} = 3.0\text{ V}$ to 5.5 V , $I_O = 26\text{ mA}/120\text{ mA}$		± 1		
	Pullup resistance	$\overline{OE}(ED2)$		500		k Ω
	Pulldown resistance	LE(ED1)		500		k Ω
T_{sd}	Overtemperature shutdown ⁽²⁾		150	175	200	$^\circ\text{C}$
T_{hys}	Restart temperature hysteresis			15		$^\circ\text{C}$
$I_{OUT,Th1}$	Threshold current for open error detection	$I_{OUT,target} = 26\text{ mA}$		$0.5 \times I_{target}$		%
$I_{OUT,Th2}$	Threshold current for open error detection	$I_{OUT,target} = 52\text{ mA}$		$0.5 \times I_{target}$		%
$I_{OUT,Th3}$	Threshold current for open error detection	$I_{OUT,target} = 104\text{ mA}$		$0.5 \times I_{target}$		%
$I_{OUT,Th}$	Threshold current for open error detection	$I_{OUT,target} = 5\text{ mA}$ to 120 mA		$0.5 \times I_{target}$		%
$V_{OUT,TTh}$	Trigger threshold voltage for short-error detection (TLC5917 only)	$I_{OUT,target} = 5\text{ mA}$ to 120 mA	2.44	2.7	3.1	V
$V_{OUT,RTh}$	Return threshold voltage for short-error detection (TLC5917 only)	$I_{OUT,target} = 5\text{ mA}$ to 120 mA	2.2			V
I_{DD}	Supply current	$R_{ext} = \text{Open}$		5	10	mA
		$R_{ext} = 720\ \Omega$		8	14	
		$R_{ext} = 360\ \Omega$		11	18	
		$R_{ext} = 180\ \Omega$		16	22	

(1) Typical values represent the likely parametric nominal values determined at the time of characterization. Typical values depend on the application and configuration and may vary over time. Typical values are not ensured on production material.

(2) Specified by design

Electrical Characteristics

$V_{DD} = 5.5\text{ V}$, $T_J = -40^\circ\text{C}$ to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
V_{DD}	Input Voltage		3		5.5	V
V_O	Supply voltage to the output pins				17	V
I_O	Output current	$V_O \geq 0.6\text{ V}$	5			mA
		$V_O \geq 1\text{ V}$			120	
I_{OH}	High-level output current, source		-1			mA
I_{OL}	Low-level output current, sink		1			mA
V_{IH}	High-level input voltage		$0.7 \times V_{DD}$		V_{DD}	V
V_{IL}	Low-level input voltage		GND		$0.3 \times V_{DD}$	V
I_{leak}	Output leakage current	$V_{OH} = 17\text{ V}$	$T_J = 25^\circ\text{C}$		0.5	μA
			$T_J = 125^\circ\text{C}$		2	
V_{OH}	High-level output voltage	SDO, $I_{OL} = -1\text{ mA}$	$V_{DD} - 0.4$			V
V_{OL}	Low-level output voltage	SDO, $I_{OH} = 1\text{ mA}$			0.4	V
$I_{O(1)}$	Output current 1	$V_{OUT} = 0.6\text{ V}$, $R_{ext} = 720\ \Omega$, CG = 0.992		26		mA
	Output current error, die-die	$I_{OL} = 26\text{ mA}$, $V_O = 0.6\text{ V}$, $R_{ext} = 720\ \Omega$, $T_J = 25^\circ\text{C}$		± 3	± 6	%
	Output current skew, channel-to-channel	$I_{OL} = 26\text{ mA}$, $V_O = 0.6\text{ V}$, $R_{ext} = 720\ \Omega$, $T_J = 25^\circ\text{C}$		± 1.5	± 3	%
$I_{O(2)}$	Output current 2	$V_O = 0.8\text{ V}$, $R_{ext} = 360\ \Omega$, CG = 0.992		52		mA
	Output current error, die-die	$I_{OL} = 52\text{ mA}$, $V_O = 0.8\text{ V}$, $R_{ext} = 360\ \Omega$, $T_J = 25^\circ\text{C}$		± 2	± 6	%
	Output current skew, channel-to-channel	$I_{OL} = 52\text{ mA}$, $V_O = 0.8\text{ V}$, $R_{ext} = 360\ \Omega$, $T_J = 25^\circ\text{C}$		± 1.5	± 3	%
I_{OUT} vs V_{OUT}	Output current vs output voltage regulation	$V_O = 1\text{ V}$ to 3 V , $I_O = 26\text{ mA}$		± 0.1		%V
		$V_{DD} = 3.0\text{ V}$ to 5.5 V , $I_O = 26\text{ mA}/120\text{ mA}$		± 1		
	Pullup resistance	$\overline{OE}(ED2)$,		500		k Ω
	Pulldown resistance	LE(ED1),		500		k Ω
T_{sd}	Overtemperature shutdown ⁽²⁾		150	175	200	$^\circ\text{C}$
T_{hys}	Restart temperature hysteresis			15		$^\circ\text{C}$
$I_{OUT,Th1}$	Threshold current for open error detection	$I_{OUT,target} = 26\text{ mA}$		$0.5 \times I_{target}$		%
$I_{OUT,Th2}$	Threshold current for open error detection	$I_{OUT,target} = 52\text{ mA}$		$0.5 \times I_{target}$		%
$I_{OUT,Th3}$	Threshold current for open error detection	$I_{OUT,target} = 104\text{ mA}$		$0.5 \times I_{target}$		%
$I_{OUT,Th}$	Threshold current for open error detection	$I_{OUT,target} = 5\text{ mA}$ to 120 mA		$0.5 \times I_{target}$		%
$V_{OUT,TTh}$	Trigger threshold voltage for short-error detection (TLC5917 only)	$I_{OUT,target} = 5\text{ mA}$ to 120 mA	2.44	2.7	3.1	V
$V_{OUT,RTh}$	Return threshold voltage for short-error detection (TLC5917 only)	$I_{OUT,target} = 5\text{ mA}$ to 120 mA	2.2			V
I_{DD}	Supply current	$R_{ext} = \text{Open}$		6	10	mA
		$R_{ext} = 720\ \Omega$		11	14	
		$R_{ext} = 360\ \Omega$		13	18	
		$R_{ext} = 180\ \Omega$		19	24	

(1) Typical values represent the likely parametric nominal values determined at the time of characterization. Typical values depend on the application and configuration and may vary over time. Typical values are not ensured on production material.

(2) Specified by design

TLC5916-Q1, TLC5917-Q1 8-BIT CONSTANT-CURRENT LED SINK DRIVERS

SLVS814–JANUARY 2008

Switching Characteristics

$V_{DD} = 3\text{ V}$, $T_J = -40^\circ\text{C}$ to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
t_{PLH1}	Low-to-high propagation delay time, CLK to $\overline{\text{OUTn}}$	$V_{IH} = V_{DD}$, $V_{IL} = \text{GND}$, $R_{ext} = 360\ \Omega$, $V_L = 4\text{ V}$, $R_L = 44\ \Omega$, $C_L = 10\text{ pF}$, $CG = 0.992$	40	65	95	ns
t_{PLH2}	Low-to-high propagation delay time, LE(ED1) to $\overline{\text{OUTn}}$		40	65	95	ns
t_{PLH3}	Low-to-high propagation delay time, $\overline{\text{OE}}(\text{ED2})$ to $\overline{\text{OUTn}}$		40	65	95	ns
t_{PLH4}	Low-to-high propagation delay time, CLK to SDO		12	20	30	ns
t_{PHL1}	High-to-low propagation delay time, CLK to $\overline{\text{OUTn}}$			300	365	ns
t_{PHL2}	High-to-low propagation delay time, LE(ED1) to $\overline{\text{OUTn}}$			300	365	ns
t_{PHL3}	High-to-low propagation delay time, $\overline{\text{OE}}(\text{ED2})$ to $\overline{\text{OUTn}}$			300	365	ns
t_{PHL4}	High-to-low propagation delay time, CLK to SDO		12	20	30	ns
$t_{w(\text{CLK})}$	Pulse duration, CLK		20			ns
$t_{w(L)}$	Pulse duration, LE(ED1)		20			ns
$t_{w(\text{OE})}$	Pulse duration, $\overline{\text{OE}}(\text{ED2})$		500			ns
$t_{w(\text{ED2})}$	Pulse duration, $\overline{\text{OE}}(\text{ED2})$ in Error Detection mode		2			μs
$t_{h(\text{ED1,ED2})}$	Hold time, LE(ED1) and $\overline{\text{OE}}(\text{ED2})$		10			ns
$t_{h(D)}$	Hold time, SDI		2			ns
$t_{su(D,ED1)}$	Setup time, SDI, LE(ED1)		4			ns
$t_{su(\text{ED2})}$	Setup time, $\overline{\text{OE}}(\text{ED2})$		8.5			ns
$t_{h(L)}$	Hold time, LE(ED1), Normal mode		15			ns
$t_{su(L)}$	Setup time, LE(ED1), Normal mode		15			ns
t_r	Rise time, CLK ⁽²⁾				500	ns
t_f	Fall time, CLK ⁽²⁾				500	ns
t_{or}	Rise time, outputs (off)	40	85	105	ns	
t_{or}	Rise time, outputs (off), $T_J = 25^\circ\text{C}$		83	100	ns	
t_{of}	Rise time, outputs (on)	100	280	370	ns	
t_{of}	Rise time, outputs (on), $T_J = 25^\circ\text{C}$		170	225	ns	
f_{CLK}	Clock frequency	Cascade operation			30	MHz

- (1) Typical values represent the likely parametric nominal values determined at the time of characterization. Typical values depend on the application and configuration and may vary over time. Typical values are not ensured on production material.
- (2) If the devices are connected in cascade and t_r or t_f is large, it may be critical to achieve the timing required for data transfer between two cascaded devices.

Switching Characteristics

$V_{DD} = 5.5\text{ V}$, $T_J = -40^\circ\text{C}$ to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
t_{PLH1}	Low-to-high propagation delay time, CLK to \overline{OUTn}	$V_{IH} = V_{DD}$, $V_{IL} = \text{GND}$, $R_{ext} = 360\ \Omega$, $V_L = 4\text{ V}$, $R_L = 44\ \Omega$, $C_L = 10\text{ pF}$, $CG = 0.992$	40	65	95	ns
t_{PLH2}	Low-to-high propagation delay time, LE(ED1) to \overline{OUTn}		40	65	95	ns
t_{PLH3}	Low-to-high propagation delay time, $\overline{OE}(ED2)$ to \overline{OUTn}		40	65	95	ns
t_{PLH4}	Low-to-high propagation delay time, CLK to SDO		8	20	30	ns
t_{PHL1}	High-to-low propagation delay time, CLK to \overline{OUTn}			300	365	ns
t_{PHL2}	High-to-low propagation delay time, LE(ED1) to \overline{OUTn}			300	365	ns
t_{PHL3}	High-to-low propagation delay time, $\overline{OE}(ED2)$ to \overline{OUTn}			300	365	ns
t_{PHL4}	High-to-low propagation delay time, CLK to SDO		8	20	30	ns
$t_{w(\text{CLK})}$	Pulse duration, CLK		20			ns
$t_{w(L)}$	Pulse duration, LE(ED1)		20			ns
$t_{w(\text{OE})}$	Pulse duration, $\overline{OE}(ED2)$		500			ns
$t_{w(\text{ED2})}$	Pulse duration, $\overline{OE}(ED2)$ in Error Detection mode		2			μs
$t_{h(\text{D,ED1,ED2})}$	Hold time, SDI, LE(ED1), and $\overline{OE}(ED2)$		10			ns
$t_{h(\text{D})}$	Hold time, SDI		2			ns
$t_{su(\text{D,ED1})}$	Setup time, SDI, LE(ED1)		4			ns
$t_{su(\text{ED2})}$	Setup time, $\overline{OE}(ED2)$		8.5			ns
$t_{h(L)}$	Hold time, LE(ED1), Normal mode		15			ns
$t_{su(L)}$	Setup time, LE(ED1), Normal mode		15			ns
t_r	Rise time, CLK ⁽²⁾				500	ns
t_f	Fall time, CLK ⁽²⁾				500	ns
t_{or}	Rise time, outputs (off)	40	85	105	ns	
t_{or}	Rise time, outputs (off), $T_J = 25^\circ\text{C}$		83	100	ns	
t_{of}	Rise time, outputs (on)	100	280	370	ns	
t_{of}	Rise time, outputs (on), $T_J = 25^\circ\text{C}$		170	225	ns	
f_{CLK}	Clock frequency	Cascade operation			30	MHz

- (1) Typical values represent the likely parametric nominal values determined at the time of characterization. Typical values depend on the application and configuration and may vary over time. Typical values are not ensured on production material.
- (2) If the devices are connected in cascade and t_r or t_f is large, it may be critical to achieve the timing required for data transfer between two cascaded devices.

PARAMETER MEASUREMENT INFORMATION

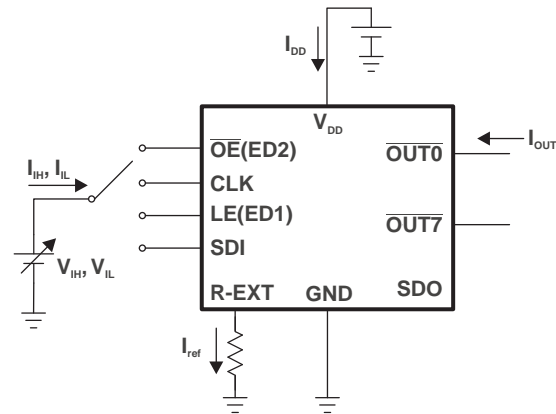


Figure 6. Test Circuit for Electrical Characteristics

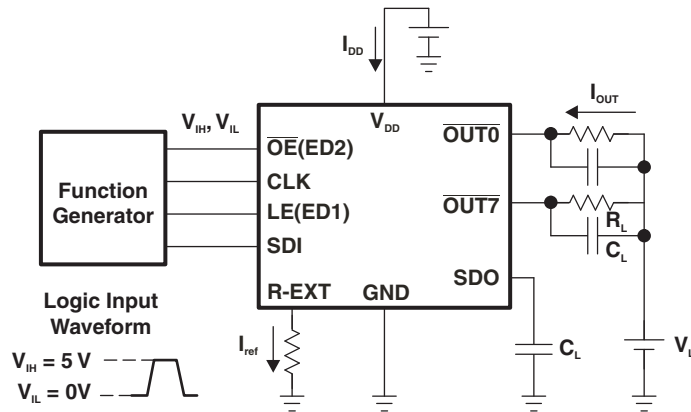


Figure 7. Test Circuit for Switching Characteristics

PARAMETER MEASUREMENT INFORMATION (continued)

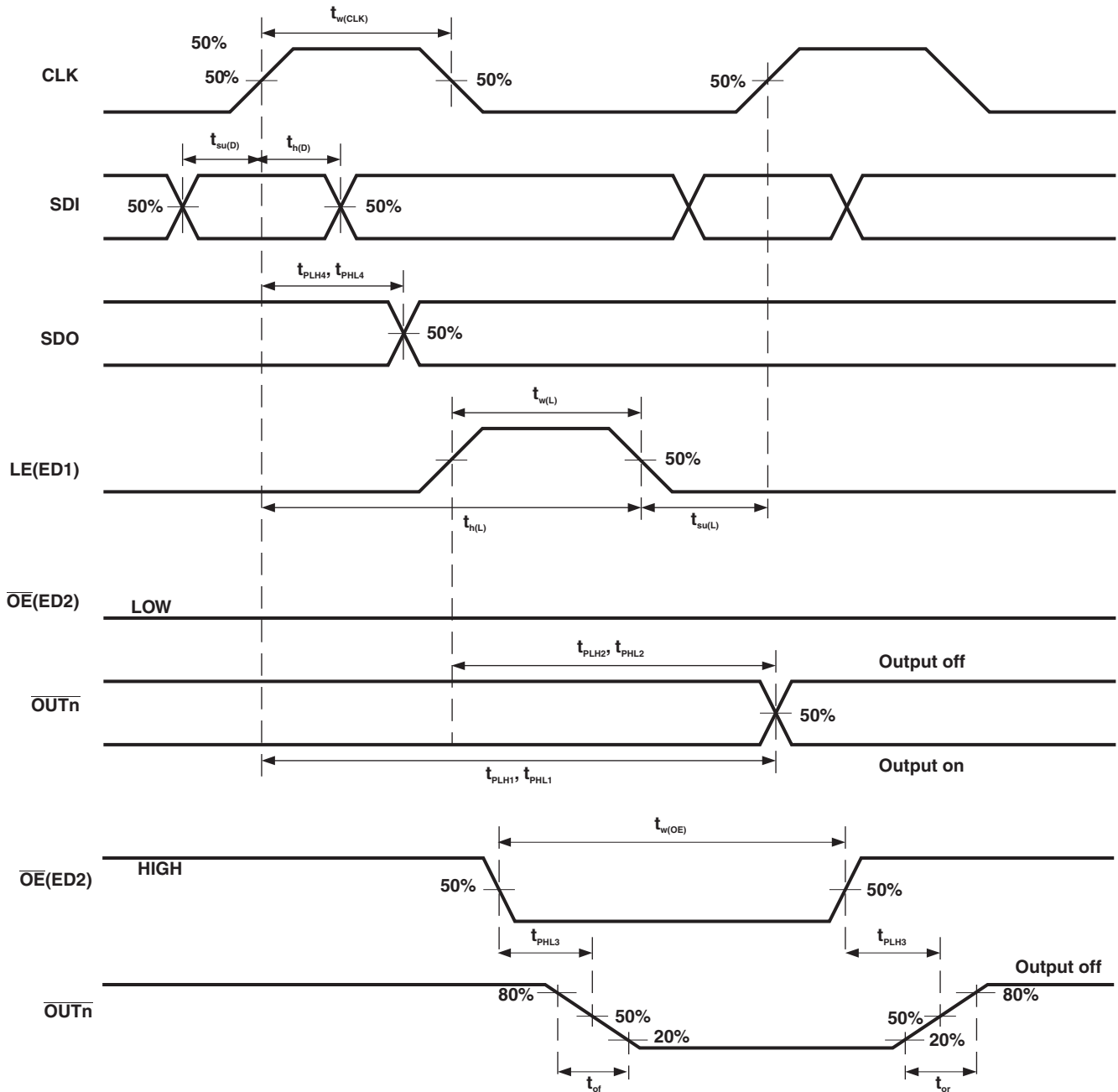


Figure 8. Normal Mode Timing Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

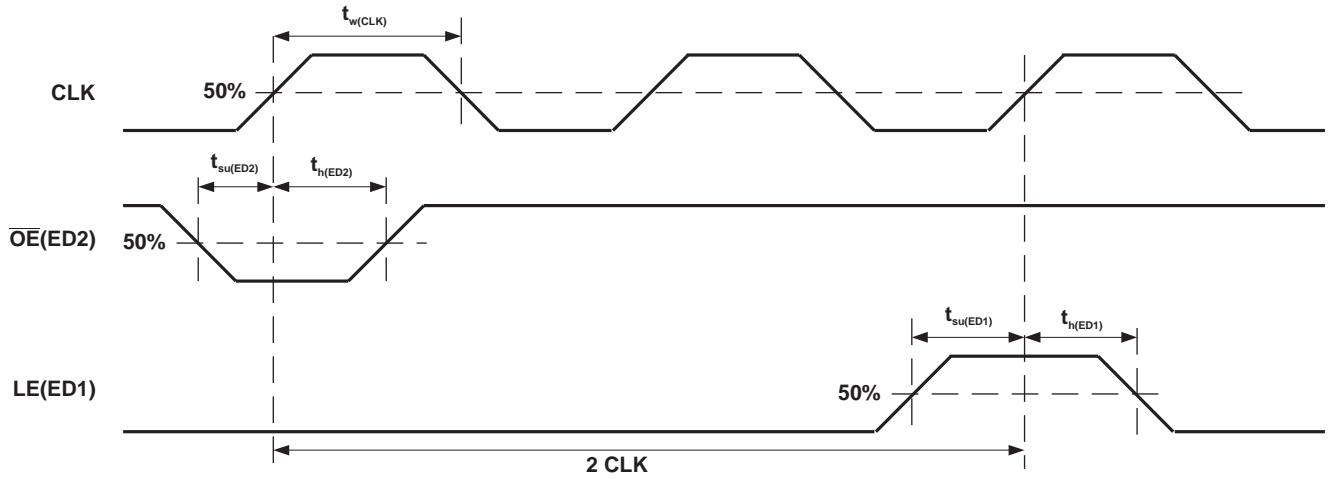


Figure 9. Switching to Special Mode Timing Waveforms

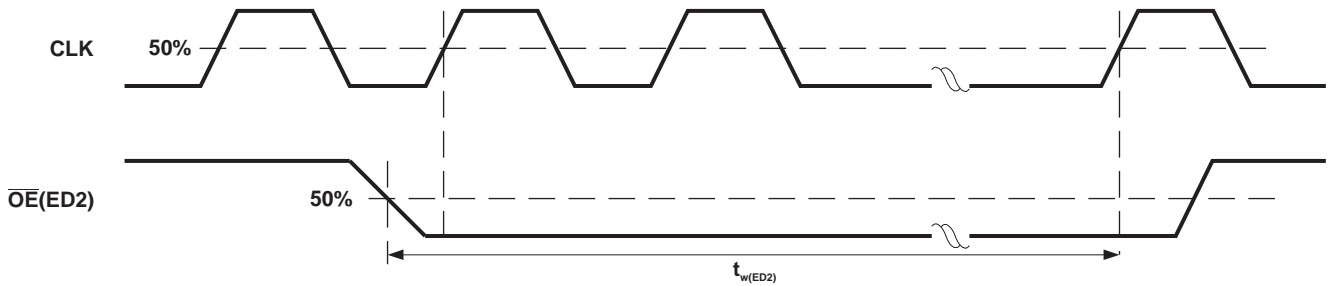


Figure 10. Reading Error Status Code Timing Waveforms

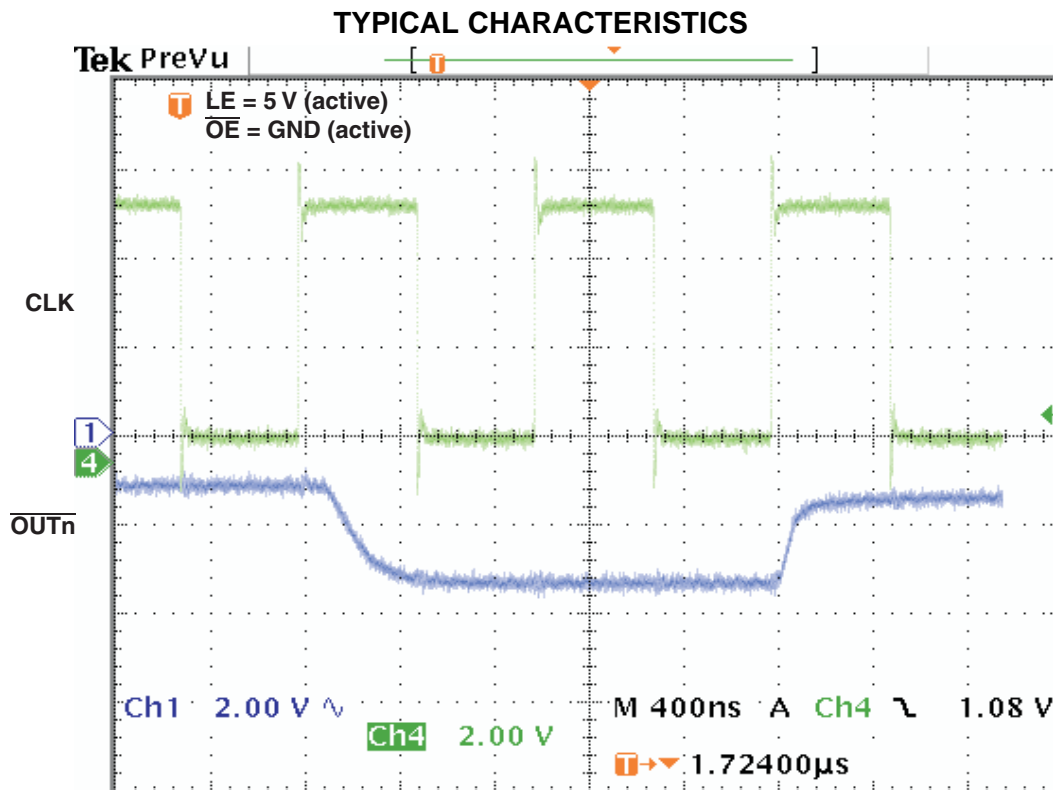


Figure 11. Response Time, CLK to $\overline{\text{OUTn}}$

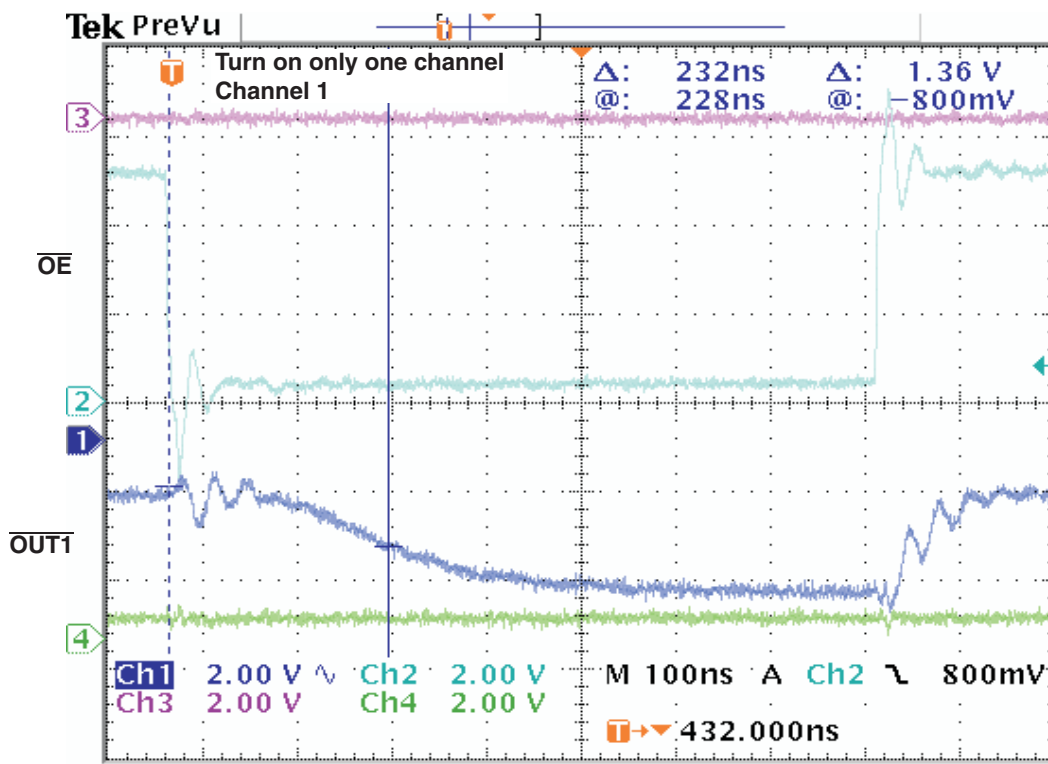


Figure 12. Response Time, $\overline{\text{OE}}$ to $\overline{\text{OUT1}}$

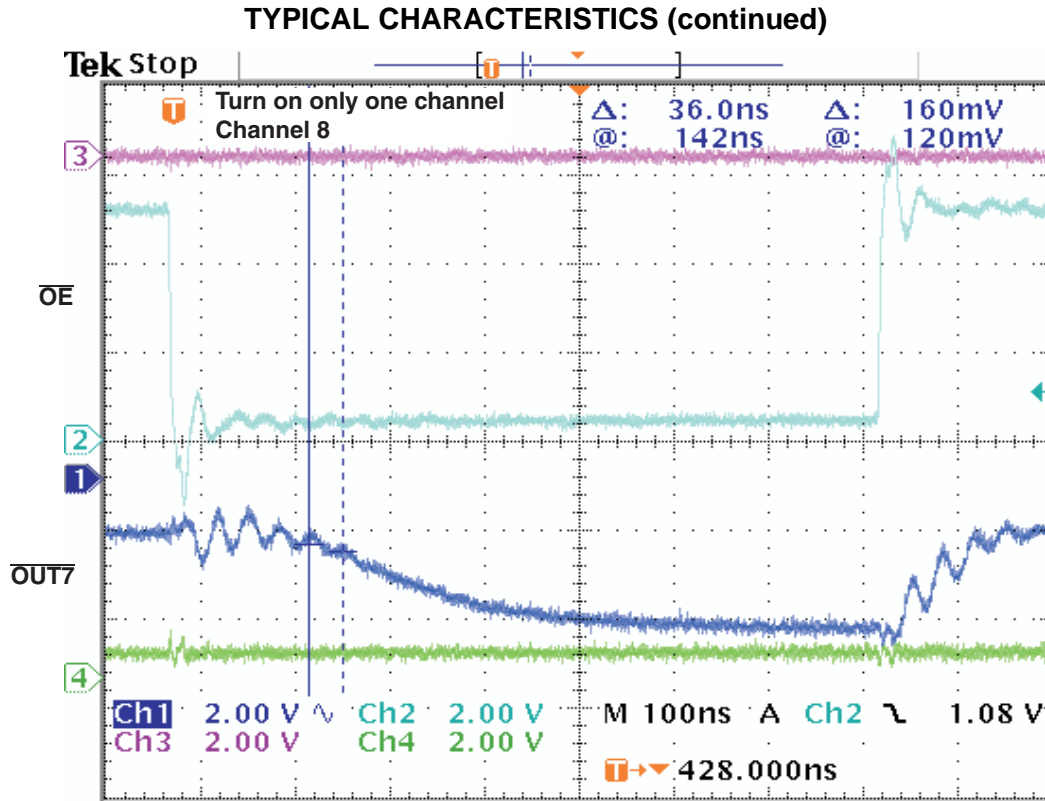


Figure 13. Response Time, OE to OUT7

APPLICATION INFORMATION

Operating Principles

Constant Current

In LED display applications, the TLC5916/TLC5917 provides nearly no current variations from channel to channel and from IC to IC. While $I_{OUT} \leq 100$ mA, the maximum current skew between channels is less than $\pm 3\%$ and between ICs is less than $\pm 6\%$.

Adjusting Output Current

The TLC5916/TLC5917 scales up the reference current, I_{ref} , set by the external resistor R_{ext} to sink a current, I_{out} , at each output port. Use the following formulas to calculate the target output current $I_{OUT,target}$ in the saturation region:

$$V_{R-EXT} = 1.26 \text{ V} \times VG$$

$I_{ref} = V_{R-EXT}/R_{ext}$, if another end of the external resistor R_{ext} is connected to ground

$$I_{OUT,target} = I_{ref} \times 15 \times 3^{CM-1}$$

Where R_{ext} is the resistance of the external resistor connected to the R-EXT terminal, and V_{R-EXT} is the voltage of R-EXT, which is controlled by the programmable voltage gain (VG), which is defined by the Configuration Code. The Current Multiplier (CM) determines that the ratio $I_{OUT,target}/I_{ref}$ is 15 or 5. After power on, the default value of VG is $127/128 = 0.992$, and the default value of CM is 1, so that the ratio $I_{OUT,target}/I_{ref} = 15$. Based on the default VG and CM.

$$V_{R-EXT} = 1.26 \text{ V} \times 127/128 = 1.25 \text{ V}$$

$$I_{OUT,target} = (1.25 \text{ V}/R_{ext}) \times 15$$

Therefore, the default current is approximately 52 mA at 360Ω and 26 mA at 720Ω . The default relationship after power on between $I_{OUT,target}$ and R_{ext} is shown in Figure 14.

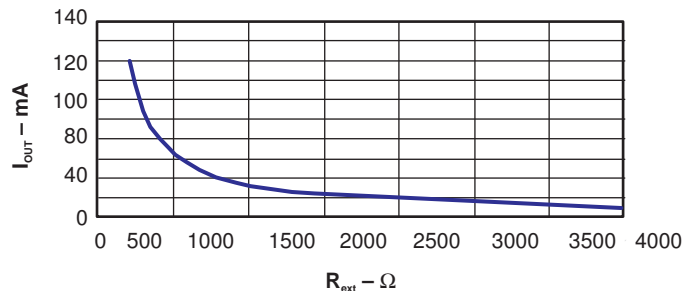


Figure 14. Default Relationship Curve Between $I_{OUT,target}$ and R_{ext} After Power Up

Operation Phases

Operation Mode Switching

In order to switch between its two modes, TLC5916/TLC5917 monitors the signal $\overline{OE}(ED2)$. When an one-clock-wide pulse of $\overline{OE}(ED2)$ appears, TLC5916/TLC5917 enters the two-clock-period transition phase, the Mode Switching phase. After power on, the default operation mode is the Normal Mode (see Figure 15).

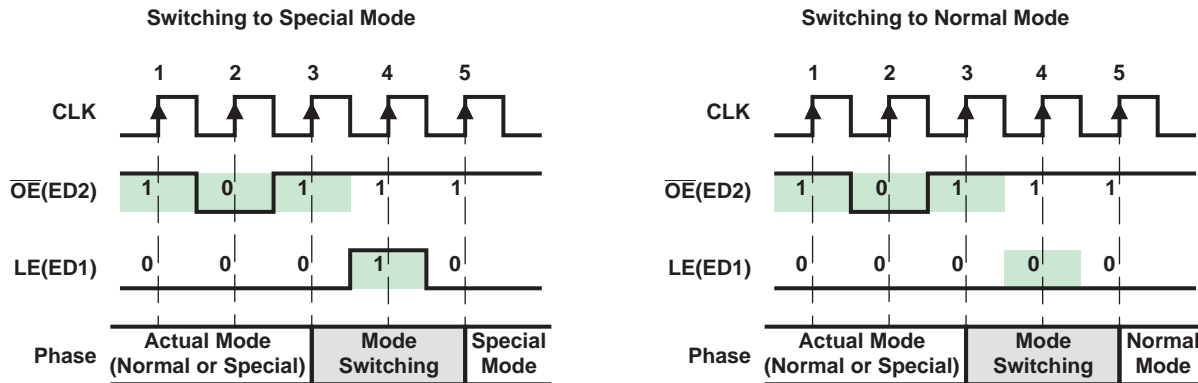


Figure 15. Mode Switching

As shown in Figure 15, once a one-clock-wide short pulse (101) of $\overline{OE}(ED2)$ appears, TLC5916/TLC5917 enters the Mode Switching phase. At the fourth rising edge of CLK, if LE(ED1) is sampled as voltage high, TLC5916/TLC5917 switches to Special mode; otherwise, it switches to Normal mode. The signal LE(ED1) between the third and the fifth rising edges of CLK cannot latch any data. Its level is used only to determine into which mode to switch. However, the short pulse of $\overline{OE}(ED2)$ can still enable the output ports. During mode switching, the serial data can still be transferred through SDI and shifted out from SDO.

NOTE:

1. The signal sequence for the mode switching may be used frequently to ensure that TLC5916/TLC5917 is in the proper mode.
2. The 1 and 0 on the LE(ED1) signal are sampled at the rising edge of CLK. The X means its level does not affect the result of mode switching mechanism.
3. After power on, the default operation mode is Normal mode.

Normal Mode Phase

Serial data is transferred into TLC5916/TLC5917 via SDI, shifted in the Shift register, and output via SDO. LE(ED1) can latch the serial data in the Shift register to the Output Latch. $\overline{OE}(ED2)$ enables the output drivers to sink current. These functions differ only as described in Operation Mode Switching, in which case, a short pulse triggers TLC5916/TLC5917 to switch the operation mode. However, as long as LE(ED1) is high in the Mode Switching phase, TLC5916/TLC5917 remains in the Normal mode, as if no mode switching occurred.

Special Mode Phase

In the Special mode, as long as $\overline{OE}(ED2)$ is not low, the serial data is shifted to the Shift register via SDI and shifted out via SDO, as in the Normal mode. However, there are two differences between Special mode and Normal mode, as shown in the following sections.

Reading Error Status Code in Special Mode

When $\overline{OE}(ED2)$ is pulled low while in Special mode, error detection and load error status codes are loaded into the Shift register, in addition to enabling output ports to sink current. Figure 16 shows the timing sequence for error detection. The 0 and 1 signal levels are sampled at the rising edge of each CLK. At least three zeros must be sampled at the voltage low signal $\overline{OE}(ED2)$. Immediately after the second zero is sampled, the data input source of the Shift register changes to the 8-bit parallel Error Status Code register, instead of from the serial data on SDI. Normally, the error status codes are generated at least 2 μ s after the falling edge of $\overline{OE}(ED2)$. The occurrence of the third or later zero saves the detected error status codes into the Shift register. Therefore, when $\overline{OE}(ED2)$ is low, the serial data cannot be shifted into TLC5916/TLC5917 via SDI. When $\overline{OE}(ED2)$ is pulled high, the data input source of the Shift register is changed back to SDI. At the same time, the output ports are disabled and the error detection is completed. Then, the error status codes saved in the Shift register can be shifted out via SDO bit by bit along with CLK, as well as the new serial data can be shifted into TLC5916/TLC5917 via SDI.

While in Special mode, the TLC5916/TLC5917 cannot simultaneously transfer serial data and detect LED load error status.

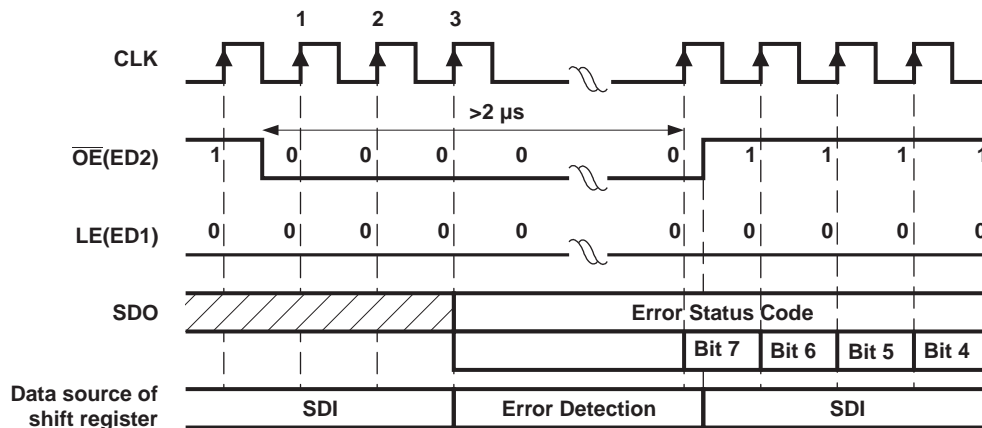


Figure 16. Reading Error Status Code

Writing Configuration Code in Special Mode

When in Special mode, the active high signal LE(ED1) latches the serial data in the Shift register to the Configuration Latch, instead of the Output Latch. The latched serial data is used as the Configuration Code.

The code is stored until power off or the Configuration Latch is rewritten. As shown in Figure 17, the timing for writing the Configuration Code is the same as the timing in the Normal Mode to latching output channel data. Both the Configuration Code and Error Status Code are transferred in the common 8-bit Shift register. Users must pay attention to the sequence of error detection and current adjustment to avoid the Configuration Code being overwritten by Error Status Code.

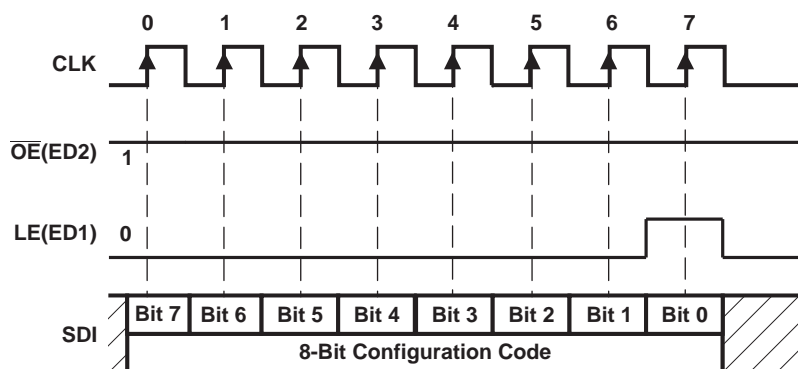


Figure 17. Writing Configuration Code

Open-Circuit Detection Principle

The LED Open-Circuit Detection compares the effective current level I_{OUT} with the open load detection threshold current $I_{OUT,Th}$. If I_{OUT} is below the $I_{OUT,Th}$ threshold, the TLC5916/TLC5917 detects an open-load condition. This error status can be read as an error status code in the Special mode. For open-circuit error detection, a channel must be on.

Table 1. Open-Circuit Detection

STATE OF OUTPUT PORT	CONDITION OF OUTPUT CURRENT	ERROR STATUS CODE	MEANING
Off	$I_{OUT} = 0 \text{ mA}$	0	Detection not possible
On	$I_{OUT} < I_{OUT,Th}^{(1)}$	0	Open circuit
	$I_{OUT} \geq I_{OUT,Th}^{(1)}$	Channel n error status bit 1	Normal

(1) $I_{OUT,Th} = 0.5 \times I_{OUT,target}$ (typical)

Short-Circuit Detection Principle (TLC5917 Only)

The LED short-circuit detection compares the effective voltage level (V_{OUT}) with the shorted-load detection threshold voltages $V_{OUT,TTh}$ and $V_{OUT,RTh}$. If V_{OUT} is above the $V_{OUT,TTh}$ threshold, the TLC5917 detects an shorted-load condition. If V_{OUT} is below the $V_{OUT,RTh}$ threshold, no error is detected/error bit is reset. This error status can be read as an error status code in the Special mode. For short-circuit error detection, a channel must be on.

Table 2. Shorted-Load Detection

STATE OF OUTPUT PORT	CONDITION OF OUTPUT VOLTAGE	ERROR STATUS CODE	MEANING
Off	$I_{OUT} = 0 \text{ mA}$	0	Detection not possible
On	$V_{OUT} \geq V_{OUT,TTh}$	0	Short circuit
	$V_{OUT} < V_{OUT,RTh}$	1	Normal

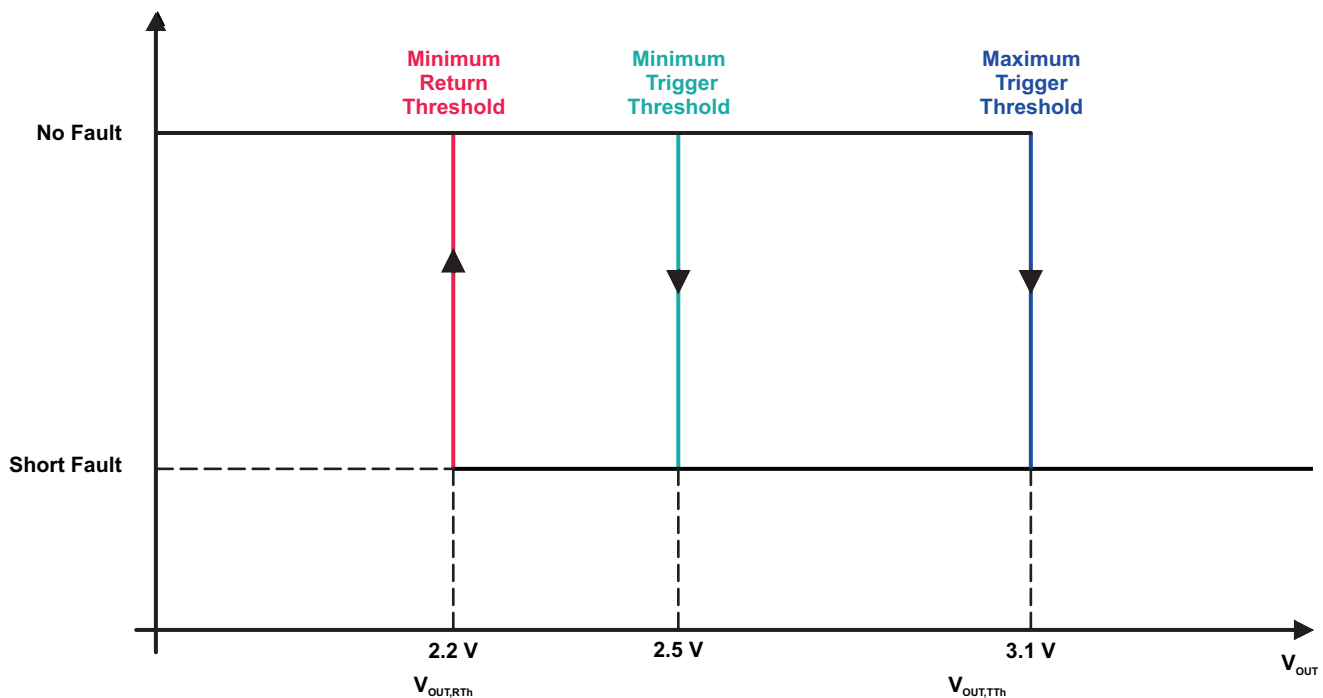


Figure 18. Short-Circuit Detection Principle

Overtemperature Detection and Shutdown

TLC5916/TLC5917 is equipped with a global overtemperature sensor and eight individual, channel-specific, overtemperature sensors.

- When the global sensor reaches the trip temperature, all output channels are shutdown, and the error status is stored in the internal Error Status register of every channel. After shutdown, the channels automatically restart after cooling down, if the control signal (output latch) remains on. The stored error status is not reset after cooling down and can be read out as the error status code in the Special mode.
- When one of the channel-specific sensors reaches trip temperature, only the affected output channel is shut down, and the error status is stored only in the internal Error Status register of the affected channel. After shutdown, the channel automatically restarts after cooling down, if the control signal (output latch) remains on. The stored error status is not reset after cooling down and can be read out as error status code in the Special mode.

For channel-specific overtemperature error detection, a channel must be on.

The error status code is reset when TLC5916/TLC5917 returns to Normal mode.

Table 3. Overtemperature Detection⁽¹⁾

STATE OF OUTPUT PORT	CONDITION	ERROR STATUS CODE	MEANING
Off	$I_{OUT} = 0 \text{ mA}$	0	
On	$T_j < T_{j,trip} \text{ global}$	1	Normal
On → all channels Off	$T_j > T_{j,trip} \text{ global}$	All error status bits = 0	Global overtemperature
On	$T_j < T_{j,trip} \text{ channel n}$	1	Normal
On → Off	$T_j > T_{j,trip} \text{ channel n}$	Channel n error status bit = 0	Channel n overtemperature

(1) The global shutdown threshold temperature is approximately 170°C.

8-Bit Configuration Code and Current Gain

Bit definition of the Configuration Code in the Configuration Latch is shown in [Table 4](#).

Table 4. Bit Definition of 8-Bit Configuration Code

	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Meaning	CM	HC	CC0	CC1	CC2	CC3	CC4	CC5
Default	1	1	1	1	1	1	1	1

Bit 7 is first sent into TLC5916/TLC5917 via SDI. Bits 1 to 7 {HC, CC[0:5]} determine the voltage gain (VG) that affects the voltage at R-EXT and indirectly affects the reference current, I_{ref} , flowing through the external resistor at R-EXT. Bit 0 is the Current Multiplier (CM) that determines the ratio $I_{OUT,target}/I_{ref}$. Each combination of VG and CM gives a specific Current Gain (CG).

- VG: the relationship between {HC,CC[0:5]} and the voltage gain is calculated as shown below:

$$VG = (1 + HC) \times (1 + D/64) / 4$$

$$D = CC0 \times 2^5 + CC1 \times 2^4 + CC2 \times 2^3 + CC3 \times 2^2 + CC4 \times 2^1 + CC5 \times 2^0$$

Where HC is 1 or 0, and D is the binary value of CC[0:5]. So, the VG could be regarded as a floating-point number with 1-bit exponent HC and 6-bit mantissa CC[0:5]. {HC,CC[0:5]} divides the programmable voltage gain VG into 128 steps and two sub-bands:

Low-voltage subband (HC = 0): $VG = 1/4 \sim 127/256$, linearly divided into 64 steps

High-voltage subband (HC = 1): $VG = 1/2 \sim 127/128$, linearly divided into 64 steps

- CM: In addition to determining the ratio $I_{OUT,target}/I_{ref}$, CM limits the output current range.

High Current Multiplier (CM = 1): $I_{OUT,target}/I_{ref} = 15$, suitable for output current range $I_{OUT} = 10 \text{ mA}$ to 120 mA .

Low Current Multiplier (CM = 0): $I_{OUT,target}/I_{ref} = 5$, suitable for output current range $I_{OUT} = 5 \text{ mA}$ to 40 mA

- CG: The total Current Gain is defined as the following.

$$V_{R-EXT} = 1.26 \text{ V} \times VG$$

$I_{ref} = V_{R-EXT}/R_{ext}$, if the external resistor, R_{ext} , is connected to ground.

$$I_{OUT,target} = I_{ref} \times 15 \times 3^{CM-1} = 1.26 \text{ V}/R_{ext} \times VG \times 15 \times 3^{CM-1} = (1.26 \text{ V}/R_{ext} \times 15) \times CG$$

$$CG = VG \times 3^{CM-1}$$

Therefore, $CG = 1/12$ to $127/128$, and it is divided into 256 steps.

Examples

- Configuration Code {CM, HC, CC[0:5]} = {1,1,111111}
 $VG = 127/128 = 0.992$ and $CG = VG \times 3^0 = VG = 0.992$
- Configuration Code = {1,1,000000}
 $VG = (1 + 1) \times (1 + 0/64)/4 = 1/2 = 0.5$, and $CG = 0.5$
- Configuration Code = {0,0,000000}
 $VG = (1 + 0) \times (1 + 0/64)/4 = 1/4$, and $CG = (1/4) \times 3^{-1} = 1/12$

After power on, the default value of the Configuration Code {CM, HC, CC[0:5]} is {1,1,111111}. Therefore, $VG = CG = 0.992$. The relationship between the Configuration Code and the Current Gain is shown in [Figure 19](#).

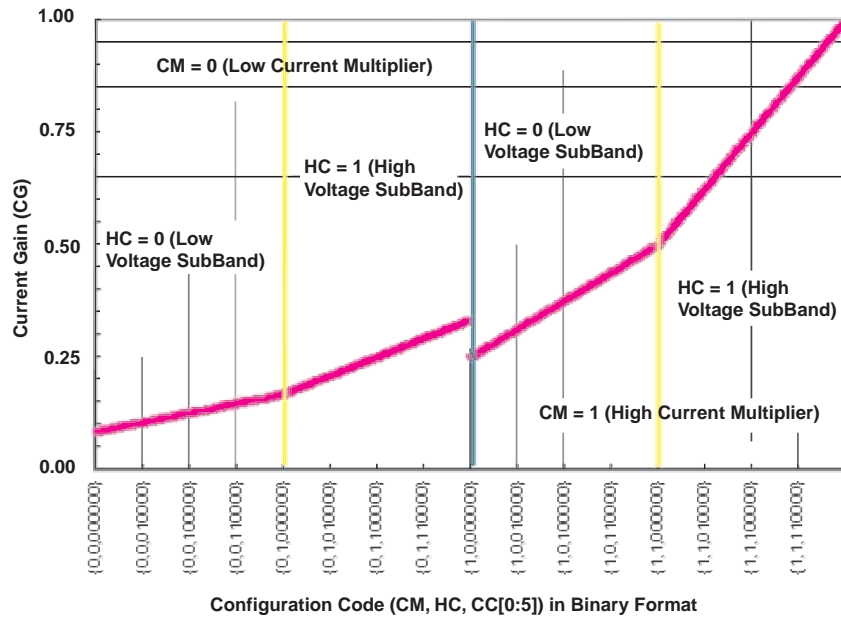


Figure 19. Current Gain vs Configuration Code

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TLC5916QDRQ1	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLC5916Q	Samples
TLC5917QDRQ1	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLC5917Q	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLC5916-Q1, TLC5917-Q1 :

- Catalog: [TLC5916](#), [TLC5917](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC5917QDRQ1	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC5917QDRQ1	SOIC	D	16	2500	333.2	345.9	28.6

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com