Dual High-Voltage Scan Driver for TFT-LCD

Check for Samples: TPS65193

FEATURES

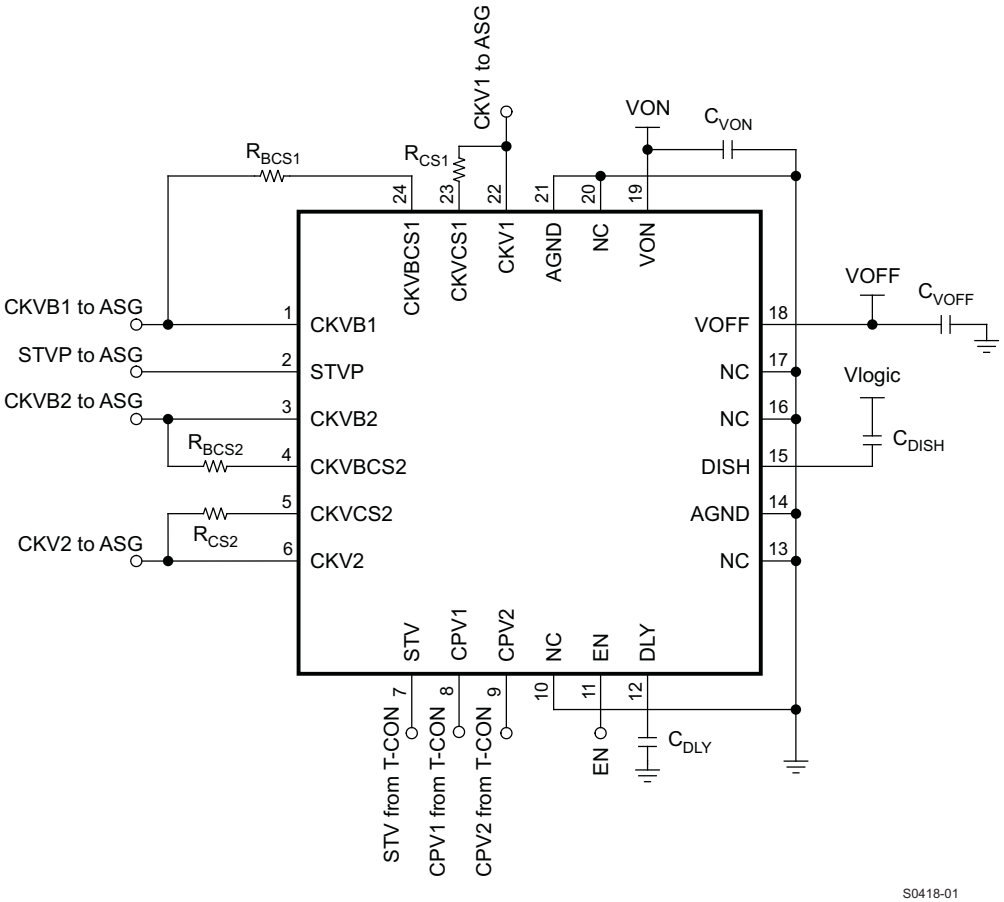
- **Dual High-Voltage Scan Driver**
- **Scan Driver Output Charge Share**
- **High Output-Voltage Level: Up to 35 V**
- **Low Output-Voltage Level: Down to –28 V**
- **Logic-Level Inputs**
- **24-Pin 4-mm × 4-mm QFN package**

APPLICATIONS

- **TFT LCD Using Amorphous Silicon Gate (ASG) Technology**

DESCRIPTION

The TPS65193 is dual high-voltage scan driver to drive an amorphous-silicon-gate (ASG) circuit on TFT glass. Each single high-voltage scan driver receives logic-level inputs of CPVx and generates two high-voltage outputs of CKVx and CKVBx. The device receives a logic-level input of STV and generates a high-voltage output of STVP. These outputs are swings from Voff (–28 V) to Von (35 V) and are used to drive the ASG circuit and charge/discharge the capacitive loads of the TFT LCD. In order to reduce the power dissipation of the device, a charge-share function is implemented. The device features a discharge function, which shorts Voff to GND in order to shut down the panel faster when the LCD is turned off.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

T_A	ORDERING P/N	PACKAGE	PACKAGE MARKING
–40°C to 85°C	TPS65193RGE	24-Pin 4-mm x 4-mm QFN	TPS65193

(1) The RGE package is available taped and reeled and shipped in quantities of 2500 devices per reel.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

	VALUE	UNIT
Voltage on pins CPVx, STV	–0.3 to 5.5	V
Voltage on pins EN	–0.3 to 5.5	V
Input voltage on VON(2)	40	V
Input voltage on VOFF(2)	–30	V
Voltage on CKVx, CKVBx, CKVCSx, CKVBCSx	–30 to 40	V
VON–VOFF	62	V
Voltage on STVP	–30 to 40	V
Voltage on DISH	–3.6 to 5.5	V
ESD rating HBM	2	kV
ESD rating MM	200	V
ESD rating CDM	700	V
Continuous power dissipation	See *Dissipation Ratings* table	
Operating junction temperature range	–40 to 150	°C
Storage temperature range	–65 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

DISSIPATION RATINGS

PACKAGE	$R_{\theta JA}$	$T_A \le 25°C$ POWER RATING	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
24-pin 4-mm x 4-mm QFN	88°C/ W (Low-K board)	1.13 W	0.62 W	0.45 W

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
VON	Positive high-voltage range	15		35	V
VOFF	Negative low-voltage range	–28		–3	V
VON-VOFF	VON to VOFF voltage range			60	V
f_{CPV}	CPV input frequency			150	kHz
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating junction temperature	–0		125	°C

ELECTRICAL CHARACTERISTICS

VOFF = –10 V, VON = 30 V, EN = 3.3 V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{QIN}	Quiescent current into VON	CPVx = GND, STV = 3.3 V		600	800	µA
	Quiescent current out of VOFF			120	200	
I_{SD}	Shutdown current into VON	CPVx = GND, STV = 3.3 V EN = GND		520	800	µA
	Shutdown current out of VOFF			260	400	
UNDERVOLTAGE LOCKOUT						
V_{UVLO}	Undervoltage lockout threshold on VON	VON rising	10		13	V
		Hysteresis		250		mV
LOGIC SIGNALS EN, CPVx, STV						
V_{IH}	High-level input voltage of CPVx, STV, EN		2			V
V_{IL}	Low-level input voltage of CPVx, STV, EN				0.5	V
OUTPUT CKVx, CKVBx, STVP, CKVCSx						
V_{OH}	Output high voltage of CKVx, CKVBx	I_{OH} = 10 mA	VON – 0.3			V
	Output high voltage of STVP		VON – 0.8			
V_{OL}	Output low voltage of CKVx, CKVBx	I_{OL} = –10 mA			VOFF + 0.2	V
	Output low voltage of STVP				VOFF + 0.4	
R_{CHSH}	Charge-sharing on-resistance	I_{CHSH} = 10 mA		120		Ω
DISCHARGING CIRCUIT						
R_{DSCHG}	Discharging resistance	DISH = –2 V		1.5		kΩ
R_{BIAS}	Resistance DISH to GND			100		kΩ
CONTROL DELAY						
V_{DLYREF}	Reference voltage for comparator			2.9		V
I_{DLYREF}	Delay charge current			15		µA
R_{DLY}	Delay resistor		140	200	260	kΩ

ELECTRICAL CHARACTERISTICS (continued)

VOFF = –10 V, VON = 30 V, EN = 3.3 V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC CHARACTERISTICS						
Slew–	Slew rate, Slew– $_{STVP}$	Load = 4.7 nF (See Figure 1)	30	55		V/µs
Slew+	Slew rate, Slew+ $_{STVP}$		20	35		Vµs
t_{pf}	Propagation delay, $t_{pf\text{-}STVP}$			40	100	ns
t_{pr}	Propagation delay, $t_{pr\text{-}STVP}$			30	100	ns

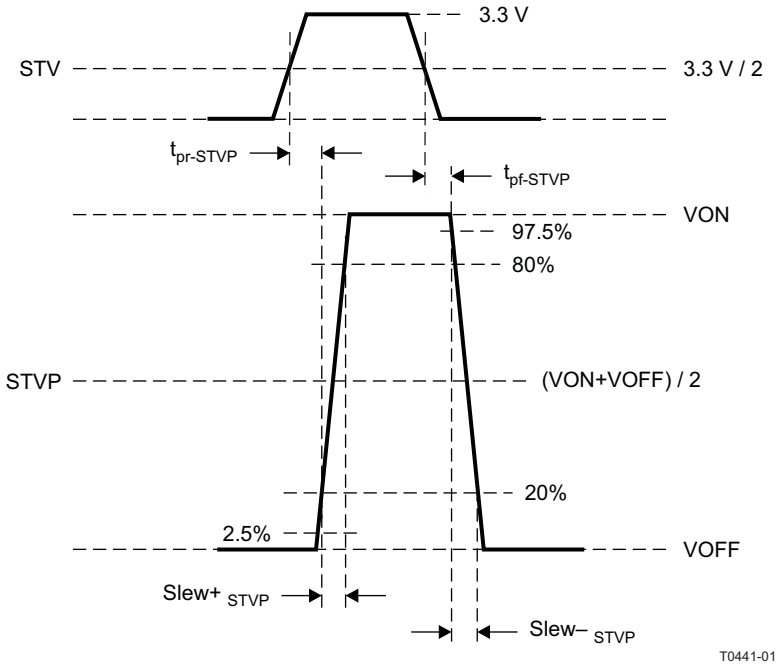


Figure 1. Switching Characteristics of STVP

CKVx, CKVBx SWITCHING CHARACTERISTICS

VOFF = –10 V, VON = 30 V, EN = 3.3 V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{csf}	$t_{csf-CPVx\_CKVx}$, $t_{csf-CPVx\_CKVBx}$	f_{CPVx} = 85 kHz, STV = GND, See Figure 2, load = 4.7 nF, $R_{CS1} = R_{BCS1} = R_{CS2} = R_{BCS2}$ = 50 Ω		80	150	ns
t_{csr}	$t_{csr-CPVx\_CKVx}$, $t_{csr-CPVx\_CKVBx}$			80	150	ns
t_f	t_{f-CPVx_CKVx}, t_{f-CPVx_CKVBx}			40	100	ns
t_r	t_{r-CPVx_CKVx}, t_{r-CPVx_CKVBx}			30	100	ns

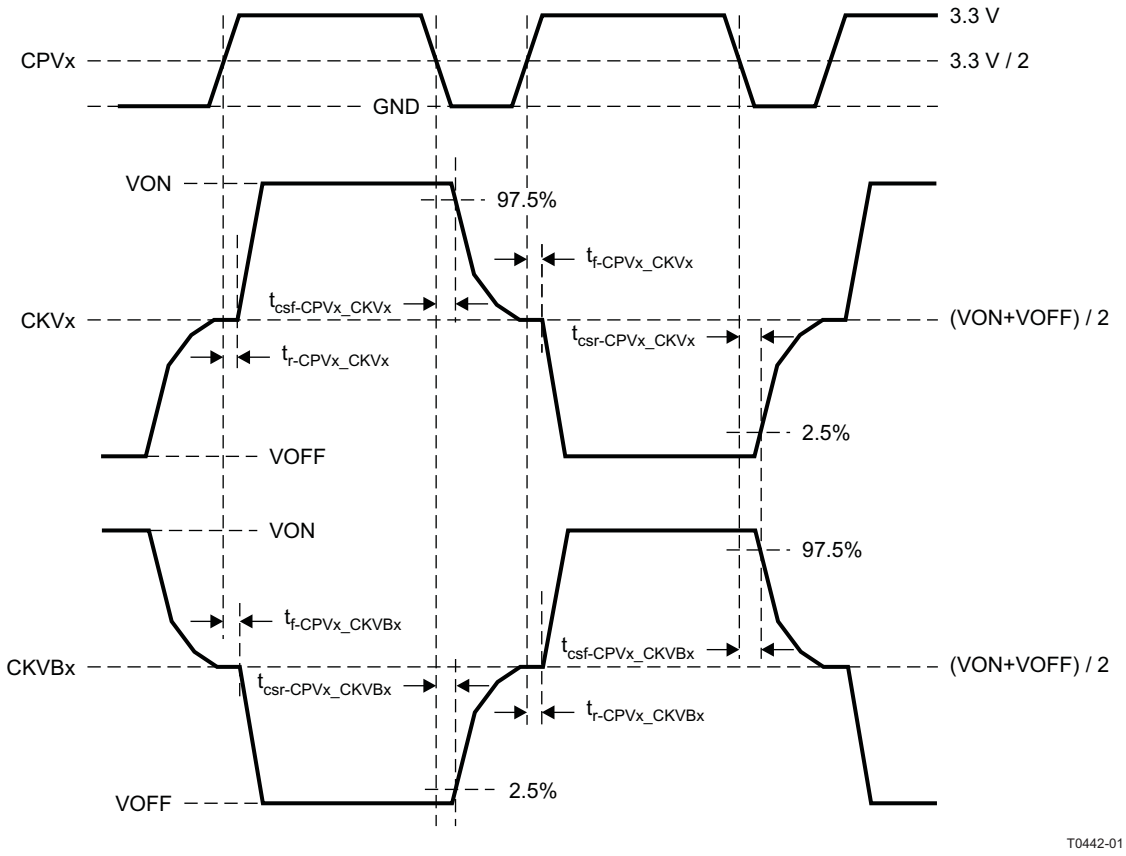


Figure 2. Switching Characteristics of CKVx, CKVBx (STV = GND)

CKVx, CKVBx SWITCHING CHARACTERISTICS (Continued)

VOFF = –10 V, VON = 30 V, EN = 3.3 V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Slew+	Slew+ $_{CKVx}$, Slew+ $_{CKVBx}$	f_{CPVx} = 85 kHz, STV = 3.3 V, See Figure 3, load = 4.7 nF, R_{CSx} = R_{BCSx} = 50 Ω	50	100		V/µs
Slew–	Slew– $_{CKVx}$, Slew– $_{CKVBx}$	f_{CPVx} = 85 kHz, STV = 3.3 V, See Figure 3, load = 4.7 nF, R_{CSx} = R_{BCSx} = 50 Ω	70	130		V/µs

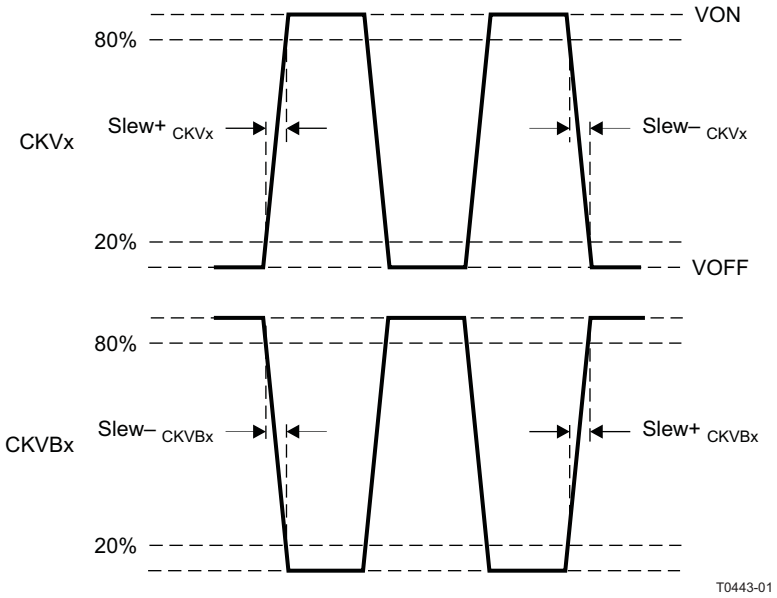
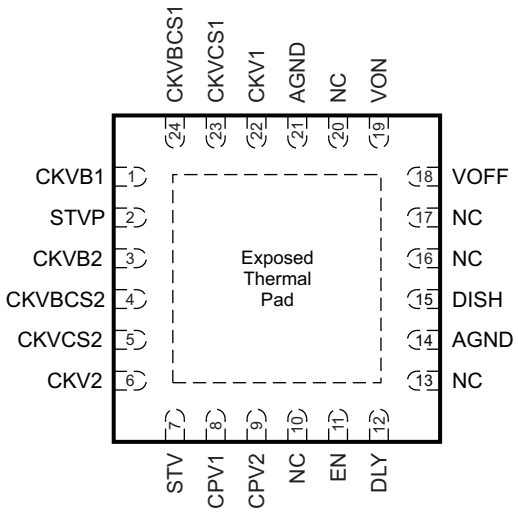


Figure 3. CKVx, CKVBx Output Rise and Fall Times (STV = 3.3 V)

DEVICE INFORMATION

RGE Package
(Top View)



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Exposed thermal pad and NC pins are recommended to be connected with ground on the PCB for better thermal dissipation.

PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
CKV1	22	O	Output vertical-scan clock 1 for ASG
CKV2	6	O	Output vertical-scan clock 2 for ASG
CKVB1	1	O	Inverted-output vertical-scan clock 1 for ASG
CKVB2	3	O	Inverted-output vertical-scan clock 2 for ASG
CKVBCS1	24	I	Charge-share input for CKVB1
CKVBCS2	4	I	Charge-share input for CKVB2
CKVCS1	23	I	Charge-share input for CKV1
CKVCS2	5	I	Charge-share input for CKV2
CPV1	8	I	Input vertical-scan clock 1
CPV2	9	I	Input vertical-scan clock 2
DISH	15	I	VOFF discharge control
DLY	12	O	Connecting a capacitor from this pin to GND allows the setting of the start-up delay.
EN	11	I	Enable pin of device. When this pin is pulled high, the device starts up after a delay time set by DLY has passed.
GND	14, 21	–	Ground
NC	10, 13, 16, 17, 20	–	Not connected
STV	7	I	Input vertical-scan start signal
STVP	2	O	Output vertical-scan start signal
VOFF	18	I	Negative low-supply voltage
VON	19	I	Positive high-supply voltage
Thermal pad		–	Not connected

TYPICAL CHARACTERISTICS

TABLE OF GRAPHS

		FIGURE
SYSTEM PERFORMANCE		
Start-up sequence CKVx	EN = HIGH after UVLO, C_{DLY} = 10 nF, STV = LOW	Figure 4
	EN = HIGH before UVLO, C_{DLY} = 10 nF, STV = LOW	Figure 5
Start-up sequence STVP	EN = HIGH after UVLO, C_{DLY} = 10 nF, CPVx = LOW	Figure 6
	EN = HIGH before UVLO, C_{DLY} = 10 nF, CPVx = LOW	Figure 7
OUTPUT CKVx, CKVBx, and STVP		
Rise time / propagation delay of CKVx	STV = HIGH, load = 4.7 nF	Figure 8
	STV = LOW, load = 4.7 nF	Figure 9
Fall time / propagation delay of CKVx	STV = HIGH, load = 4.7 nF	Figure 10
	STV = LOW, load = 4.7 nF	Figure 11
Rise time / propagation delay of STVP	CPV1 = LOW, load = 4.7 nF	Figure 12
Fall time / propagation delay of STVP	CPV1 = LOW, load = 4.7 nF	Figure 13
STVP output	CPV1 = HIGH	Figure 14
	CPV1 = LOW	Figure 15
CKVx, CKVBx outputs	STV = HIGH	Figure 16
	STV = LOW	Figure 17

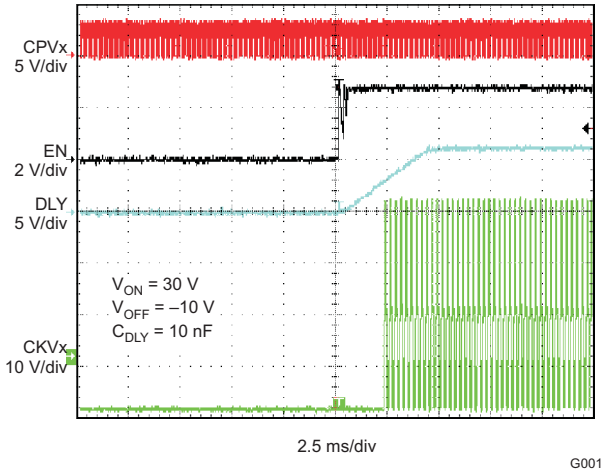


Figure 4. Start-Up Sequence CKVx, EN = HIGH After UVLO

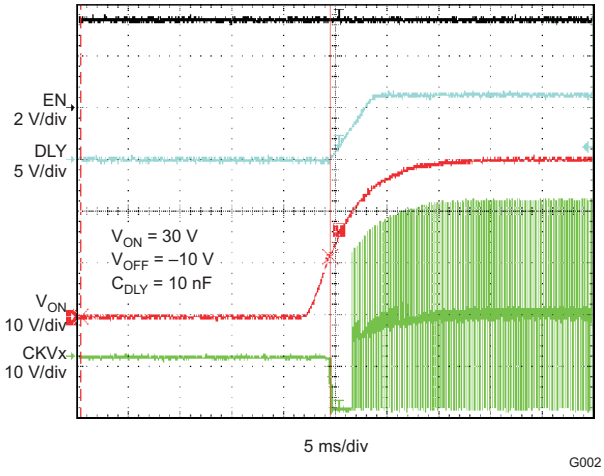


Figure 5. Start-Up Sequence CKVx, EN = HIGH Before UVLO

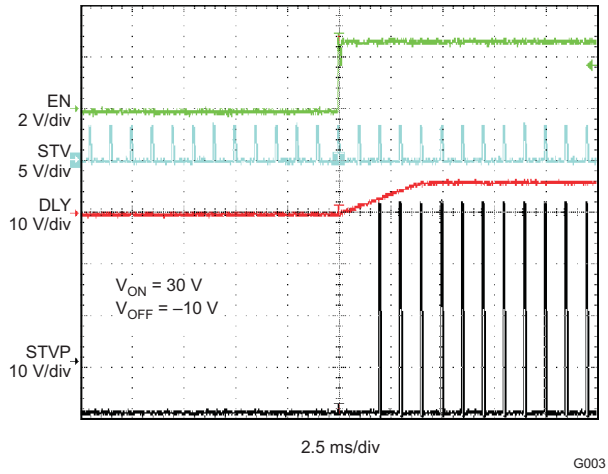


Figure 6. Start-Up Sequence STVP, EN = HIGH After UVLO

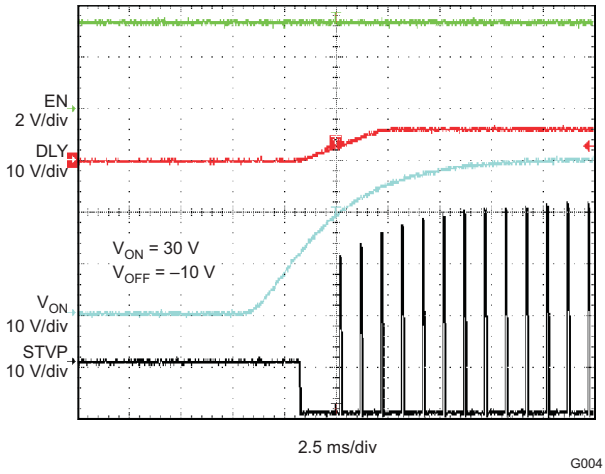


Figure 7. Start-Up Sequence STVP, EN = HIGH After UVLO

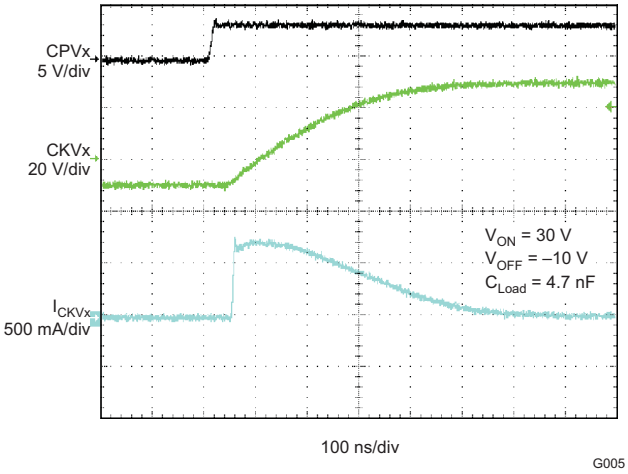


Figure 8. Rise Time / Propagation Delay of CKVx, STV = HIGH

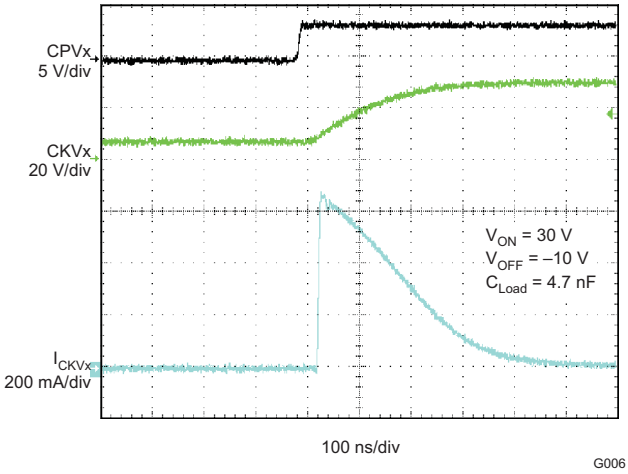


Figure 9. Rise Time / Propagation Delay of CKVx, STV = LOW

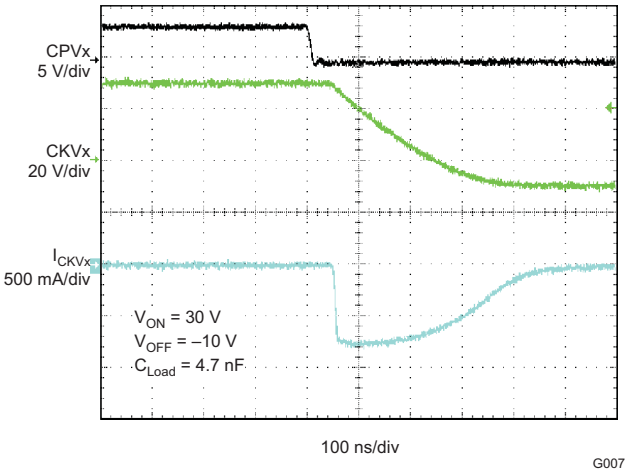


Figure 10. Fall Time / Propagation Delay of CKVx, STV = HIGH

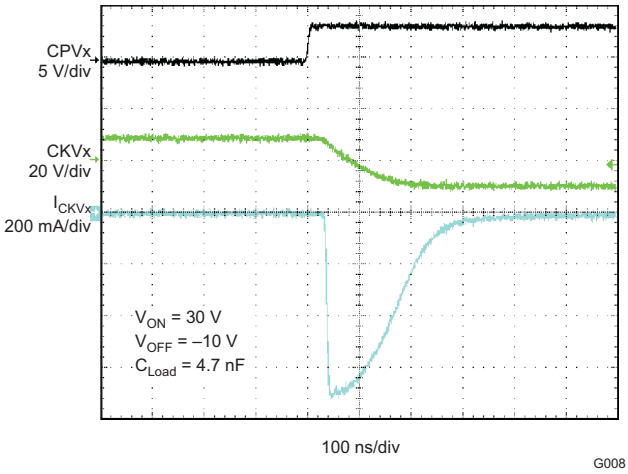


Figure 11. Fall Time / Propagation Delay of CKVx, STV = LOW

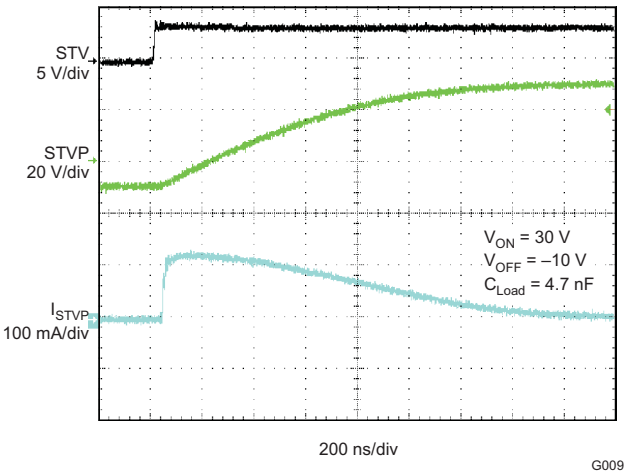


Figure 12. Rise Time / Propagation Delay of STVP, CPV1 = LOW

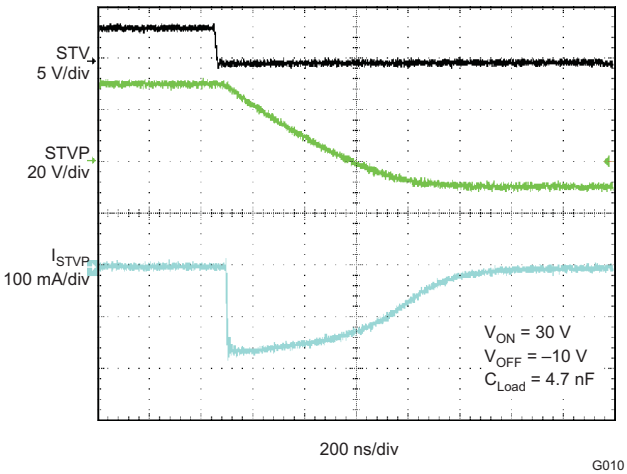


Figure 13. Fall Time / Propagation Delay of STVP, CPV1 = LOW

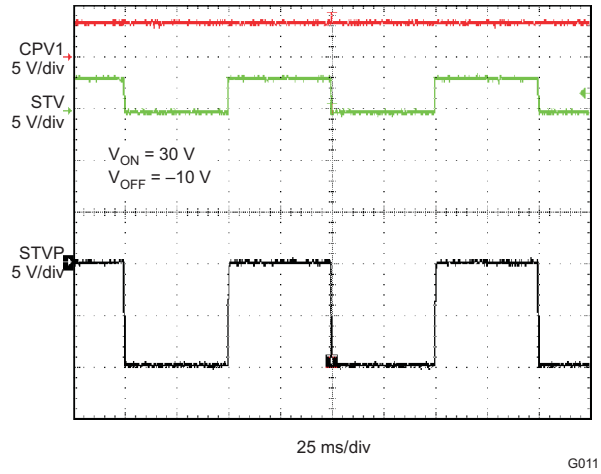


Figure 14. STVP Output, CPV1 = HIGH

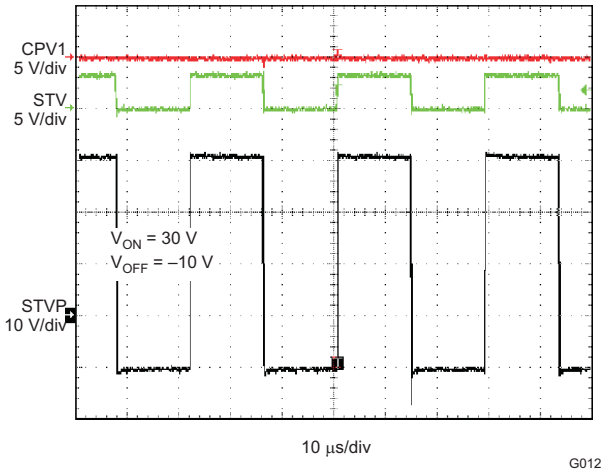


Figure 15. STVP Output, CPV1 = LOW

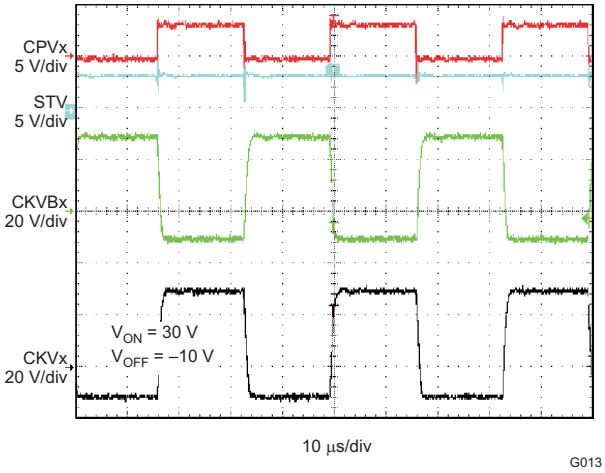


Figure 16. CKVx, CKVBx Outputs, STV = HIGH

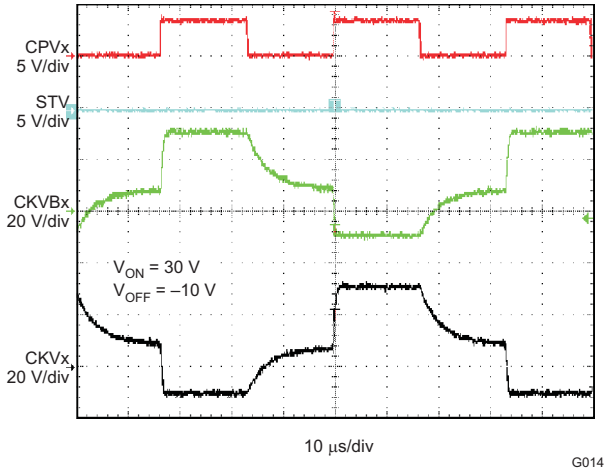
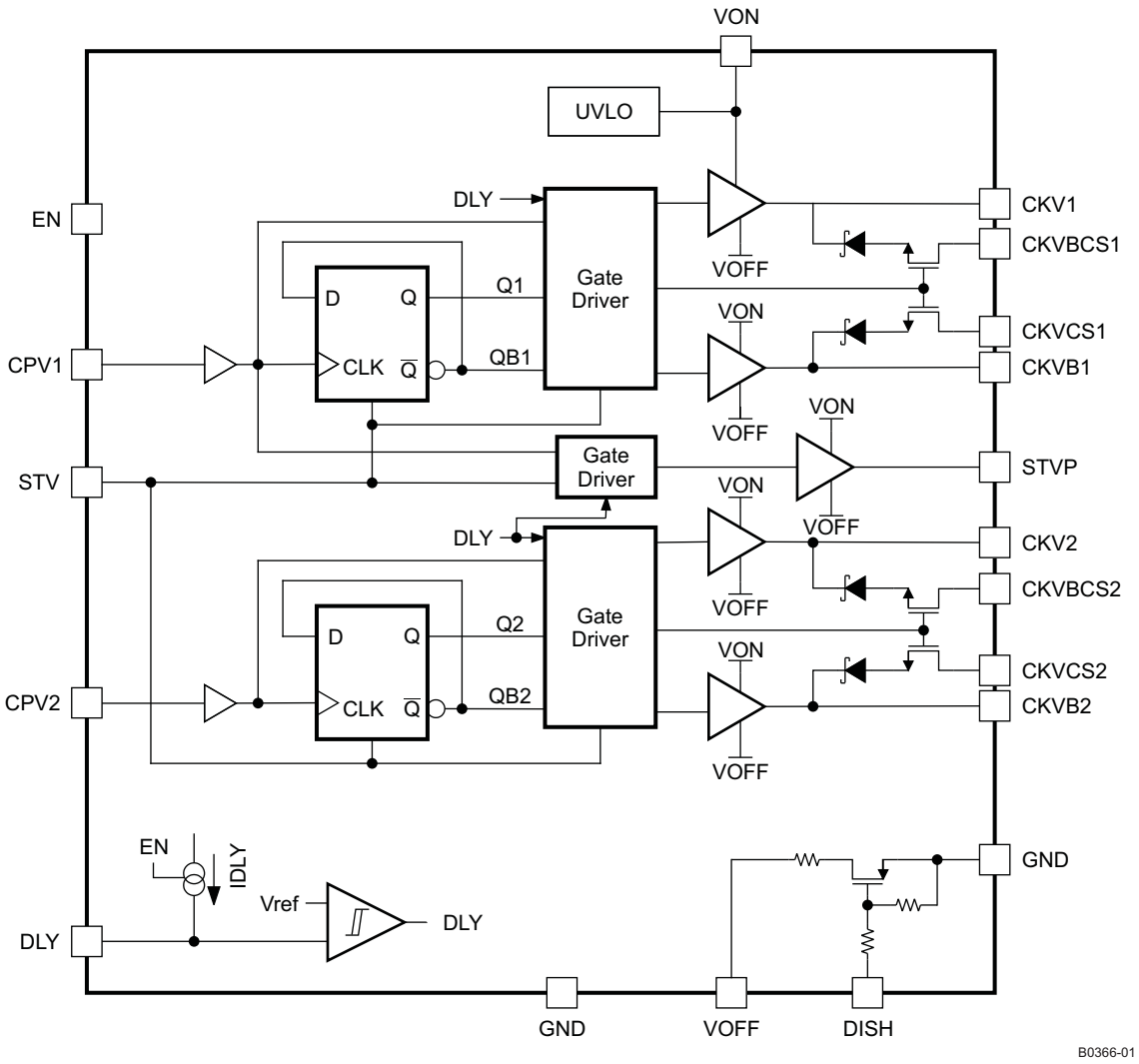


Figure 17. CKVx, CKVBx Outputs, STV = LOW

BLOCK DIAGRAM



DETAILED DESCRIPTION

UNDERVOLTAGE LOCKOUT

The device has an undervoltage lockout feature to avoid improper operation of the device when input voltage VON is low. When VON is lower than 10 V, the device shuts down, and outputs CKVx, CKVBx, and STVP enter the high-impedance state.

INPUT SIGNALS

The timing controller in the system provides input signals to the TPS65193. STV is the synchronous signal for picture frames, and its frequency depends on the frame rate. CPVx are the synchronous signals for horizontal lines, and their frequency depends on the frame rate and vertical resolution.

OUTPUT SIGNALS

The STVP, CKVx, and CKVBx scan-driver outputs are generated with internal switches. Table 1 and Table 2 show the logic diagrams of the scan-driver outputs.

Table 1. STVP Logic Diagram

INPUT		OUTPUT
STV	**CPV1**	**STVP**
LOW	Don't care	VOFF
HIGH	LOW	VON
HIGH	HIGH	High impedance

Table 2. CKVx, CKVBx, and Output Charge-Share Logic

INPUT		OUTPUT		
STV	**CPVx**	**CKVx**	**CKVBx**	**CHARGE SHARE**
LOW	LOW	High impedance	High impedance	Enable
LOW	Rising edge	Toggle state	Toggle state	Disable
LOW	HIGH	Previous state	Previous state	Disable
HIGH	LOW	VOFF	VON	Disable
HIGH	HIGH	VON	VOFF	Disable

OUTPUT CHARGE SHARE

Power dissipation can be reduced by the output charge share. Figure 18 shows the current flows when the charge share is enabled. CKVCSx and CKVBCSx are charge-share inputs. When the charge share is enabled, the charge that is in the capacitor of the positive voltage line is transferred to the capacitor of the negative voltage line. Charge-sharing resistors RCSx and RBCSx reduce the peak current into the charge-share inputs, CKVCSx and CKVBCSx, during the output charge share. These resistors also control the slope of the output charge-share waveform. The smaller RCSx and RBCSx, the bigger the peak current into the charge-share inputs and the steeper the slope of output charge-share waveform. The power dissipation in charge-sharing resistors should be taken into consideration. With 0603 size resistors, the power rating of two in parallel is good for most applications.

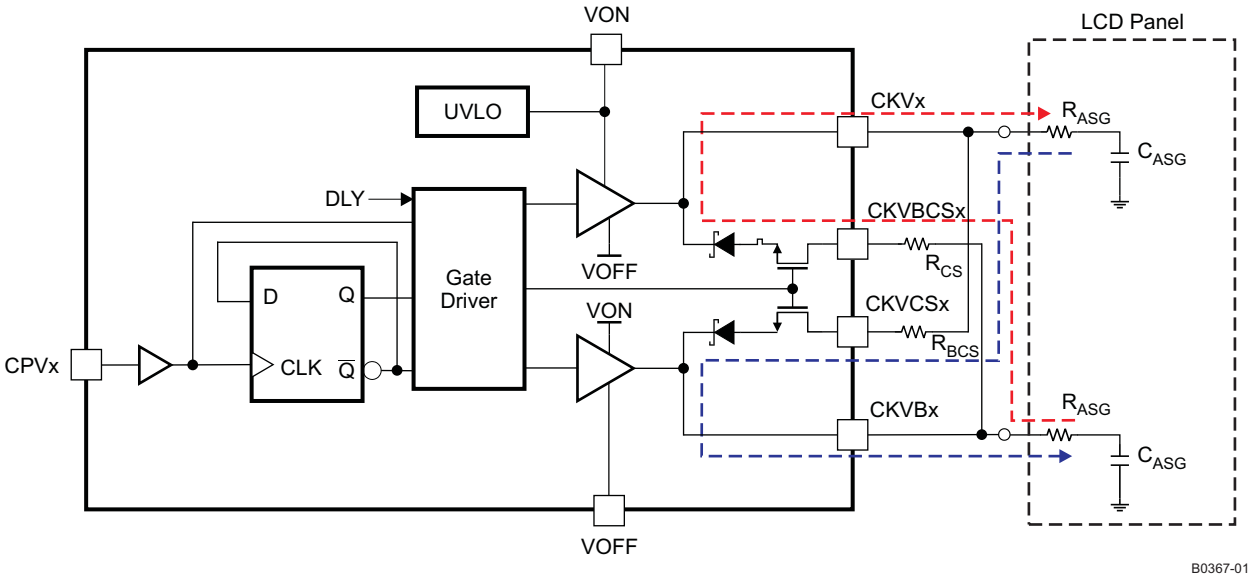


Figure 18. Single-Scan Driver Block Diagram

START-UP SEQUENCE (EN, DLY)

The TPS65193 has adjustable start-up sequencing that is set by EN and DLY. When VON is below the UVLO threshold, all outputs are at high impedance. When EN is pulled LOW after the UVLO threshold is reached, all

outputs follow VOFF. Pulling EN high enables the device after a delay time set by the capacitor connected to DLY, and the delay time starts with EN = HIGH. If EN is pulled high before the UVLO threshold is reached, the delay starts when VON reaches the UVLO threshold. Pulling EN low disables the device and outputs CKVx, CKVBx, and STVP follow VOFF as long as VON is higher than the UVLO threshold. For the typical start-up sequence, see Figure 19 and Figure 20.

SETTING THE DELAY TIME (DLY)

Connecting an external capacitor to the DLY pin sets the delay time. If no delay time is required, the DLY pin can be left floating. The external capacitor is charged with a constant-current source of typically 15 μA. The delay time is terminated when the capacitor voltage reaches the internal reference voltage of 2.9 V, and the final DLY voltage on an external capacitor is maximum 8 V.The voltage rating of the external capacitor must be higher than 8 V.

The external delay capacitor is calculated using the following formula:

$$C_{DLY} = \frac{\text{Delay time}}{R_{DLY}} = \frac{\text{Delay time}}{200\,k\Omega} \quad (1)$$

Example for setting a delay time of 10 ms:

$$C_{DLY} = \frac{10\,ms}{200\,k\Omega} = 50\,nF \approx 47\,nF \quad (2)$$

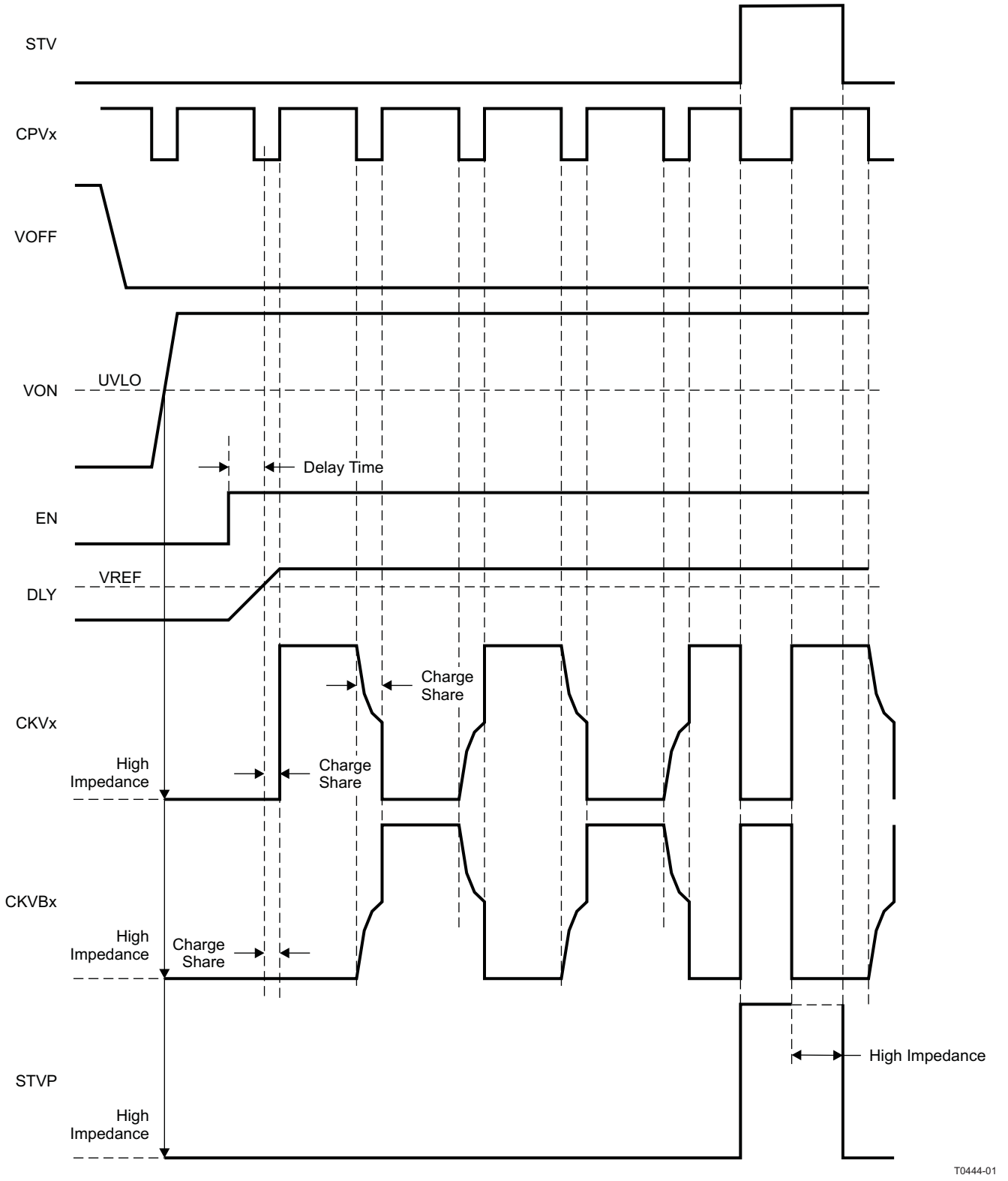


Figure 19. Start-Up Sequence With EN = High After UVLO Threshold

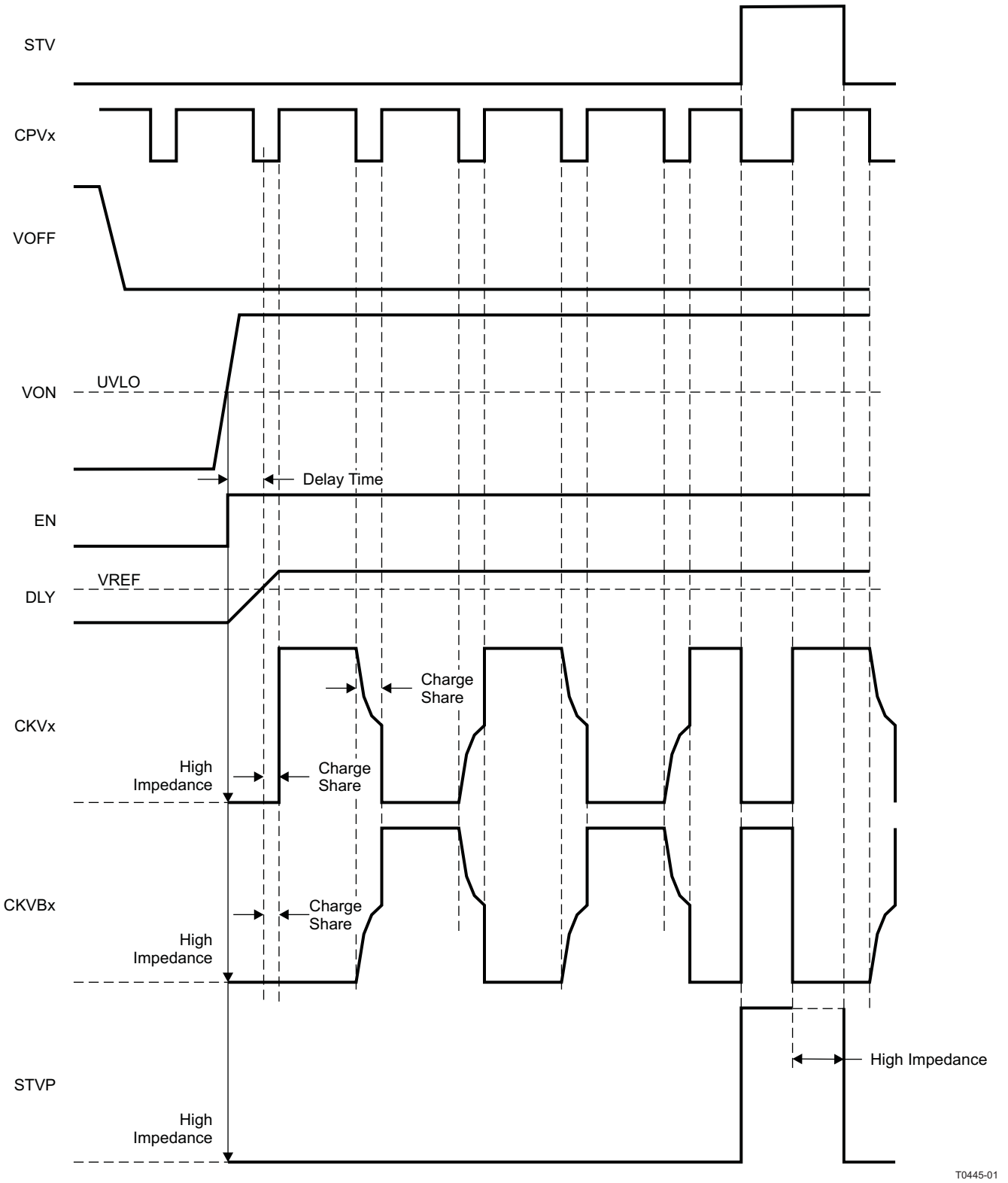


Figure 20. Start-Up Sequence With EN = High Before UVLO Threshold

TIMING DIAGRAM OF SCAN DRIVER

Figure 21 shows the typical timing diagram of the TPS65193.

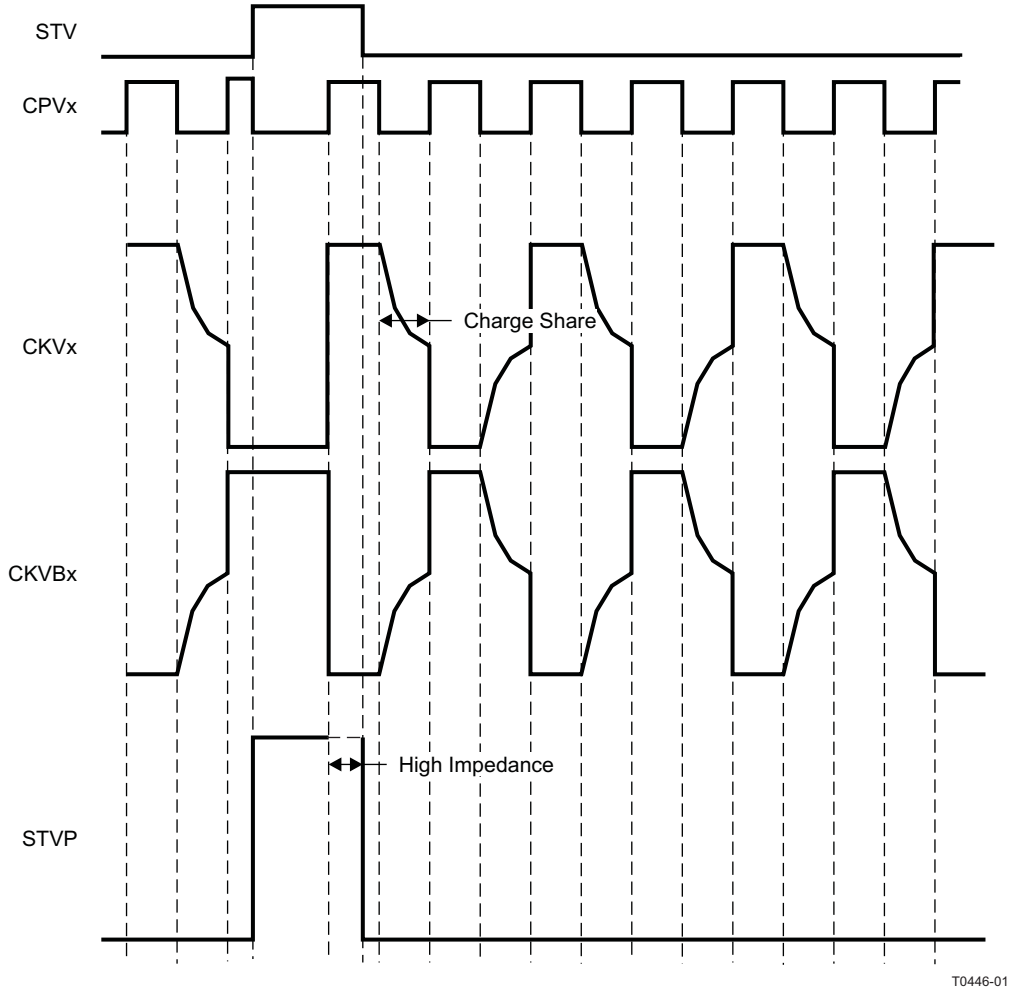


Figure 21. Scan Driver Timing Diagram

SUPPLY VOLTAGE, VON and VOFF

The TPS65193 drives the capacitive load. The high peak currents should be supplied from VON on the rising edges of the outputs and VOFF on the falling edges of the outputs, respectively. Bypass capacitors of 1 μF must be placed as close as possible on both VON and VOFF supplies. Depending on the peak current that the TPS65193 must deliver, the bypass capacitor can be bigger than 1 μF.

VOFF DISCHARGE

DISH controls the VOFF discharging time during the system power off. Figure 22 shows a typical application for VOFF discharge. DISH is connected to the system logic voltage through a capacitor. During power off, the system logic voltage falls, and the voltage on DISH falls below ground level. An internal switch turns on when DISH is below –0.6 V and VOFF is connected to ground through 1 kΩ, which helps VOFF discharge. A 1-μF DISH capacitor is good for most applications. Figure 23 shows the typical power-off sequence of VOFF discharging. VOFF discharge can be disabled by connecting DISH to GND directly.

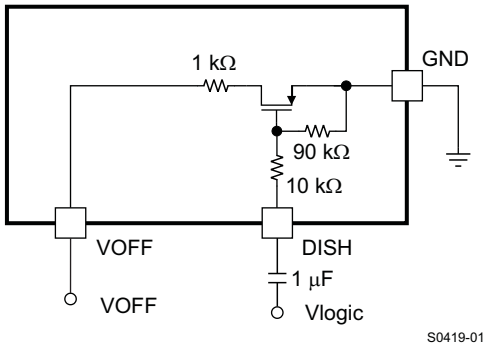


Figure 22. Typical Application for VOFF Discharge

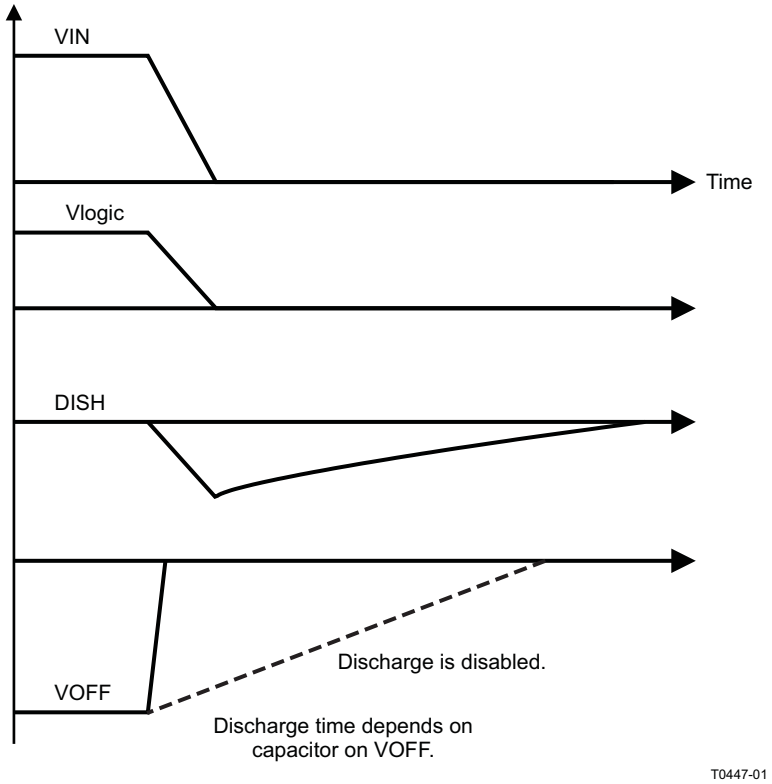


Figure 23. Power-Off Sequence of VOFF Discharge

TYPICAL APPLICATION

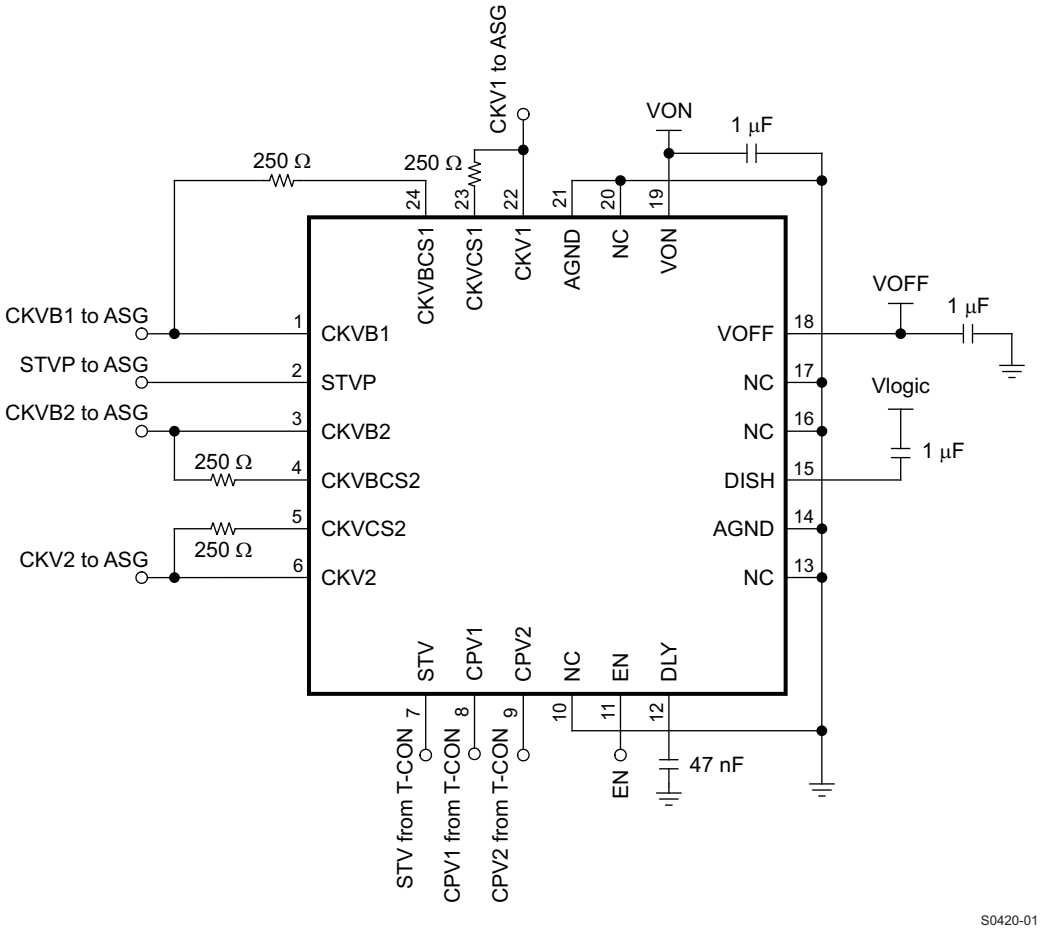


Figure 24. Typical Application With VOFF Discharge Enabled

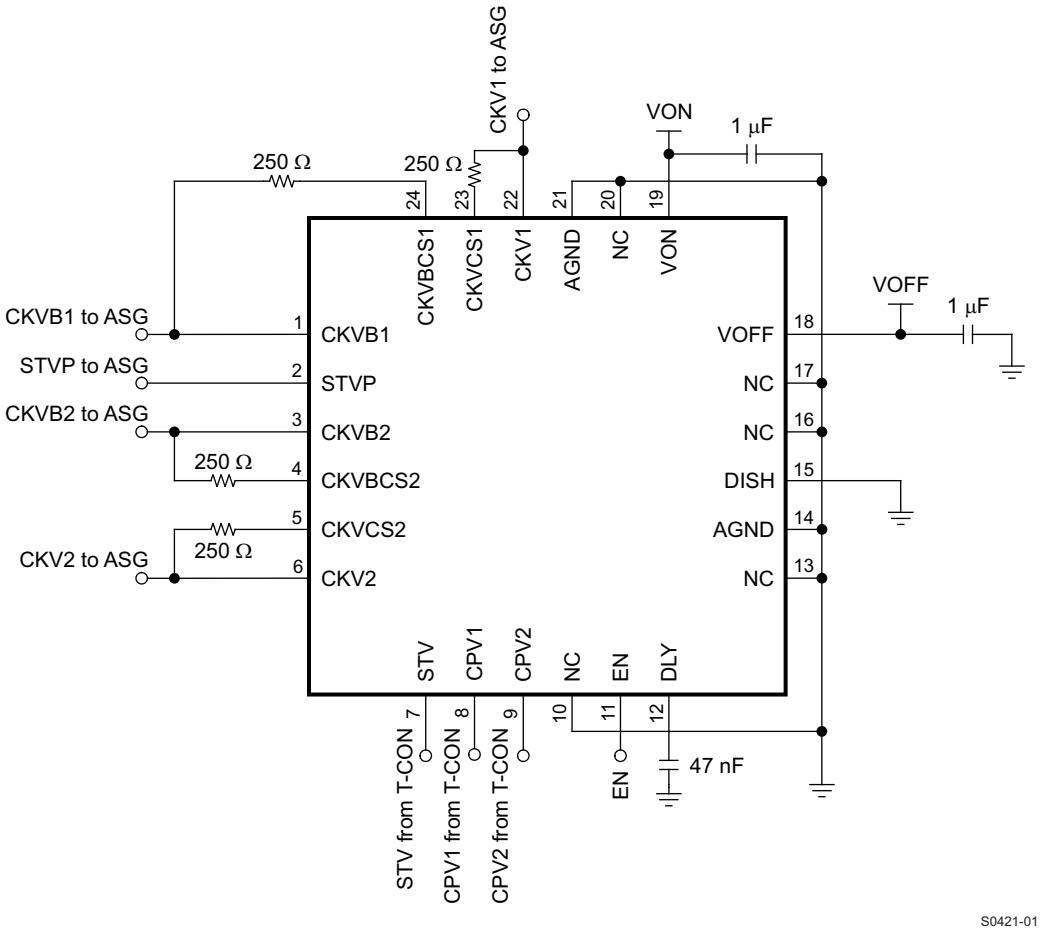


Figure 25. Typical Application With VOFF Discharge Disabled

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS65193RGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65193	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

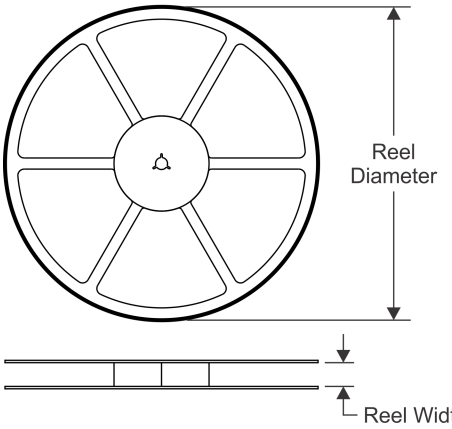
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

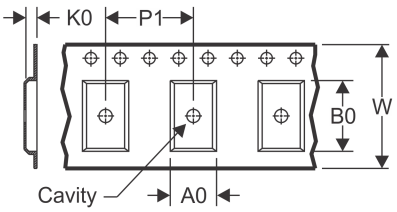
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

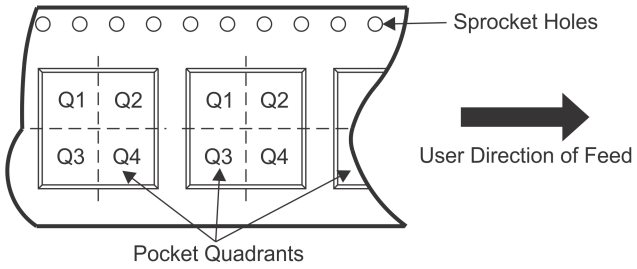


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

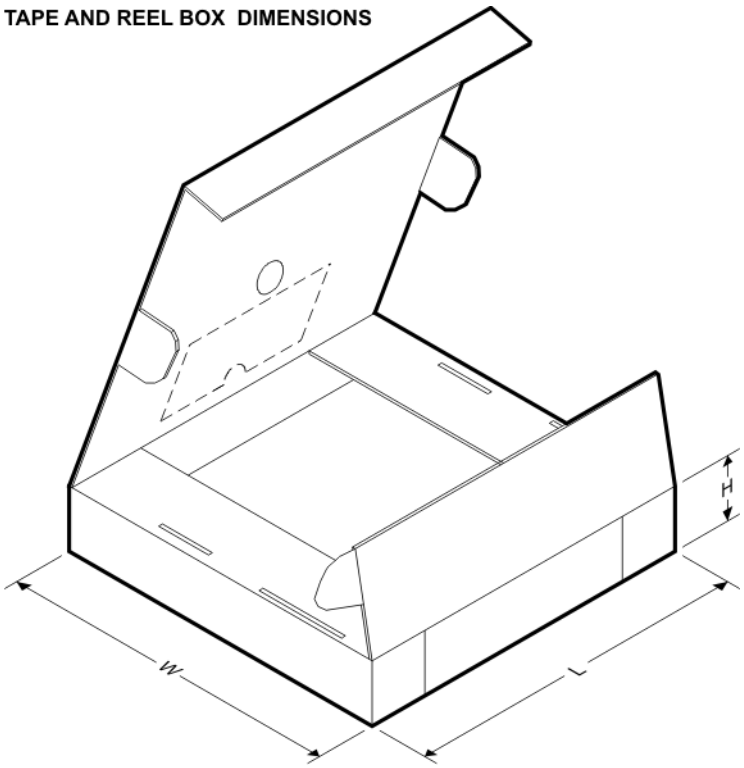
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65193RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

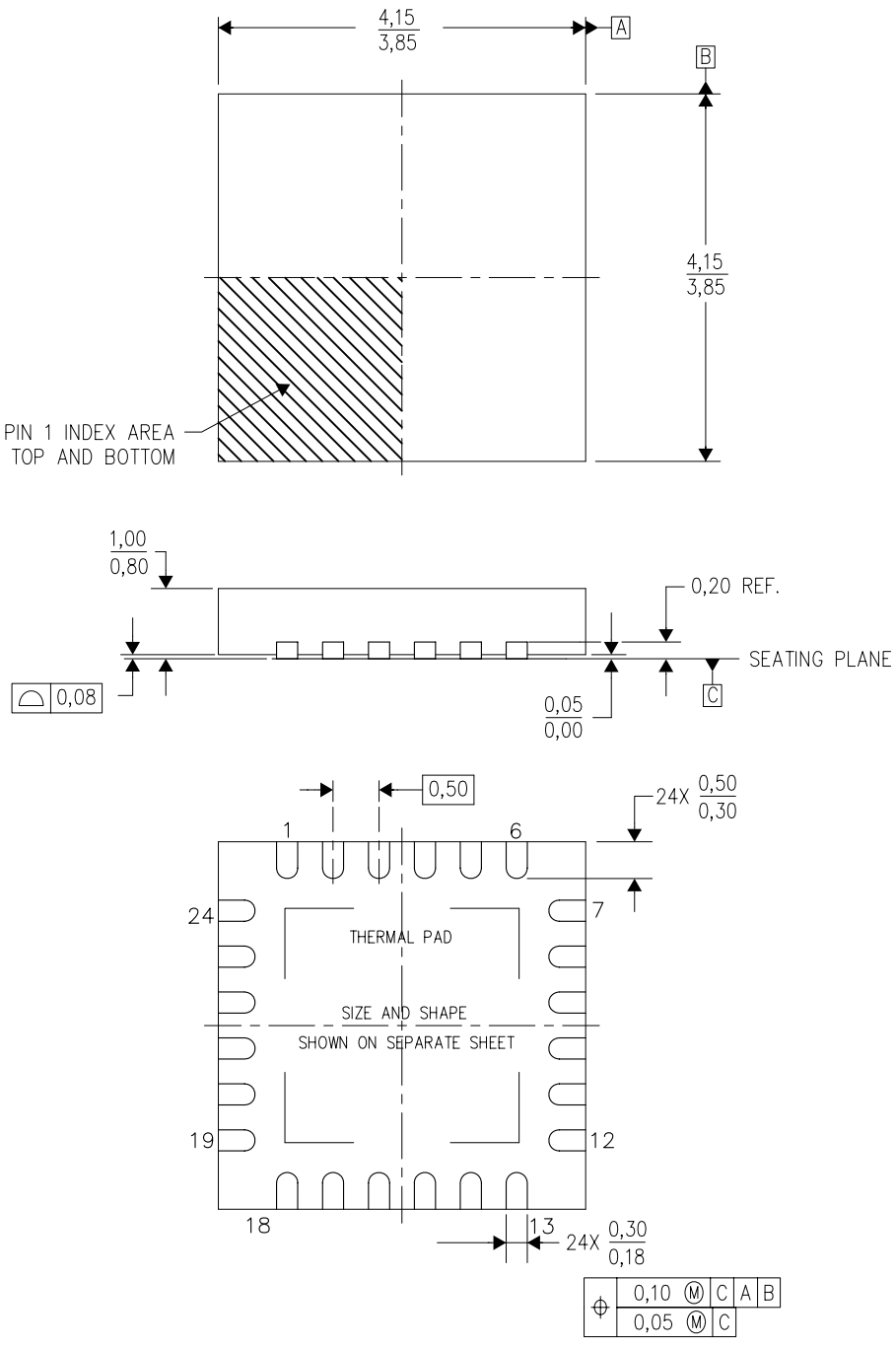
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65193RGER	VQFN	RGE	24	3000	367.0	367.0	35.0

RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

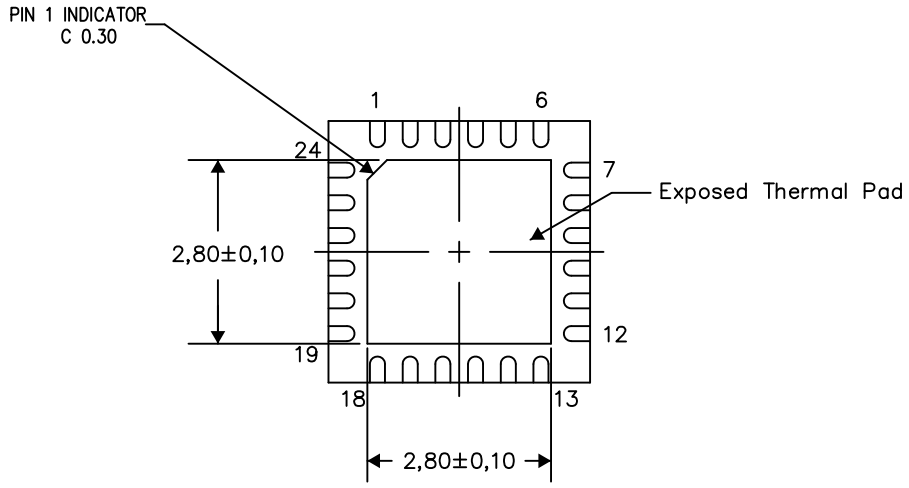
RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



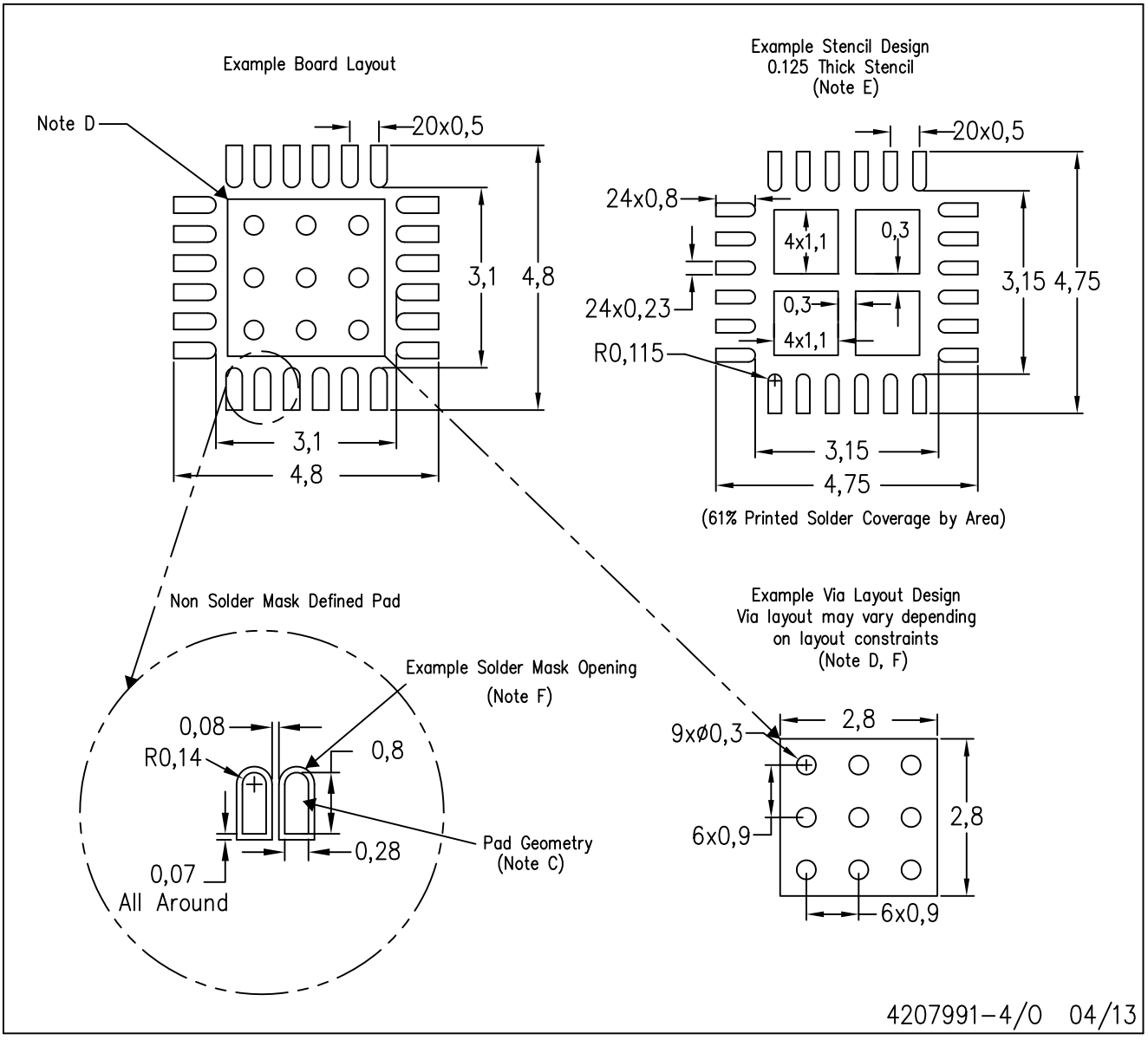
Bottom View

Exposed Thermal Pad Dimensions

4206344–5/AC 03/13

NOTES: A. All linear dimensions are in millimeters

RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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