TPS60151 5V/140mA Charge Pump Device

FEATURES

- 2.7V to 5.5V Input Voltage Range
- Fixed Output Voltage of 5.0V
- Output Reverse Current Protection
- X2 Charge Pump
- 1.5 MHz Switching Frequency
- Maximum Output Current : 140mA
- 2X2 QFN With 0.8mm Height
- Typical 90μA Quiescent Current at no Load Condition (Skip mode)
- Hardware En/Disable Function
- Built-in Soft Start
- Built-in Under Voltage Lock Out Protection
- Thermal and Over Current Protection

APPLICATIONS

- USB OTG
- HDMI
- Portable Communication Devices
- Personal Digital Assistance
- PCMCIA Cards
- Cellular Phones
- Handheld Meters

DESCRIPTION

The TPS60151 is a switched capacitor voltage converter which produces a regulated, low noise, and low-ripple output voltage (5V) from an unregulated input voltage. It maintains 5V regulation even when V_{IN} is greater than 5V.

The 5V output can supply a minimum of 140mA current with a small 2X2 QFN package.

TPS60151 operates in *skip mode* when the load current falls below 8mA under typical condition. In skip mode operation, quiescent current is reduced to 90μA.

Only 3 external capacitors are needed to generate the output voltage, thereby saving PCB space.

Inrush current is limited by the soft start function during power on and power transient states.

The TPS60151 has built-in current limit and output reverse current protection that are ideal for HDMI, USB OTG and other battery powered applications.
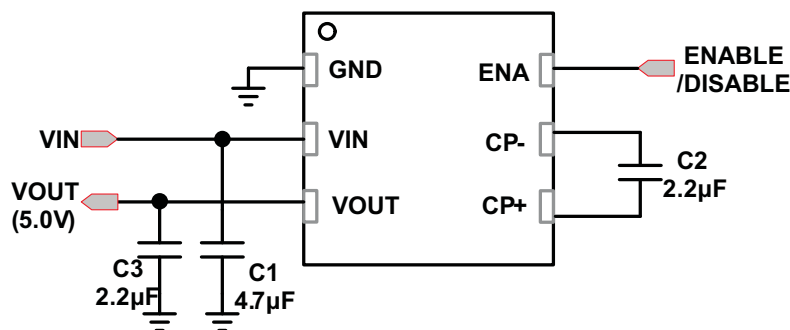

Figure 1. Typical Application Circuit

ORDERING INFORMATION

T$_A$	PART NUMBER[1]	OUTPUT VOLTAGE	PACKAGE[2]	PACKAGE DESIGNATOR	ORDERING	PKG MARKING
−40°C to 85°C	TPS60151	5.0V	SON 2x2-6	DRV	TPS60151DRV	OCN

(1) The DRV (2-mm x 2-mm 6-terminal SON) package is available in tape on reel. Add R suffix to order quantities of 3000 parts per reel and T suffix to order quantities with 250 parts per reel.

(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) [1]

		VALUE	UNIT
V_I	Input voltage range (all pins)	−0.3 to 7	V
	HBM ESD Rating [2]	2	kV
	CDM ESD Rating [3]	500	V
	MM ESD Rating [4]	200	V
T_A	Operating temperature range	−40 to 85	°C
T_J	Maximum operating junction temperature	150	°C
T_{st}	Storage temperature	−55 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The Human body model (HBM) is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. The testing is done according JEDECs EIA/JESD22-A114.
(3) Charged Device Model
(4) Machine Model (MM) is a 200pF capacitor discharged through a 500nH inductor with no series resistor into each pin. The testing is done according JEDECs EIA/JESD22-A115.

DISSIPATION RATINGS[1] [2]

PACKAGE	THERMAL RESISTANCE RΘJA	T_A = 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 85°C POWER RATING
Low-K(1) DRV	140°C/W	715 mW	7.1 mW/°C	285 mW
High-K(2) DRV	65°C/W	1540 mW	15.4 mW/°C	615 mW

(1) The JEDEC low-K (1s) board used to derive this data was a 3inx3in, two-layer board with 2-ounce copper traces on top of the board.
(2) The JEDEC high-K (2s2p) board used to derive this data was a 3inx3in, multilayer board with 1-ounce internal power and ground planes and 2-ounce copper traces on top and bottom of the board.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range	2.7		5.5	V
T_A	Operating ambient temperature	−40		85	°C
T_J	Operating junction temperature	−40		125	°C
C_{in}	Input capacitor	2.2			µF
C_o	Output capacitor	2.2			µF
C_f	Flying capacitor	1.0			µF

ELECTRICAL CHARACTERISTICS

V_{IN}=3.6V, T_A = −40°C to 85°C, typical values are at T_A = 25°C, C1 = C3 = 2.2µF, C2 = 1.0µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER STAGE						
V_{IN}	Input voltage range		2.7		5.5	V
V_{UVLO}	Undervoltage lockout threshold			1.9	2.1	
I_Q	Operating quiescent current	I_{OUT} = 140 mA, Enable = V_{IN}		4.7		mA
I_{Qskip}	Skip mode operating quiescent current	I_{OUT} = 0 mA, Enable=V_{IN} (No switching)		80		µA
		I_{OUT} = 0 mA, Enable = V_{IN}(Minimum switching)		90		µA
I_{SD}	Shut down current	2.7 V ≤ V_{IN} ≤ 5.5 V, Enable = 0 V		4	10	µA
V_{OUT}	Output voltage[1]	I_{OUT} ≤ 50 mA, 2.7 V ≤ V_{IN} < 5.5V	4.8	5.0	5.2	V
$V_{OUT(skip)}$	Skip mode output voltage	I_{OUT} = 0 mA, 2.7 V ≤ V_{IN} ≤ 5.5 V		V_{OUT}+0.1		V
F_{SW}	Switching frequency			1.5		MHz

(1) When in skip mode, Output voltage can exceed V_{OUT} spec because $V_{OUT(skip)}$= V_{OUT}+0.1.

Product Folder Link(s) :*TPS60151*

ELECTRICAL CHARACTERISTICS (continued)

V_{IN}=3.6V, T_A = −40°C to 85°C, typical values are at T_A = 25°C, C1 = C3 = 2.2µF, C2 = 1.0µF (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{SS}	Soft-start time	From the rising edge of enable to 90% output		150		µs
OUTPUT CURRENT						
I_{OUT_nom}	Maximum output current	V_{OUT} remains between 4.8 V and 5.2 V, 3.1 V ≤ V_{IN} ≤ 5.5 V	120			mA
		3.3 V < V_{IN} < 5.5 V	140			
I_{OUT_max}	Current limit	V_{OUT} = 4.5 V			500	mA
I_{OUT_short}	Short circuit current[2]	V_{OUT} = 0 V		80		mA
RIPPLE VOLTAGE						
V_R	Output ripple voltage	I_{OUT} = 140 mA		30		mV
ENABLE CONTROL						
V_{HI}	Logic high input voltage	2.7 V ≤ V_{IN} ≤ 5.5 V	1.3		V_{IN}	V
V_{LI}	Logic low input voltage		−0.2		0.4	V
I_{HI}	Logic high input current				1	µA
I_{LI}	Logic low input current				1	µA
THERMAL SHUTDOWN						
T_{SD}	Shutdown temperature			160		°C
T_{RC}	Shutdown recovery			140		°C

(2)   TPS60151 has internal protection circuit to protect IC when V_{OUT} shorted to GND.
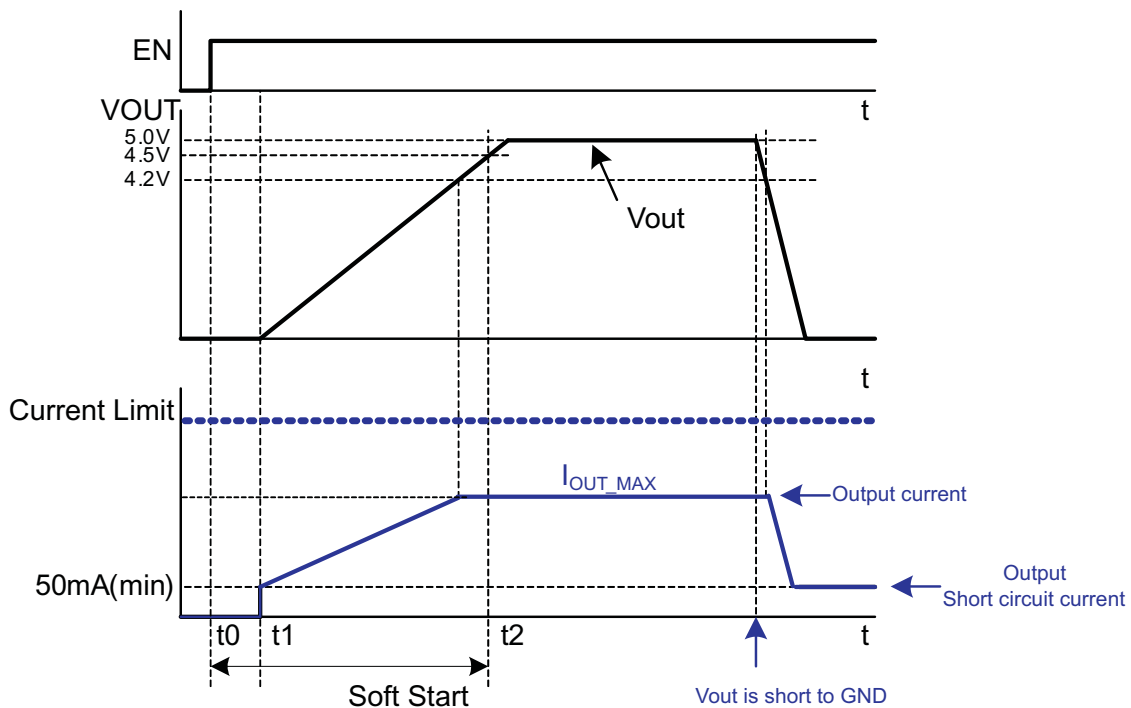
Figure 2. Maximum Output Current Capability and Short Circuit protection

DEVICE INFORMATION

PIN ASSIGNMENTS (TOP VIEW)

QFN (2x2)
(TOP VIEW)

GND — ENA
VIN — CP-
VOUT — CP+
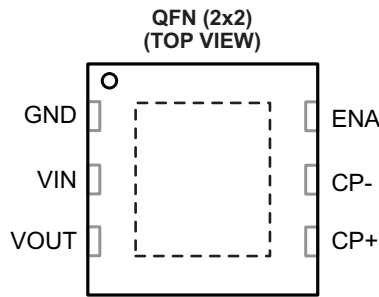
PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	1	–	Ground
VIN	2	I	Supply voltage input
VOUT	3	O	Output, Connect to the output capacitor
CP+	4	–	Connect to the flying capacitor
CP–	5	–	Connect to the flying capacitor
ENA	6	I	Hardware Enable/Disable Pin (High = Enable)

FUNCTIONAL BLOCK DIAGRAM
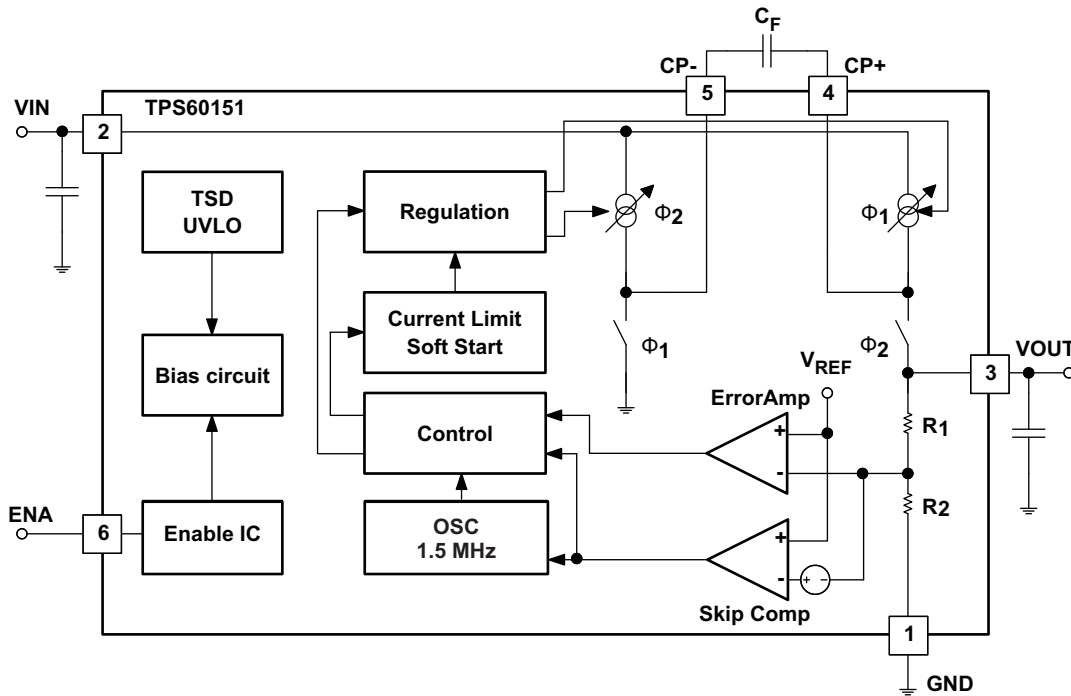
Figure 3. Functional Block Diagram

Product Folder Link(s) :*TPS60151*

TYPICAL CHARACTERISTICS

Table of Graphs

TITLE	DESCRIPTION	FIGURE
Load Regulation Curve	Output voltage vs output current, V_{IN} = Variable, I_{OUT} = Sweep, Temperature = 25°C	Figure 4
Line Regulation Curve	Output voltage vs input voltage, V_{IN} = Sweep, I_{OUT} = Variable, Temperature = 25°C	Figure 5
Efficiency Curve	Efficiency vs input voltage, V_{IN} = Sweep, I_{OUT} = Variable, Temperature = 25°C	Figure 6
Quiescent Current Curve	Quiescent current vs input voltage, V_{IN} = Sweep, I_{OUT} = 0, Temperature = Variable	Figure 7
Maximum Output Current Curve	Maximum output current vs input voltage, V_{IN} = Sweep, Temperature = Variable	Figure 8
Load Transient Curve	Output voltage vs load current	Figure 9
		Figure 10
Output Ripple	Output ripple	Figure 11
	Load transient	Figure 12
	Output ripple voltage (Normal mode)	Figure 13
		Figure 14
Power ON	Power on start up	Figure 15
		Figure 16
Enable / Disable	Soft start when enable	Figure 17
		Figure 18
TSD Operation	V_{IN} = 5.5V, R_{LOAD} = 20Ω	Figure 19

OUTPUT VOLTAGE vs OUTPUT CURRENT

Figure 4.

OUTPUT VOLTAGE vs INPUT VOLTAGE

Figure 5.

**EFFICIENCY
vs
INPUT VOLTAGE**

Figure 6.

**QUIESCENT CURRENT
vs
INPUT VOLTAGE**

Figure 7.

**MAXIMUM OUTPUT CURRENT
vs
INPUT VOLTAGE AT TEMPERATURE**
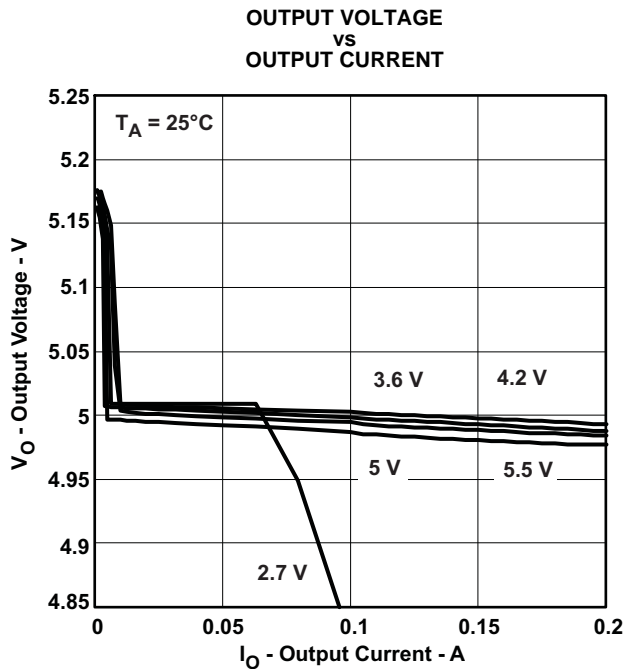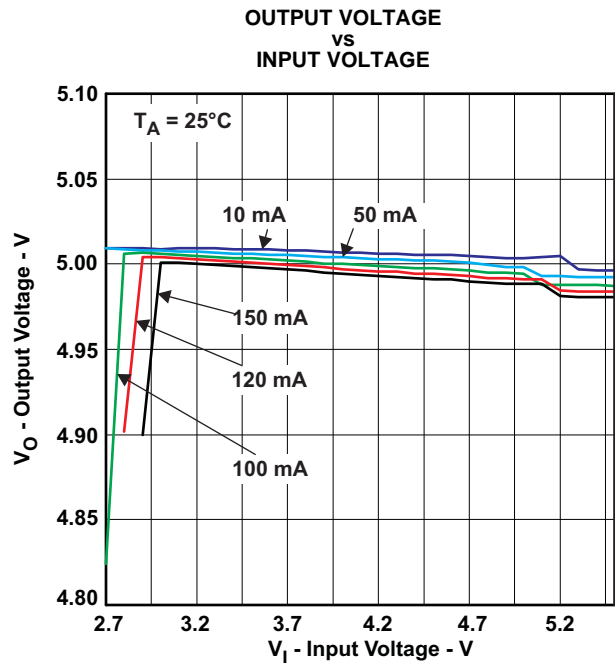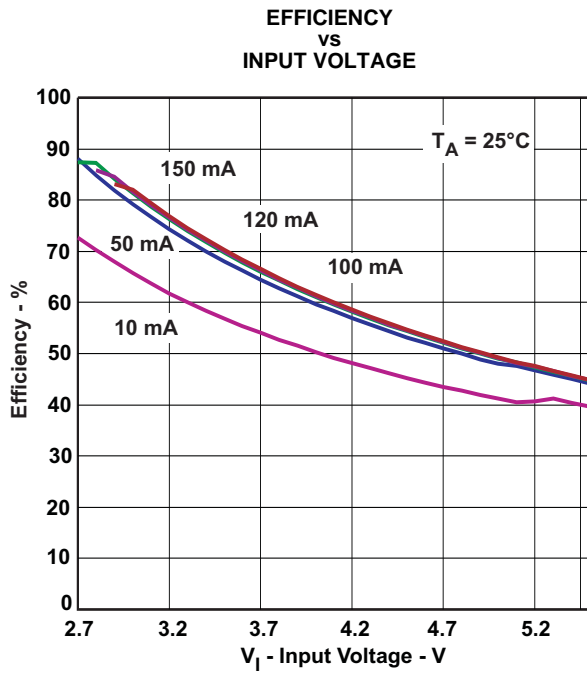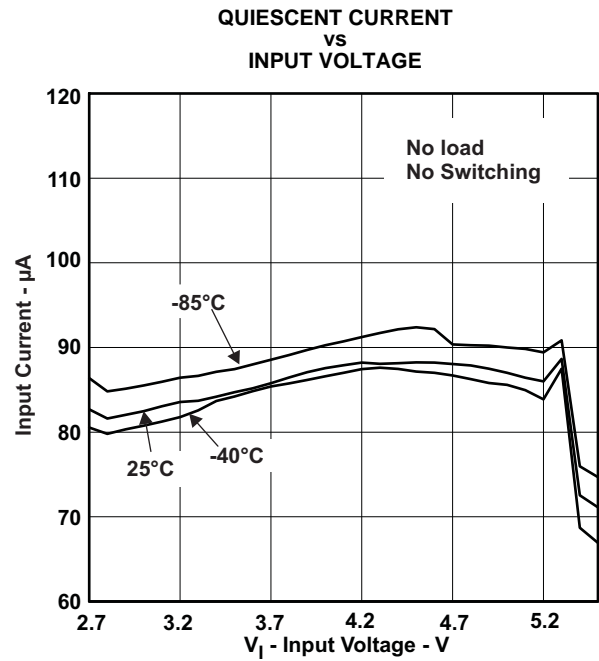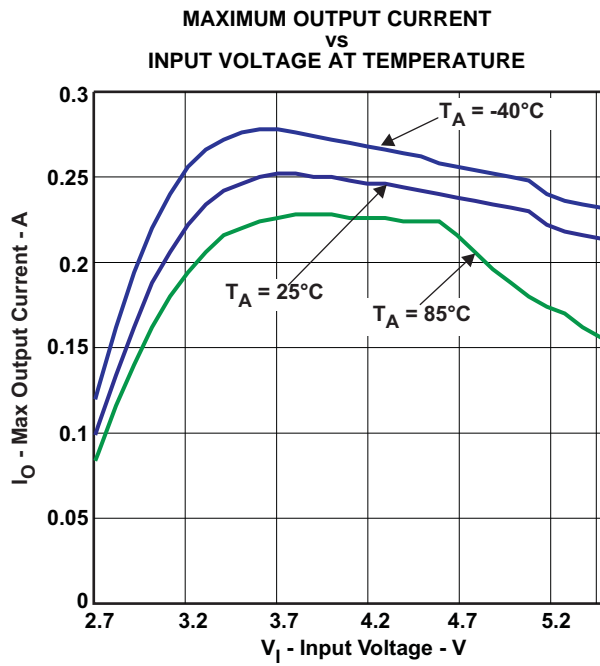
Figure 8.

LOAD TRANSIENT RESPONSE
V_{IN} = 2.7 V, Io = 30 mA to 50 mA
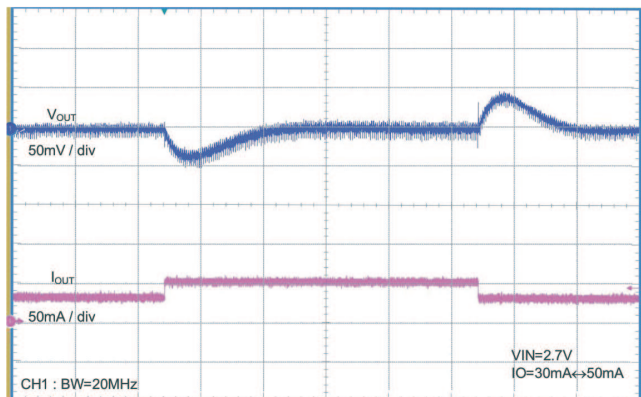
20 µs/div

Figure 9.

LOAD TRANSIENT RESPONSE
V_{IN} = 3.6 V, Io = 60 mA to 100 mA
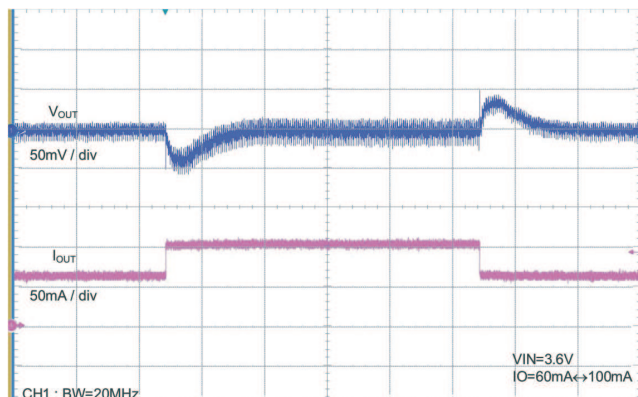
20 µs/div

Figure 10.

OUTPUT RIPPLE
V_{CC} = 2.7 V, Io = 0 mA
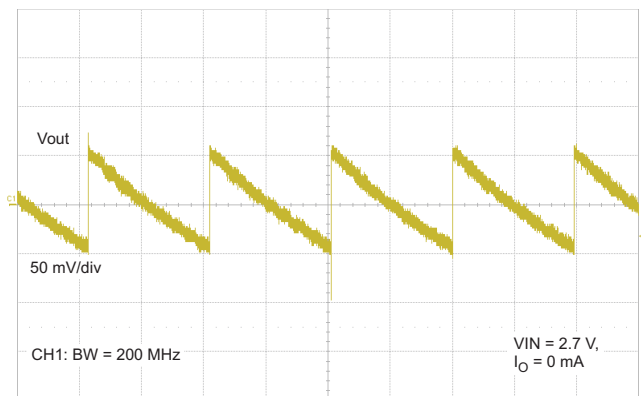
5 ms/div

Figure 11.

LOAD TRANSIENT
V_{CC} = 3.6 V, Io = 0 mA
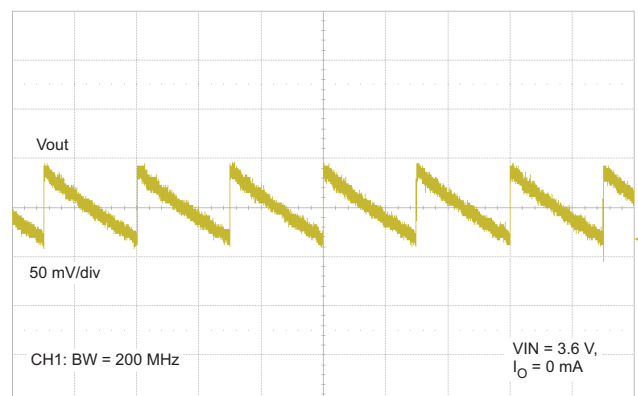
5 ms/div

Figure 12.

OUTPUT RIPPLE VOLTAGE (NORMAL MODE)
V_{IN} = 2.7 V, Io = 50 mA
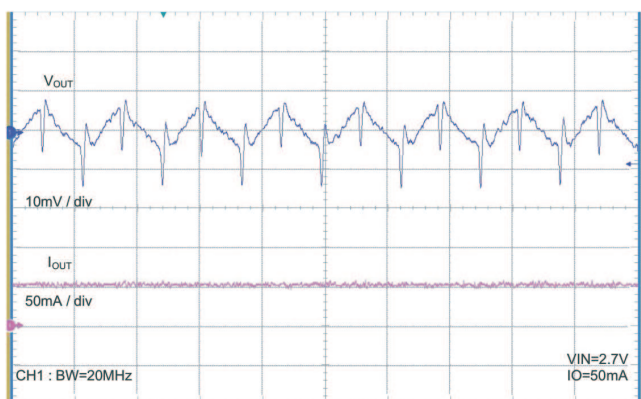
500 ns/div

Figure 13.

OUTPUT RIPPLE (NORMAL MODE)
V_{IN} = 3.6 V, Io = 100 mA
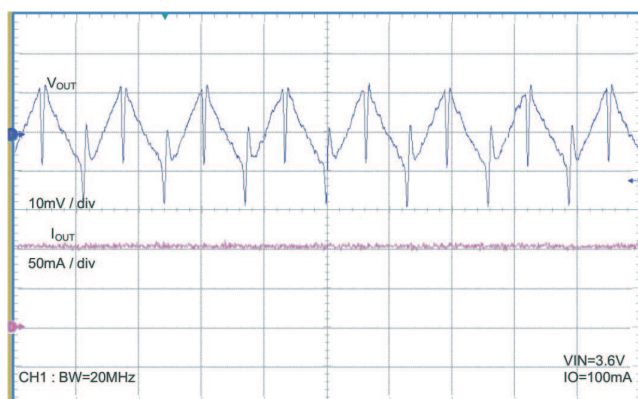
500 ns/div

Figure 14.

POWER ON
V_{IN} = 2.7 V, Io = 50 mA
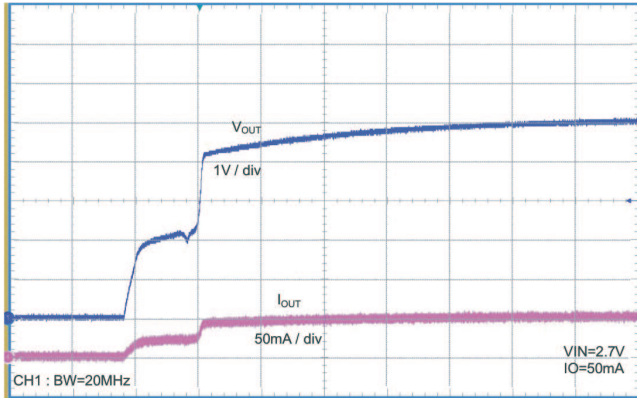
1 ms/div

Figure 15.

POWER ON
V_{IN} = 3.6 V, Io = 100 mA
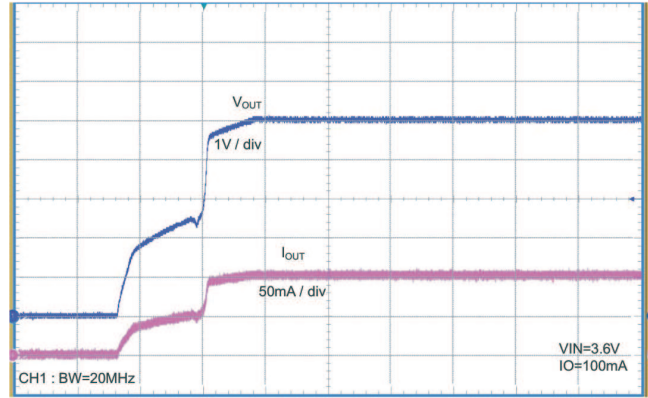
1 ms/div

Figure 16.

ENABLE / DISABLE
V_{IN} = 2.7 V, Io = 50 mA
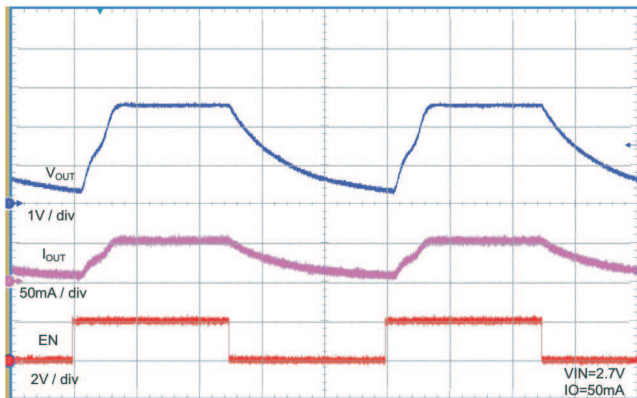
200 µs/div

Figure 17.

ENABLE / DISABLE
V_{IN} = 3.6 V, Io = 100 mA
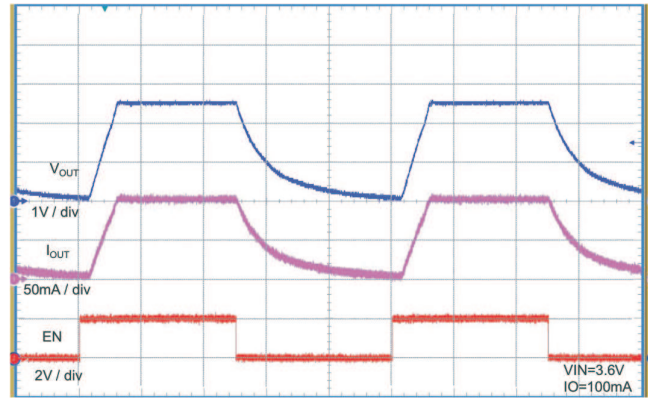
200 µs/div

Figure 18.

THERMAL SHUT DOWN OPERATION
V_{IN} = 5.5 V, R_{LOAD}=20Ω

50 ms/div

Figure 19.

Product Folder Link(s) :*TPS60151*
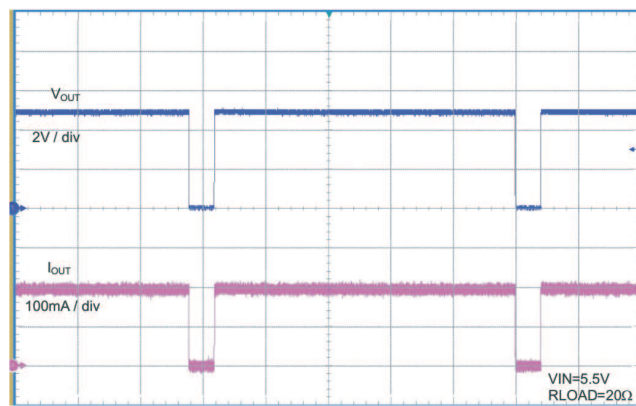
APPLICATION INFORMATION

APPLICATION OVERVIEW

Most of today's battery-powered portable electronics allow and/or require data transfer with a PC. One of the fastest data transfer protocols is via USB On the Go (OTG). As Figure 20 shows, the USB OTG circuitry in the portable device requires a 5-V power rail and up to 140mA of current. The HDMI specification calls for a 5-V power rail that can source 55mA or more current. The TPS60151 may be utilized to provide a 5-V power rail in a battery powered system.

Alternatively, low-cost portable electronics with small LCD displays require a low-cost solution for providing the WLED backlight. As shown in Figure 21, the TPS60151 can also be used to drive several WLEDs in parallel, with the help of ballast resistors.
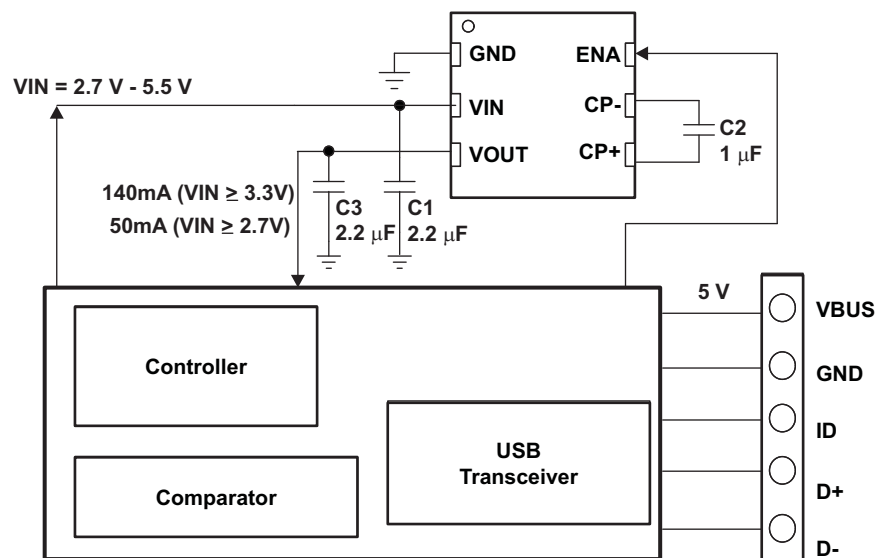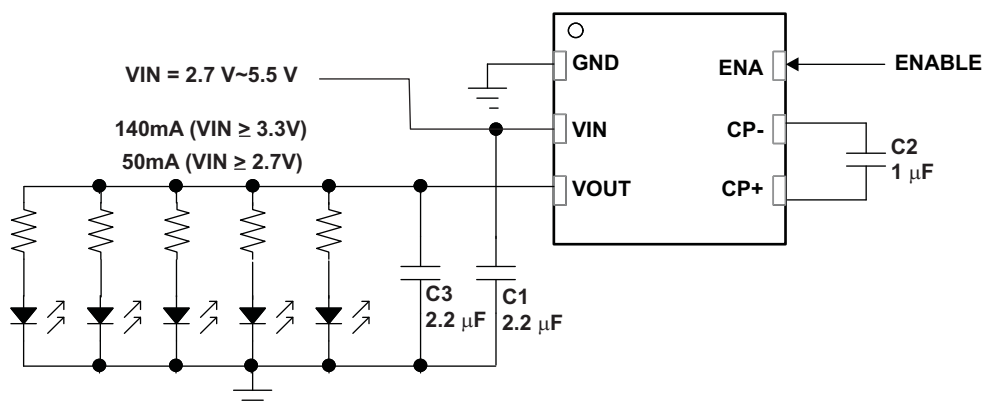

Figure 20. Application Circuit for OTG System

Figure 21. Application Circuit for Driving White LEDs

BASIC OPERATION PRINCIPLE

The TPS60151, regulated charge pump, provides a regulated output voltage for various input voltages. The TPS60151 regulates the voltage across the flying capacitor to 2.5V and controls the voltage drop of Q1 and Q2 while a conversion clock with 50% duty cycle drives the FETs.

Product Folder Link(s) :TPS60151
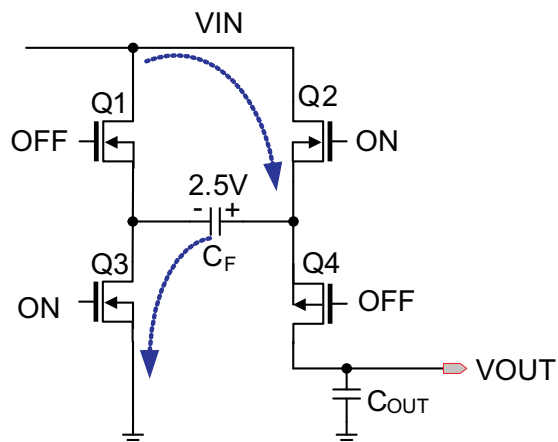
Figure 22. Charging Mode

During the first half cycle, Q2 and Q3 transistors are turned on and flying capacitor, C_F, will be charged to 2.5V ideally.
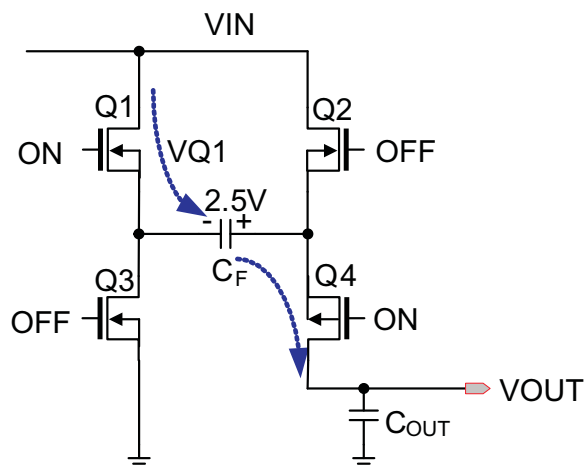
Figure 23. Discharging Mode

During the second half cycle, Q1 and Q4 transistors are turned on. Capacitor C_F will then be discharged to output.

The output voltage can be calculated as follows:

Vout = V_{IN} - VQ1 + V(C_F) - VQ4 = VIN - VQ1 + 2.5V - VQ4 = 5 V. (Ideal)

The output voltage is regulated by output feedback and an internally compensated voltage control loop.
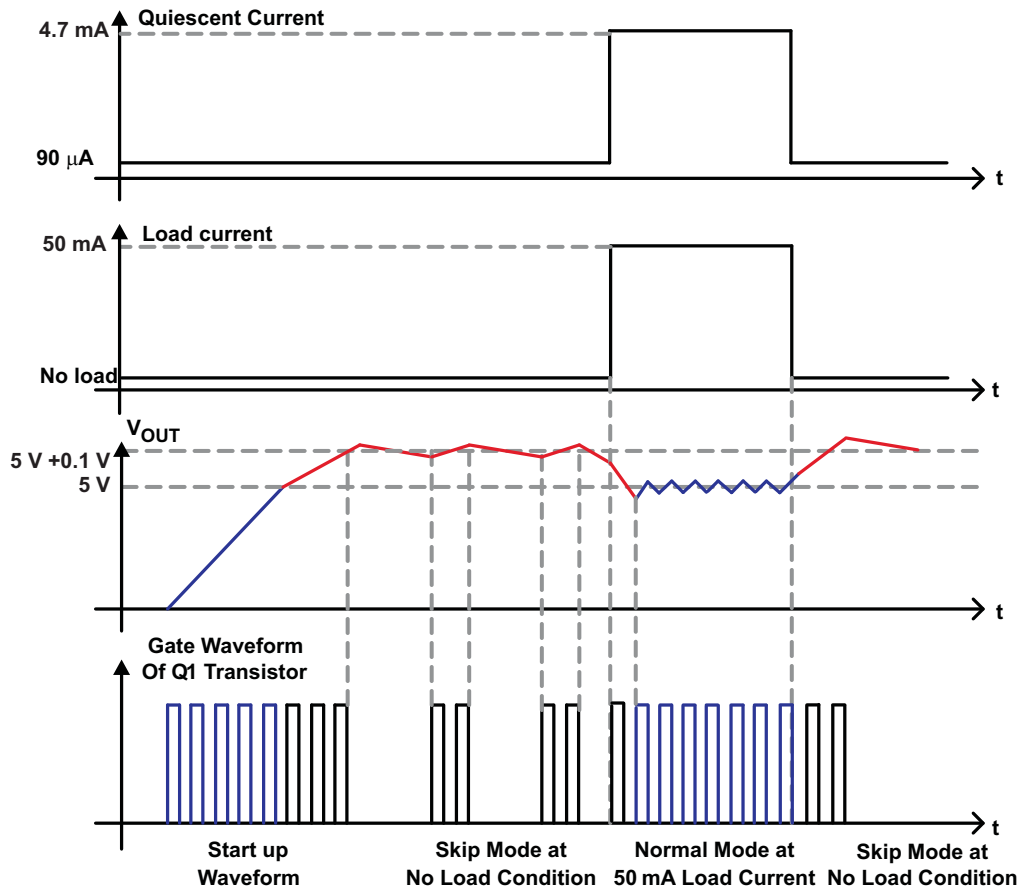
NORMAL MODE AND SKIP MODE OPERATION

Figure 24. Normal Mode and Skip Mode Operation

The TPS60151 has skip mode operation as shown in Figure 24. The TPS60151 enters skip mode if the output voltage reaches 5V+0.1V and the load current is below 8mA (typ). In Skip Mode, the TPS60151 disables the oscillator and decreases the pre-bias current of the output stage to reduce the power consumption. Once the output voltage dips below threshold voltage, 5V+0.1V, the TPS60151 begins switching to increase output voltage until the output reaches 5V+0.1V. When the output voltage dips below 5V, the TPS60151 returns to normal PWM mode; thereby re-enabling the oscillator and increasing the pre_bias current of the output stage to supply output current.

The skip threshold voltage and current depend on input voltage and output current conditions.

OVER CURRENT PROTECTION AND SHORT CIRCUIT PROTECTION

The TPS60151 has internal short circuit protection to protect the IC when the output is over loaded or shorted to ground. Figure 25 illustrates the protection circuit. I_P is directly related to I_O and the maximum I_P is clamped by IR3*k*n. The TPS60151 ensures a current limit of 500mA or less which is mandated by the HDMI electrical specification. To further avoid damage when output is shorted to ground, the short circuit protection circuitry senses the output voltage and adjusts V_{bias} down to clamp the maximum output current to a lower value – 80mA (typ).
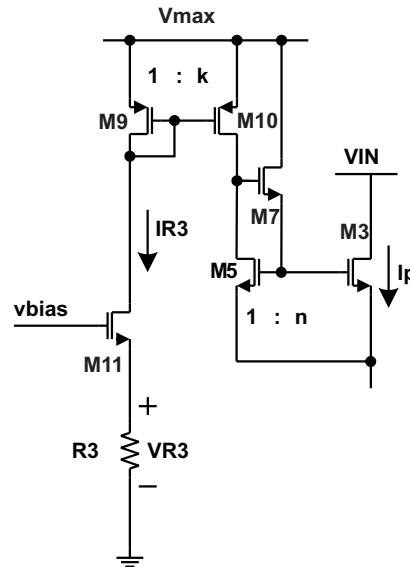
Figure 25. Current Limit

OUTPUT REVERSE CURRENT PROTECTION

Applications like HDMI or USB OTG generally do not tolerate output reverse current that can drain power from connected devices. Special considerations were put in place to prevent that from happening. Figure 26 is a testing circuit; and, Figure 27 shows reverse current protection test results under various conditions.
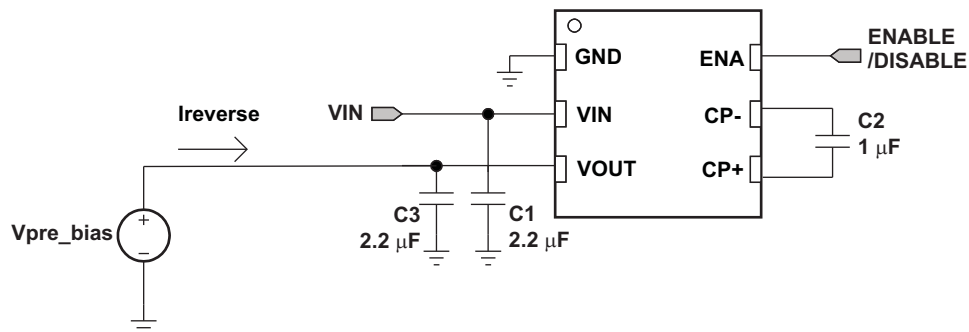

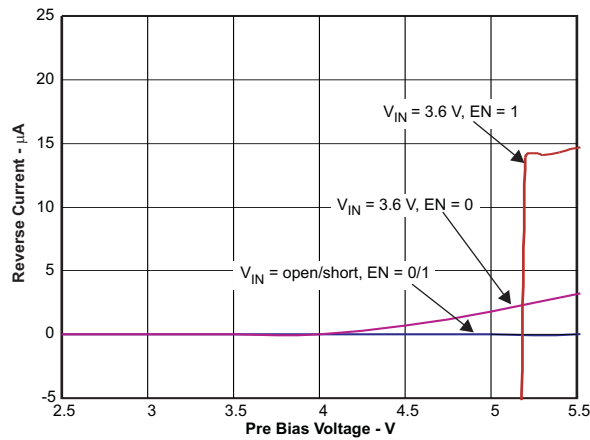**Figure 26. Output Reverse Current Test Setup**

Figure 27. Reverse Current Test Results (Typical)

THERMAL SHUT DOWN PROTECTION

The regulator has thermal shutdown circuitry that protects it from damage caused by overload conditions. The thermal protection circuitry disables the output when the junction temperature reached approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is automatically re-enabled. Continuously running the regulator into thermal shutdown can degrade reliability. The regulator also provides current limit to protect itself and the load.

SHUTDOWN MODE

An enable pin on the regulator may be used to place the device into an energy-saving shutdown mode. In this mode, the output is disconnected from the input and the input quiescent current is reduced to 10μA maximum.

CAPACITOR SELECTION

For minimum output voltage ripple, the output capacitor (C_{OUT}) should be a surface-mount ceramic capacitor. Tantalum capacitors generally have a higher Effective Series Resistance (ESR) and may contribute to higher output voltage ripple. Leaded capacitors also increase ripple due to the higher inductance of the package itself. To achieve the best operation with low input voltage and high load current, the input and flying capacitors (C_{IN} and C_{FLY}, respectively) should also be surface-mount ceramic types.
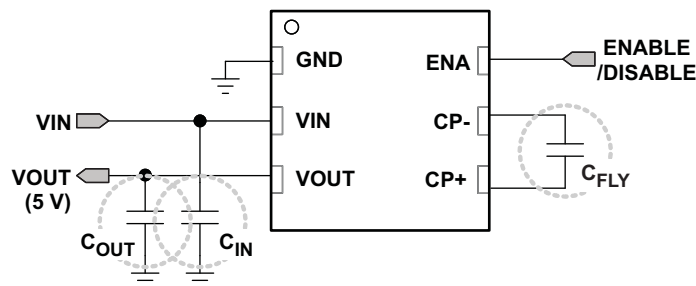

Figure 28. Capacitors

Generally, C_{FLY} can be calculated by the following simple equation,

$$Q_{charging} = c \times v = C_{FLY} \times \Delta V_{CFLY},$$

$$Q_{discharging} = i_{discharge} \times t = 2 \times I_{LOAD(MAX)} \times \left(\frac{T}{2}\right), \text{ half duty.}$$

(1)

Both equation should be same,
$$\therefore 2 \times I_{LOAD(MAX)} \times \left(\frac{T}{2}\right) = C_{FLY} \times \Delta V_{CFLY}$$

$$\therefore C_{FLY} \geq \frac{2 \times I_{LOAD(MAX)} \times \left(\frac{T}{2}\right)}{\Delta V_{CFLY}} = \frac{I_{LOAD(MAX)}}{\Delta V_{CFLY} \times f}$$

(2)

If I_{LOAD} = 140 mA, f = 1.5MHZ, and ΔV_{CFLY} = 100mV, the minimum value of the flying capacitor should be 1μF.

Output capacitance, C_{OUT}, is also strongly related to output ripple voltage and loop stability,

$$V_{OUT(RIPPLE)} = \frac{I_{LOAD(MAX)}}{\left(2 \times f \times C_{OUT}\right)} + 2I_{LOAD(MAX)} \times ESR_{COUT}$$

(3)

The minimum output capacitance for all output levels is 2.2μF due to control stability. Larger ceramic capacitors or low ESR capacitors can be used to lower the output ripple voltage.

Suggested Capacitors (Input / Output / Flying Capacitor)

Manufacturer	Part Number	Value	Tolerance	Dielectric Material	Package Size	Rated Working Voltage
		4.7μF 2.2μF		X7R		6.3V

The efficiency of the charge pump regulator varies with the output voltage, the applied input voltage and the load current.

The approximate efficiency in normal operating mode is given by:

$$\text{Efficiency(\%)} = \frac{PD(out)}{PD(in)} \times 100 = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}} \times 100 , \quad I_{IN} = 2 \times I_{OUT} + I_Q$$

(4)

$$\text{Efficiency(\%)} = \frac{V_{OUT}}{2 \times V_{IN}} \times 100 \quad \left(I_{IN} = 2 \times I_{OUT}\right) \quad \text{Quiescent current was neglected.}$$

(5)

PCB LAYOUT

Large transient currents flow in the VIN, VOUT, and GND traces. To minimize both input and output ripple, keep the capacitors as close as possible to the regulator using short, direct circuit traces.
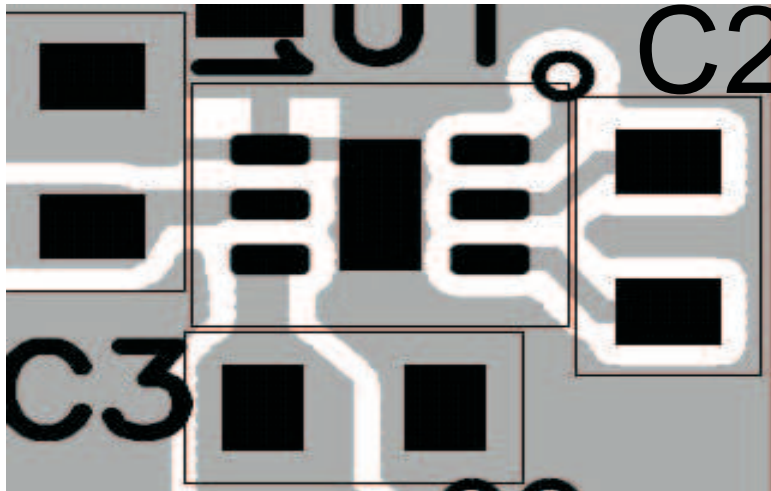
Figure 29. Recommended PCB Layout

PACKAGE OPTION ADDENDUM

![Texas Instruments logo]

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
TPS60151DRVR	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS60151DRVT	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS
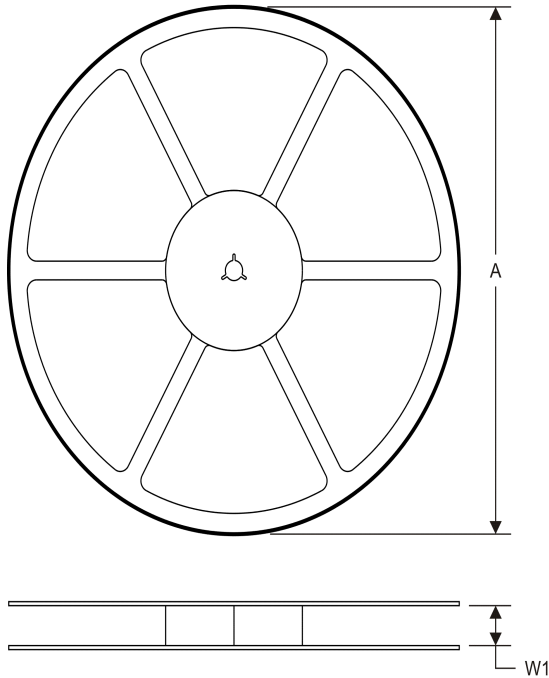
TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS60151DRVR	SON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS60151DRVR	SON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS60151DRVT	SON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS60151DRVT	SON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS60151DRVR	SON	DRV	6	3000	210.0	185.0	35.0
TPS60151DRVR	SON	DRV	6	3000	210.0	185.0	35.0
TPS60151DRVT	SON	DRV	6	250	210.0	185.0	35.0
TPS60151DRVT	SON	DRV	6	250	210.0	185.0	35.0

DRV (S−PWSON−N6)   PLASTIC SMALL OUTLINE NO−LEAD

$\dfrac{2,10}{1,90}$

$\dfrac{2,10}{1,90}$

PIN 1 INDEX AREA

$\dfrac{0,80}{0,70}$

0,20 REF.

◁ 0,08

SEATING PLANE

$\dfrac{0,05}{0,00}$

6X $\dfrac{0,30}{0,20}$

6X $\dfrac{0,35}{0,25}$

EXPOSED THERMAL PAD
⟨D⟩

6

0,65
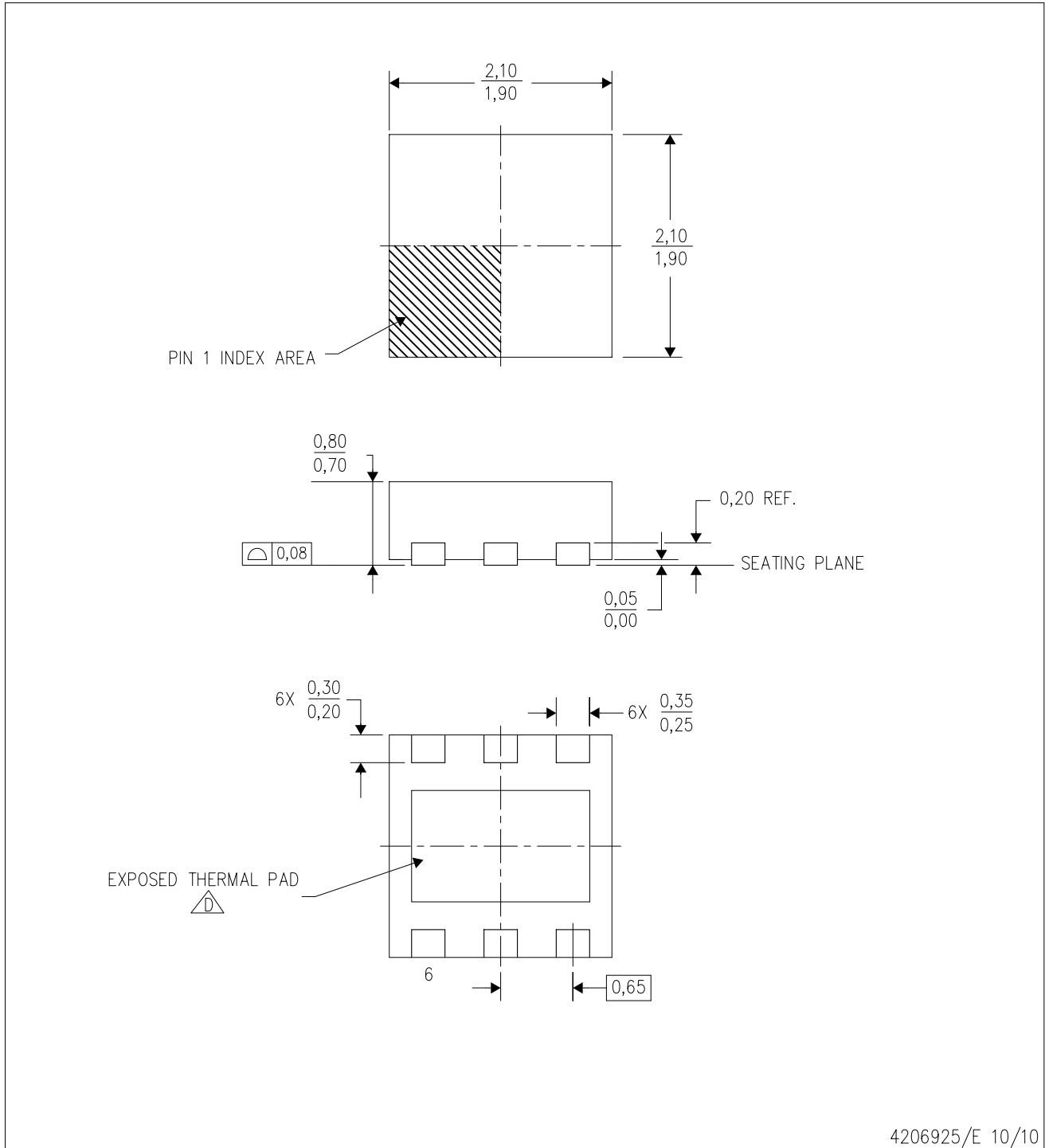
4206925/E 10/10

NOTES: A.   All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.   This drawing is subject to change without notice.
         C.   Small Outline No−Lead (SON) package configuration.
         ⟨D⟩ The package thermal pad must be soldered to the board for thermal and mechanical performance.
              See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

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DRV (S-PWSON-N6)   PLASTIC SMALL OUTLINE NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

(C0.30)

PIN 1 IDENTIFICATION

1,00±0,10

Exposed Thermal Pad

1   3

6   4

1,60±0,10
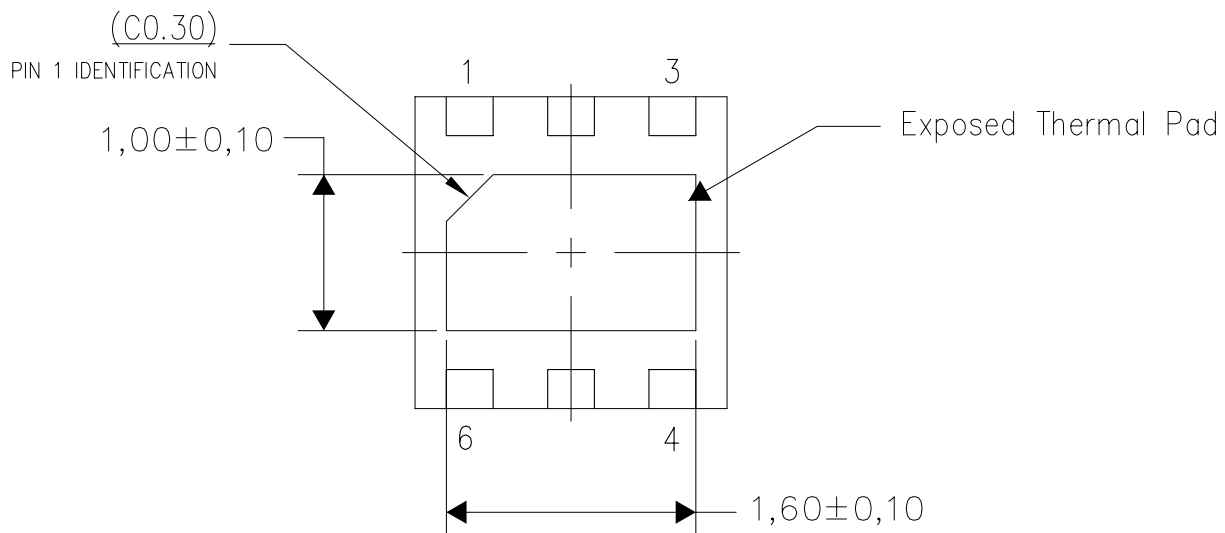
Bottom View

Exposed Thermal Pad Dimensions

4206926-2/L 11/11

NOTE: A. All linear dimensions are in millimeters

DRV (S−PWSON−N6)   PLASTIC SMALL OUTLINE NO−LEAD

Example Board Layout

0,65

Note D

2,8 1,4

Example Stencil Design
0.125mm Stencil Thickness
(Note E)

0,65

0,65

0,80 1,45 2,75

1,4

0,25

70% Printed solder coverage on center pad

Non Solder Mask Defined Pad

Example
Solder Mask Opening
(Note F)

Pad Geometry
(Note C)

0,7

0,07
all around

0,3

Center Pad Layout
(Note D)

1,6

2xØ0,3

1,0

0,8
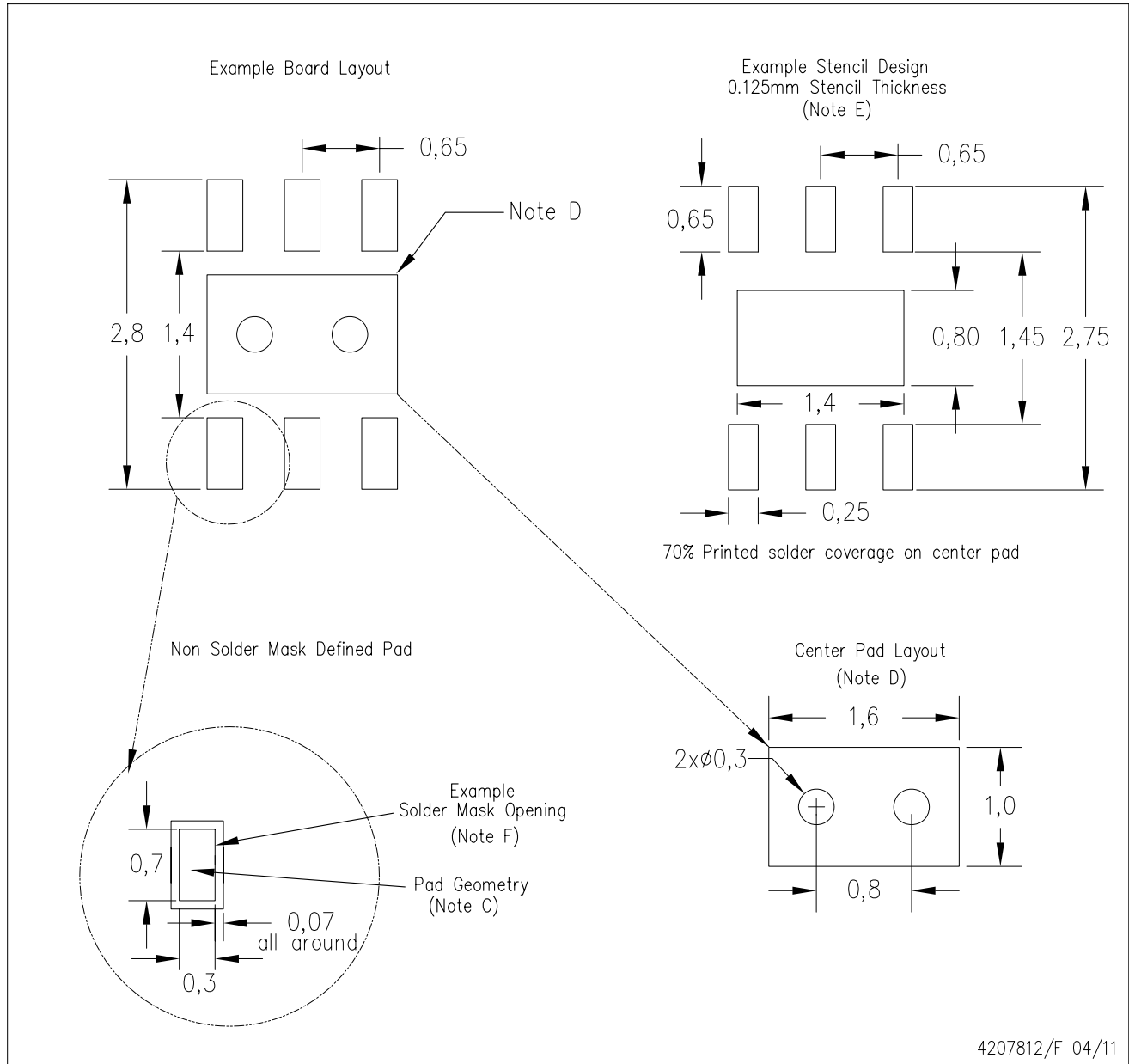
4207812/F 04/11

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Publication IPC−7351 is recommended for alternate designs.
        D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note,
            QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets
            for specific thermal information, via requirements, and recommended board layout.
            These documents are available at www.ti.com <http://www.ti.com>.
        E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
            contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
        F. Customers should contact their board fabrication site for solder mask tolerances.

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