LCD Bias Supply With Integrated Level Shifters

Check for Samples :TPS65163

FEATURES

- **8.6-V to 14.7-V Input Voltage Range**
- **2.8-A Boost Converter Switch Current Limit**
- **Boost Converter Output Voltages up to 18.5 V**
- **Boost and Buck Converter Short-Circuit Protection**
- **1.5-A Buck Converter (3.3 V) Switch Current Limit**
- **Fixed 750-kHz Switching Frequency for Buck and Boost Converters**
- **Buck Converter and Boost Converter Soft-Start**
- **Two Charge-Pump Controllers to Regulate V_{GH} and V_{GL}**
- **Control Signal for External High-Side MOSFET Isolation Switch**
- **9-Channel Level Shifter Organized in Two Groups of 7 and 2 Channels (Separate V_{GH})**
- **Gate Shaping (Level Shifter Channels 1 to 6)**
- **Display Panel Discharge Function**
- **Supports V_{GH} Voltages up to 38 V**
- **Supports V_{GL} Voltages Down to –13 V**
- **Reset Signal With Programmable Reset-Pulse Duration**
- **Thermal Shutdown**
- **48-Pin 7-mm × 7-mm QFN Package**

APPLICATIONS

- **LCD TVs and Monitors Using GIP Technology**

DESCRIPTION

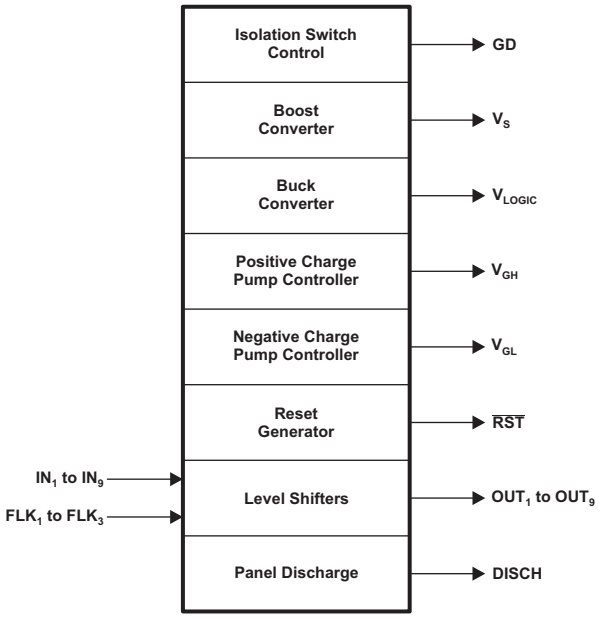
The TPS65163 integrates a boost converter, buck converter, reset generator, two charge pump controllers and a nine-channel level shifter in a single device.

In typical display panel applications, the boost converter generates the display panel source voltage, V_S; the buck converter generates the system logic supply, V_{LOGIC}; and the two charge pump controllers regulate the external charge pumps generating the display transistors' on and off supplies, V_{GH} and V_{GL}.

The level shifters transform the logic-level control signals generated by the display timing controller into the high-level signals needed by the LCD panel. The nine level-shifter channels are organized in two groups, each with its own positive supply voltage (V_{GH}). Each channel uses a low-impedance output stage to achieve fast rise and fall times, even when driving the capacitive loads present in LCD applications. Channels 1 to 6 also support gate voltage shaping.

The TPS65163 also provides a reset circuit that monitors the buck converter output (V_{LOGIC}) and generates a reset signal for the timing controller during power up and power down.

A control signal can also be generated to control an external MOSFET isolation switch located between the output of the boost converter and the display panel.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

T_A	ORDERING	PACKAGE	PACKAGE MARKING
–40°C to 85°C	TPS65163RGZR	48-Pin 7x7 QFN	TPS65163

(1) The device is supplied taped and reeled, with 3000 (TBC) devices per reel.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

		VALUE	UNIT
Supply voltage(2)	VIN	–0.3 to 20	V
	VGH1, VGH2	–0.3 to 45	
	VGL	0.3 to –15	
Input voltage(2)	FBN, FBP, FBB, FB, DLY, CRST, SS, COMP, VL, FLK1–FLK3, IN1–IN9, VSENSE	–0.3 to 7	V
Output voltage(2)	$\overline{RST}$	–0.3 to 7	V
	SWB, CTRLP, GD, SW, CTRLN	–0.3 to 20	
	RE	–0.3 to 45	
	OUT1–OUT9, DISCHARGE	–15 to 45	
Output current	GD	1	mA
	RE	100	
ESD rating	Human-body model	2000	V
	Machine model	200	V
	Charged-device model	700	V
	Continuous power dissipation	See Dissipation Table	W
Operating ambient temperature range		–40 to 85	°C
Operating junction temperature range		–40 to 150	°C
Storage temperature range		–65 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) With respect to the GND and AGND pins.

DISSIPATION RATINGS

PACKAGE	$R_{\theta JA}$	$T_A \le 25°C$ POWER RATING	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
48-pin QFN	36 °C/W	2.78 W	1.53 W	1.11 W

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{IN}	Supply voltage range	8.6	12	14.7	V
V_S	Boost converter output voltage range	V_{IN} + 1	15	18.5	V
C_{IN}	Input capacitance	10	20	44	µF
L	Boost converter inductance	6.8	10	15	µH
C_{OUT}	Boost converter output capacitance	40	60	100	µF
L	Buck converter inductance	6.8	10	15	µH
C_{OUT}	Buck converter output capacitance	20	44	100	µF
T_A	Operating ambient temperature	–40	25	85	°C
T_J	Operating junction temperature	–40	85	125	°C

ELECTRICAL CHARACTERISTICS

V_{IN} = 12 V; V_S = 16 V; V_{LOGIC} = 3.3 V; V_{GH1} = V_{GH2} = 30 V; V_{GL} = –7 V; T_A = –40°C to 85°C; typical values are at 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
I_{IN}	Supply current			1	15	mA
UVLO	UVLO threshold		7.8	8.2	8.5	V
V_{HYS}	UVLO hysteresis					V
INTERNAL OSCILLATOR						
f_{SW}	Switching frequency		600	750	900	kHz
VOLTAGE REFERENCE						
V_{REF}	Voltage reference			1.24		V
BOOST CONVERTER						
V_S	Output voltage	Measured after isolation switch	V_{IN}+1		18.5	V
V_{FB}	Feedback regulation voltage		1.228	1.24	1.252	V
I_{FB}	Feedback input bias current	V_{FB} = 1.24 V		±0.01	±1	µA
I_{LIM}	Switch current limit		2.8	3.5	4.2	A
I_{LEAK}	Switch leakage current	V_{SW} = 15 V			10	µA
$r_{DS(ON)}$	Switch ON resistance	I_{SW} = I_{LIM}		0.15	0.25	Ω
t_{SW}	Switching time	Turnon and turnoff		10		ns
	Line regulation	9.6 V < V_{IN} < 14.4 V, I_S = 750 mA		0.02		%/V
	Load regulation	V_S = 17 V, I_S = 100 mA to 1.5 A		0.1		%/A
V_{OVP}	Overvoltage threshold			1.03 × V_{FB}		V
I_{SS}	Soft-start capacitor charge current			11		µA
$V_{FB(SC)}$	Short circuit threshold	V_{FB} rising		200		mV
GATE DRIVE SIGNAL						
V_{GD}	Output low voltage	I_{GD} = 500 µA (sinking)			0.5	V
I_{LK}	Leakage current	V_{GD} = 20 V		0.05	1	µA

ELECTRICAL CHARACTERISTICS (continued)

V_{IN} = 12 V; V_S = 16 V; V_{LOGIC} = 3.3 V; V_{GH1} = V_{GH2} = 30 V; V_{GL} = –7 V; T_A = –40°C to 85°C; typical values are at 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BUCK CONVERTER						
V_{LOGIC}	Output voltage		3.2	3.3	3.4	V
I_{FBB}	Feedback input bias current	V_{FBB} = 3.3 V, sourcing (i.e. flowing out of IC).			125	µA
I_{LIM}	Switch current limit		1.5	2.1	2.8	A
I_{LKG}	Switch leakage current	V_{SWB} = 0 V			10	µA
$r_{DS(on)}$	Switch ON resistance			0.21		Ω
t_{SW}	Switching time	Turnon and turnoff		10		ns
	Line regulation	V_{IN} = 9.6 V to 14.4 V, I_{LOGIC} = 0.5 A		0.01		%/V
	Load regulation	I_{LOGIC} = 150 mA to 1.5 A		0.2		%/A
$V_{FB(SC)}$	Short-circuit threshold	V_{FBB} rising		1.065		V
V_{PG}	Power-good threshold	V_{LOGIC} rising		3.2		V
		V_{LOGIC} falling		2.9		
t_{SS}	Soft start time			0.66		ms
POSITIVE CHARGE PUMP CONTROLLER						
V_{FBP}	Feedback regulation voltage		1.203	1.24	1.277	V
I_{FBP}	Feedback input bias current	V_{FBP} = 1.24 V		±10	±100	nA
I_{CTRLP}	Base drive current for external transistor	Normal operation	5			mA
$I_{CTRLP(SC)}$	Base drive current for external transistor	Short-circuit operation	40	55	75	µA
	Line regulation	V_{IN} = 9.6 V to 14.4 V, V_{GH} = 27 V, I_{GH} = 50 mA, including external components		±0.1		%/V
	Load regulation	V_{GH} = 27 V, I_{GH} = 0 to 50 mA, including external components		±1		%/A
NEGATIVE CHARGE PUMP CONTROLLER						
V_{FBN}	Feedback regulation voltage		–36	0	36	mV
I_{FBN}	Feedback input bias current	V_{FBP} = 1.24 V		±10	±100	nA
I_{CTRLN}	Base drive current for external transistor	Normal operation	2.5			mA
$I_{CTRLN(SC)}$	Base drive current for external transistor	Short-circuit operation	200	300	480	µA
	Line regulation	V_{IN} = 9.6 V to 14.4 V, V_{GL} = –7 V, I_{GL} = 50 mA, including external components		±0.1		%/V
	Load regulation	V_{GL} = –7 V, I_{GH} = 0 to 50 mA, including external components		±1		%/A
RESET GENERATOR						
V_{OL}	Output voltage low	I_{OL} = 1 mA (sinking)			0.5	V
I_{OH}	Output current high	V_{RST} = 3.3 V			±1	µA
I_{CRST}	Reset delay capacitor charge current			10		µA
V_{CRST}	Reset delay threshold voltage			1.24		V
DELAY						
I_{DLY}	Delay capacitor charge current			10		µA
V_{DLY}	Delay threshold voltage			1.24		V
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown threshold			150		°C
T_{HYS}	Thermal shutdown hysteresis			10		°C

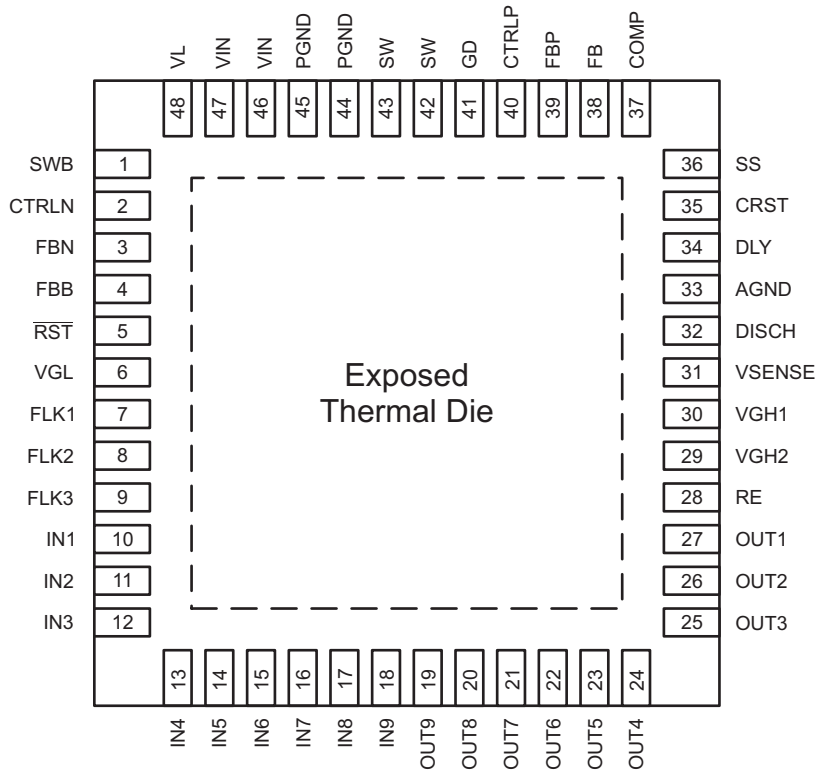
ELECTRICAL CHARACTERISTICS (continued)

V_{IN} = 12 V; V_S = 16 V; V_{LOGIC} = 3.3 V; V_{GH1} = V_{GH2} = 30 V; V_{GL} = –7 V; T_A = –40°C to 85°C; typical values are at 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
I_{GH1}	V_{GH1} supply current	IN1 to IN7 = VSENSE = 0 V		0.35	3	mA
I_{GH2}	V_{GH2} supply current	IN8 and IN9 = 0V		0.012	1	mA
I_{GL}	V_{GL} supply current	IN1 to IN9 = VSENSE = 0 V		0.144	4	mA
UVLO	Undervoltage lockout threshold (V_{GH1})	V_{GH1} rising	10.5		13.5	V
V_{HYS}	Undervoltage lockout hysteresis (V_{GH1})	V_{GH1} falling		450		mV
LEVEL SHIFTERS						
I_{OUT}	Output current	OUT1 to OUT7, continuous	±15			mA
		OUT1 to OUT7, peak	±300			
		OUT8 to OUT9, DISCGARGE, continuous	±15			
		OUT8 to OUT9, DISCHARGE, peak	±150			
I_{IN}	Input current	IN1 to IN9 = 0 V			±1	µA
		IN1 to IN9 = 3.3 V			±1	µA
V_{IH}	High level input threshold	IN1 to IN9			2	V
V_{IL}	Low level input threshold	IN1 to IN9	0.5			V
V_{DROPL}	Output voltage drop low	OUT1 to OUT7, I_{OUT} = –10 mA (sinking)	0.1	0.3		V
		OUT8 to OUT9, DISCHARGE, I_{OUT} = –10 mA (sinking)		0.2	1	
V_{DROPH}	Output voltage drop high	OUT1 to OUT7, I_{OUT} = 10 mA (sourcing)		0.15	0.4	V
		OUT8 to OUT9, DISCHARGE, I_{OUT} = 10 mA (sourcing)		0.35	1	V
t_R	Rise time	OUT1 to OUT7, C_{OUT} = 4.7 nF		300	520	ns
		OUT8 to OUT9, C_{OUT} = 4.7 nF		800	1200	
t_F	Fall time	OUT1 to OUT7, C_{OUT} = 4.7 nF		200	370	ns
		OUT8 to OUT9, C_{OUT} = 4.7 nF		500	850	
t_{PH}	Propagation delay	Rising edge, C_{OUT} = 150 pF			60	ns
t_{PL}		Falling edge, C_{OUT} = 150 pF			60	
GATE VOLTAGE SHAPING						
t_{PH}	Propagation delay, gate voltage shaping enabled	FLK falling			100	ns
t_{SU}	Set-up time	Time IN signals must be stable before falling edge of FLK			70	ns
$r_{DS(on)}$	Resistance between OUT and RE pins			60	100	Ω
I_{lkg}	Leakage current from RE pin			±1	±10	µA
DISCHARGE						
V_{SENSE}	Discharge voltage sense threshold	V_{SENSE} falling	1.275	1.5	1.725	V
I_{SENSE}	Discharge voltage sense current	V_{SENSE} = 2V		±0.1	±1	µA
V_{HYS}	Discharge voltage sense hysteresis	V_{SENSE} rising		50		mV

DEVICE INFORMATION

PIN ASSIGNMENT



PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
AGND	33	P	Analog ground
BOOT	48	I	Buck converter bootstrap capacitor connection
COMP	37	I	Boost converter compensation network connection.
CRST	35	I	Reset generator timing capacitor connection.
CTRLN	2	O	Base drive signal for an external transistor positive linear regulator
CTRLP	40	O	Base drive signal for an external transistor negative linear regulator
DISCH	32	I	Panel discharging connection
DLY	34	I	Positive charge pump and boost converter delay capacitor connection
FB	38	I	Boost regulator feedback. Connect this pin to the center of a resistor divider connected between the boost converter output and AGND.
FBB	4	I	Buck converter feedback connection
FBN	3	I	Feedback pin for an external transistor positive linear regulator
FBP	39	I	Feedback pin for an external transistor negative linear regulator
FLK1	7	I	Flicker clock for level-shifter channels 1 and 4
FLK2	8	1	Flicker clock for level-shifter channels 2 and 5
FLK3	9	I	Flicker clock for level-shifter channels 3 and 6
GD	41	O	Gate drive signal for the external MOSFET isolation switch
IN1–IN7	10, 11, 12, 13, 14, 15, 16	I	Inputs for level-shifter channels 1 through 7 (connected to VGH1)
IN8–IN9	17, 18	I	Inputs for level-shifter channels 8 and 9 (connected to VGH2)

PIN FUNCTIONS (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
OUT7–OUT1	21, 22, 23, 24, 25, 26, 27	O	Outputs for level-shifter channels 1 through 7 (connected to VGH1)
OUT9–OUT8	19, 20	O	Outputs for level-shifter channels 8 and 9 (connected to VGH2)
PGND	44, 45	P	Power ground
RE	28	O	Gate shaping slope resistor connection
$\overline{\text{RST}}$	5	O	Reset generator open-drain output
SS	36	I	Soft-start timing-capacitor connection.
SW	42, 43	O	Boost converter switching node
SWB	1	O	Buck converter switch node
VGH1	30	P	Positive supply voltage for level-shifter channels 1 through 7
VGH2	29	P	Positive supply voltage for level-shifter channels 8 and 9
VGL	6	P	Negative supply voltage for level-shifter channels 1 through 9
VIN	46, 47	P	Supply-voltage connection
VSENSE	31	I	Discharge sense voltage
Exposed thermal die		P	Connect to the system GND

TYPICAL CHARACTERISTICS

TABLE OF GRAPHS

		FIGURE NO.
BOOST CONVERTER		
Efficiency		Figure 1
Load Transient Response	V_{IN} = 12 V, V_S = 15.5 V, I_S = 250 mA to 750 mA	Figure 2
Line Transient Response	V_{IN} = 11.5 V to 12.5 V, V_S = 15.5 V, I_S = 750 mA	Figure 3
Output Voltage Ripple	V_{IN} = 12 V, V_S = 15.5 V, I_S = 500 mA	Figure 4
Switch Node (SW) Waveform	CCM Operation	Figure 5
	DCM Operation	Figure 5
BUCK CONVERTER		
Efficiency		Figure 7
Load Transient Response	V_{IN} = 12 V, V_{LOGIC} = 3.3 V, I_{LOGIC} = 250 mA to 500 mA	Figure 8
Line Transient Response	V_{IN} = 11.5 V to 12.5 V, V_{LOGIC} = 3.3 V, I_{LOGIC} = 500 mA	Figure 9
Output Voltage Ripple	V_{IN} = 12 V, V_{LOGIC} 3.3 V, I_{LOGIC} = 500 mA	Figure 10
Switch Node (SW) Waveform	CCM Operation	Figure 11
	DCM Operation	Figure 12
	Skip Mode	Figure 13
POSITIVE CHARGE PUMP		
Load Transient Response	V_{IN} = 12 V, V_{GH} = 26 V, I_{GH} = 10 mA to 50 mA	Figure 14
Line Transient Response	V_{IN} = 11.5 V to 12.5 V, V_{GH} = 26 V, I_{GH} = 50 mA	Figure 15
Output Voltage Ripple	V_{IN} = 12 V, V_{GH} = 26 V, I_{GH} = 50 mA	Figure 16
NEGATIVE CHARGE PUMP		
Load Transient Response	V_{IN} = 12 V, V_{GL} = –7 V, I_{GL} = 10 mA to 50 mA	Figure 17
Line Transient Response	V_{IN} = 11.5 V to 12.5 V, V_{GL} = –7 V, I_{GL} = 50 mA	Figure 18
Output Voltage Ripple	V_{IN} = 12 V, V_{GL} = –7 V, I_{GL} = 50 mA	Figure 19
START-UP SEQUENCING		
Power-Up Sequencing	C_{DLY} = 100 nF	Figure 20
Reset Sequencing	C_{DLY} = 100 nF, C_{RST} = 22 nF	Figure 21
LEVEL SHIFTERS		
Output Rise and Fall Time	Channels 1–7, C_L = 4.7 nF, rising edge	Figure 22
	Channels 1–7, C_L = 4.7 nF, falling edge	Figure 23
	Channels 8–9, C_L = 4.7 nF, rising edge	Figure 24
	Channels 8–9, C_L = 4.7 nF, falling edge	Figure 25
	Channels 1–7, R_L = 47 Ω, C_L = 10 nF, rising edge	Figure 26
	Channels 1–7, R_L = 47 Ω, C_L = 10 nF, falling edge	Figure 27
Propagation Delay	IN to OUT, channels 1–7, C_L = 150 pF, rising edge	Figure 28
	IN to OUT, channels 1–7, C_L = 150 pF, falling edge	Figure 29
	IN to OUT, channels 8–9, C_L = 150 pF, rising edge	Figure 30
	IN to OUT, channels 8–9, C_L = 150 pF, falling edge	Figure 31
	FLK-RE, channels 1–6, C_L = 150 pF, R_E=1k	Figure 32
Output Current	Channels 1–7, C_L = 10 nF	Figure 33
	Channels 8–9, C_L = 10 nF	Figure 34
Panel Discharge	Power on	Figure 35
	Power off	Figure 36

BOOST CONVERTER EFFICIENCY

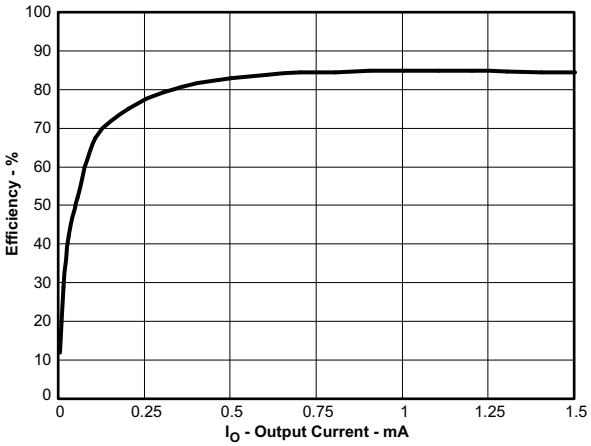


Figure 1.

BOOST CONVERTER LOAD TRANSIENT RESPONSE
I_S = 250 mA TO 750 mA

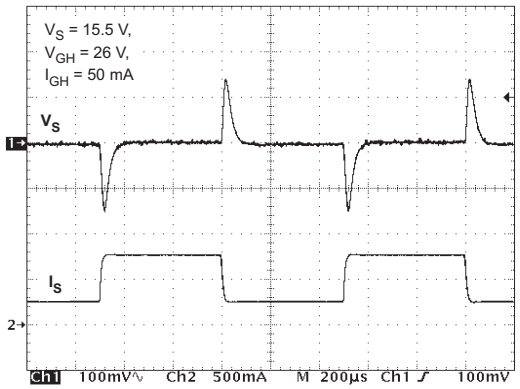


Figure 2.

BOOST CONVERTER LINE TRANSIENT RESPONSE
V_{IN} = 11.5 V TO 12.5 V

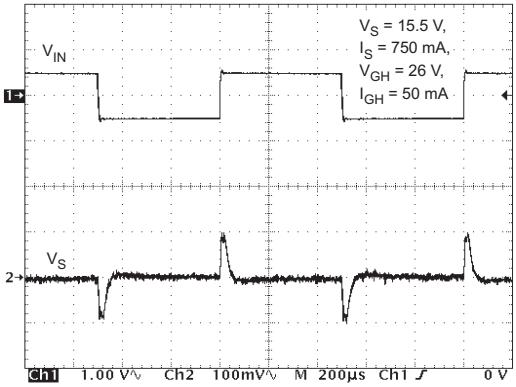


Figure 3.

BOOST CONVERTER OUTPUT VOLTAGE RIPPLE
I_S = 500 mA

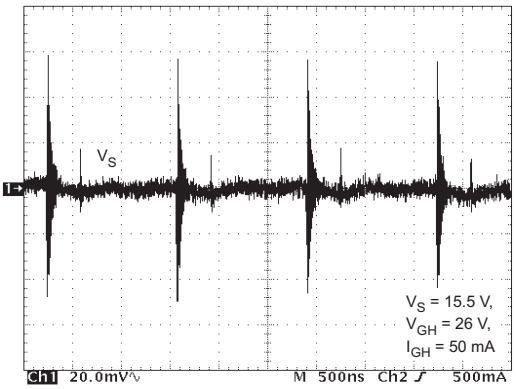


Figure 4.

BOOST CONVERTER SWITCH NODE WAVEFORM
CONTINUOUS CONDUCTION MODE

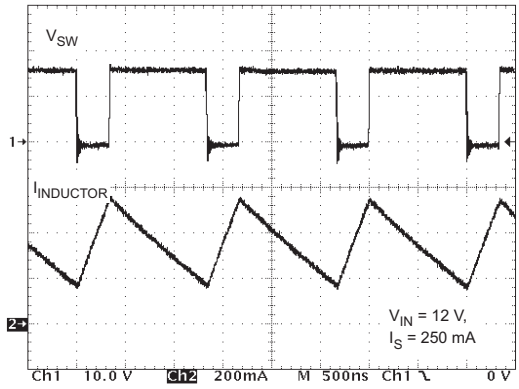


Figure 5.

BOOST CONVERTER SWITCH NODE WAVEFORM
DISCONTINUOUS CONDUCTION MODE

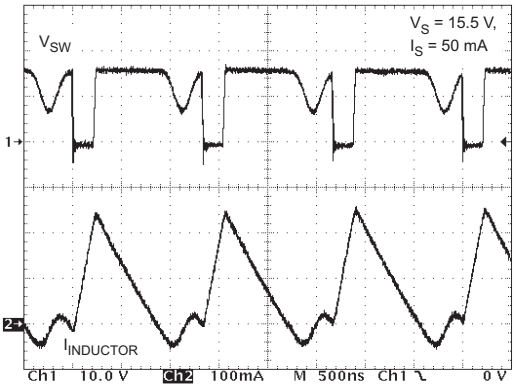


Figure 6.

BUCK CONVERTER EFFICIENCY

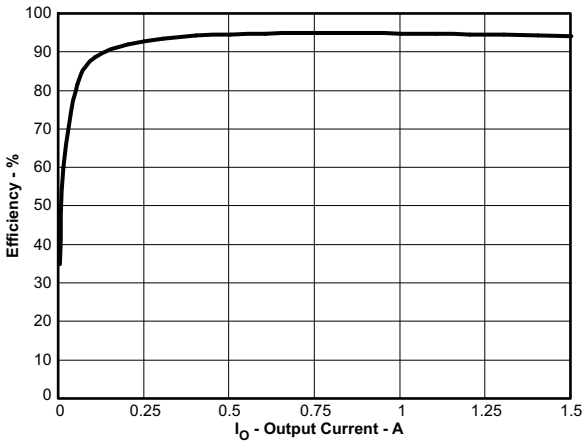


Figure 7.

BUCK CONVERTER LOAD TRANSIENT RESPONSE
I_{LOGIC} = 250mA TO 500mA

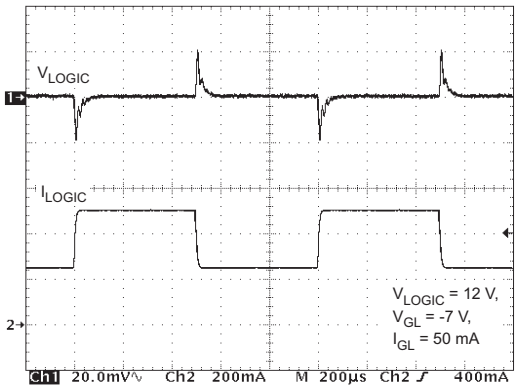


Figure 8.

BUCK CONVERTER LINE TRANSIENT RESPONSE
V_{IN} = 11.5 V TO 12.5 V

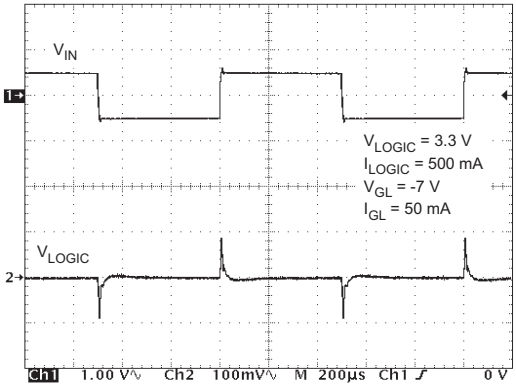


Figure 9.

BUCK CONVERTER OUTPUT VOLTAGE RIPPLE
I_{LOGIC} = 500 mA

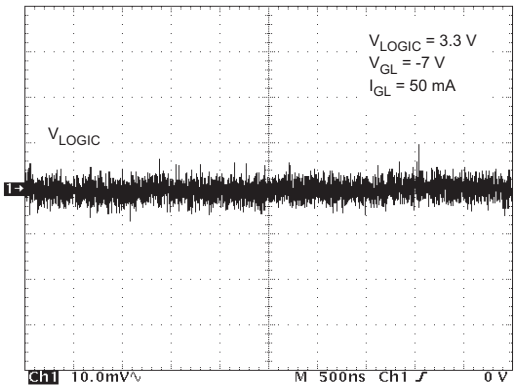


Figure 10.

BUCK CONVERTER SWITCH NODE WAVEFORM
CONTINUOUS CONDUCTION MODE

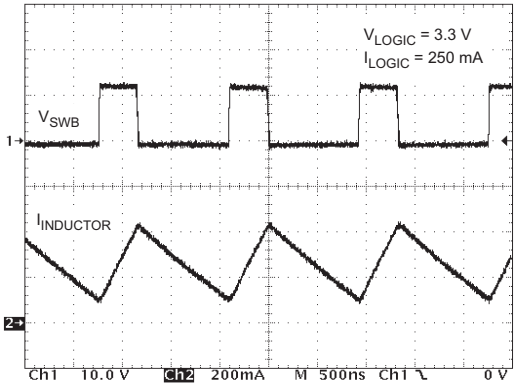


Figure 11.

BUCK CONVERTER SWITCH NODE WAVEFORM
DISCONTINUOUS CONDUCTION MODE

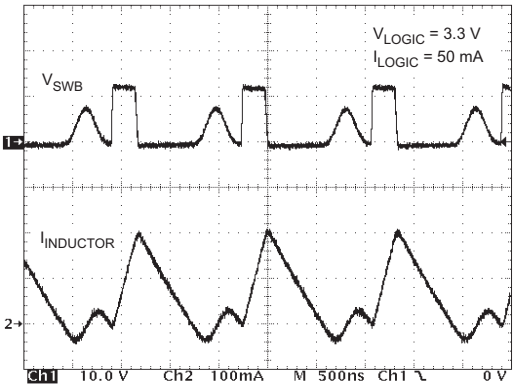


Figure 12.

BUCK CONVERTER SWITCH WAVEFORM
SKIP MODE

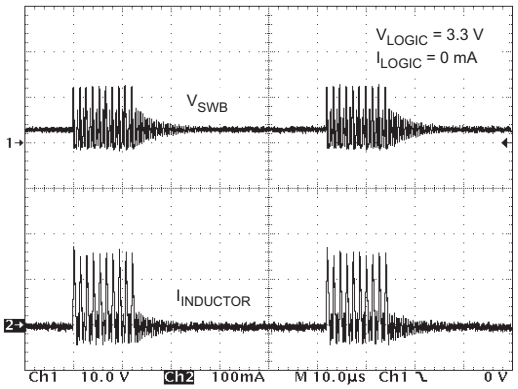


Figure 13.

POSITIVE CHARGE PUMP LOAD TRANSIENT RESPONSE
I_{GH} = 10 mA to 50 mA

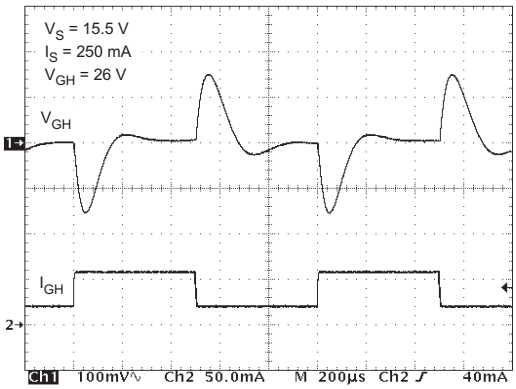


Figure 14.

POSITIVE CHARGE PUMP LINE TRANSIENT RESPONSE
V_{IN} = 11.5 V TO 12.5 V

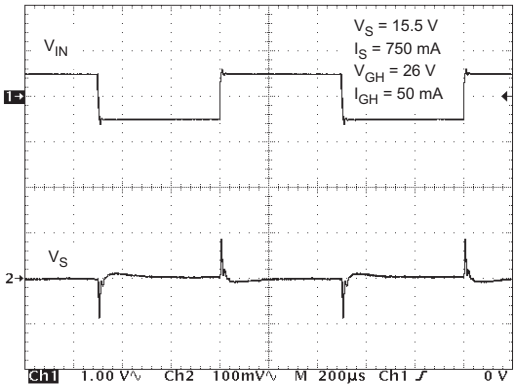


Figure 15.

POSITIVE CHARGE PUMP OUTPUT VOLTAGE RIPPLE
I_{GH} = 50 mA

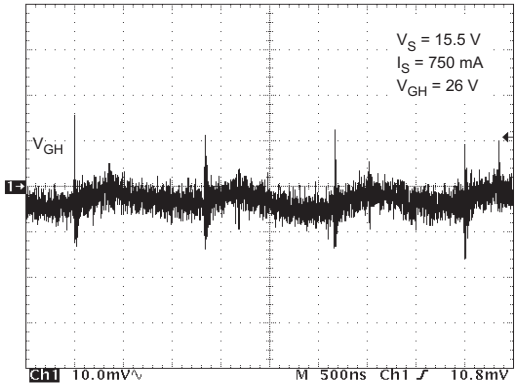


Figure 16.

NEGATIVE CHARGE PUMP LOAD TRANSIENT RESPONSE
I_{GL} = 10 mA to 50 mA

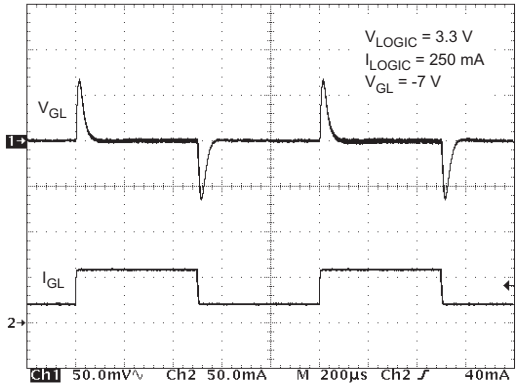


Figure 17.

NEGATIVE CHARGE PUMP LINE TRANSIENT RESPONSE
V_{IN} = 11.5 V to 12.5 V

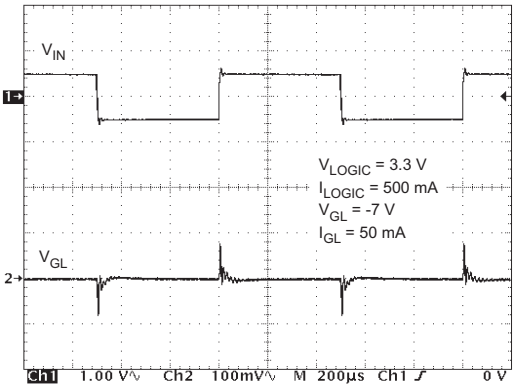


Figure 18.

NEGATIVE CHARGE PUMP OUTPUT VOLTAGE RIPPLE
I_{GL} = 50 mA

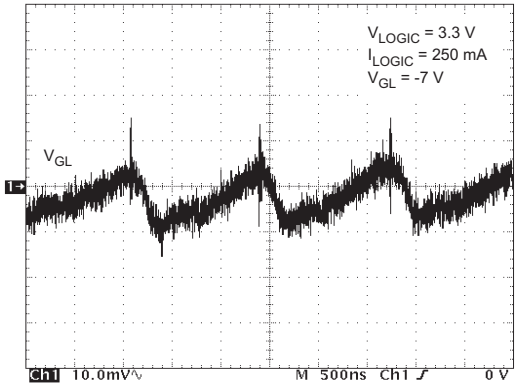


Figure 19.

POWER-UP SEQUENCING

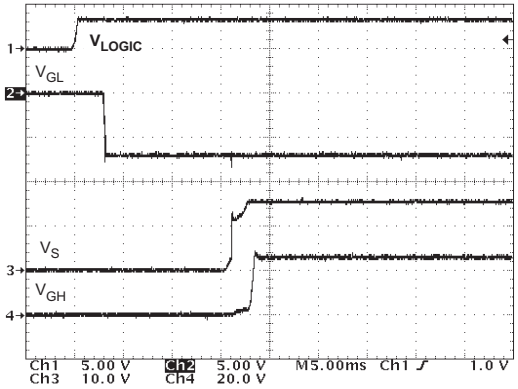


Figure 20.

RESET SEQUENCING

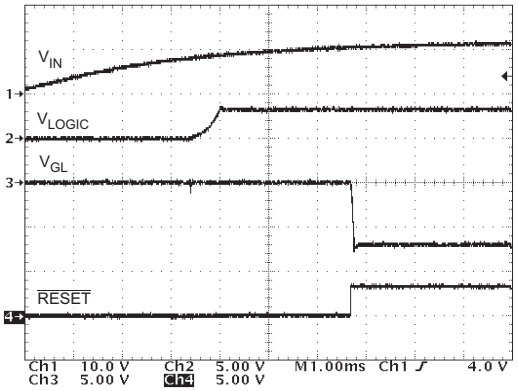


Figure 21.

LEVEL SHIFTER OUTPUT RISE TIME
CHANNELS 1-7

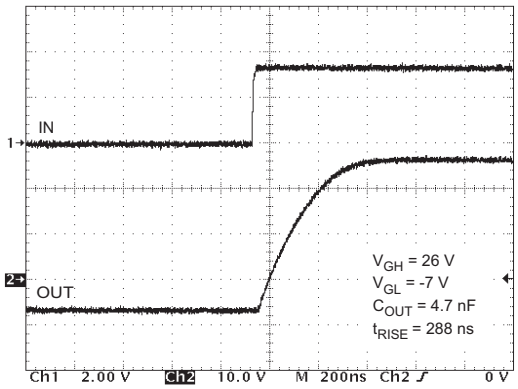


Figure 22.

LEVEL SHIFTER OUTPUT FALL TIME
CHANNELS 1-7

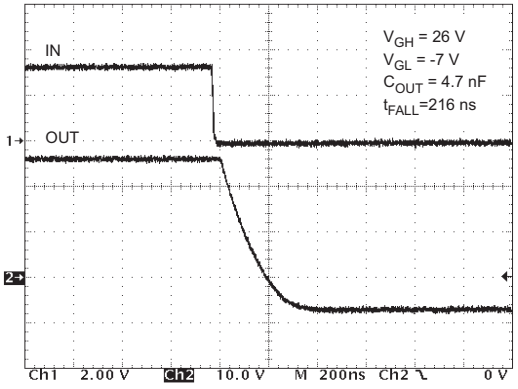


Figure 23.

LEVEL SHIFTER OUTPUT RISE TIME
CHANNELS 8-9

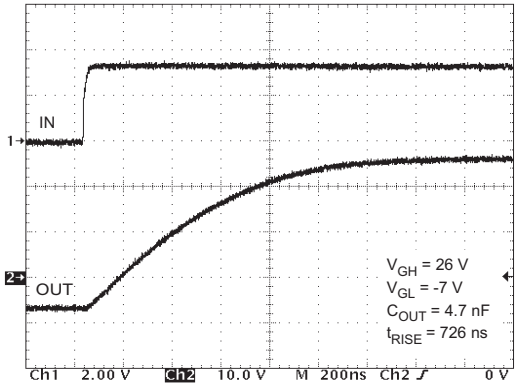


Figure 24.

LEVEL SHIFTER OUTPUT FALL TIME CHANNELS 8-9

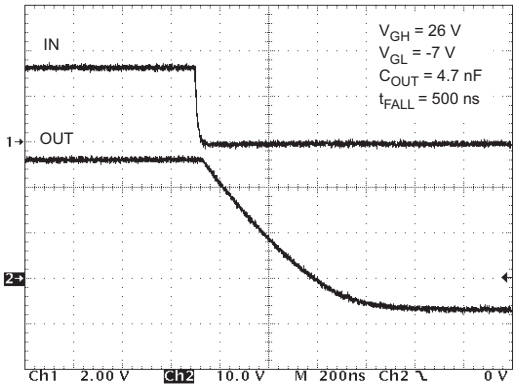


Figure 25.

LEVEL SHIFTER OUTPUT RISE TIME CHANNELS 1-7

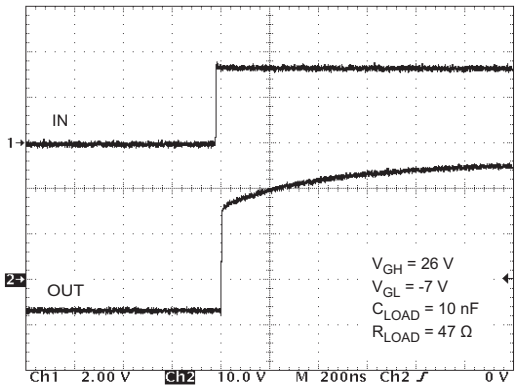


Figure 26.

LEVEL SHIFTER OUTPUT FALL TIME CHANNELS 1-7

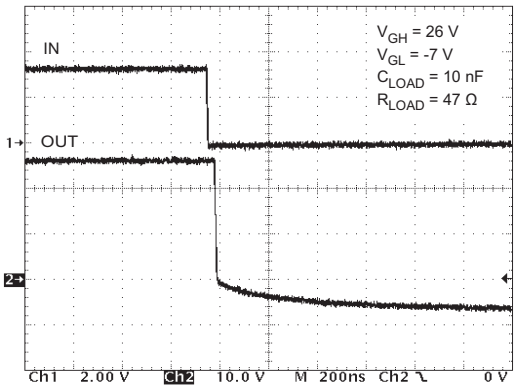


Figure 27.

LEVEL SHIFTER PROPAGATION DELAY IN-OUT, LOW-HIGH, CHANNELS 1-7

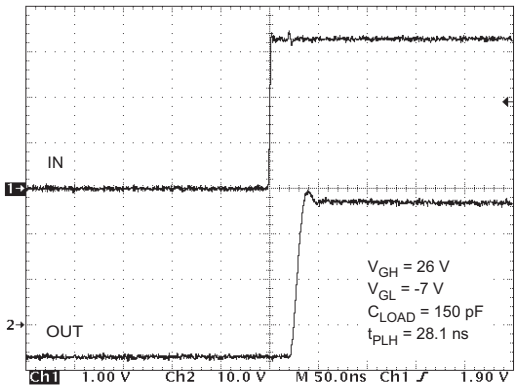


Figure 28.

LEVEL SHIFTER PROPAGATION DELAY IN-OUT, HIGH-LOW, CHANNELS 1-7

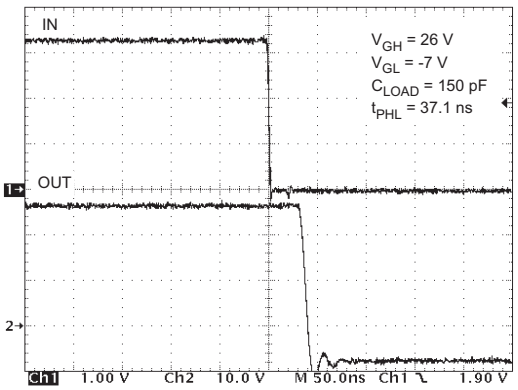


Figure 29.

LEVEL SHIFTER PROPAGATION DELAY IN-OUT, LOW-HIGH, CHANNELS 8-9

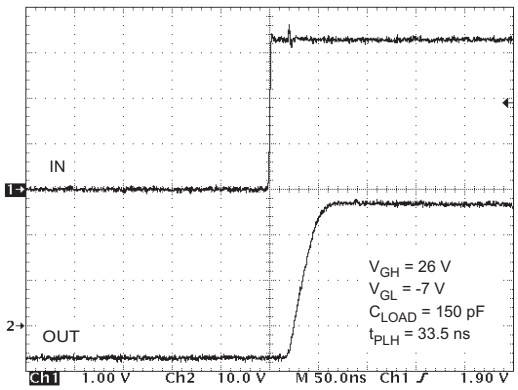


Figure 30.

LEVEL SHIFTER PROPAGATION DELAY IN-OUT, HIGH-LOW, CHANNELS 8-9

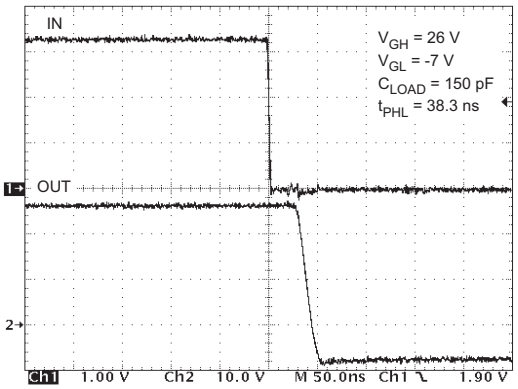


Figure 31.

LEVEL SHIFTER PROPAGATION DELAY FLK-RE, HIGH-LOW, CHANNELS 1-6

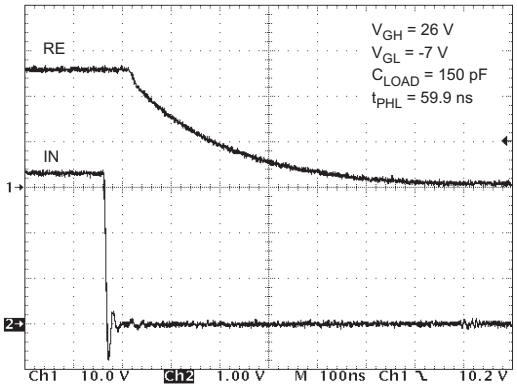


Figure 32.

LEVEL SHIFTER OUTPUT CURRENT CHANNELS 1-7

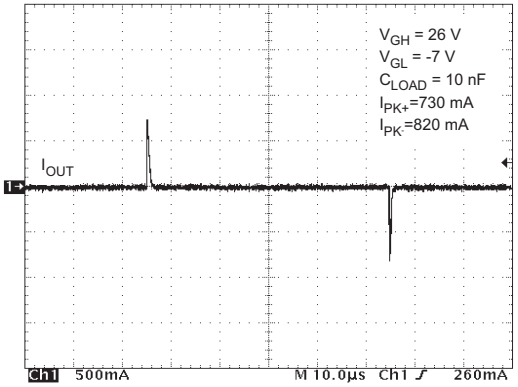


Figure 33.

LEVEL SHIFTER OUTPUT CURRENT CHANNELS 8-9

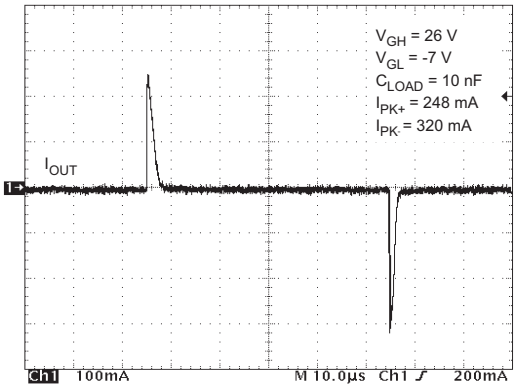


Figure 34.

LEVEL SHIFTER DISCHARGE DURING POWER-UP

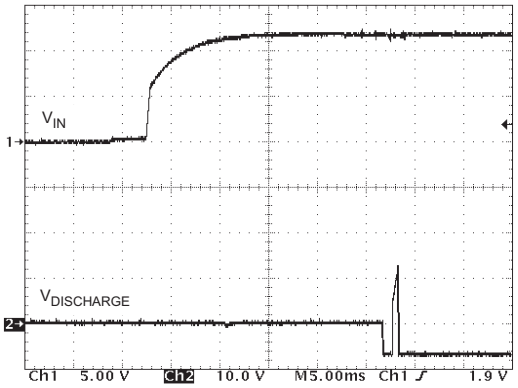


Figure 35.

LEVEL SHIFTER DISCHARGE DURING POWER-DOWN

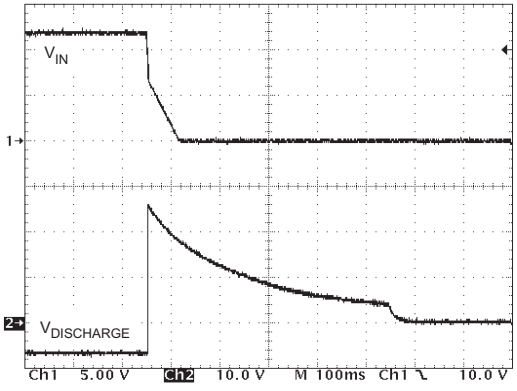


Figure 36.

DETAILED DESCRIPTION

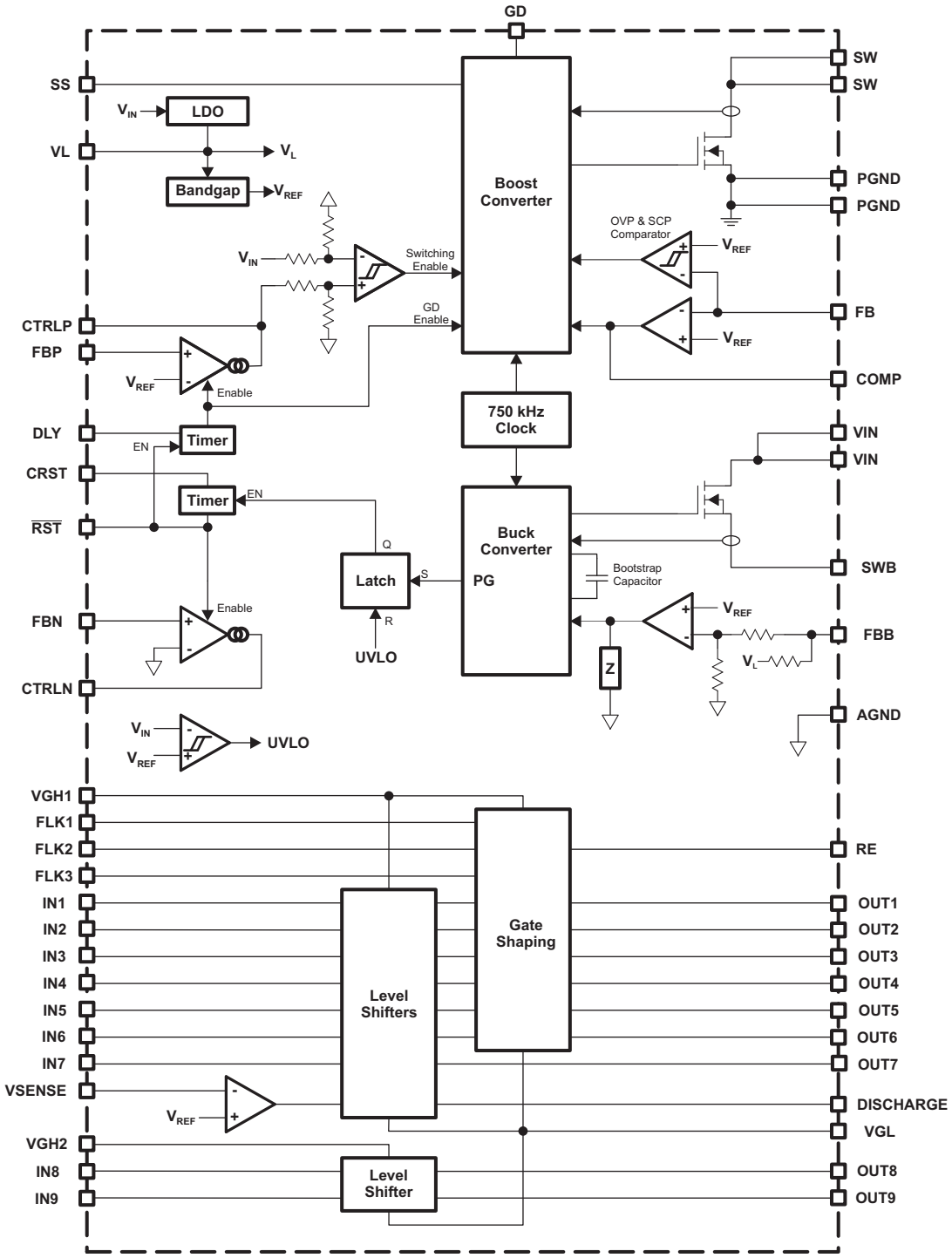


Figure 37. TPS65163 Internal Block Diagram

BOOST CONVERTER

The non-synchronous boost converter uses a current-mode topology and operates at a fixed frequency of 750 kHz. The internal block diagram of the boost converter is shown in Figure 38, and a typical application circuit in Figure 39. External compensation allows designers to optimize performance for individual applications, and is easily implemented by connecting a suitable capacitor/resistor network between the COMP pin and AGND (see the Boost Converter Design Procedure section for more details). The boost converter also controls a GD pin that can be used to drive an external isolation MOSFET.

The boost converter can operate in either continuous conduction mode (CCM) or discontinuous conduction mode (DCM), depending on the load current. At medium and high load currents, the inductor current is always greater than zero and the converter operates in CCM; at low load currents, the inductor current is zero during part of each switching cycle, and the converter operates in DCM. The switch node waveforms for CCM and DCM operation are shown in Figure 5 and Figure 6. Note that the ringing seen during DCM operation occurs because of parasitic capacitance in the PCB layout and is quite normal for DCM operation. There is very little energy contained in the ringing waveform and it does not significantly affect EMI performance.

Equation 1 can be used to calculate the load current below which the boost converter operates in DCM.

$$I_{DCM} = \frac{(V_S - V_{IN})}{2 \times L \times f_{SW}} \times \frac{V_{IN}}{V_{OUT}} \quad (1)$$

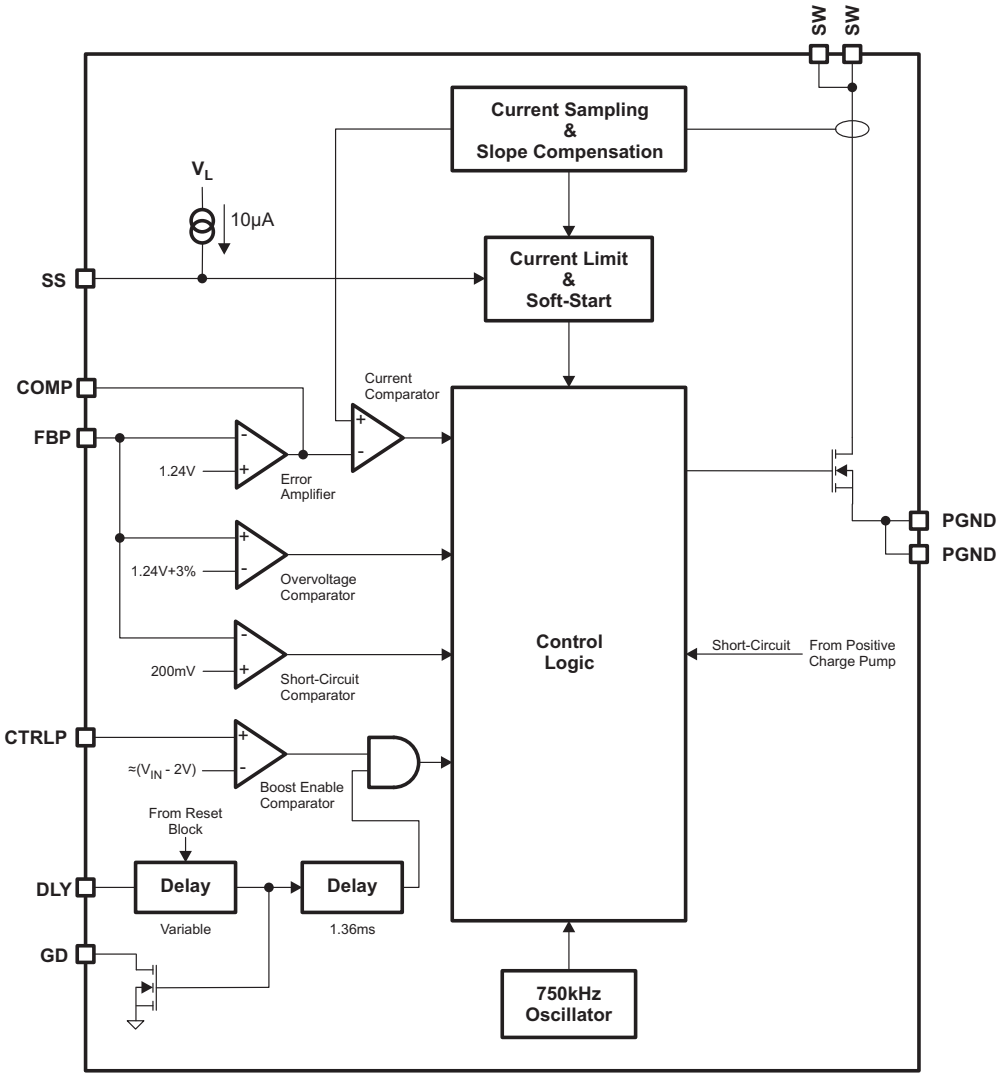


Figure 38. Boost Converter Internal Block Diagram

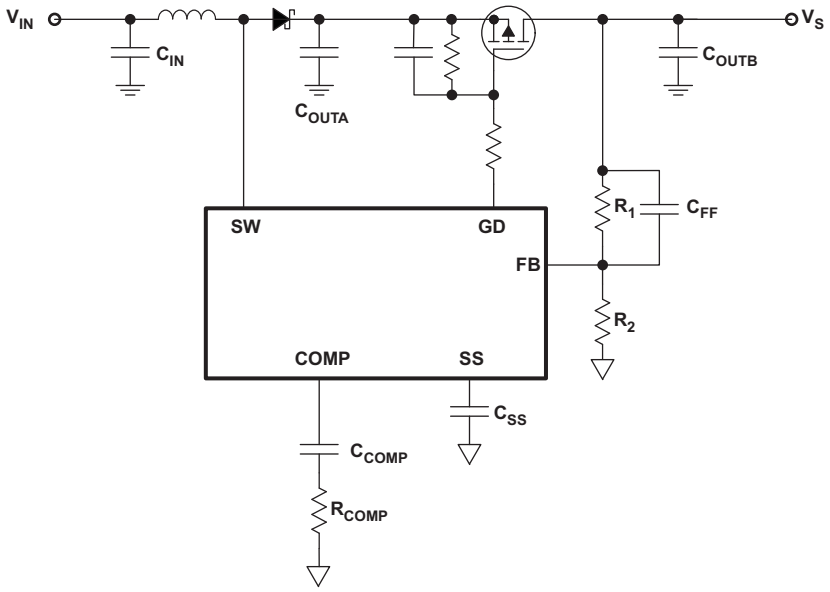


Figure 39. Boost Converter Typical Application Circuit

PROTECTION (BOOST CONVERTER)

The boost converter is protected against potentially damaging conditions such as overvoltage and short circuits. An error condition is detected if the voltage on the converter's FB pin remains below 200 mV for longer than 1.36 ms, in which case the converter stops switching and is latched in the OFF condition. To resume normal operation, the TPS65163 must be turned off and then turned on again.

Note: Because the positive charge pump is driven from its switch node, an error condition on the boost converter output also causes the loss of V_{GH} until the circuit recovers.

The boost converter also stops switching while the positive charge pump is in a short-circuit condition. This condition is not latched, however, and the boost converter automatically resumes normal operation once the short-circuit condition has been removed from the positive charge pump.

BOOST CONVERTER DESIGN PROCEDURE

Calculate Converter Duty Cycle (Boost Converter)

The simplest way to calculate the boost converter duty cycle is to use the efficiency curve in Figure 1 to determine the converter efficiency under the anticipated load conditions and insert this value into Equation 2 (1). Alternatively, a worst-case value (e.g., 90%) can be used for efficiency.

$$D = 1 - \frac{V_{IN} \times \eta}{V_S} \tag{2}$$

(1) Valid only when boost converter operates in CCM.

where V_S is the output voltage of the boost converter.

Calculate Maximum Output Current (Boost Converter)

The maximum output current I_S that the boost converter can supply can be calculated using Equation 3. The minimum specified output current occurs at the maximum duty cycle (which occurs at minimum V_{IN}) and minimum frequency (600 kHz).

$$I_S = \left(I_{LIM} - \frac{V_{IN} \times D}{2 \times f_{SW} \times L} \right) \times (1 - D) \tag{3}$$

where I_{LIM} is the minimum specified switch current limit (2.8 A) and f_{SW} is the converter switching frequency.

Calculate Peak Switch Current (Boost Converter)

Equation 4 can be used to calculate the peak switch current occurring in a given application. The worst-case (maximum) peak current occurs at the minimum input voltage and maximum duty cycle.

$$I_{SW(PK)} = \frac{I_S}{1 - D} + \frac{V_{IN} \times D}{2 \times f_{SW} \times L} \quad (4)$$

Inductor Selection (Boost Converter)

The boost converter is designed for use with inductors in the range 6.8 µH to 15 µH. A 10-µH inductor is typical. Inductors should be capable of supporting at least 125% of the peak current calculated by Equation 4 without saturating. This ensures sufficient margin to tolerate heavy load transients. Alternatively, a more conservative approach can be used in which an inductor is selected whose saturation current is greater than the maximum switch current limit (4.2 A).

Another important parameter is dc resistance, which can significantly affect the overall converter efficiency. Physically larger inductors tend to have lower dc resistance (DCR) because they can use thicker wire. The type and core material of the inductor can also affect efficiency, sometimes by as much as 10%. Table 1 shows some suitable inductors.

Table 1. Boost Converter Inductor Selection

PART NUMBER	INDUCTOR VALUE	COMPONENT SUPPLIER	SIZE (L×W×H, mm)	I_{SAT} / DCR
CDRH8D43	10 µH	Sumida	8.3 × 8.3 × 4.5	4 A / 29 mΩ
CDRH8D38	10 µH	Sumida	8.3 × 8.3 × 4	3 A / 38 mΩ
MSS 1048-103	10 µH	Coilcraft	10.5 × 10.5 × 5.1	4.8 A / 26 mΩ
744066100	10 µH	Wuerth	10 × 10 × 3.8	4 A / 28 mΩ

Rectifier Diode Selection (Boost Converter)

For highest efficiency, the rectifier diode should be a Schottky type. Its reverse voltage rating should be higher than the maximum output voltage V_S. The average rectified forward current through the diode is the same as the output current.

$$I_{D(AVG)} = I_S \quad (5)$$

A Shottky diode with a 2-A average rectified current rating is adequate for most applications. Smaller diodes can be used in applications with lower output current; however, the diode must be able to handle the power dissipated in it, which can be calculated using Equation 6. Table 2 lists some diodes suitable for use in typical applications.

$$P_D = I_{D(AVG)} \times V_F \quad (6)$$

Table 2. Boost Converter Rectifier Diode Selection

PART NUMBER	V_R / I_{AVG}	V_F	$R_{\theta JA}$	SIZE	COMPONENT SUPPLIER
MBRS320	20 V / 3 A	0.44 V at 3 A	46°C/W	SMC	International Rectifier
SL22	20 V / 2 A	0.44 V at 2 A	75°C/W	SMB	Vishay Semiconductor
SS22	20 V / 2 A	0.5 V at 2 A	75°C/W	SMB	Fairchild Semiconductor

Output Capacitance Selection (Boost Converter)

For best performance, a total output capacitance (C_{OUTA} + C_{OUTB} in Figure 39) in the range 50 µF to 100 µF is recommended. At least 20 µF of the total output capacitance should be connected directly to the cathode of the boost converter rectifier diode, i.e., in front of the isolation switch.

Operating the boost converter with little or no capacitance in front of the isolation switch may cause overvoltage conditions that reduce reliability of the TPS65163.

Table 3 suggests some output capacitors suitable for use with the boost converter.

Table 3. Boost Converter Output Capacitor Selection

PART NUMBER	VALUE / VOLTAGE RATING	COMPONENT SUPPLIER
GRM32ER61E226KE15	22 µF / 25 V	Murata
GRM31CR61E106KA12	10 µF / 25 V	Murata
UMK325BJ106MM	10 µF / 50 V	Taiyo Yuden

Setting the Output Voltage (Boost Converter)

The boost converter output voltage is programmed by a resistor divider according to Equation 7.

$$V_S = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right) \quad (7)$$

where V_{REF} is the internal 1.24-V reference of the IC.

A current of the order of 100 µA through the resistor network ensures good accuracy and improves noise immunity. A good approach is to assume a value of about 12 kΩ for the lower resistor (R_2) and then select the upper resistor (R_1) to set the desired output voltage.

Compensation (Boost Converter)

Boost converter external compensation can be fine-tuned for each individual application. Recommended starting values are 33 kΩ and 1 nF, which introduce a pole at the origin for high dc gain and a zero for good transient response. The frequency of the zero set by the compensation components can be calculated using Equation 8.

$$f_z = \frac{1}{2 \times \pi \times R_{COMP} \times C_{COMP}} \quad (8)$$

Selecting the Soft-Start Capacitor (Boost Converter)

The boost converter features a programmable soft-start function that ramps up the output voltage to limit the inrush current drawn from the supply voltage. The soft-start duration is set by the capacitor connected between the SS pin and AGND according to Equation 9.

$$t_{SS} = \frac{C_{SS} \times V_{REF}}{I_{SS}} \quad (9)$$

where C_{SS} is the capacitor connected between the SS pin and GND, V_{REF} is the internal 1.24-V reference of the IC, and I_{SS} is the internally generated 10-µA soft-start current.

Selecting the Isolation Switch Gate Drive Components

The isolation switch is controlled by an active-low signal generated by the GD pin. Because this signal is open-drain, an external pullup resistor is required to turn the MOSFET switch off. If the maximum MOSFET gate-source voltage rating is less than the maximum V_{IN}, two resistors in series can be used to reduce the maximum V_{GS} applied to the device. The exact value of the gate drive resistors is not critical: 100 kΩ for both is a good value to start with.

A capacitor can also be connected in parallel with the top resistor, as illustrated in Figure 39. The effect of this capacitor is to slow down the speed with which the transistor turns on, thereby limiting inrush current. (Note that the capacitor also slows down the speed with which the transistor turns off, and therefore the speed with which it can respond to error conditions.)

Even when trying to limit inrush current, the capacitor must not be too large or the output voltage will rise so slowly the condition will be interpreted as an error (see the *Power Supply Sequencing in Detail* section). Typical values are 10 nF to 100 nF, depending on the transistor used for the isolation switch and the value of the gate-drive resistors.

Note that even in applications that do not use an isolation switch, an external pullup resistor (typically 100 kΩ) between GD and V_{IN} is required.

BUCK CONVERTER

The buck converter is a non-synchronous type that runs at a fixed frequency of 750 kHz. The converter features integrated soft-start (0.66 ms), bootstrap, and compensation circuits to minimize external component count. The buck converter internal block diagram is shown in Figure 40, and a typical application circuit in Figure 41.

The output voltage of the buck converter is internally programmed to 3.3 V and is enabled as soon as V_{IN} exceeds the UVLO threshold. For best performance, the buck converter FB pin should be connected directly to the positive terminal of the output capacitor(s).

The buck converter can operate in either continuous conduction mode (CCM) or discontinuous conduction mode (DCM), depending on the load current. At medium and high load currents, the inductor current is always greater than zero and the converter operates in CCM; at low load currents, the inductor current is zero during part of each switching cycle, and the converter operates in DCM. The switch node waveforms for CCM and DCM operation are shown in Figure 11 and Figure 12. Note that the ringing seen during DCM operation occurs because of parasitic capacitance in the PCB layout and is quite normal for DCM operation. However, there is little energy contained in the ringing waveform, and it does not significantly affect EMI performance. Equation 10 can be used to calculate the load current below which the buck converter operates in DCM.

$$I_{DCM} = \frac{(V_{IN} - V_{LOGIC})}{2 \times L \times f_{SW}} \times \frac{V_{LOGIC}}{V_{IN}} \quad (10)$$

The buck converter uses a skip mode to regulate V_{LOGIC} at low load currents. This mode allows the converter to maintain its output at the required voltage while still meeting the requirement of a *minimum on-time*. The buck converter enters skip mode when its feedback voltage exceeds the skip-mode threshold (25% above the normal V_{FBB} regulation voltage). During skip mode, the buck converter switches for a few cycles, then stops switching for a few cycles, and then starts switching again, and so on, for as long as V_{FBB} remains above the skip-mode threshold. Output voltage ripple can be higher during skip mode (see Figure 13).

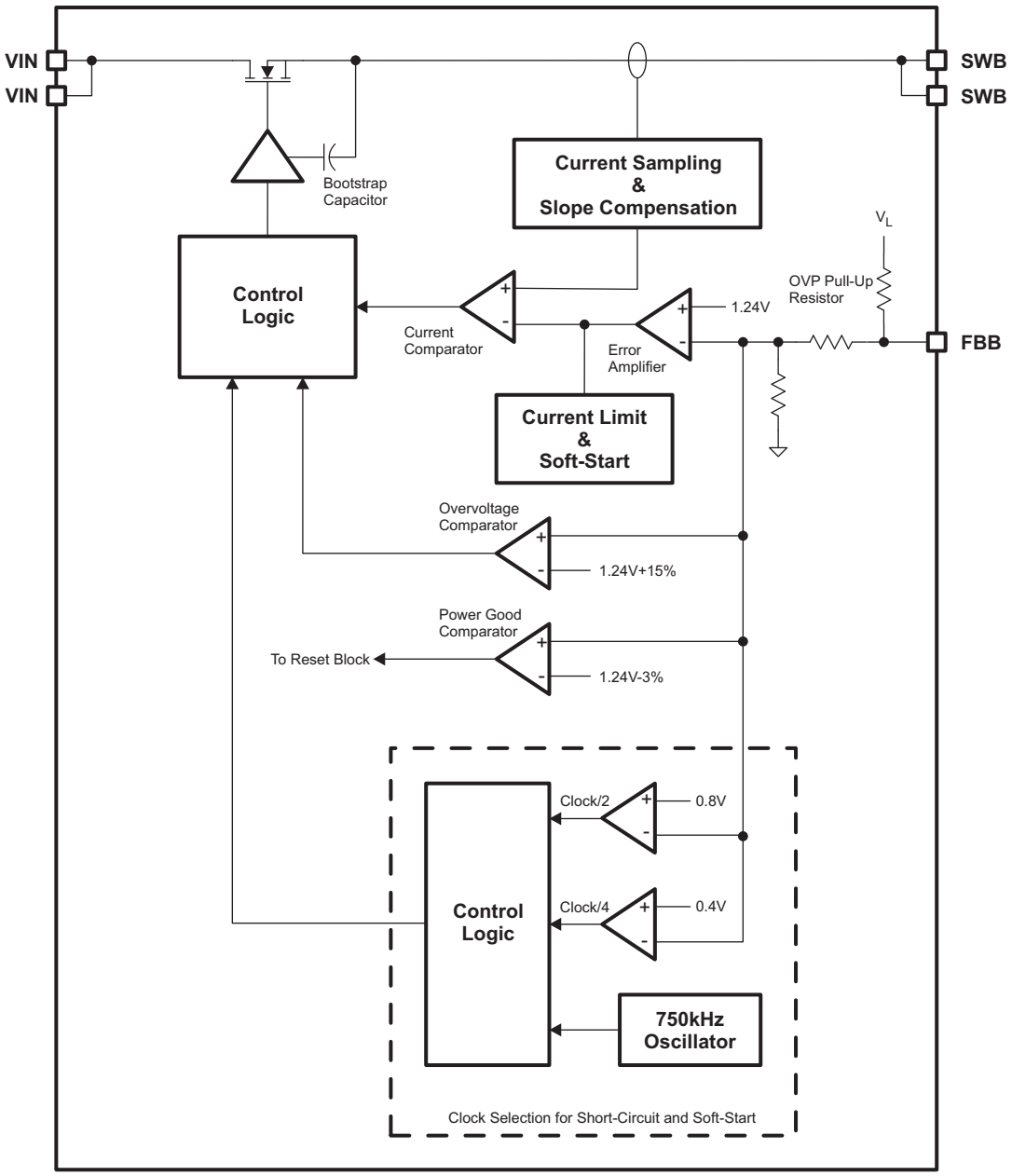


Figure 40. Buck Converter Internal Block Diagram

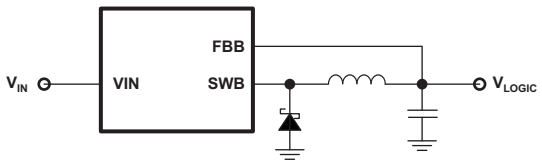


Figure 41. Buck Converter Application Circuit

PROTECTION (BUCK CONVERTER)

To protect against short-circuit conditions, the buck converter automatically limits its output current when the voltage applied to its FBB pin is less than 1.065 V. To reduce power dissipation in the IC, the buck converter switches at 25% of its nominal switching frequency as long as V_{FBB} < 1.065 V. When V_{FBB} is between 1.065 V and 2.13 V, the buck converter switches at 50% of its nominal switching frequency.

Note: Because the negative charge pump is driven from its switch node, a short-circuit condition on the buck converter output also causes the loss of V_{GL} until the short circuit is removed.

An internal pullup prevents the buck converter from generating excessive output voltages if its FBB pin is left floating.

Buck Converter Design Procedure

Because the negative charge pump is driven from the buck converter switch node, the effective output current for design purposes is greater than I_{LOGIC} alone. For best performance, the effective current calculated using Equation 11 should be used during the design.

$$I_{LOGIC(EFFECTIVE)} = I_{LOGIC} + \frac{|V_{GL}| \times I_{GL}}{V_{LOGIC}} \quad (11)$$

Calculate Converter Duty Cycle (Buck Converter)

The simplest way to calculate the converter duty cycle is to use the efficiency curve in Figure 7 to determine the converter efficiency under the anticipated load conditions and insert this value into Equation 12 (1). Alternatively, a worst-case value (e.g., 80%) can be used for efficiency.

$$D = \frac{V_{LOGIC}}{V_{IN} \times \eta} \quad (12)$$

(1) Valid only when buck converter operates in CCM.

Calculate Maximum Output Current (Buck Converter)

The maximum output current that the buck converter can supply can be calculated using Equation 13. The minimum specified output current occurs at the minimum duty cycle (which occurs at maximum V_{IN}) and maximum frequency (900 kHz).

$$I_{LOGIC(EFFECTIVE)} = I_{SW(LIM)} - \frac{V_{IN} \times (1 - D)}{2 \times f_{SW} \times L} \times D \quad (13)$$

Where $I_{SW(LIM)}$ is the minimum specified switch current limit (1.5 A) and f_{SW} is the converter switching frequency.

Calculate Peak Switch Current (Buck Converter)

Equation 14 can be used to calculate the peak switch current occurring in a given application. The worst-case (maximum) peak current occurs at maximum V_{IN}.

$$I_{SW(PK)} = I_{LOGIC(EFFECTIVE)} + \frac{V_{IN} \times (1 - D)}{2 \times f_{SW} \times L} \times D \quad (14)$$

Inductor Selection (Buck Converter)

The buck converter is designed for use with inductors in the range 6.8 µH to 15 µH, and is optimized for 10 µH. The inductor must be capable of supporting the peak current calculated by Equation 14 without saturating. Alternatively, a more conservative approach can be used in which an inductor is selected whose saturation current is greater than the maximum switch current limit (2.25 A).

Another important parameter is dc resistance, which can significantly affect the overall converter efficiency. Physically larger inductors tend to have lower dc resistance (DCR) due to the use of thicker wire. The type and core material of the inductor can also affect efficiency, sometimes by as much as 10%. Table 4 shows some suitable inductors.

Table 4. Buck Converter Inductor Selection

PART NUMBER	INDUCTOR VALUE	COMPONENT SUPPLIER	SIZE (L×W×H, mm)	I_{SAT} / DCR
CDRH8D43	10 µH	Sumida	8.3 × 8.3 × 4.5	4 A / 29 mΩ
CDRH8D38	10 µH	Sumida	8.3 × 8.3 × 4	3 A / 38 mΩ
MSS 1048-103	10 µH	Coilcraft	10.5 × 10.5 × 5.1	4.8 A / 26 mΩ
744066100	10 µH	Wuerth	10 × 10 × 3.8	4 A / 28 mΩ

Rectifier Diode Selection (Buck Converter)

To achieve good efficiency, the rectifier diode should be a Schottky type. Its reverse voltage rating should be higher than the maximum V_{IN}. The average rectified forward current through the diode can be calculated using Equation 15.

$$I_{RECT(AVG)} = I_{LOGIC(EFFECTIVE)} \times (1 - D) \quad (15)$$

A Schottky diode with a 2-A average rectified current rating is adequate for most applications. Smaller diodes can be used in applications with lower output current; however, the diode must be able to handle the power dissipated in it, which can be calculated using Equation 16.

$$P_{RECT} = I_{RECT(AVG)} \times V_F \quad (16)$$

Table 5. Buck Converter Rectifier Diode Selection

PART NUMBER	V_R / I_{AVG}	V_F	$R_{\theta JA}$	SIZE	COMPONENT SUPPLIER
MBRS320	20 V / 3 A	0.44 V at 3 A	46°C/W	SMC	International Rectifier
SL22	20 V / 2 A	0.44 V at 2 A	75°C/W	SMB	Vishay Semiconductor
SS22	20 V / 2 A	0.5 V at 2 A	75°C/W	SMB	Fairchild Semiconductor

Output Capacitance Selection (Buck Converter)

To minimize output voltage ripple, the output capacitors should be good-quality ceramic types with low ESR. The buck converter is stable over a range of output capacitance values, but an output capacitance of 44 µF is a good starting point for typical applications.

POSITIVE CHARGE PUMP CONTROLLER

The positive charge pump is driven directly from the boost converter switch node and regulated by controlling the current through an external PNP transistor. An internal block diagram of the positive charge pump is shown in Figure 42 and a typical application circuit in Figure 43.

During normal operation, the TPS65163 is able to provide up to 5 mA of base current and is designed to work best with transistors whose dc gain (h_{FE}) is between 100 and 300. The charge pump is protected against short circuits on its output, which are detected when the voltage on the charge pump feedback pin (V_{FBP}) is below 100 mV. During short-circuit mode, the base current available from the CTRLP pin is limited to 55 µA. Note that if a short circuit is detected during normal operation, boost converter switching is also halted until V_{FBP} > 100 mV.

NOTE

The emitter of the external PNP transistor should always be connected to V_S, the output of the boost converter at the output side of the isolation switch. The TPS65163 uses the CTRLP pin to sense the voltage across the isolation switch and control boost converter start-up. Connecting the emitter of the external PNP transistor to any other voltage (e.g., V_{IN}) prevents proper start-up of the boost converter and positive charge pump.

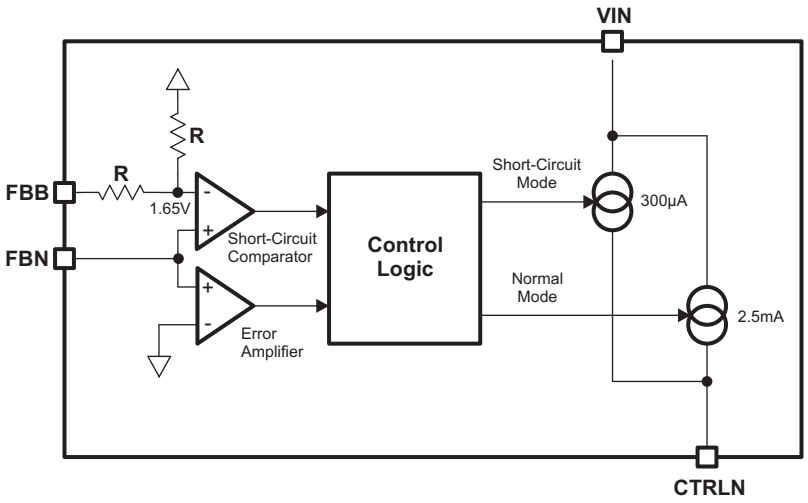


Figure 42. Positive Charge Pump Internal Block Diagram

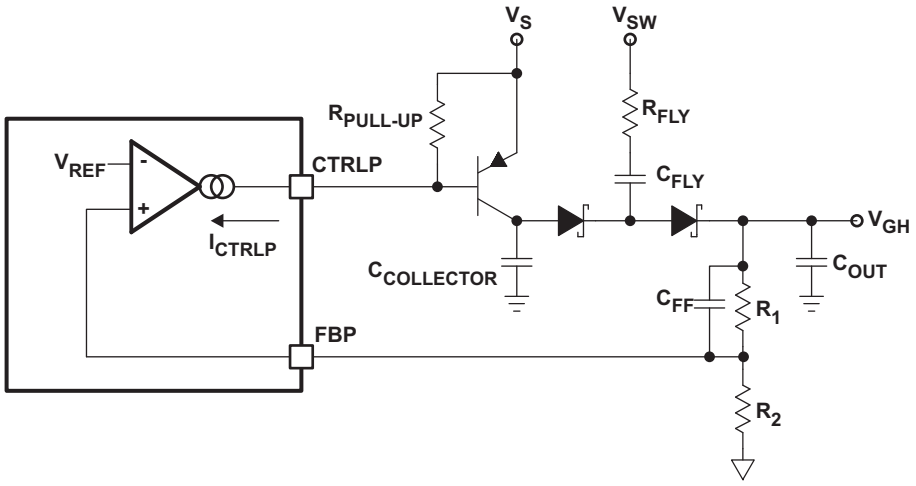


Figure 43. Positive Charge Pump Application Circuit

POSITIVE CHARGE PUMP DESIGN PROCEDURE

Setting the Output Voltage (Positive Charge Pump)

The positive charge pump output voltage is programmed by a resistor divider according to Equation 17.

$$V_{GH} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right) \tag{17}$$

where V_{REF} is the internal 1.24-V reference of the TPS65163.

Rearranging Equation 17, the values of R_1 and R_2 are calculated:

$$R_1 = R_2 \times \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \tag{18}$$

A current of the order of 1 mA through the resistor network ensures good accuracy and increases the circuit's immunity to noise. It also ensures a minimum load on the charge pump, which reduces output voltage ripple under no-load conditions. A good approach is to assume a value of about 1.2 kΩ for the lower resistor (R_2) and then select the upper resistor (R_1) to set the desired output voltage.

Note that the maximum voltage in an application is determined by the boost converter output voltage and the voltage drop across the diodes and PNP transistor. For a typical application in which the positive charge pump is configured as a voltage doubler, the maximum output voltage is given by Equation 19.

$$V_{GH(MAX)} = (2 \times V_S) - (2 \times V_F) - V_{CE} \quad (19)$$

where V_S is the output voltage of the boost converter, V_F is the forward voltage of each diode, and V_{CE} is the collector-emitter voltage of the PNP transistor (recommended to be at least 1 V to avoid transistor saturation).

Selecting the Feed-Forward Capacitor (Positive Charge Pump)

To improve transient performance, a feed-forward capacitor connected across the upper feedback resistor (R1) is recommended. The feed-forward capacitor modifies the frequency response of the feedback network by adding the zero, which improves high frequency gain. For typical applications, a zero at 5 kHz is a good place to start, in which case C_{FF} can be calculated using Equation 20.

$$C_{FF} = \frac{1}{2 \times \pi \times 5\,kHz \times R_1} \quad (20)$$

Selecting the PNP Transistor (Positive Charge Pump)

The PNP transistor used to regulate V_{GH} should have a dc gain (h_{FE}) of at least 100 when its collector current is equal to the charge pump output current. The transistor should also be able to withstand voltages up to $2 \times V_S$ across its collector-emitter junction (V_{CE}).

The power dissipated in the transistor is given by Equation 21. The transistor must be able to dissipate this power without its junction becoming too hot. Note that the ability to dissipate power depends on adequate PCB thermal design.

$$P_Q = \left[(2 \times V_S) - (2 \times V_F) - V_{GH}\right] \times I_{GH} \quad (21)$$

where I_{GH} is the mean (not RMS) output current drawn from the charge pump.

A pullup resistor is also required between the base and emitter of the transistor. The value of this resistor is not critical, but it should be large enough not to divert significant current away from the base of the transistor. A value of 100 kΩ is suitable for most applications.

Selecting the Diodes (Positive Charge Pump)

Small-signal diodes can be used for most low-current applications (<50 mA), and higher-rated diodes for higher-power applications. The average current through the diode is equal to the output current, so that the power dissipated in the diode is given by Equation 22.

$$P_D = I_{GH} \times V_F \quad (22)$$

The peak current through the diode occurs during start-up, and for a few cycles may be as high as a few amperes. However, this condition typically lasts for <1 ms and can be tolerated by many diodes whose repetitive current rating is much lower. The reverse voltage rating of the diodes should be equal to $2 \times V_S$.

Table 6. Positive Charge-Pump Diode Selection

PART NUMBER	I_{AVG}	I_{PK}	V_R	V_F	COMPONENT SUPPLIER
BAV99W	150 mA	1 A for 1 ms	75 V	1 V at 50 mA	NXP
BAT54S	200 mA	600 mA for 1 s	30 V	0.8 V at 100 mA	Fairchild Semiconductor
MBR0540	500 mA	5.5 A for 8 ms	40 V	0.51 at 500 mA	Fairchild Semiconductor

Selecting the Capacitors (Positive Charge Pump)

For lowest output voltage ripple, low-ESR ceramic capacitors are recommended. The actual value is not critical, and 1 µF to 10 µF is suitable for most applications. Larger capacitors provide better performance in applications where large load transient currents are present.

A flying capacitor in the range 100 nF to 1 µF is suitable for most applications. Larger values experience a smaller voltage drop by the end of each switching cycle and allow higher output voltages and/or currents to be achieved. Smaller values tend to be physically smaller and a bit cheaper. For best performance, it is recommended to include a resistor of a few ohms (2 Ω is a good value to start with) in series with the flying capacitor to limit peak currents occurring at the instant of switching.

A collector capacitor in the range 100 nF to 1 µF is suitable for most applications. Larger values are more suitable for high-current applications but can affect stability if they are too big.

A combination of C_{OUT} = 10 µF, C_{FLY} = 1 µF, and $C_{COLLECTOR}$ = 100 nF is a good starting point for most applications (the final values can be optimized on a case-by-case basis if necessary).

NEGATIVE CHARGE PUMP

The negative charge pump controller uses an external NPN transistor to regulate an external charge pump circuit. The IC is optimized for use with transistors having a dc gain (h_{FE}) in the range 100 to 300; however, it is possible to use transistors outside this range, depending on the application requirements. Regulation of the charge pump is achieved by using the external transistor as a controlled current source whose output depends on the voltage applied to the FBN pin: the higher the transistor current, the greater the charge transferred to the output during each switching cycle and therefore the higher (i.e., the more negative) the output voltage. The internal block diagram of the negative charge pump is shown in Figure 44, and a typical application circuit in Figure 45.

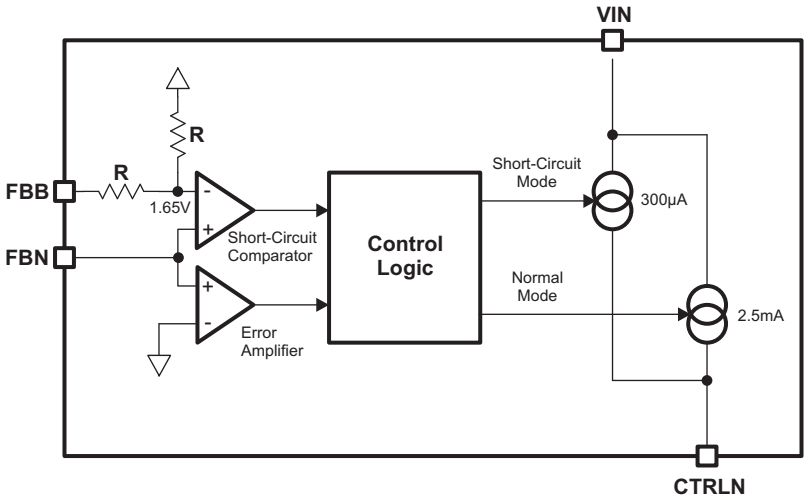


Figure 44. Negative Charge Pump Internal Block Diagram

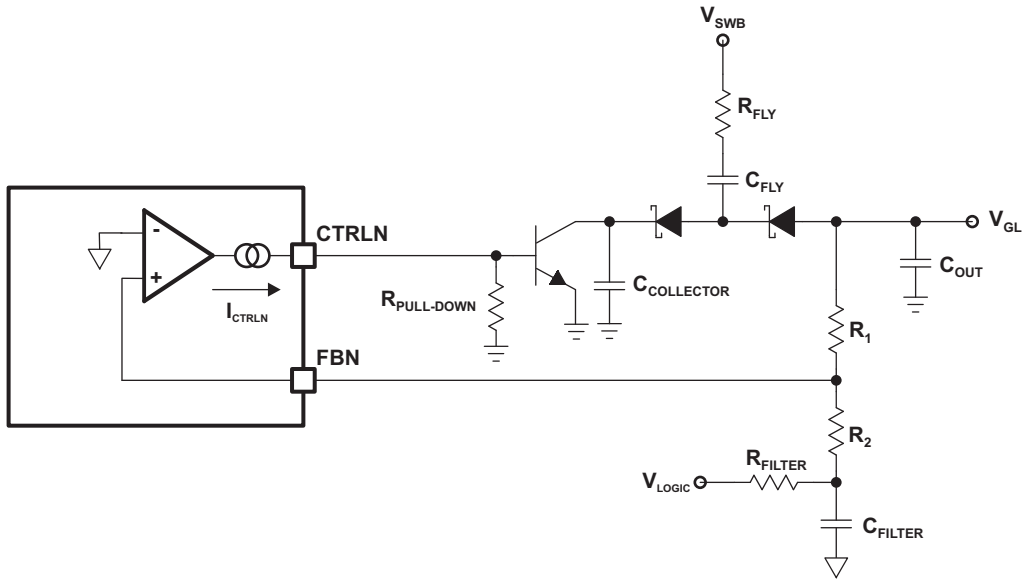


Figure 45. Negative Charge Pump Application Circuit

The TPS65163 contains a circuit to protect the negative charge pump against short circuits on its output. A short-circuit condition is detected as long as the FBN pin remains above 1.65 V, during which time the charge pump output current is limited.

To ensure proper start-up under normal conditions, circuit designers should make sure the full load current is not drawn by the load until the feedback voltage V_{FBN} is below the short-circuit threshold voltage. The value of V_{GL} beyond which the negative charge pump no longer works in short-circuit mode is given by Equation 23.

$$V_{GL(SC)} = -1.65\ V \times \left(1 - \frac{R_1}{R_2}\right) \quad (23)$$

NEGATIVE CHARGE PUMP DESIGN PROCEDURE

Setting the Output Voltage (Negative Charge Pump)

The negative charge pump output voltage is programmed by a resistor divider according to Equation 24.

$$V_{GL} = -V_{LOGIC} \times \frac{R_1}{R_2} \quad (24)$$

Rearranging Equation 25, the values of R_1 and R_2 are calculated.

$$R_1 = R_2 \times \frac{|V_{GL}|}{V_{LOGIC}} \quad (25)$$

A current of the order of 1 mA through the resistor network ensures accuracy and increases the circuit's immunity to noise. It also ensures a minimum load on the charge pump, which reduces output voltage ripple under no-load conditions. A good approach is to assume a value of about 3.3 kΩ for the lower resistor (R_2) and then select the upper resistor (R_1) to set the desired output voltage.

Note that the maximum voltage in an application is determined by the boost converter output voltage and the voltage drop across the diodes and NPN transistor. For a typical application in which the negative charge pump is configured as a voltage inverter, the maximum (i.e., most negative) output voltage is given by Equation 26.

$$V_{GL(MAX)} = -V_{IN} + (2 \times V_F) + V_{CE} \quad (26)$$

where V_F is the forward voltage of each diode and V_{CE} is the collector-emitter voltage of the NPN transistor (recommended to be at least 1 V to avoid transistor saturation).

Selecting the NPN Transistor (Negative Charge Pump)

The NPN transistor used to regulate V_{GL} should have a dc gain (h_{FE}) of at least 100 when its collector current is equal to the charge pump output current. The transistor should also be able to withstand voltages up to V_{IN} across its collector-emitter junction (V_{CE}).

The power dissipated in the transistor is given by Equation 27. The transistor must be able to dissipate this power without its junction becoming too hot. Note that the ability to dissipate power depends heavily on adequate PCB thermal design.

$$P_Q = \left[V_{IN} - (2 \times V_F) - \left| V_{GL} \right| \right] \times I_{GL} \quad (27)$$

where I_{GL} is the *mean* (not RMS) output current drawn from the charge pump.

Selecting the Diodes (Negative Charge Pump)

Small-signal diodes can be used for most low-current applications (<50 mA) and higher-rated diodes for higher-power applications. The average current through the diode is equal to the output current, so that the power dissipated in the diode is given by Equation 28.

$$P_D = I_{GL} \times V_F$$

The peak current through the diode occurs during start-up and for a few cycles may be as high as a few amperes. However, this condition typically lasts for <1 ms and can be tolerated by many diodes whose repetitive current rating is much lower. The diodes' reverse voltage rating should be equal to at least $2 \times V_{IN}$.

Table 7. Negative Charge Pump Diode Selection

PART NUMBER	I_{AVG}	I_{PK}	V_R	V_F	COMPONENT SUPPLIER
BAV99W	150 mA	1 A for 1 ms	75 V	1 V at 50 mA	NXP
BAT54S	200 mA	600 mA for 1 s	30 V	0.8 V at 100 mA	Fairchild Semiconductor
MBR0540	500 mA	5.5 A for 8 ms	40 V	0.51 A at 500 mA	Fairchild Semiconductor

Selecting the Capacitors (Negative Charge Pump)

For lowest output voltage ripple, low-ESR ceramic capacitors are recommended. The actual value is not critical, and 1 µF to 10 µF is suitable for most applications. Larger capacitors provide better performance in applications where large load transient currents are present.

A flying capacitor in the range 100 nF to 1 µF is suitable for most applications. Larger values experience a smaller voltage drop by the end of each switching cycle and allow higher output voltages and/or currents to be achieved. Smaller values tend to be physically smaller and a bit cheaper.

A collector capacitor in the range 100 nF to 1 µF is suitable for most applications. Larger values are more suitable for high-current applications but can affect stability if they are too big.

A combination of C_{OUT} = 10 µF, C_{FLY} = 1 µF, and $C_{COLLECTOR}$ = 100 nF is a good starting point for most applications (the final values can be optimized on a case-by-case basis if necessary).

POWER-SUPPLY SEQUENCING

Figure 46 shows the power-supply sequencing block diagram. The four supply rails generated by the TPS65163 turn on the following sequence: first V_{LOGIC}, then V_{GL}, then V_{GH} and V_S, as shown in Figure 46.

The buck converter turns on when the supply voltage exceeds the undervoltage threshold.

When the internal power-good signal of the buck converter has been asserted, the reset timer starts; after the reset time is over, $\overline{RST}$ goes high and the negative charge pump is enabled. This sequence ensures that the negative charge pump, which is driven by the switch node of the buck converter, does not attempt to draw current until the T-CON is out of reset and drawing current from V_{LOGIC}.

At the same time as the negative charge pump is enabled, an internal delay timer is started. This timer generates a delay, after which the boost converter and positive charge pump are enabled. The delay time t_{DLY} is determined by the capacitor C_{DLY} connected between the DLY pin and AGND according to Equation 29.

$$t_{DLY} = \frac{C_{DLY} \times V_{REF}}{I_{DLY}} \quad (29)$$

No special sequencing is implemented during power-down, and all power supplies are disabled if V_{IN} falls below V_{UVLO}.

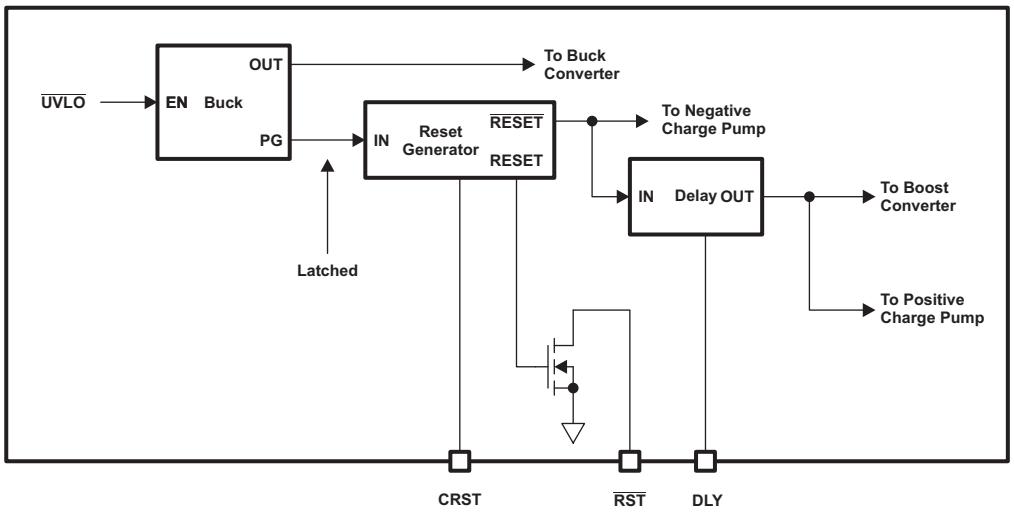


Figure 46. Power Supply Sequencing Block Diagram

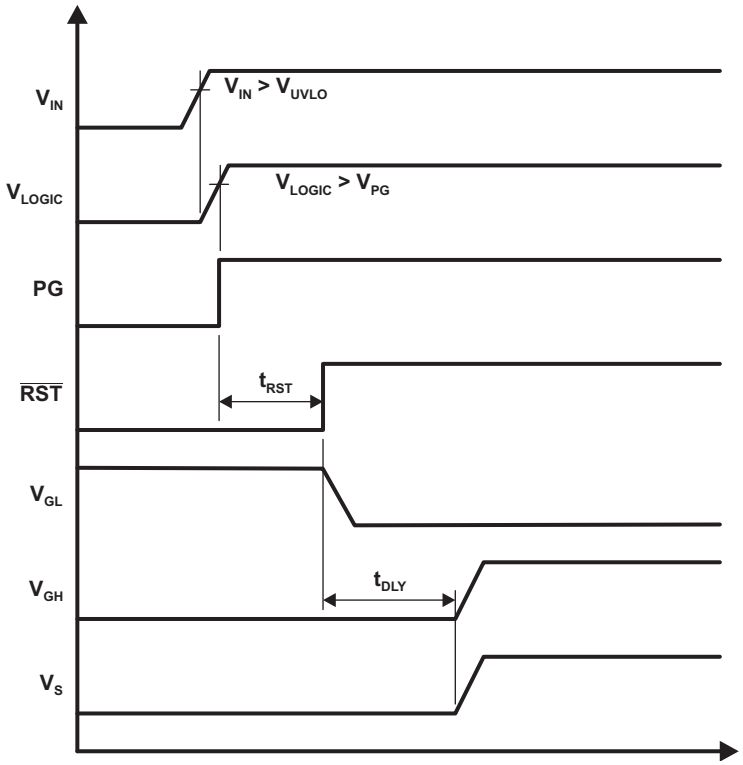


Figure 47. Power Supply Sequencing

POWER-SUPPLY SEQUENCING IN DETAIL

The detailed start-up behavior of the boost converter and positive charge pump is illustrated in Figure 48.

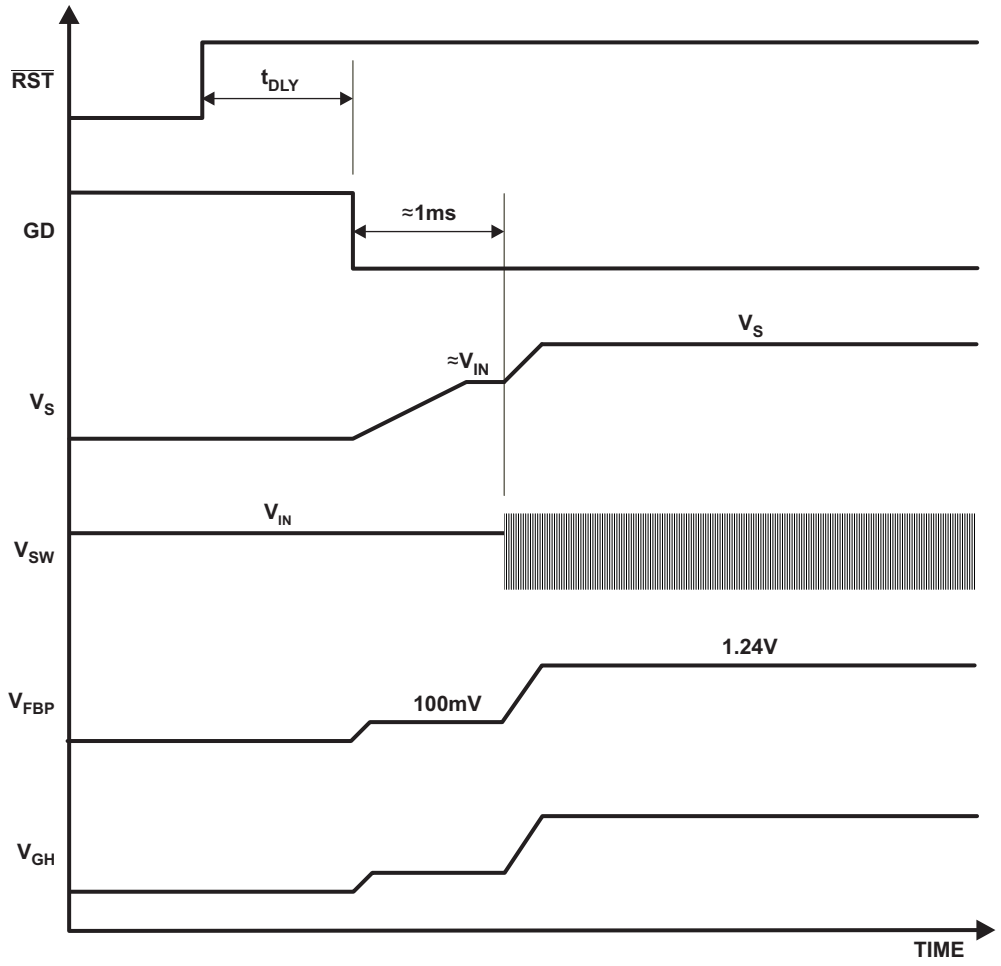


Figure 48. Boost Converter and Positive Charge Pump Detailed Start-Up Behavior

The isolation switch is enabled when the GD pin goes low, t_{DLY} seconds after $\overline{RST}$ goes high. When the isolation switch turns on, V_S rises at a rate determined by the RC network controlling the switch's gate and the amount of capacitance on the output. The TPS65163 senses the rising V_S via the CTRLP pin, and 1 ms after GD goes low checks that $V_S \approx V_{IN}$. If it is, then the boost converter is enabled. This scheme prevents the boost converter from switching before the isolation switch is fully enabled, which could otherwise cause overvoltage conditions to damage the switch node. If V_S does not reach $\approx V_{IN}$ within 1 ms of the GD pin going low, the TPS65163 detects an error condition and the boost converter is not enabled.

The positive charge pump short-circuit mode is enabled when the GD pin goes low. Although the boost converter is not switching at this point, there is a dc path from V_S to V_{GH}, and the output ramps up as current flows into the collector capacitor and output capacitors. When V_{FBP} reaches 100 mV, the IC determines that no short circuit exists, and the output current from the CTRLP pin is disabled temporarily. (If there is no significant load connected to V_{GH}, the output voltage remains almost constant, held up by the output capacitance; if there is a load, the output voltage decays.) When the boost converter starts switching, normal operation of the positive charge pump is enabled, and V_{GH} ramps up to its programmed value. (Note that the positive charge pump implements a soft-start characteristic that ramps the current available from the CTRLP pin over time. This causes the collector voltage of the regulating PNP to go temporarily negative.)

RESET GENERATOR

The reset generator generates an active low signal that can used to reset the timing controller used in LCD applications. The $\overline{RST}$ output is an open-drain type and requires an external pullup resistor. This signal is typically pulled up to the 3.3-V supply generated by the buck converter, which also supplies the timing controller I/O functions.

Reset pulse timing starts when the internal power-good signal of the buck converter is asserted, and its duration is set by the size of the capacitor connected between the CRST pin and AGND, as described by Equation 30.

$$t_{RST} = \frac{C_{RST} \times V_{REF}}{I_{RST}} \quad (30)$$

The duration of the reset pulse also affects power-supply sequencing, as the boost converter and positive charge pump are not enabled until the reset pulse is finished. In applications that do not require a reset signal, the $\overline{RST}$ pin can be left floating or tied to AGND. This does not prevent the boost converter or positive charge pump from starting.

If the CRST pin is left open-circuit, the duration of the reset pulse is close to zero (determined only by the parasitic capacitance present), and the boost converter and positive charge pump start up instantaneously.

Alternatively, the CRST pin can be used to enable the boost converter and charge pumps by connecting a 3.3-V logic-level ENABLE signal via a 10-kΩ resistor, as shown in Figure 49. Using this scheme, the buck converter starts as soon as VIN exceeds the UVLO threshold, but the negative charge pump is not enabled until ENABLE goes high. The boost converter and positive charge pump are enabled t_{DLY} seconds after ENABLE goes high, where t_{DLY} is defined by the capacitor connected to the DLY pin. The resulting power-supply sequencing is shown in Figure 50.

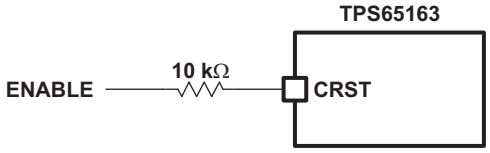


Figure 49. Using an ENABLE Signal to Control Boost Converter and Charge Pumps

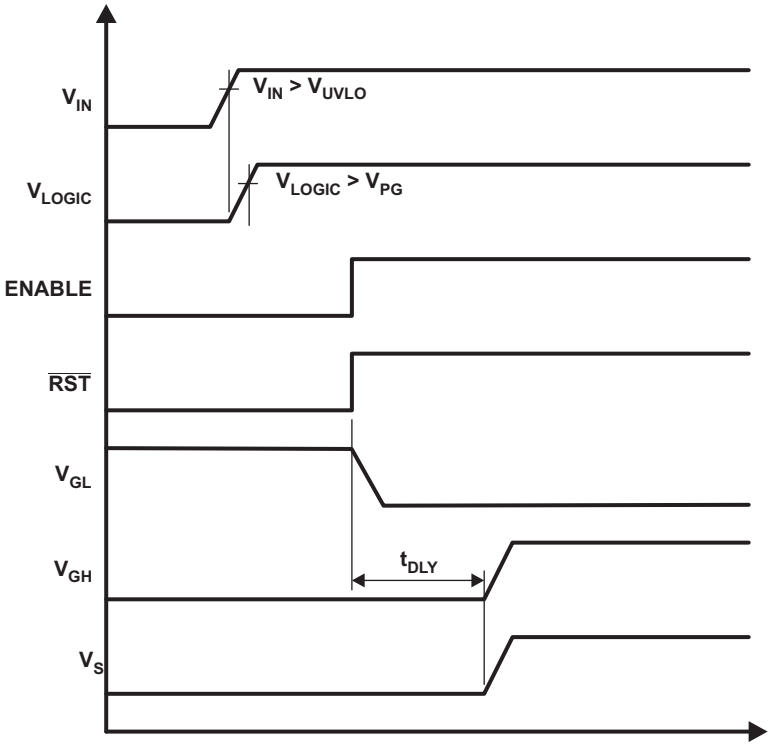


Figure 50. Power-Supply Sequencing Using an ENABLE Signal

Undervoltage Lockout

An undervoltage lockout function inhibits the device if the supply voltage V_{IN} is below the minimum needed for proper operation.

Thermal Shutdown

A thermal shutdown function automatically disables all LCD bias functions if the device junction temperature exceeds ≈150°C. The device automatically starts operating again once it has cooled down to ≈140°C.

Level Shifters and Gate Shaping

The nine level-shifter channels in the TPS65163 are divided into two groups. Channels 1 through 7 are powered from V_{GH1} and V_{GL}, channels 8 and 9 are powered from V_{GH2} and V_{GL}. Channels 1 to 6 support gate shaping and channels 7 through 9 do not. Figure 51 contains a simplified block diagram of one channel with gate voltage shaping.

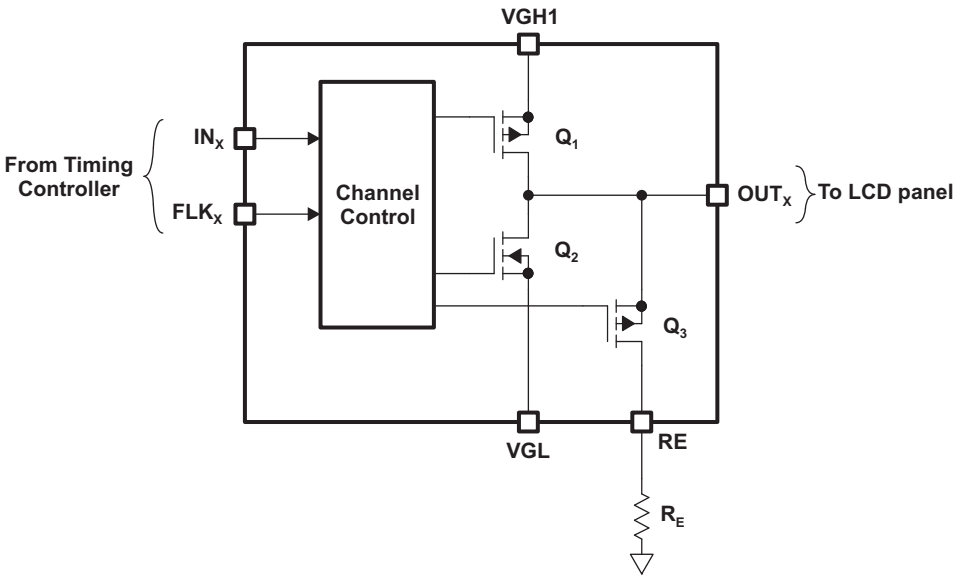


Figure 51. Level Shifter Channel with Gate Voltage Shaping

On the rising edge of IN, Q_1 turns on, Q_2 and Q_3 turn off, and OUT is driven to V_{GH1}. On the falling edge of FLK, Q1 turns off, Q_3 is turned on, and the panel now discharges through Q_3 and R_E (see Figure 52). On the falling edge of IN, Q_2 turns on and Q_3 turns off, and OUT is driven to V_{GL}. This sequence is repeated in turn for each channel.

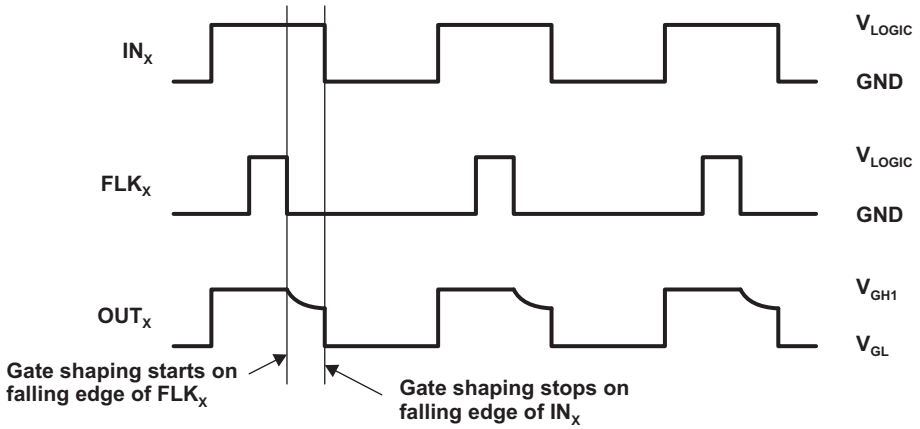


Figure 52. Gate Voltage Shaping Timing Diagram

The alternative configuration shown in Figure 53 can be used to define a minimum gate voltage reached during gate voltage shaping.

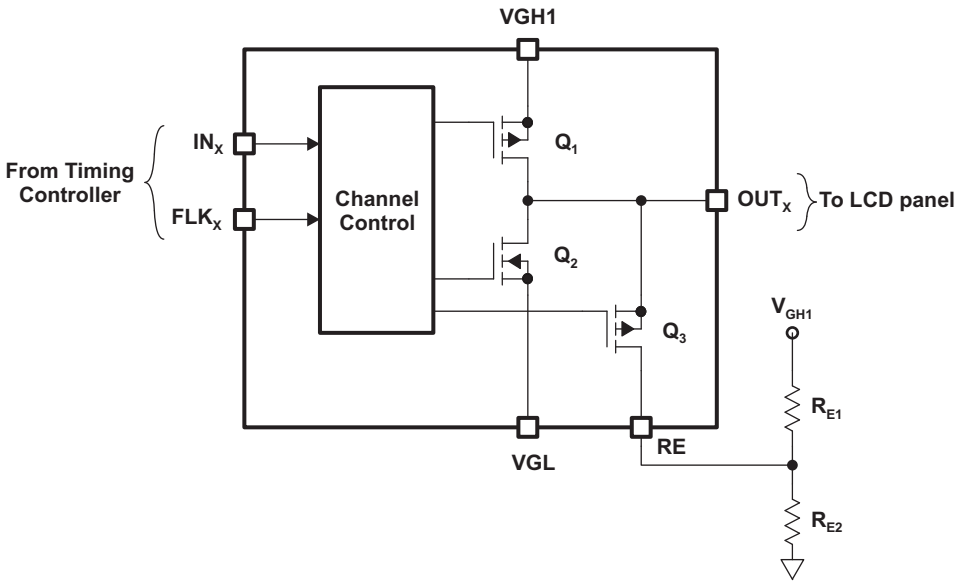


Figure 53. Alternative Gate Voltage Shaping Circuit Configuration

In this circuit, resistors R_{E1} and R_{E2} define both the rate of change of gate voltage decay and the minimum gate voltage V_{MIN}. Using the Thevenin equivalent, the operating parameters of Figure 53 are calculated.

$$V_{MIN} = V_{GH1} \times \frac{R_{E2}}{R_{E1} + R_{E2}} \quad (31)$$

$$R_E = \frac{R_{E1} \times R_{E2}}{R_{E1} + R_{E2}} \quad (32)$$

Flicker Clocks

The gate voltage shaping control logic in the TPS65163 allows the device to be used with one, two or three flicker clock signals, according to the application requirements.

In six-phase applications where one signal controls gate voltage shaping for six CLK channels, the flicker clock should be connected to FLK1 and the unused pins FLK2 and FLK3 connected to GND.

In six-phase applications where three signals control gate voltage shaping for six CLK channels, the flicker clock for channels 1 and 4 should be connected to FLK1, the flicker clock for channels 2 and 5 connected to FLK2, and the flicker clock for channels 3 and 6 connected to FLK3.

In four-phase applications where two signals control gate voltage shaping for four CLK channels, the flicker clock for phases 1 and 3 should be connected to FLK1, the flicker clock for phases 2 and 4 connected to FLK2, and the unused FLK3 pin connected to GND. The unused pins IN3 and IN6 should be connected to V_{LOGIC}. Alternatively, IN3 can be connected to IN2 and IN6 connected to IN5; this arrangement can simplify PCB layout.

Gate voltage shaping is started by the falling edge of the FLK signal(s), which must occur during a valid part of the clock waveform. For six-phase systems, this means the last 60° of the clock waveform; for four-phase systems, this means the last 90° of the clock waveform (see Figure 54 and Figure 55). Falling edges of the FLK signal(s) occurring outside the valid part of the clock waveform are ignored. The rising edge of the FLK signal(s) has no effect, regardless of when it occurs.

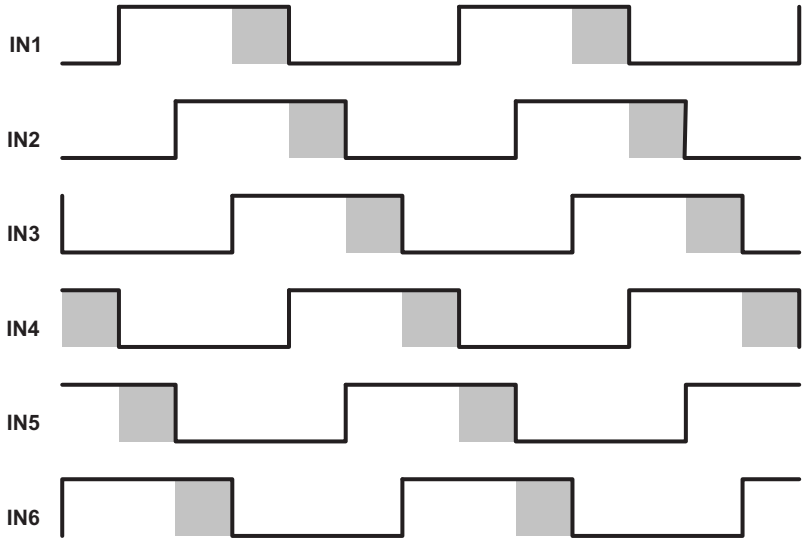


Figure 54. FLK Falling Edge Validity, Six-Phase Applications

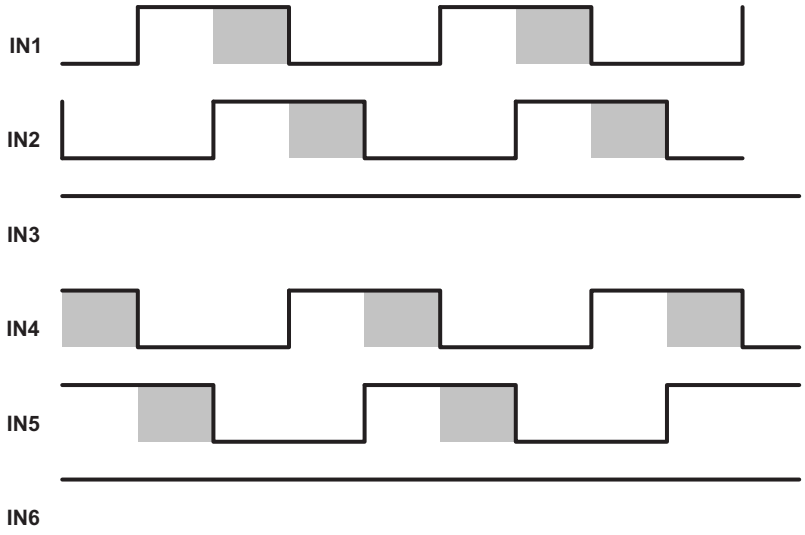


Figure 55. FLK Falling Edge Validity, Four-Phase Applications

Level Shifters Without Gate Voltage Shaping

Channels 7 through 9 do not support gate voltage shaping and are controlled only by the logic level applied to their INx pin. Figure 56 contains a block diagram of a channel that does not support gate voltage shaping.

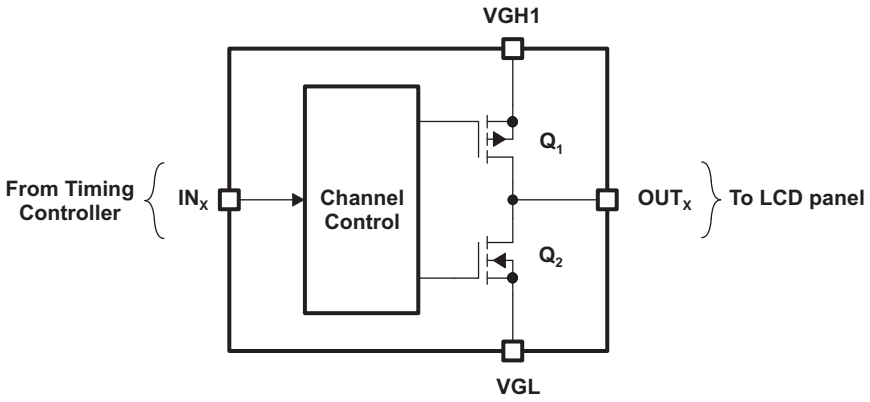


Figure 56. Block Diagram of Level Shifter Without Gate Voltage Shaping

Panel Discharge

The TPS65163 contains a function for discharging the display panel during power down. The discharge function comprises a comparator and a level shifter (see Figure 57). During normal operation, the voltage applied to the VSENSE pin is greater than V_{REF}, the output of the level shifter is low, and the DISCHARGE signal is at V_{GL}. During power down, when the voltage applied to the VSENSE pin falls below V_{REF}, the level shifter output goes high and the DISCHARGE signal tracks V_{GH1} as it discharges (see Figure 35 and Figure 36).

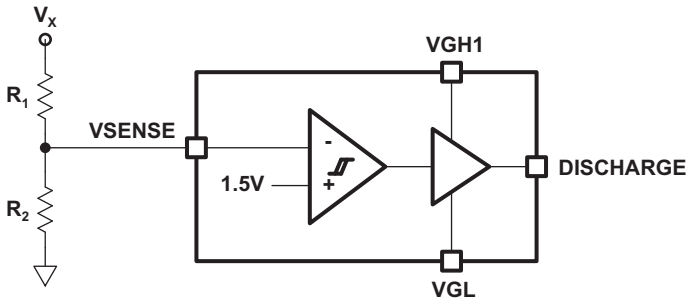


Figure 57. Panel Discharge Function Block Diagram

Suitable values for resistors R_1 and R_2 in Figure 57 are calculated using Equation 33.

$$R_1 = R_2 \times \left(\frac{V_X}{1.5V} - 1 \right) \tag{33}$$

where V_X is the voltage used to activate/deactivate the discharge function.

For most applications, a value between 1 kΩ and 10 kΩ for R_2 can be used (R_1 depends on the value of R_2 and the value of V_X).

APPLICATION INFORMATION

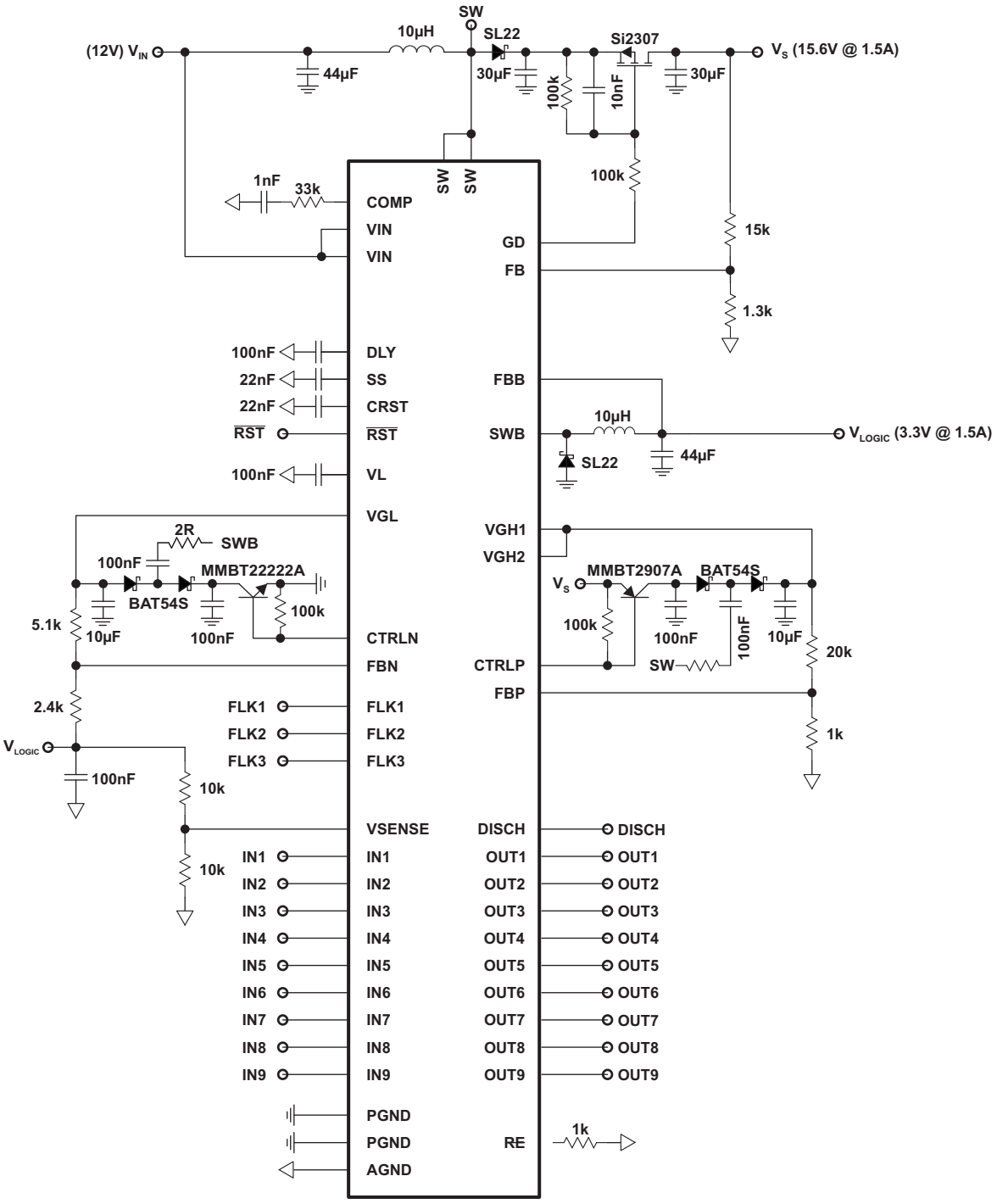


Figure 58. Typical LCD Bias Application Circuit

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS65163RGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	Call TI	Level-3-260C-168 HR	-40 to 85	TPS65163	Samples
TPS65163RGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TPS65163	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

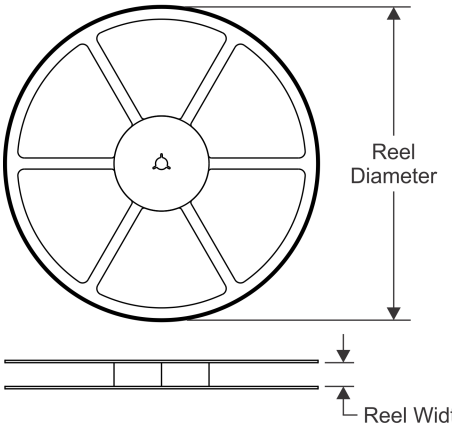
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

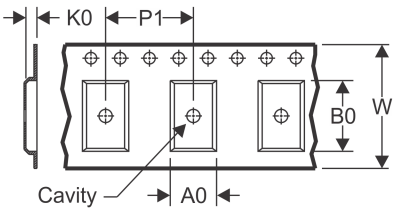
(4) Only one of markings shown within the brackets will appear on the physical device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

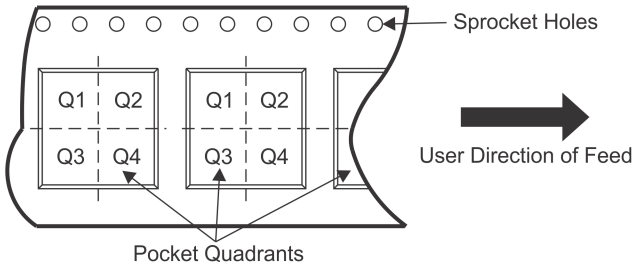


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

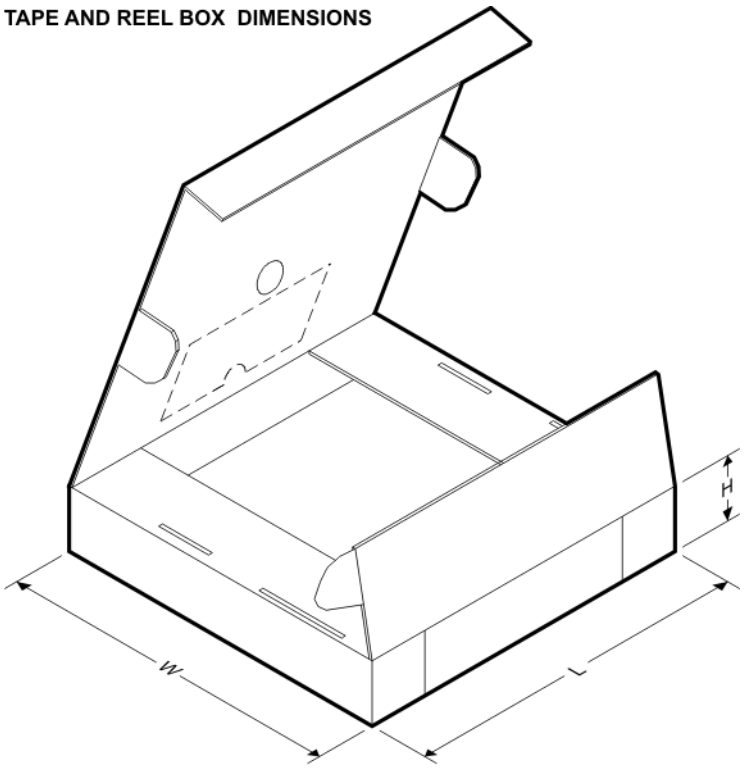
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65163RGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2

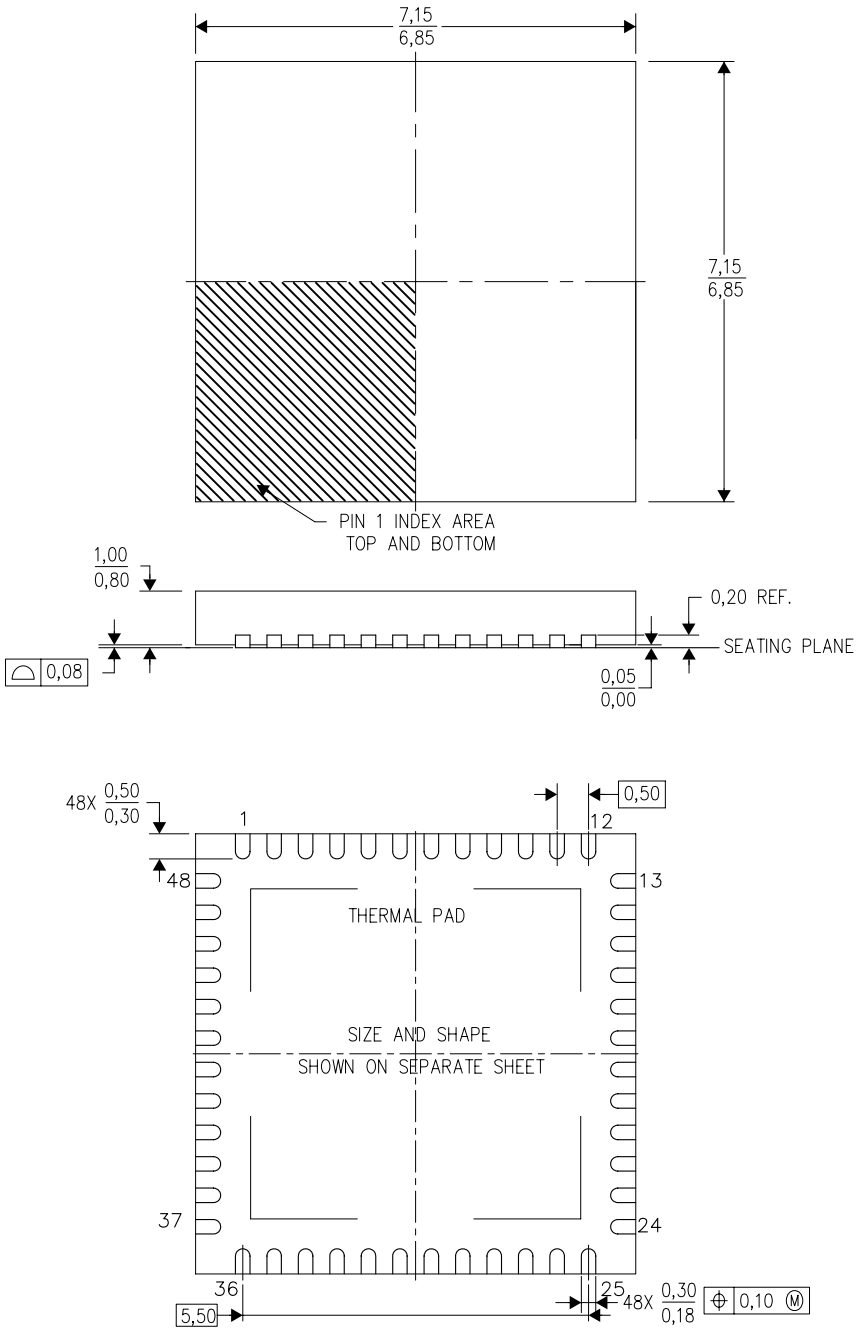
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65163RGZR	VQFN	RGZ	48	2500	367.0	367.0	38.0

RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

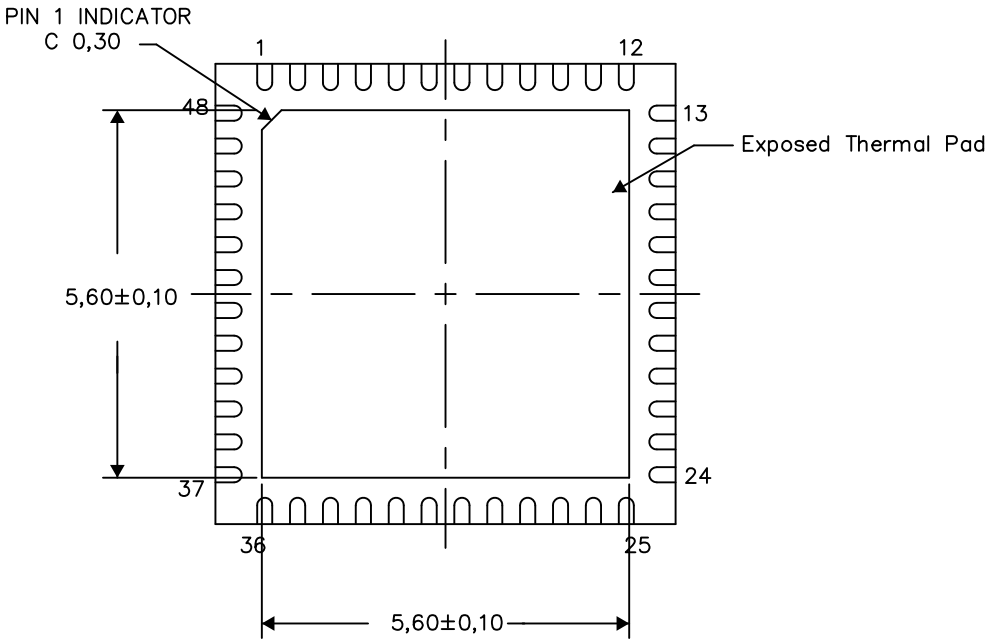
RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



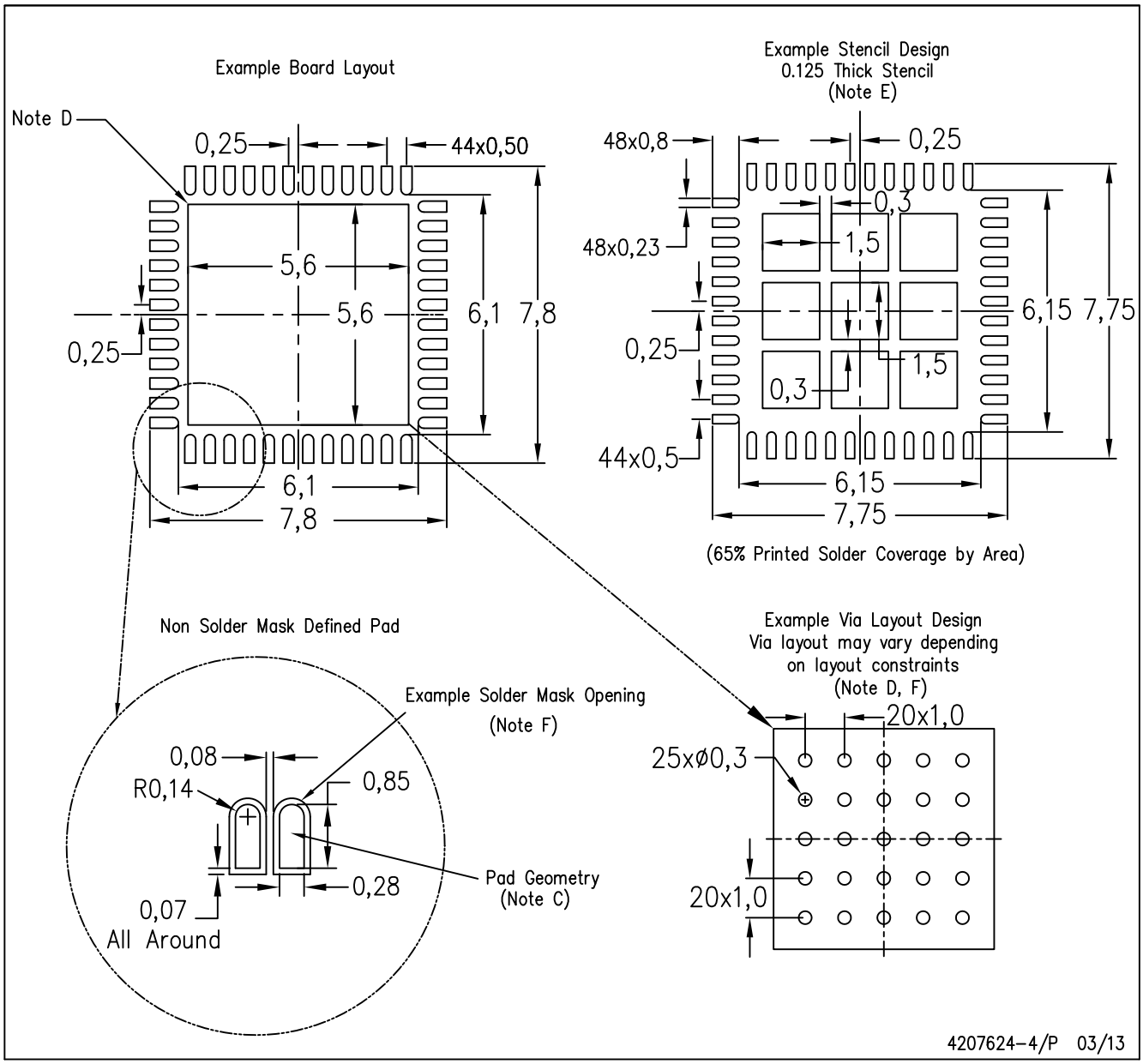
Bottom View

Exposed Thermal Pad Dimensions

4206354–5/T 03/13

NOTE: All linear dimensions are in millimeters

RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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