# ULTRA SMALL, LOW-INPUT VOLTAGE, LOW $r_{ON}$ LOAD SWITCH

**Check for Samples: TPS22907**

## FEATURES

- Low Input Voltage: 1.1 V to 3.6 V
- Ultra-Low ON-State Resistance
  - $r_{ON}$ = 44 mΩ at $V_{IN}$ = 3.6 V
  - $r_{ON}$ = 50 mΩ at $V_{IN}$ = 2.5 V
  - $r_{ON}$ = 58 mΩ at $V_{IN}$ = 1.8 V
  - $r_{ON}$ = 83 mΩ at $V_{IN}$ = 1.2 V
- 1-A Maximum Continuous Switch Current
- Quiescent Current < 1 µA
- Shutdown Current < 1 µA
- Low Control Input Thresholds Enable Use of Low-Voltage Logic
- Controlled Slew Rate to Avoid Inrush Currents
- ESD Performance Tested Per JESD 22
  - 3000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)
- Ultra Small Four-Terminal Wafer Chip Scale Package (WCSP)
  - 0.9 mm × 0.9 mm, 0.5-mm Pitch, 0.5-mm Height

## APPLICATIONS

- Battery Powered Equipment
- Portable Industrial Equipment
- Portable Medical Equipment
- Portable Media Players
- Point Of Sales Terminal
- GPS Devices
- Digital Cameras
- Portable Instrumentation
- Smartphones

YZT PACKAGE

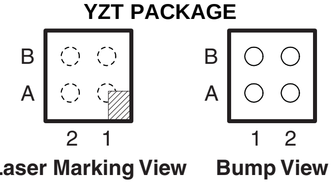



**Table 1. TERMINAL ASSIGNMENTS**

| | | |
|---|---|---|
| **B** | ON | GND |
| **A** | $V_{IN}$ | $V_{OUT}$ |
| | **2** | **1** |

## DESCRIPTION

The TPS22907 is an ultra small, low $R_{ON}$ load switch with controlled turn on. The device contains a P-channel MOSFET that operates over an input voltage range of 1.1 V to 3.6 V. The switch is controlled by an on/off input (ON), which is capable of interfacing directly with low-voltage control signals.

The TPS22907 is available in a space-saving 4-terminal WCSP with 0.5-mm pitch (YZT). The device is characterized for operation over the free-air temperature range of –40°C to 85°C.

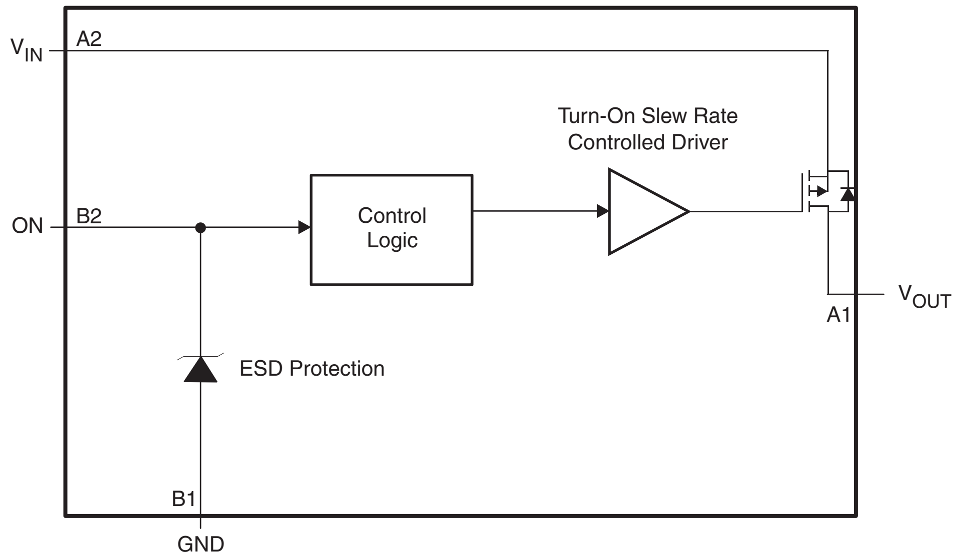
| DEVICE | $r_{ON}$ (TYP at 1.8 V) | SLEW RATE (TYP at 1.8 V) | MAXIMUM OUTPUT CURRENT | ENABLE |
|---|---|---|---|---|
| TPS22907 | 58 mΩ | 36 µs | 1000 mA | Active high |

**ORDERING INFORMATION**

| $T_A$ | PACKAGE(1) (2) | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| –40°C to 85°C | WCSP – YZT (0.5-mm pitch) | Tape and reel | TPS22907YZTR | _ _ _ 5K_(3) |

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(3) The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the wafer fab/assembly site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

## FUNCTIONAL BLOCK DIAGRAM




## FUNCTION TABLE

| ON (Control Input) | $V_{IN}$ to $V_{OUT}$ |
|---|---|
| L | OFF |
| H | ON |

## TERMINAL FUNCTIONS

| TERMINAL | | DESCRIPTION |
|---|---|---|
| BALL NO. | NAME | |
| A1 | $V_{OUT}$ | Switch output |
| A2 | $V_{IN}$ | Switch input. Bypass this input with a ceramic capacitor to ground. |
| B1 | GND | Ground |
| B2 | ON | Switch control input. Active high, do not leave floating |

## ABSOLUTE MAXIMUM RATINGS[1]

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IN}$ | Input voltage range | | –0.3 | 4 | V |
| $V_{OUT}$ | Output voltage range | | | $V_{IN}$ + 0.3 | V |
| $V_{ON}$ | Input voltage range | | –0.3 | 4 | V |
| $I_{MAX}$ | Maximum continuous switch current, $T_A$ = -40°C to 85°C | | | 1 | A |
| $I_{PLS}$ | Maximum pulsed current (100-µs pulse, 2% duty cycle), $T_A$ = -40°C to 85°C | | | 2.7 | A |
| $T_A$ | Operating free-air temperature range | | –40 | 85 | °C |
| $T_{stg}$ | Storage temperature range | | –65 | 150 | °C |
| ESD | Electrostatic discharge protection | Human-Body Model (HBM) | | 3000 | V |
| | | Charged-Device Model (CDM) | | 1000 | |

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## DISSIPATION RATINGS

| BOARD | PACKAGE | $R_{\theta JC}$ | $R_{\theta JA}$ | DERATING FACTOR ABOVE $T_A$ = 25°C | $T_A$ < 25°C | $T_A$ = 70°C | $T_A$ = 85°C |
|---|---|---|---|---|---|---|---|
| High-K[1] | YZT | 28.6°C/W | 116.32°C/W | -8.5969 mW/°C | 859.69 mW | 472.83 mW | 343.87 mW |

(1) The JEDEC high-K (2s2p) board used to derive this data was a 3- × 3-inch, multilayer board with 1-ounce internal power and ground planes and 2-ounce copper traces on top and bottom of the board.

## RECOMMENDED OPERATING CONDITIONS

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{IN}$ | Input voltage range | 1.1 | 3.6 | V |
| $V_{OUT}$ | Output voltage range | | $V_{IN}$ | V |
| $V_{IH}$ | High-level input voltage, ON | 0.85 | 3.6 | V |
| $V_{IL}$ | Low-level input voltage, ON | | 0.4 | V |
| $C_{IN}$ | Input capacitor | 1[1] | | µF |

(1) See Application Information.

## ELECTRICAL CHARACTERISTICS

$V_{IN}$ = 1.1 V to 3.6 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $T_A$ (1) | MIN | TYP (2) | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{IN}$ | Quiescent current | $I_{OUT}$ = 0, $V_{IN}$ = $V_{ON}$ | | | 0.07 | 1 | µA |
| $I_{IN(OFF)}$ | Off supply current | $V_{ON}$ = GND, OUT = Open | | | 0.05 | 1 | µA |
| $I_{IN(LEAKAGE)}$ | Leakage current | $V_{ON}$ = GND, $V_{OUT}$ = 0 | | | 0.05 | 1 | µA |
| $r_{ON}$ | ON-state resistance | $V_{IN}$ = 3.6 V, $I_{OUT}$ = -200 mA | 25°C | | 44 | 60 | mΩ |
| | | | Full range | | | 67 | |
| | | $V_{IN}$ = 2.5 V, $I_{OUT}$ = -200 mA | 25°C | | 50 | 63 | |
| | | | Full range | | | 70 | |
| | | $V_{IN}$ = 1.8 V, $I_{OUT}$ = -200 mA | 25°C | | 58 | 72 | |
| | | | Full range | | | 80 | |
| | | $V_{IN}$ = 1.2 V, $I_{OUT}$ = -200 mA | 25°C | | 83 | 106 | |
| | | | Full range | | | 117 | |
| | | $V_{IN}$ = 1.1 V, $I_{OUT}$ = -200 mA | 25°C | | 97 | 125 | |
| | | | Full range | | | 140 | |
| $I_{ON}$ | ON input leakage current | $V_{ON}$ = 1.1 V to 3.6 V or GND | Full range | | 0.005 | 1 | µA |

(1) Full range $T_A$ = –40°C to 85°C
(2) Typical values are at the specified $V_{IN}$ and $T_A$ = 25°C.

## SWITCHING CHARACTERISTICS

$V_{IN}$ = 3.6 V, $T_A$ = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{ON}$ | Turn-ON time | $R_L$ = 500 Ω | $C_L$ = 0.1 µF | | 28 | | µs |
| $t_{OFF}$ | Turn-OFF time | $R_L$ = 500 Ω | $C_L$ = 0.1 µF | | 40 | | µs |
| $t_r$ | $V_{OUT}$ rise time | $R_L$ = 500 Ω | $C_L$ = 0.1 µF | | 25 | | µs |
| $t_f$ | $V_{OUT}$ fall time | $R_L$ = 500 Ω | $C_L$ = 0.1 µF | | 116 | | µs |

## SWITCHING CHARACTERISTICS

$V_{IN}$ = 1.8 V, $T_A$ = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{ON}$ | Turn-ON time | $R_L$ = 500 Ω | $C_L$ = 0.1 µF | | 48 | | µs |
| $t_{OFF}$ | Turn-OFF time | $R_L$ = 500 Ω | $C_L$ = 0.1 µF | | 40 | | µs |
| $t_r$ | $V_{OUT}$ rise time | $R_L$ = 500 Ω | $C_L$ = 0.1 µF | | 36 | | µs |
| $t_f$ | $V_{OUT}$ fall time | $R_L$ = 500 Ω | $C_L$ = 0.1 µF | | 113 | | µs |

## SWITCHING CHARACTERISTICS

$V_{IN}$ = 1.1 V, $T_A$ = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{ON}$ | Turn-ON time | $R_L$ = 500 Ω | $C_L$ = 0.1 µF | | 81 | | µs |
| $t_{OFF}$ | Turn-OFF time | $R_L$ = 500 Ω | $C_L$ = 0.1 µF | | 42 | | µs |
| $t_r$ | $V_{OUT}$ rise time | $R_L$ = 500 Ω | $C_L$ = 0.1 µF | | 57 | | µs |
| $t_f$ | $V_{OUT}$ fall time | $R_L$ = 500 Ω | $C_L$ = 0.1 µF | | 113 | | µs |

## TYPICAL CHARACTERISTICS

**ON-STATE RESISTANCE vs INPUT VOLTAGE**

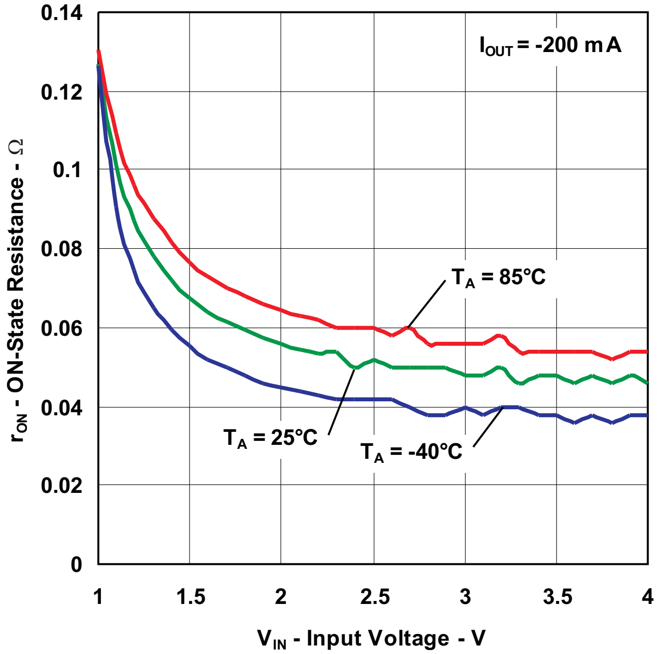



Figure 1.

**ON-STATE RESISTANCE vs TEMPERATURE**

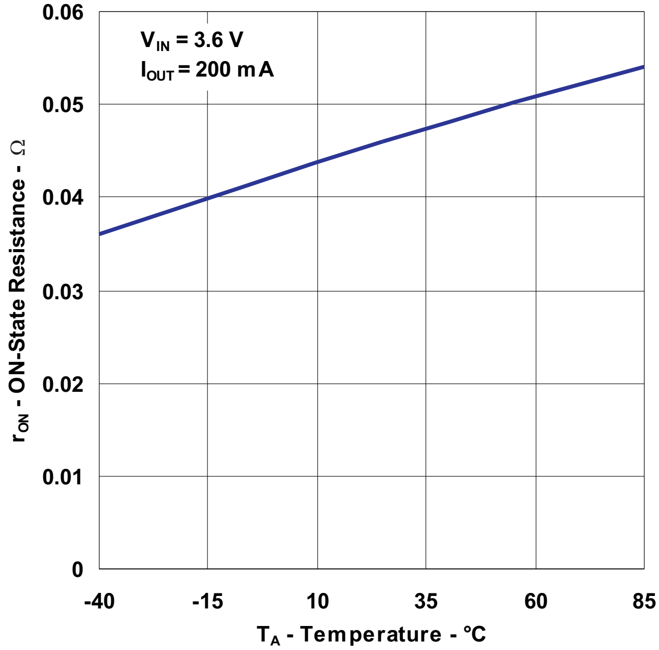



Figure 2.

**QUIESCENT CURRENT vs INPUT VOLTAGE**

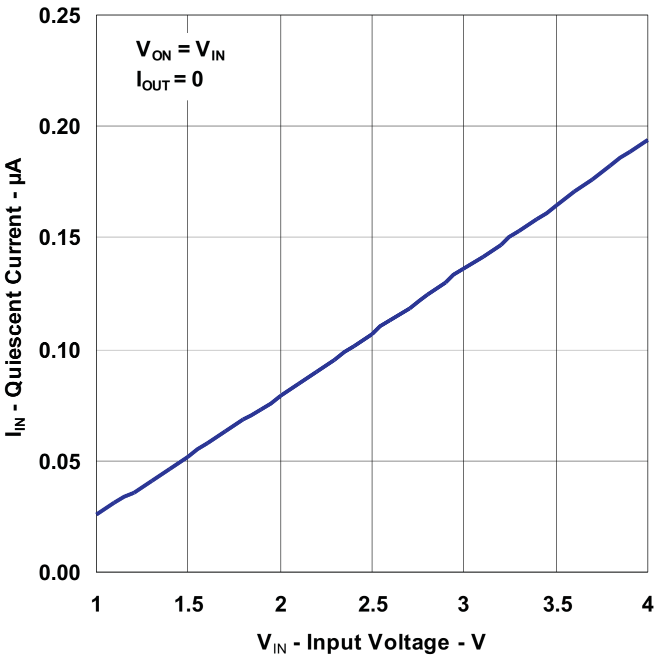



Figure 3.

**QUIESCENT CURRENT vs TEMPERATURE**

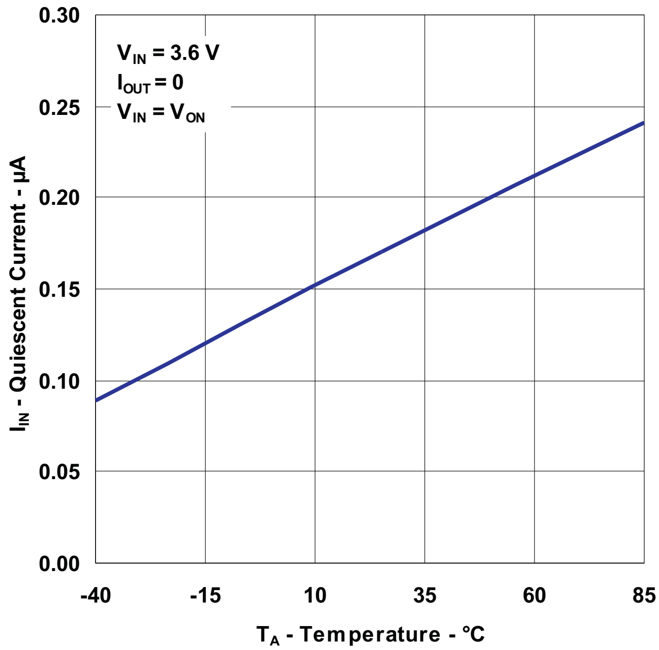



Figure 4.

## TYPICAL CHARACTERISTICS (continued)

OFF SUPPLY CURRENT
vs
INPUT VOLTAGE

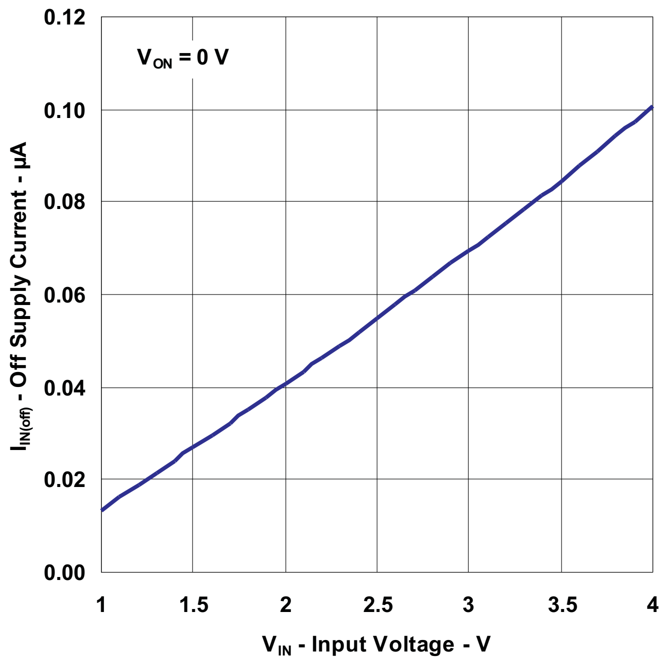



Figure 5.

OFF SUPPLY CURRENT
vs
TEMPERATURE

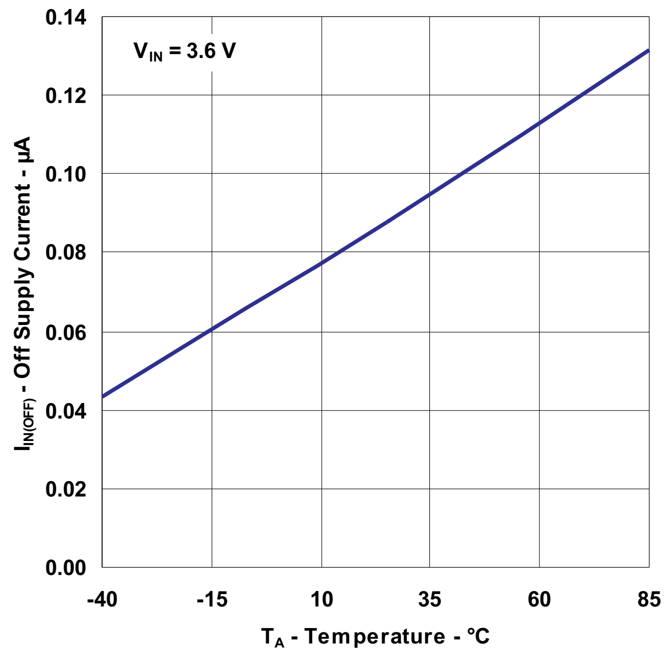



Figure 6.

LEAKAGE CURRENT
vs
INPUT VOLTAGE

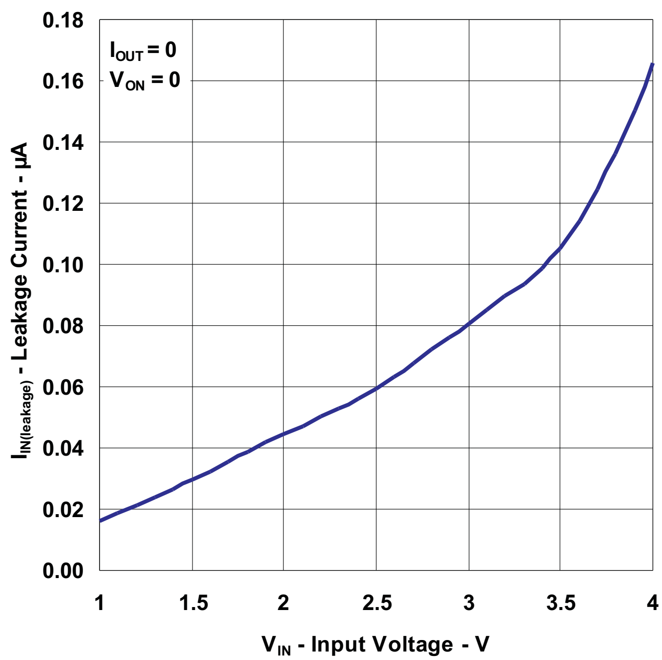



Figure 7.

LEAKAGE CURRENT
vs
TEMPERATURE

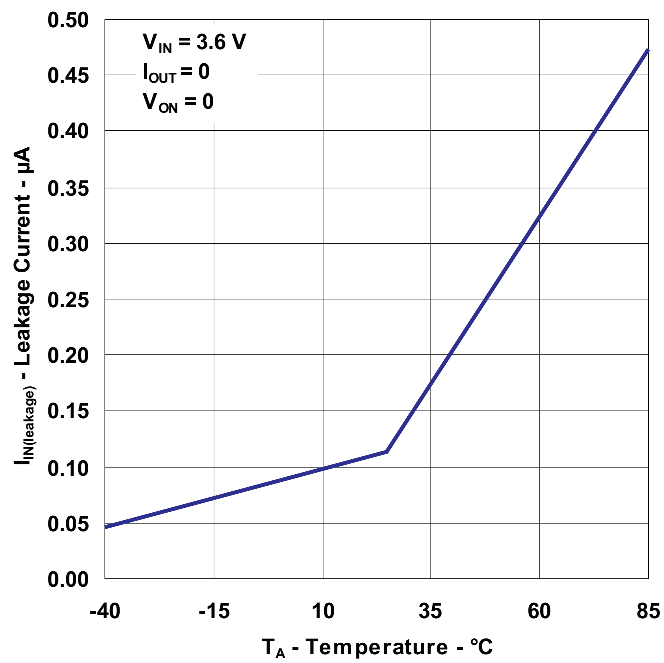



Figure 8.

## TYPICAL CHARACTERISTICS (continued)

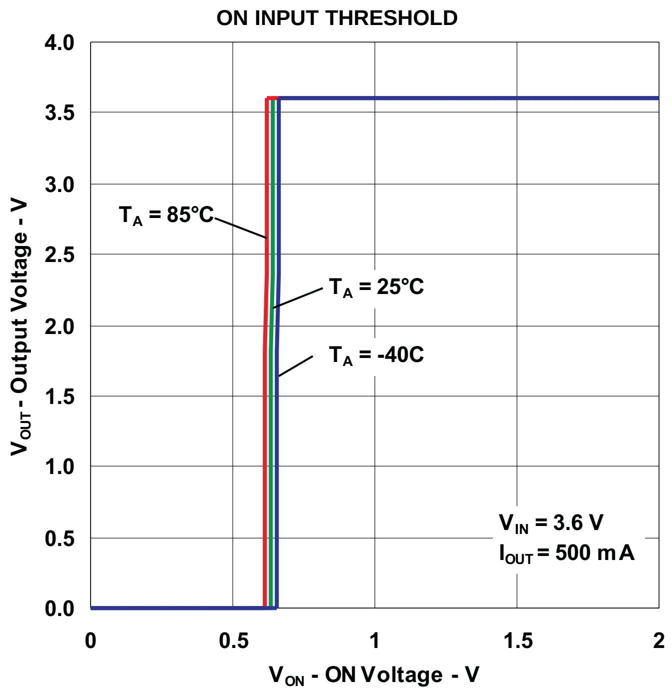



Figure 9.

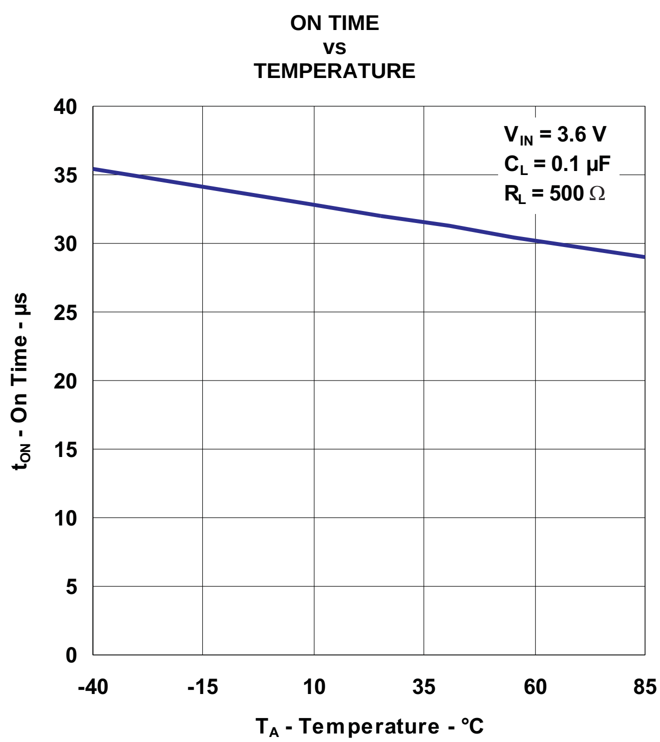



Figure 10.

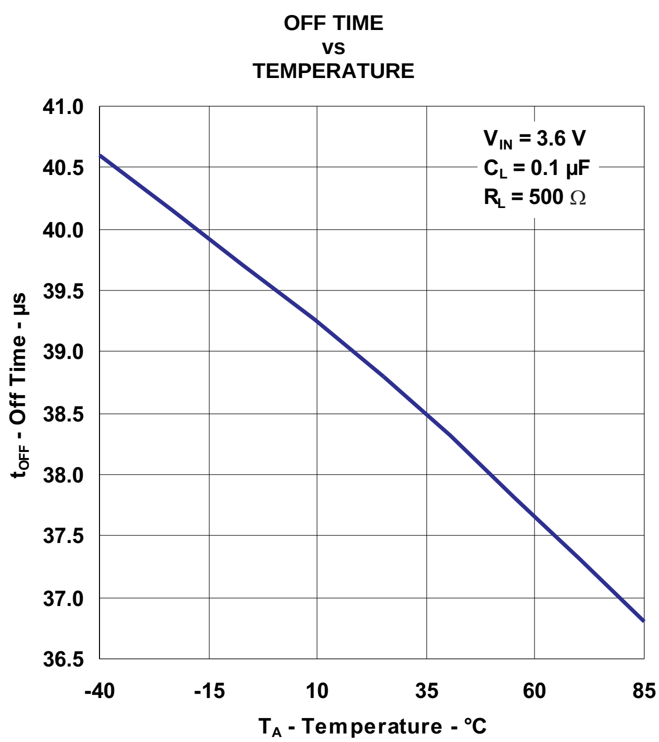



Figure 11.

## TYPICAL CHARACTERISTICS (continued)

RISE TIME
vs
TEMPERATURE

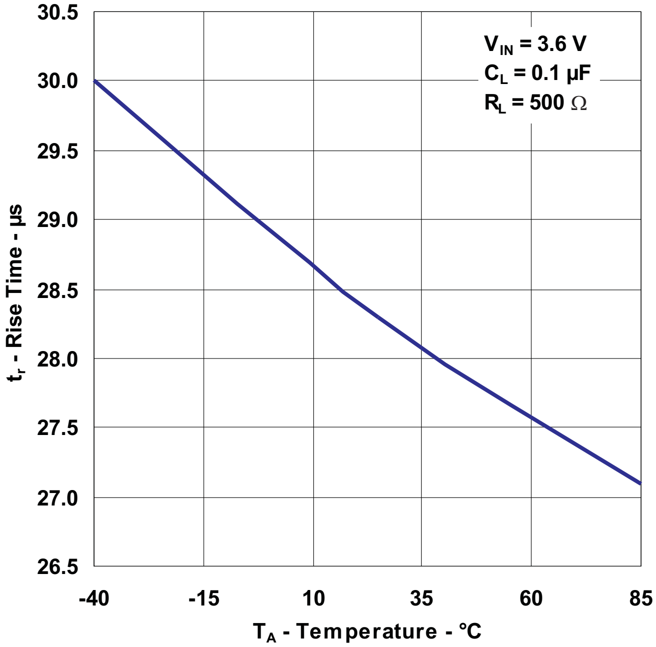



Figure 12.

FALL TIME
vs
TEMPERATURE

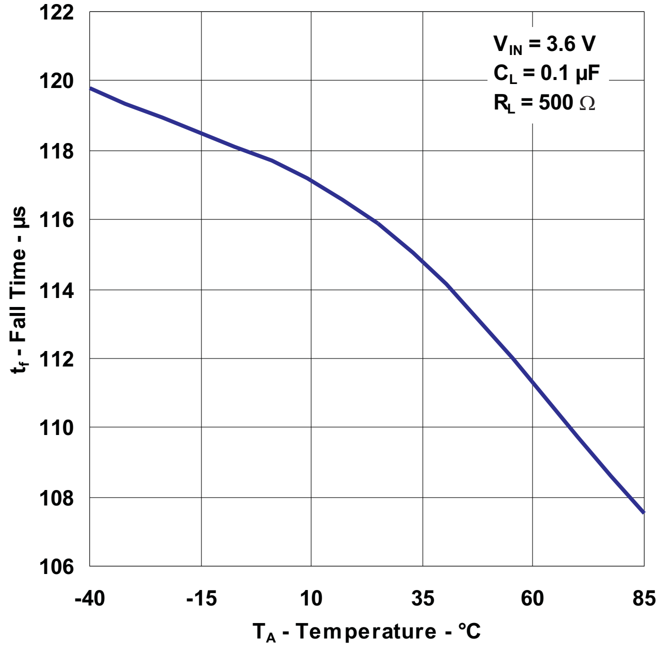



Figure 13.

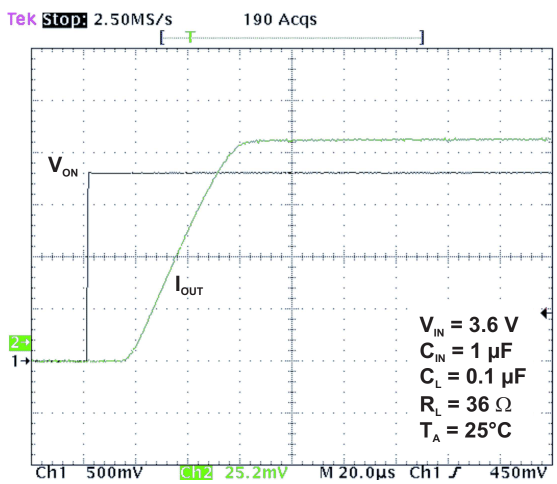



Figure 14. $t_{ON}$ RESPONSE

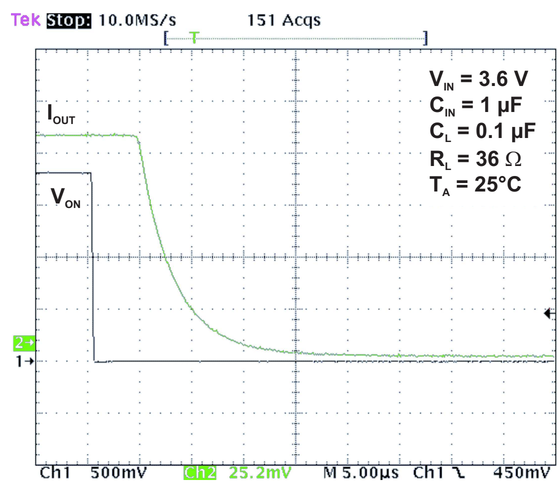



Figure 15. $t_{OFF}$ RESPONSE

## TYPICAL CHARACTERISTICS (continued)

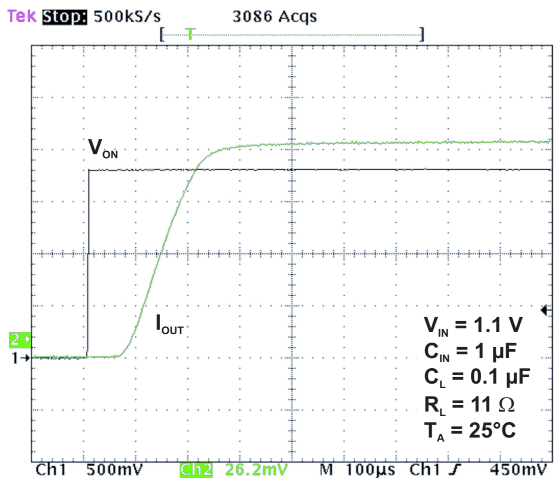



Figure 16. $t_{ON}$ RESPONSE

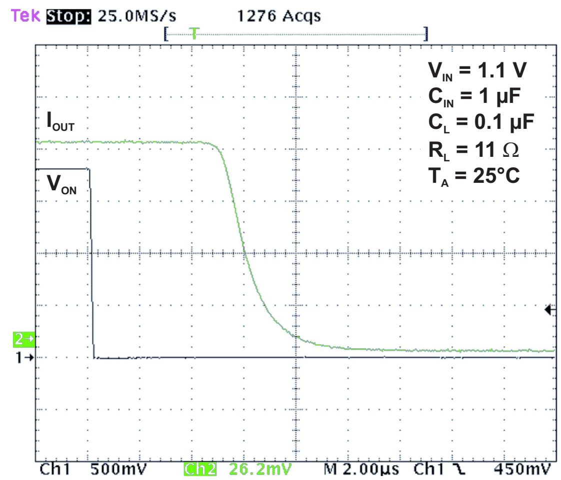



Figure 17. $t_{OFF}$ RESPONSE

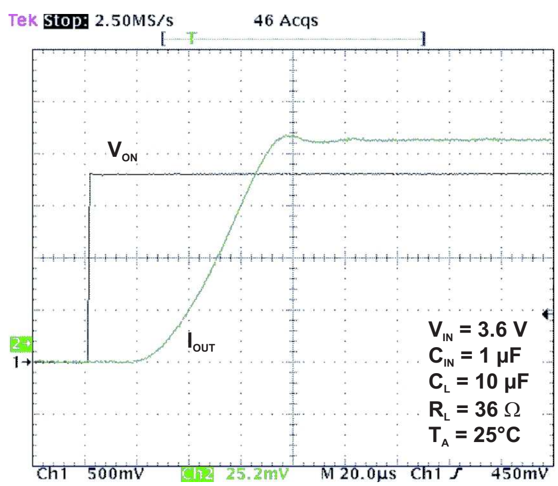



Figure 18. $t_{ON}$ RESPONSE

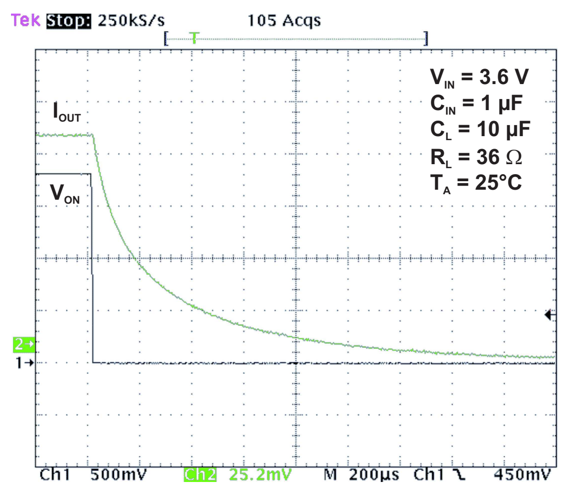



Figure 19. $t_{OFF}$ RESPONSE

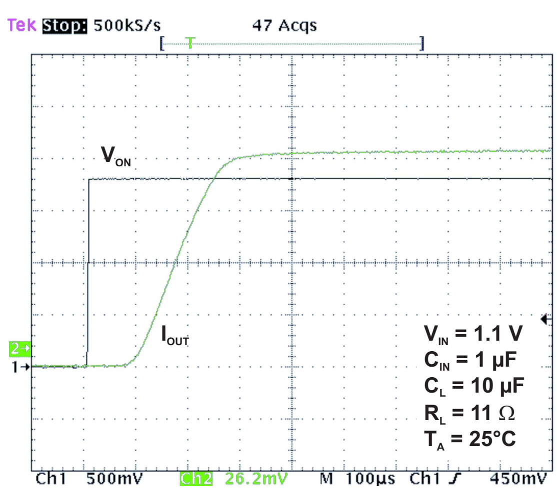



Figure 20. $t_{ON}$ RESPONSE

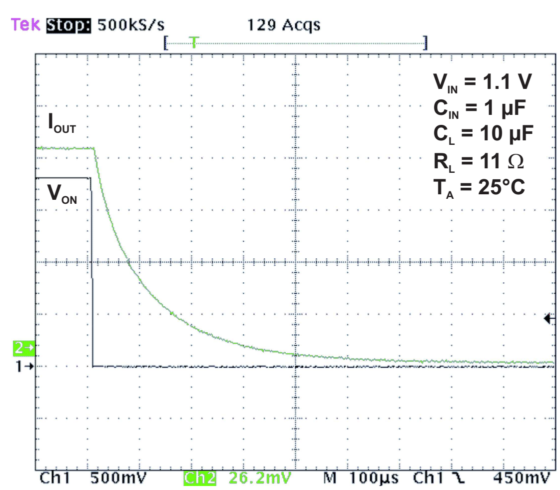
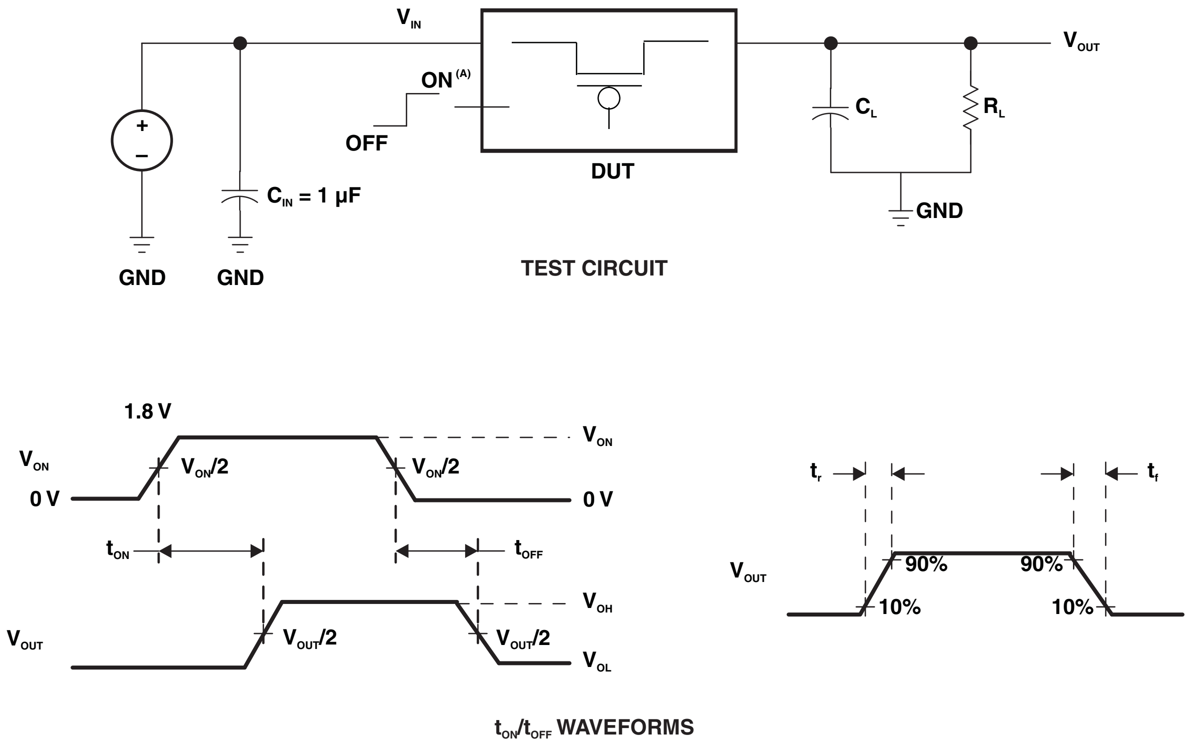



Figure 21. $t_{OFF}$ RESPONSE

## PARAMETER MEASUREMENT INFORMATION




A. $t_{rise}$ and $t_{fall}$ of the control signal is 100 ns.

**Figure 22. Test Circuit and $t_{ON}/t_{OFF}$ Waveforms**

## APPLICATION INFORMATION

### On/Off Control

The ON pin controls the state of the switch. Activating ON continuously holds the switch in the on state so long as there is no fault. ON is active high and has a low threshold, making it capable of interfacing with low-voltage signals. The ON pin is compatible with standard GPIO logic threshold. It can be used with any microcontroller with 1.2-V, 1.8-V, 2.5-V, or 3.3-V GPIOs.

### Input Capacitor

To limit the voltage drop on the input supply caused by transient in-rush currents when the switch turns on into a discharged load capacitor or short-circuit, a capacitor needs to be placed between $V_{IN}$ and GND. A 1-μF ceramic capacitor, $C_{IN}$, place close to the pins is usually sufficient. Higher values of $C_{IN}$ can be use to further reduce the voltage drop during high-current application. When switching heavy loads, it is recommended to have an input capacitor approximately ten times higher than the output capacitor to avoid excessive voltage drop.

### Output Capacitor

Due to the integral body diode in the PMOS switch, a $C_{IN}$ greater than $C_L$ is highly recommended. A $C_L$ greater than $C_{IN}$ can cause $V_{OUT}$ to exceed $V_{IN}$ when the system supply is removed. This could result in current flow through the body diode from $V_{OUT}$ to $V_{IN}$.

### Board Layout

For best performance, all traces should be as short as possible. To be most effective, the input and output capacitors should be placed close to the device to minimize the effects that parasitic trace inductances may have on normal and short-circuit operation. Using wide traces for $V_{IN}$, $V_{OUT}$, and GND helps minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS22907YZTR | ACTIVE | DSBGA | YZT | 4 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | 5K (F ~ G) | Samples |
| TPS22907YZTT | ACTIVE | DSBGA | YZT | 4 | 250 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | 5K (F ~ G) | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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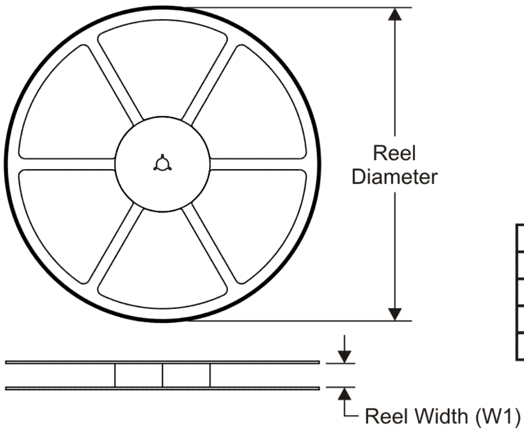
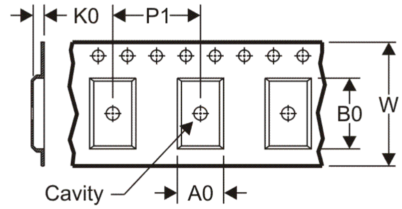
## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

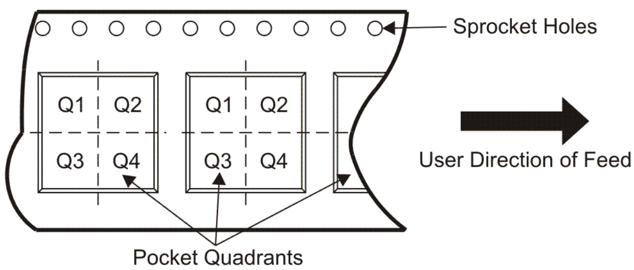



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

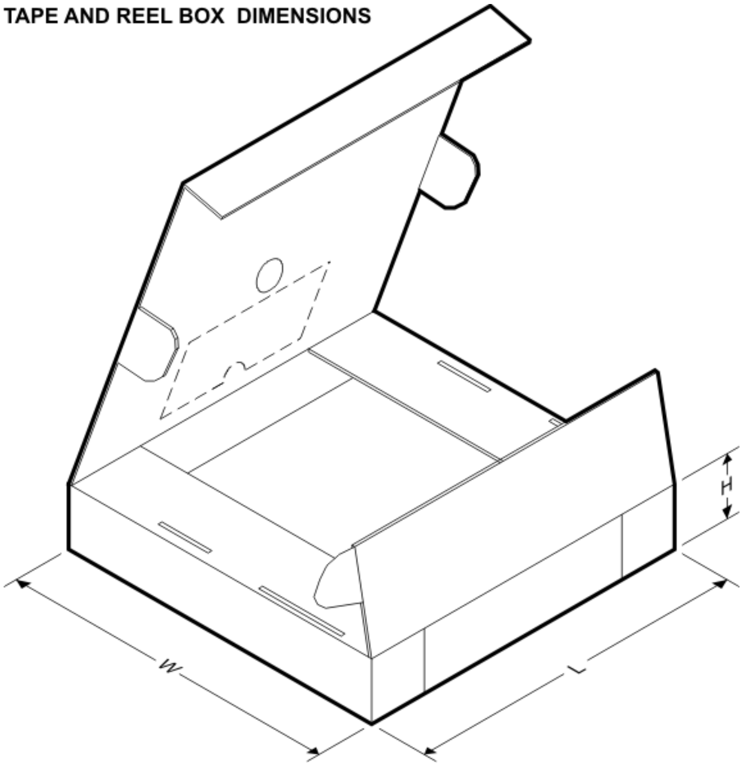
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS22907YZTR | DSBGA | YZT | 4 | 3000 | 178.0 | 9.2 | 1.0 | 1.0 | 0.73 | 4.0 | 8.0 | Q1 |
| TPS22907YZTT | DSBGA | YZT | 4 | 250 | 178.0 | 9.2 | 1.0 | 1.0 | 0.73 | 4.0 | 8.0 | Q1 |

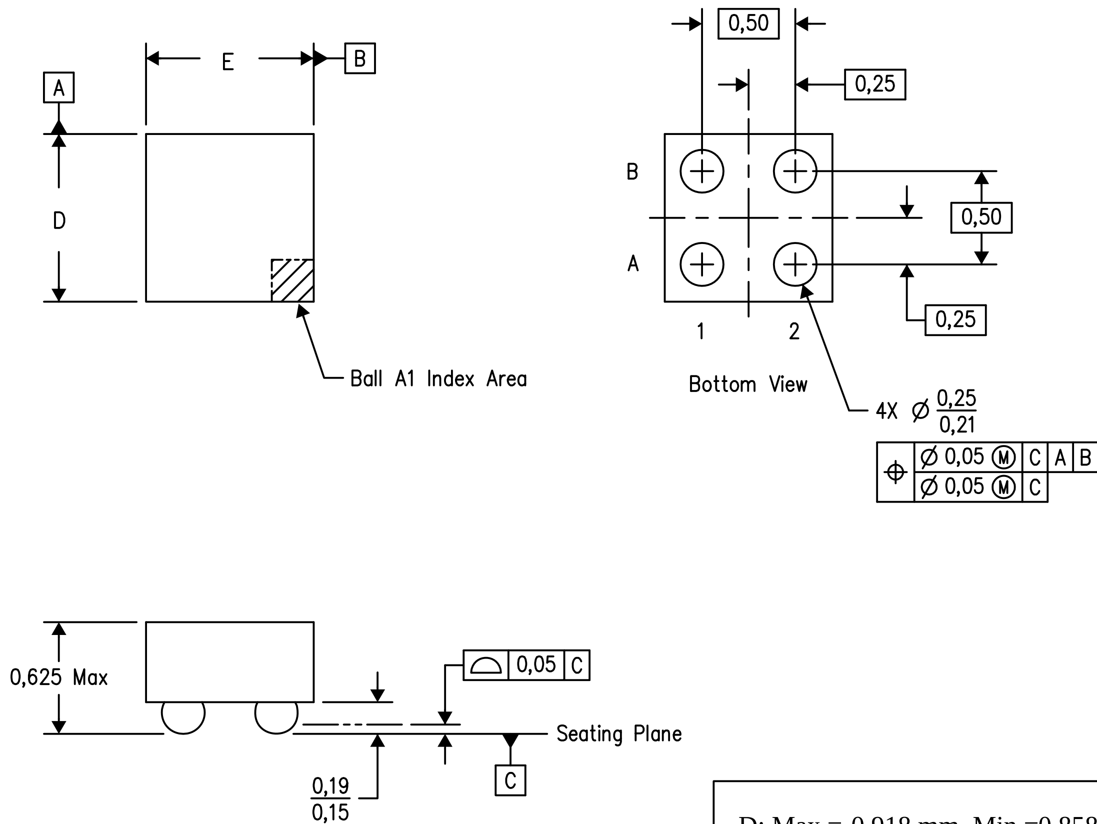
**TAPE AND REEL BOX DIMENSIONS**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS22907YZTR | DSBGA | YZT | 4 | 3000 | 220.0 | 220.0 | 35.0 |
| TPS22907YZTT | DSBGA | YZT | 4 | 250 | 220.0 | 220.0 | 35.0 |

YZT (S-XBGA-N4) DIE-SIZE BALL GRID ARRAY




D: Max = 0.918 mm, Min =0.858 mm

E: Max = 0.918 mm, Min =0.858 mm

4205418-2/H 05/13

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

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