

FIREWIRE ESD CLAMP WITH LIVE-INSERTION DETECTION CIRCUIT

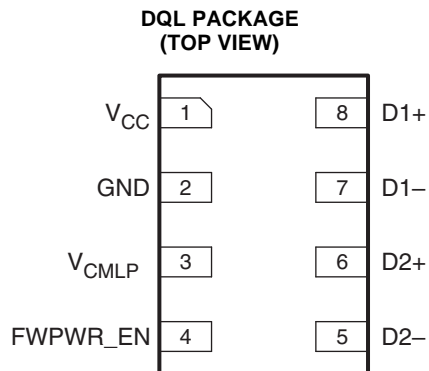
Check for Samples: [TPD4S1394](#)

FEATURES

- IEEE1394 Live Insertion Protection
- Exceeds ESD protection to IEC61000-4- 2 (Level 4)
 - ±15-kV Human-Body Model (HBM)
 - ±6-kV IEC 61000-4-2 Contact Discharge
- 4-Channel Matching ESD Clamps for High-Speed Differential Lines
- Flow-Through, Single-in-Line Pin Mapping Simplifies Board Layout
- Available in an 8-Pin X2SON (DQL) package

APPLICATIONS

- IEEE 1394 Live Insertion Protection



DESCRIPTION

The TPD4S1394 provides robust system level ESD solution for the IEEE.1394 port along with a live insertion detection mechanism for high-speed lines interfacing a low-voltage, ESD sensitive core chipset. This device protects and monitors up to two differential input pairs. The optimized line capacitance allows to protect the data lines with data rate in excess of 1.6 GHz without degrading signal integrity.

The TPD4S1394 incorporates a live insertion circuit whose output state changes when improper voltage levels are present on the input data lines. The FWPWR_EN signal controls an external FireWire port power switch. During the live insertion event if there is a floating GND or a high level signal at the D+, D– pins, the internal comparator will detect the changes and pull the FWPWR_EN signal to low state. When FWPWR_EN is driven low, there is an internal delay mechanism preventing it from being driven to the high state regardless of the inputs to the comparator.

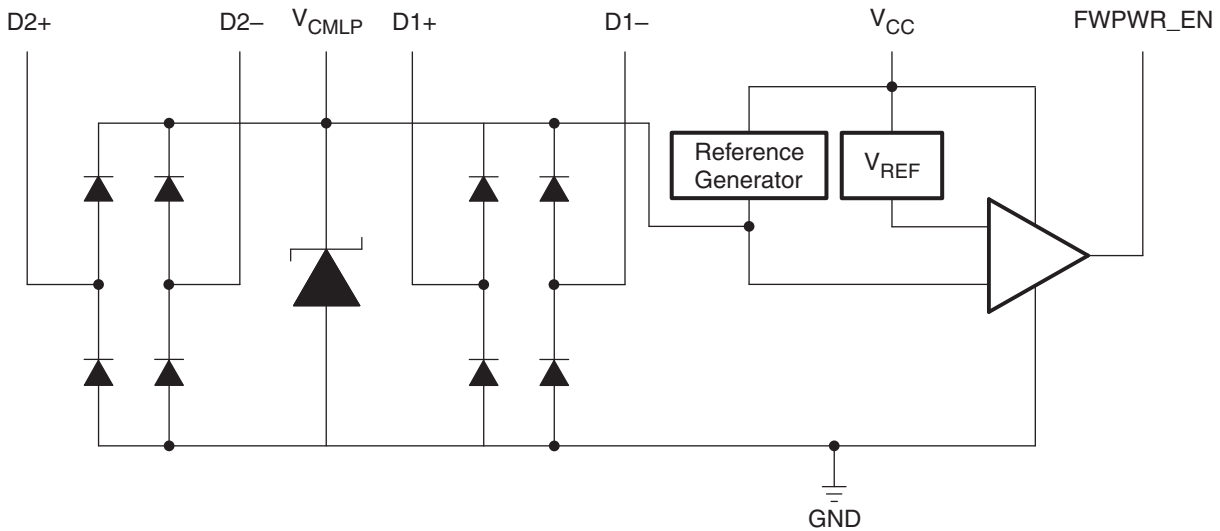
Additionally, the TPD4S1394 performs ESD protection on the four inputs pins: D1+, D1–, D2+, and D2–. The TPD4S1394 conforms to the IEC61000-4-2 (Level 4) ESD protection and ±15 kV HBM ESD protection. The TPD4S1394 is characterized for operation over ambient air temperature of –40°C to 85°C.

A 0.1uF decoupling capacitor is required at VCC (pin1)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

FUNCTIONAL BLOCK DIAGRAM



TERMINAL FUNCTIONS

TERMINAL		TYPE	DESCRIPTION
PIN NO.	NAME		
1	V _{CC}	Power	Power supply
2	GND	GND	Ground
3	V _{CLMP}	O	Comparator trip reference
4	FWPWR_EN	O	Control output
5, 6, 7, 8	D2+, D2-, D1+, D1-	I	High-speed ESD clamp inputs

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	-0.5	4.6	V
V _{IO}	IO voltage range at D+, D-, V _{CLMP}	0	4	V
FWPWR_EN	Switch output	-0.5	4.6	V
T _{stg}	Storage temperature range	-65	150	°C
T _A	Operating free-air temperature range	-40	85	°C
IEC 61000-4-2 Contact Discharge		D+, D- pins		±6 kV
HBM ESD		D+, D- pins		±15 kV

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	3.0		3.6	V

ELECTRICAL CHARACTERISTICS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{dx}	Voltage at D1+, D1-, D2+, and D2- to trip the FWPWR_EN from high to low		2.9	3.4	4.0	V
	Voltage to trip the FWPWR_EN from low to high		2.7	3.2	3.8	
V _{CLMP}	Value on pin	No connect		2.45		V
t _{trip}	Time for FWPWR_EN to go low	Loading on FWPWR_EN = 50 pF	0.5	2	5	μs
t _{reset}	Time delay for the FWPWR_EN to go high after trip condition is met	FWPWR_EN = V _{CC}	300	450	600	ms
V _{BR}	Breakdown voltage at V _{CLAMP}	I _I = 1 mA		4.2		V
V _D	Diode forward voltage for lower clamp	I _D = 8 mA lower clamp diode	-0.6	-0.8	-0.95	V
FWPWR_EN	Switch output			V _{CC}		V
R _{DYN}	Dynamic resistance (for in and out clamp) of the D+, D-	I = 1 A		1		Ω
C _{IO}	IO Capacitance of D+, D-	V _{IO} = 2.5 V		1.5	2	pF
I _{CC}	Current Consumption	V _{CC} = 3.3 V, FWPWR_EN = high		130	200	μA

(1) A 0.1-μF decoupling capacitor is required at V_{CC} (pin 1).

TYPICAL CHARACTERISTICS

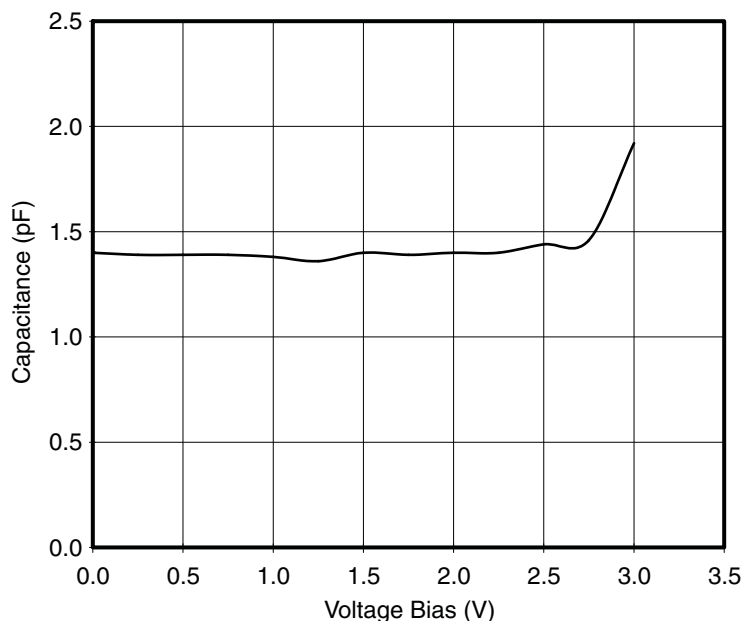


Figure 1. IO Capacitance vs IO Voltage (D+, D- Pins)

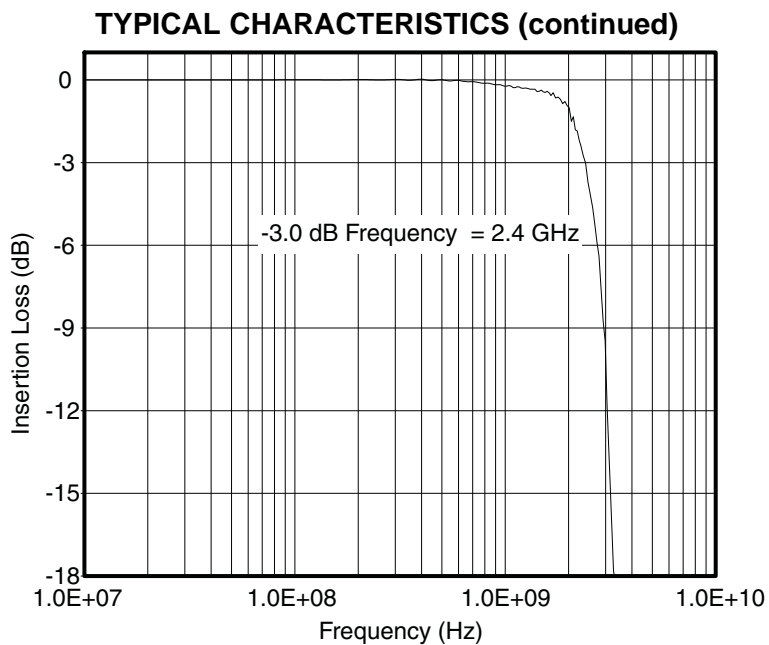


Figure 2. Insertion Loss (S21) for D+, D- Pins

REVISION HISTORY

Changes from Original (November 2009) to Revision A	Page
<ul style="list-style-type: none">Removed hard coded ordering information table. Information contained in Package Orderable Addendum.	2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPD4S1394DQLR	ACTIVE	X2SON	DQL	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(5J7 ~ 5JR)	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD4S1394DQLR	X2SON	DQL	8	3000	180.0	9.5	1.6	2.3	0.5	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS

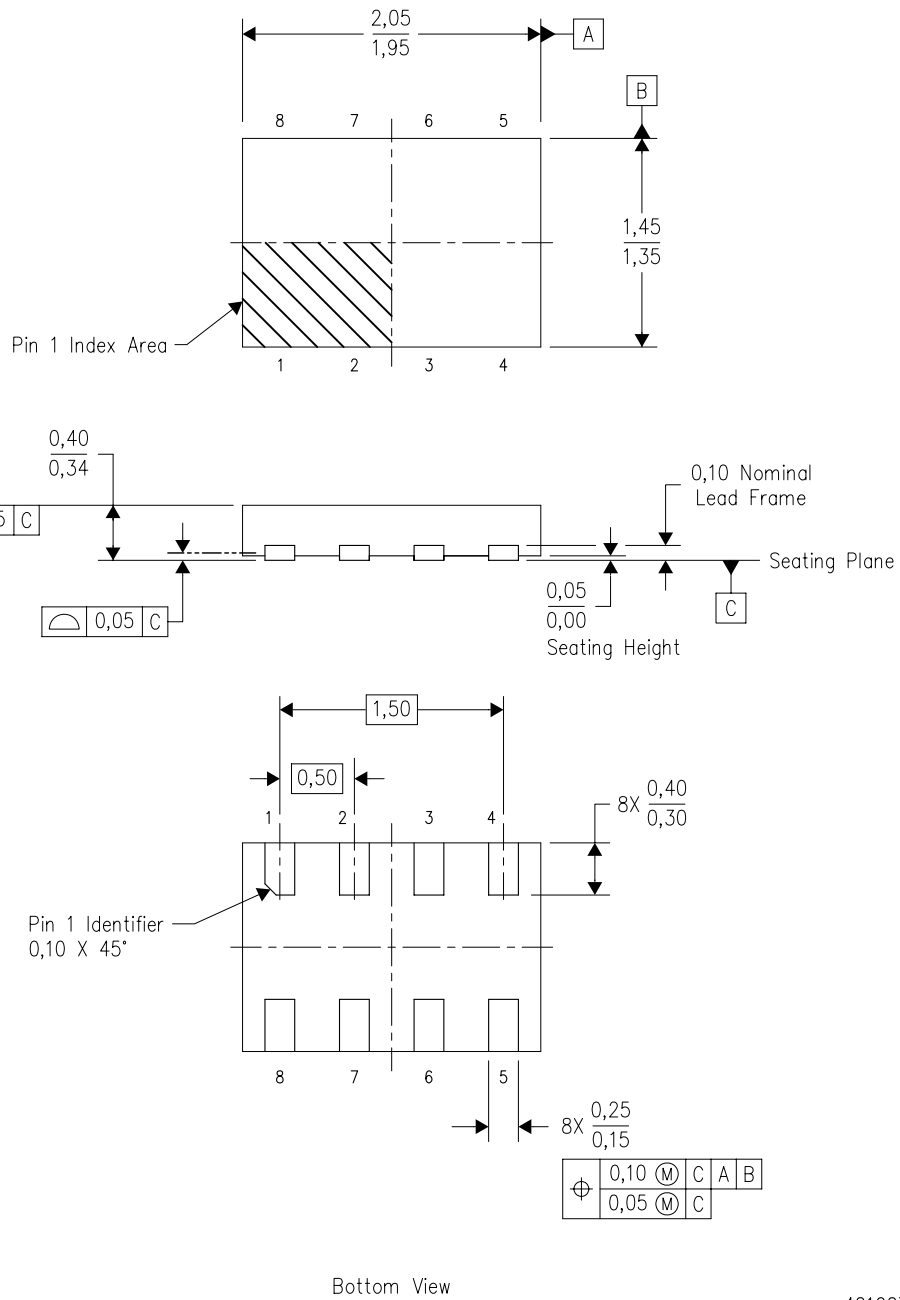


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD4S1394DQLR	X2SON	DQL	8	3000	180.0	180.0	30.0

DQL (R-PX2SON-N8)

PLASTIC SMALL OUTLINE NO-LEAD



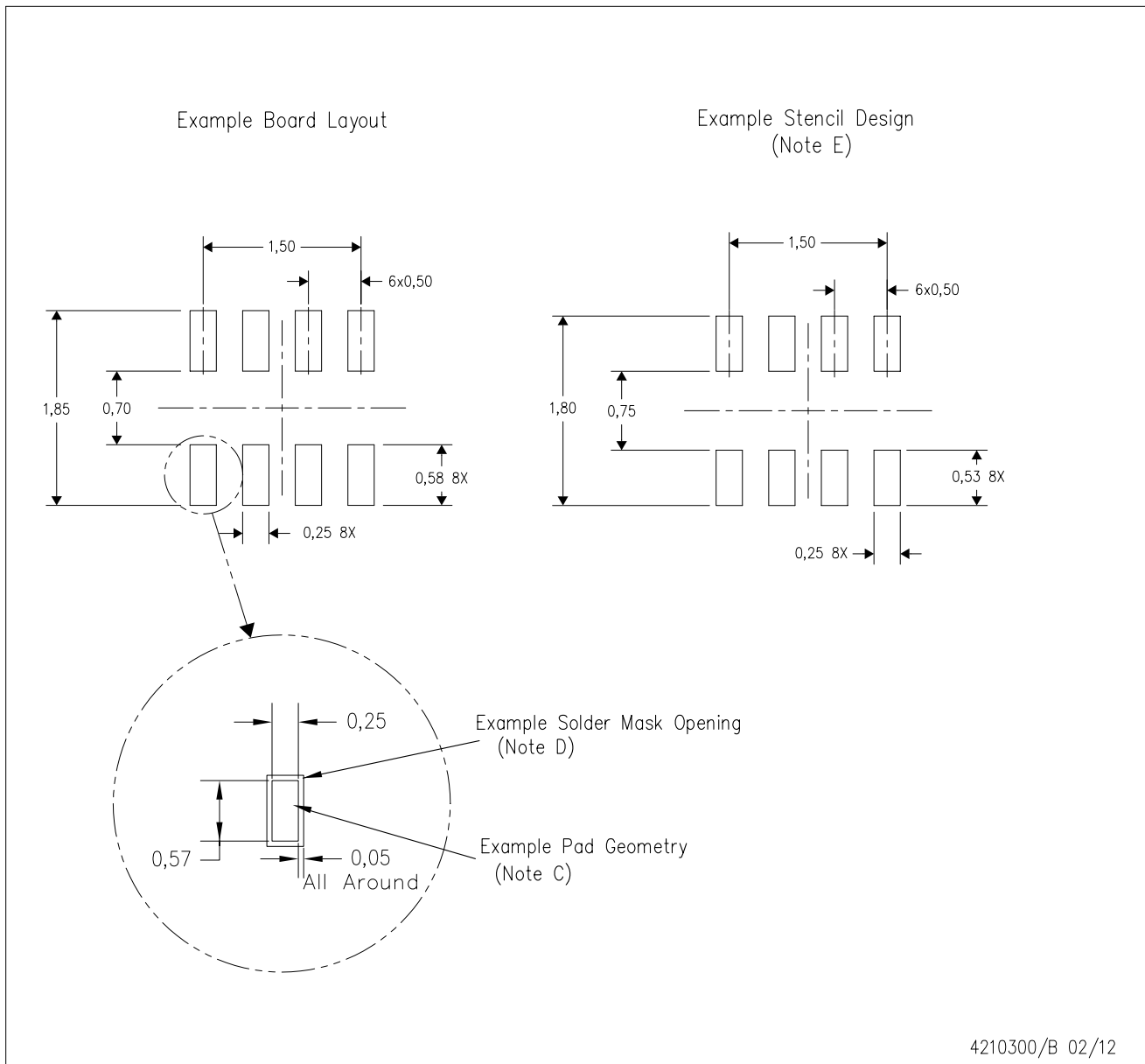
Bottom View

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- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. SON (Small Outline No-Lead) package configuration.

DQL (R-PX2SON-N8)

PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
 - E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
 - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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