1.6-V TO 6.3-V INPUT, 3-A/6-A SYNCHRONOUS STEP DOWN SWIFT™ CONVERTER

Check for Samples: TPS50301-HT, TPS50601-SP

FEATURES

- **Peak Efficiency: 95% (V_O = 3.3 V)**
- **Integrated 55-mΩ/50-mΩ MOSFETs**
- **Split Power Rail: 1.6 V to 6.3 V on PVIN**
- **Power Rail: 3 V to 6.3 V on VIN**
- **TPS50301-HT: 3 A**
- **TPS50601-SP: 6 A**
- **TPS50601-SP:**
  SEL Latchup Immune to LET = 85 MeV-cm^2/mg
- **TPS50601-SP:**
  Total Dose (TID) tolerance = 100kRad (Si)
- **Flexible Switching Frequency Options:**
  - **100-kHz to 1-MHz Adjustable Internal Oscillator**
  - **External Sync Capability from 100 kHz to 1 MHz**
  - **Sync Pin Can Be Configured as a 500-kHz Output for Master/Slave Applications**
- **0.795-V ±1.258% Voltage Reference at 25°C**
- **Monotonic Start-Up into Pre-Biased Outputs**
- **Adjustable Slow Start and Power Sequencing**
- **Power Good Output Monitor for Undervoltage and Overvoltage**
- **Adjustable Input Undervoltage Lockout**
- **For SWIFT™ Documentation, Visit http://www.ti.com/swift**

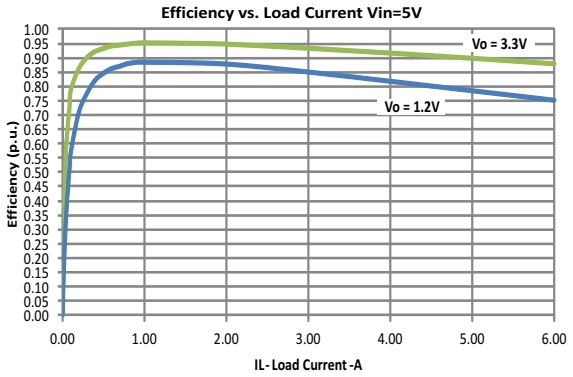
APPLICATIONS

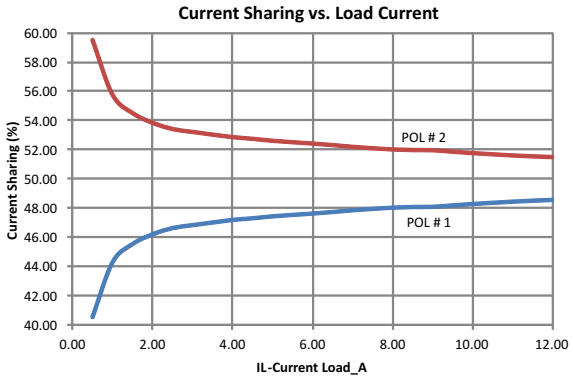
- **Point of Load Regulation**
- **TPS50601-SP: Rad Tolerant Applications**
- **TPS50301-HT: Down-Hole Drilling**
- **Supports Harsh Environment Applications**
- **TPS50301-HT Available in Extreme (–55°C to 210°C) Temperature Range TPS50601-SP Available in Military (–55°C to 125°C) Temperature Range** (1)
- **TPS50301-HT: Texas Instruments' high temperature products utilize highly optimized silicon (die) solutions with design and process enhancements to maximize performance over extended temperatures.**

(1) Custom temperature ranges available

DESCRIPTION

The TPS50301 is a 6.3-V, 3-A and the TPS50601 is a 6.3-V, 6-A synchronous step down converter which is optimized for small designs through high efficiency and integrating the high-side and low-side MOSFETs. Further space savings are achieved through current mode control, which reduces component count, and a high switching frequency, reducing the inductor's footprint. The devices are offered in a thermally enhanced 20-pin ceramic, dual in-line flatpack package.





DESCRIPTION (CONTINUED)

The output voltage startup ramp is controlled by the SS/TR pin which allows operation as either a stand alone power supply or in tracking situations. Power sequencing is also possible by correctly configuring the enable and the open drain power good pins.

Cycle by cycle current limiting on the high-side FET protects the device in overload situations and is enhanced by a low-side sourcing current limit which prevents current runaway. There is also a low-side sinking current limit which turns off the low-side MOSFET to prevent excessive reverse current. Thermal shutdown disables the part when die temperature exceeds thermal shutdown temperature.

SIMPLIFIED SCHEMATIC

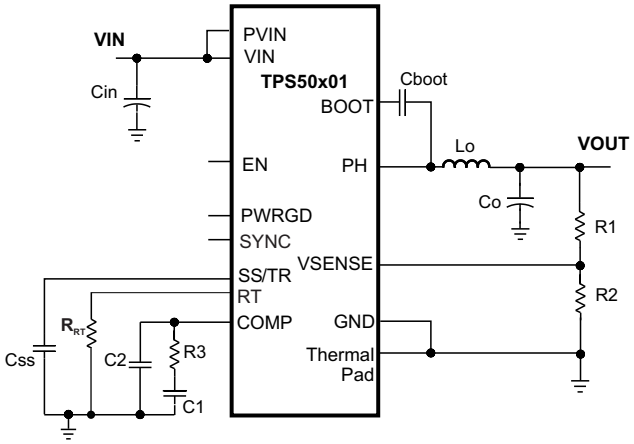


Table 1. ORDERING INFORMATION(1)

T_J	PACKAGE(2)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 210°C	20-pin ceramic flatpack (HKH)	TPS50301SHKH	TPS50301SHKH
–55°C to 125°C		TPS50601MHKHV	5962-1022101VSC TPS50601MHKHV
		5962-1022101VSC	
25°C		TPS50601HKHMPR(3)	TPS50601HKH/EM (EVAL ONLY)

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(3) These units are intended for engineering evaluation only. They are processed to a non-compliant flow (e.g. no burn-in, etc.) and are tested to temperature rating of 25°C only. These units are not suitable for qualification, production, radiation testing or flight use. Parts are not warranted for performance on full MIL specified temperature range of -55°C to 125°C or operating life.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS(1)

over operating temperature range (unless otherwise noted)			
		VALUE	UNIT
Input Voltage	VIN	-0.3 to 7	V
	PVIN	-0.3 to 7	V
	EN	-0.3 to 5.5	V
	BOOT	-0.3 to 14	V
	VSENSE	-0.3 to 3.3	V
	COMP	-0.3 to 3.3	V
	PWRGD	-0.3 to 5.5	V
	SS/TR	-0.3 to 5.5	V
	SYNC	-0.3 to 7	V
Output Voltage	BOOT-PH	0 to 7	V
	PH	-1 to 7	V
	PH 10ns Transient	-3 to 7	V
Output current	TPS50301	3	A
	TPS50601	6	A
Vdiff (GND to exposed thermal pad)		-0.2 to 0.2	V
Source Current	PH	Current Limit	A
	RT	±100	µA
Sink Current	PH	Current Limit	A
	PVIN	Current Limit	A
	COMP	±200	µA
	PWRGD	–0.1 to 5	mA
Electrostatic Discharge (HBM) QSS 009-105 (JESD22-A114A)		1	kV
Electrostatic Discharge (CDM) QSS 009-147 (JESD22-C101B.01)		1	kV
Operating Junction Temperature	TPS50301	–55 to 220	°C
	TPS50601	-55 to 150	
Storage Temperature	TPS50301	–65 to 220	°C
	TPS50601	-65 to 150	

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

PACKAGE DISSIPATION RATINGS(1)(2)(3)(4)(5)

PACKAGE	θ_{JA} THERMAL IMPEDANCE JUNCTION TO AMBIENT	θ_{JC} THERMAL IMPEDANCE JUNCTION TO CASE (THERMAL PAD)	θ_{JB} THERMAL IMPEDANCE JUNCTION TO BOARD
HKH	39.9°C/W	0.52°C/W	43.1°C/W

(1) Maximum power dissipation may be limited by overcurrent protection
(2) Power rating at a specific ambient temperature T_A should be determined with a junction temperature of 150°C. This is the point where distortion starts to substantially increase. Thermal management of the PCB should strive to keep the junction temperature at or below 150°C for best performance and long-term reliability. See power dissipation estimate in application section of this data sheet for more information.
(3) Test board conditions:
  (a) 2.5 inches × 2.5 inches, 4 layers, thickness: 0.062 inch
  (b) 2 oz. copper traces located on the top of the PCB
  (c) 2 oz. copper ground planes on the 2 internal layers and bottom layer
  (d) 4 0.010 inch thermal vias located under the device package
(4) For information on thermal characteristics see SPRA953A
(5) For TPS50301-HT, use polyimide PCB and thermal management to ensure operation below maximum T_J operation.

TPS50301 ELECTRICAL CHARACTERISTICS

T_J = –55°C to 210°C, VIN = 3 V to 6.3 V, PVIN = 1.6 V to 6.3 V (unless otherwise noted)

DESCRIPTION	CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN AND PVIN PINS)						
PVIN operating input voltage			1.6		6.3	V
VIN operating input voltage			3		6.3	V
VIN internal UVLO threshold	VIN rising			2.75	3	V
VIN internal UVLO hysteresis				50		mV
VIN shutdown supply current	EN = 0 V			2.5	8	mA
VIN operating – non switching supply current	VSENSE = VBG			5	10	mA
ENABLE AND UVLO (EN PIN)						
Enable threshold	Rising			1.13	1.19	V
Enable threshold	Falling		0.97	1.03		V
Input current	EN = 1.1 V			3.2		µA
Hysteresis current	EN = 1.3 V			3		µA
VOLTAGE REFERENCE						
Voltage reference	0 A ≤ Iout ≤ 3 A	-55°C	0.767	0.795	0.805	V
		25°C	0.785	0.795	0.805	
		210°C	0.785	0.795	0.830	
MOSFET						
High-side switch resistance	BOOT-PH = 2.2 V			55		mΩ
High-side switch resistance(1) (2)	BOOT-PH = 6.3 V			50		mΩ
Low-side switch resistance(1) (2)	VIN = 3 V			50		mΩ
ERROR AMPLIFIER						
Error amplifier transconductance (gm)(2)	–2 µA < ICOMP < 2 µA, V(COMP) = 1 V			1300		µMhos
Error amplifier dc gain(2)	VSENSE = 0.8 V			39000		V/V
Error amplifier source/sink(2)	V(COMP) = 1 V, 40 mV input overdrive			±125		µA
Start switching threshold(2)				0.25		V
COMP to Iswitch gm(2)				18		A/V
CURRENT LIMIT						
High-side switch current limit threshold	VIN = 6.3 V		7.8	11		A
Low-side switch sourcing current limit	VIN = 6.3 V		6	10		A
Low-side switch sinking current limit	VIN = 6.3 V			3		A

(1) Measured at pins
(2) Ensured by design only. Not tested in production.

TPS50301 ELECTRICAL CHARACTERISTICS (continued)

T_J = –55°C to 210°C, VIN = 3 V to 6.3 V, PVIN = 1.6 V to 6.3 V (unless otherwise noted)

DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
INTERNAL SWITCHING FREQUENCY					
Internally set frequency	RT = Open	395	500	585	kHz
Externally set frequency	RT = 100 kΩ (1%)		480		kHz
	RT = 485 kΩ (1%)		100		
	RT = 47 kΩ (1%)		1000		
EXTERNAL SYNCHRONIZATION					
SYNC out low-to-high rise time (10%/90%)	Cload = 25 pF		25	126	ns
SYNC out high-to-low fall time (90%/10%)	Cload = 25 pF		3	15	ns
Falling edge delay time(3)			180		°
SYNC out high level threshold	IOH = 50 µA	2			V
SYNC out low level threshold	IOL = 50 µA			600	mV
SYNC in low level threshold		800			mV
SYNC in high level threshold				1.85	V
SYNC in frequency range	% of program frequency	-5		5	%
		100		1000	kHz
PH (PH PIN)					
Minimum on time	Measured at 90% to 90% of VIN, 25°C, I_{PH} = 2A		94	236	ns
Minimum off time	BOOT-PH ≥ 2.2 V		500		ns
BOOT (BOOT PIN)					
BOOT-PH UVLO			2.2	3	V
SLOW START AND TRACKING (SS/TR PIN)					
SS charge current			2.5		µA
SS/TR to VSENSE matching	V(SS/TR) = 0.4 V		30	90	mV
POWER GOOD (PWRGD PIN)					
VSENSE threshold	VSENSE falling (Fault)		91		% Vref
	VSENSE rising (Good)		94		% Vref
	VSENSE rising (Fault)		109		% Vref
	VSENSE falling (Good)		106		% Vref
Output high leakage	VSENSE = Vref, V(PWRGD) = 5 V		0.03	2.9	µA
Output low	I(PWRGD) = 2 mA			0.3	V
Minimum VIN for valid output	V(PWRGD) < 0.5V at 100 µA		0.6	1	V
Minimum SS/TR voltage for PWRGD				1.4	V

(3) Bench verified. Not tested in production.

TPS50601 ELECTRICAL CHARACTERISTICS

T_J = –55°C to 125°C, V_{IN} = 3 V to 6.3 V, P_{VIN} = 1.6 V to 6.3 V (unless otherwise noted)

DESCRIPTION	CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN AND PVIN PINS)						
PVIN operating input voltage			1.6		6.3	V
VIN operating input voltage			3		6.3	V
VIN internal UVLO threshold	VIN rising			2.75	3	V
VIN internal UVLO hysteresis				50		mV
VIN shutdown supply current	EN = 0 V			2.5	5.9	mA
VIN operating – non switching supply current	VSENSE = VBG			5	10	mA
ENABLE AND UVLO (EN PIN)						
Enable threshold	Rising			1.13	1.18	V
Enable threshold	Falling		1.05	1.09		
Input current	EN = 1.1 V			3.2		µA
Hysteresis current	EN = 1.3 V			3		µA
VOLTAGE REFERENCE						
Voltage reference	0 A ≤ Iout ≤ 6 A	-55°C	0.767	0.795	0.804	V
		25°C	0.785	0.795	0.804	
		125°C	0.785	0.795	0.815	
MOSFET						
High-side switch resistance	BOOT-PH = 2.2 V			55		mΩ
High-side switch resistance(1)	BOOT-PH = 6.3 V			50		mΩ
Low-side switch resistance(1)	VIN = 6.3 V			50		mΩ
ERROR AMPLIFIER						
Error amplifier transconductance (gm)(2)	–2 µA < ICOMP < 2 µA, V(COMP) = 1 V			1300		µMhos
Error amplifier dc gain(2)	VSENSE = 0.792 V			39000		V/V
Error amplifier source/sink(2)	V(COMP) = 1 V, 40 mV input overdrive			±125		µA
Start switching threshold(2)				0.25		V
COMP to Iswitch gm(2)				18		A/V
CURRENT LIMIT						
High-side switch current limit threshold	VIN = 6.3 V		8	11		A
Low-side switch sourcing current limit	VIN = 6.3 V		7	10		A
Low-side switch sinking current limit	VIN = 6.3 V			3		A

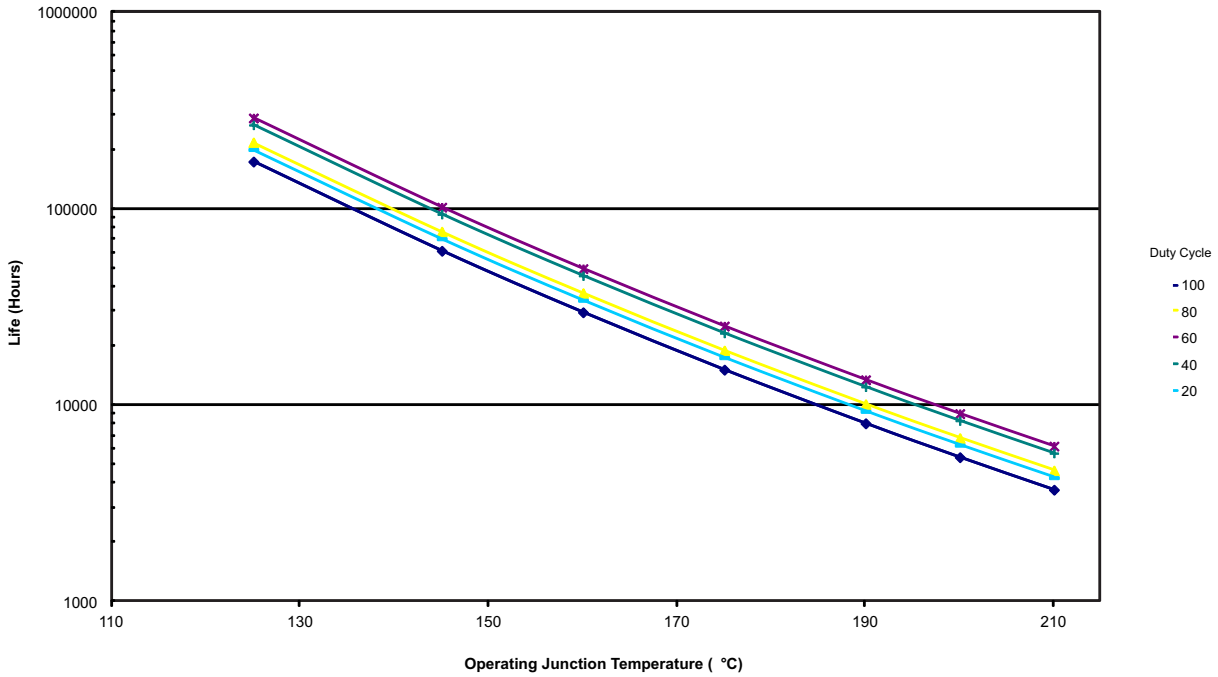
(1) Measured at pins
(2) Ensured by design only. Not tested in production.

TPS50601 ELECTRICAL CHARACTERISTICS (continued)

T_J = –55°C to 125°C, V_{IN} = 3 V to 6.3 V, P_{VIN} = 1.6 V to 6.3 V (unless otherwise noted)

DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
THERMAL SHUTDOWN					
Thermal shutdown			175		°C
Thermal shutdown hysteresis			10		°C
INTERNAL SWITCHING FREQUENCY					
Internally set frequency	RT = Open	395	500	585	kHz
Externally set frequency	RT = 100 kΩ (1%)		480		kHz
	RT = 485 kΩ (1%)		100		
	RT = 47 kΩ (1%)		1000		
EXTERNAL SYNCHRONIZATION					
SYNC out low-to-high rise time (10%/90%)	Cload = 25 pF		25	111	ns
SYNC out high-to-low fall time (90%/10%)	Cload = 25 pF		3	15	ns
Falling edge delay time(3)			180		°
SYNC out high level threshold	IOH = 50 µA	2			V
SYNC out low level threshold	IOL = 50 µA			600	mV
SYNC in low level threshold		800			mV
SYNC in high level threshold				1.85	V
SYNC in frequency range	% of program frequency	-5		5	%
		100		1000	kHz
PH (PH PIN)					
Minimum on time	Measured at 90% to 90% of VIN, 25°C, I_{PH} = 2A		94	175	ns
Minimum off time	BOOT-PH ≥ 3 V		500		ns
BOOT (BOOT PIN)					
BOOT-PH UVLO			2.2	3	V
SLOW START AND TRACKING (SS/TR PIN)					
SS charge current			2.5		µA
SS/TR to VSENSE matching	V(SS/TR) = 0.4 V		30	90	mV
POWER GOOD (PWRGD PIN)					
VSENSE threshold	VSENSE falling (Fault)		91		% Vref
	VSENSE rising (Good)		94		% Vref
	VSENSE rising (Fault)		109		% Vref
	VSENSE falling (Good)		106		% Vref
Output high leakage	VSENSE = Vref, V(PWRGD) = 5 V		30	181	nA
Output low	I(PWRGD) = 2 mA			0.3	V
Minimum VIN for valid output	V(PWRGD) < 0.5V at 100 µA		0.6	1	V
Minimum SS/TR voltage for PWRGD				1.4	V

(3) Bench verified. Not tested in production.



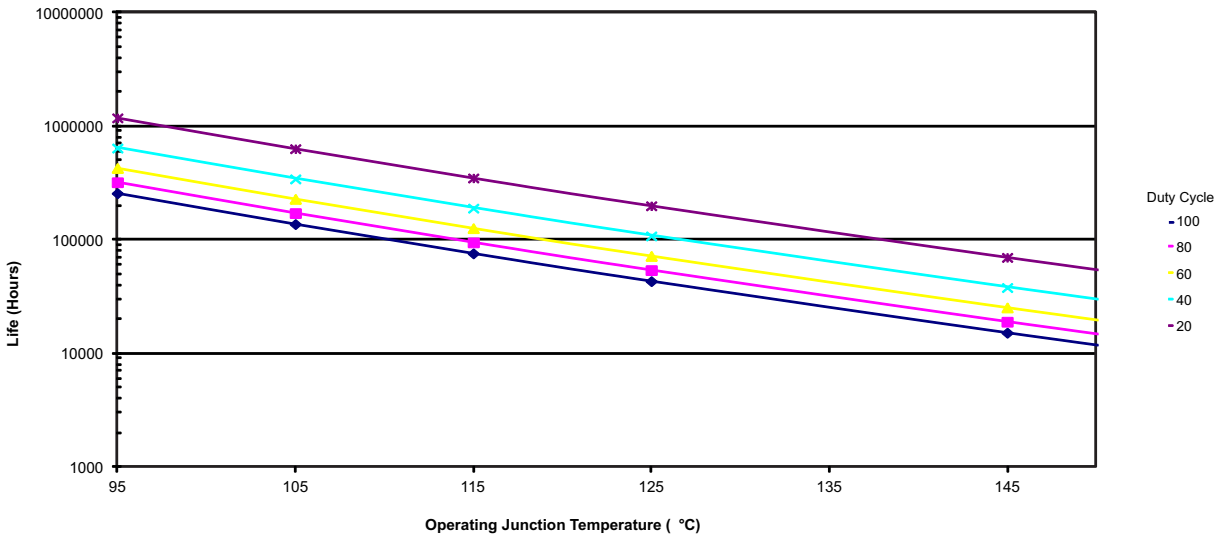
A. See datasheet for absolute maximum and minimum recommended operating conditions.

B. Silicon operating life design goal is 10 years at 125°C junction temperature (does not include package interconnect life).

C. The predicted operating lifetime vs. junction temperature is based on reliability modeling using electromigration as the dominant failure mechanism affecting device wearout for the specific device process and design characteristics.

D. This device is rated for 1000 hours of continuous operation at maximum rated temperature at 210°C.

Figure 1. TPS50301-HT 3-A Continuous Current Estimated Device Life



A. See datasheet for absolute maximum and minimum recommended operating conditions.

B. Product operating life design goal is > 15 years for 65°C ≤ T_J ≤ 95°C based on silicon technology characterization per MIL-PRF-38535.

C. The predicted operating lifetime vs. junction temperature is based on reliability modeling using electromigration as the dominant failure mechanism affecting device wearout for the specific device process and design characteristics.

Figure 2. TPS50601-SP 6-A Continuous Current Estimated Device Life

DEVICE INFORMATION

PIN ASSIGNMENTS

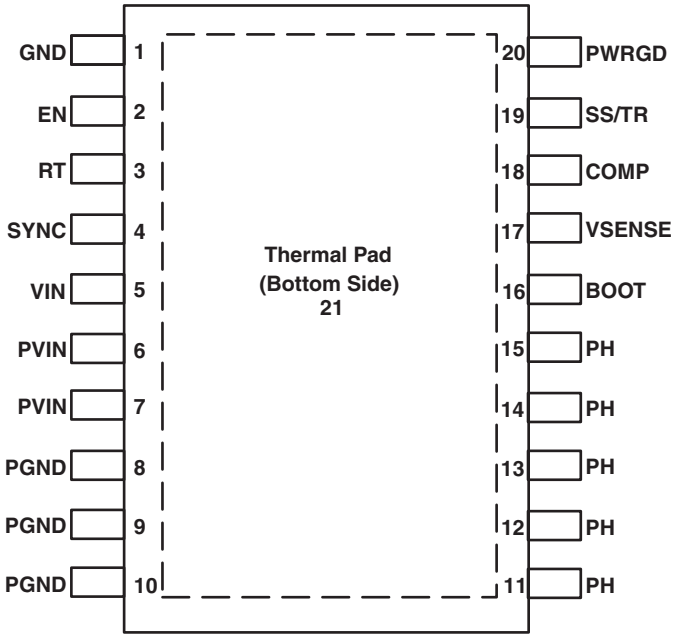
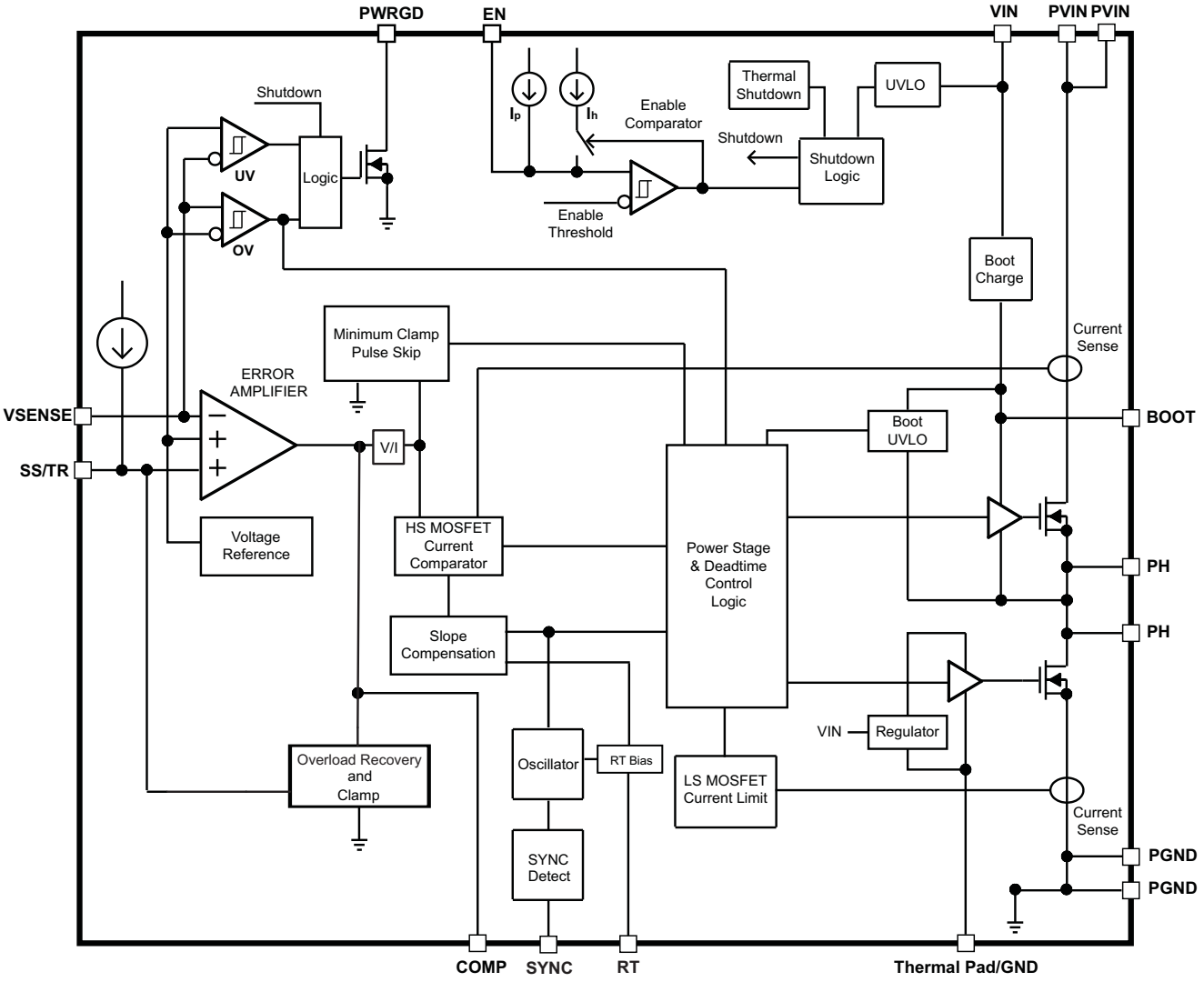


Table 2. PIN FUNCTIONS

PIN		DESCRIPTION
NAME	No.	
GND	1	Return for control circuitry/Thermal pad (1)
EN	2	Enable pin. Float to enable. Adjust the input undervoltage lockout with two resistors.
RT	3	In internal oscillation mode, a resistor is connected between the RT pin and GND to set the switching frequency.
SYNC	4	Optoinal 1-MHz external system clock input. The device operates with an internal oscillator if this pin is left open.
VIN	5	Supplies the power to the output FET controllers.
PVIN	6, 7	Power input. Supplies the power switches of the power converter.
PGND	8, 9, 10	Return for low side Power MOSFET
PH	11, 12, 13, 14, 15	The switch node
BOOT	16	A bootstrap cap is required between BOOT and PH. The voltage on this cap carries the gate drive voltage for the high-side MOSFET.
VSENSE	17	Inverting input of the gm error amplifier
COMP	18	Error amplifier output, and input to the output switch current comparator. Connect frequency compensation to this pin.
SS/TR	19	Slow-start and tracking. An external capacitor connected to this pin sets the internal voltage reference rise time. The voltage on this pin overrides the internal reference. It can be used for tracking and sequencing.
PWRGD	20	Power Good fault pin. Asserts low if output voltage is low due to thermal shutdown, dropout, over-voltage, EN shutdown or during slow start.

(1) Thermal pad (analog ground) must be connected to PGND external to the package.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

OVERVIEW

The device is a 6.3-V, 3-A or 6-A, synchronous step-down (buck) converter with two integrated n-channel MOSFETs. To improve performance during line and load transients the device implements a constant frequency, peak current mode control which also simplifies external frequency compensation. The wide switching frequency, 100 kHz to 1 MHz, allows for efficiency and size optimization when selecting the output filter components.

The device has been designed for safe monotonic startup into pre-biased loads. The default start up is when VIN is typically 3 V. The EN pin has an internal pull-up current source that can be used to adjust the input voltage under voltage lockout (UVLO) with two external resistors. In addition, the EN pin can be floating for the device to operate with the internal pull-up current. The total operating current for the device is approximately 5 mA when not switching and under no load. When the device is disabled, the supply current is typically less than 2.5 mA.

The integrated MOSFETs allow for high efficiency power supply designs with continuous output currents up to 6 amperes. The MOSFETs have been sized to optimize efficiency for lower duty cycle applications.

The device reduces the external component count by integrating the boot recharge circuit. The bias voltage for the integrated high-side MOSFET is supplied by a capacitor between the BOOT and PH pins. The boot capacitor voltage is monitored by a BOOT to PH UVLO (BOOT-PH UVLO) circuit allowing PH pin to be pulled low to recharge the boot capacitor. The device can operate over duty cycle range per Equation 2 and Equation 3 as long as the boot capacitor voltage is higher than the preset BOOT-PH UVLO threshold which is typically 2.2 V. The output voltage can be stepped down to as low as the 0.795 V voltage reference (Vref).

The device has a power good comparator (PWRGD) with hysteresis which monitors the output voltage through the VSENSE pin. The PWRGD pin is an open drain MOSFET which is pulled low when the VSENSE pin voltage is less than 91% or greater than 109% of the reference voltage Vref and asserts high when the VSENSE pin voltage is 94% to 106% of the Vref.

The SS/TR (slow start/tracking) pin is used to minimize inrush currents or provide power supply sequencing during power up. A small value capacitor or resistor divider should be coupled to the pin for slow start or critical power supply sequencing requirements.

The device is protected from output overvoltage, overload and thermal fault conditions. The device minimizes excessive output overvoltage transients by taking advantage of the overvoltage circuit power good comparator. When the overvoltage comparator is activated, the high-side MOSFET is turned off and prevented from turning on until the VSENSE pin voltage is lower than 106% of the Vref. The device implements both high-side MOSFET overload protection and bidirectional low-side MOSFET overload protections which help control the inductor current and avoid current runaway. The device also shuts down if the junction temperature is higher than thermal shutdown trip point. The device is restarted under control of the slow start circuit automatically when the junction temperature drops 10°C typically below the thermal shutdown trip point.

TYPICAL CHARACTERISTICS (continued)

VOLTAGE REFERENCE vs TEMPERATURE

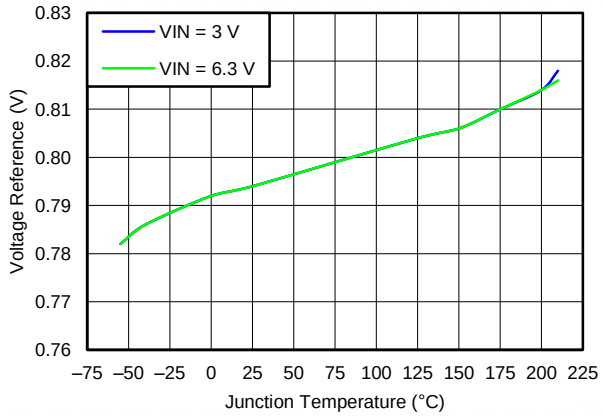


Figure 3.

OSCILLATOR FREQUENCY vs TEMPERATURE

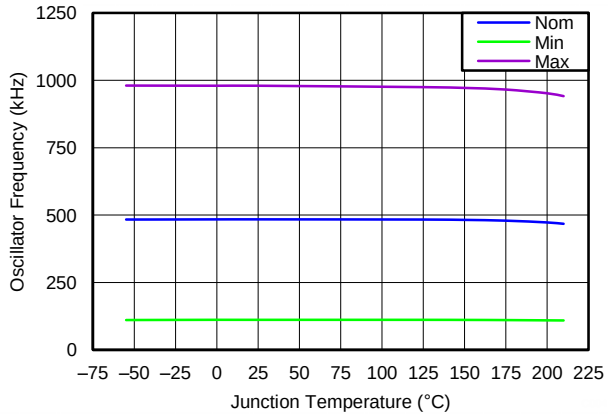


Figure 4.

SHUTDOWN QUIESCENT CURRENT vs TEMPERATURE

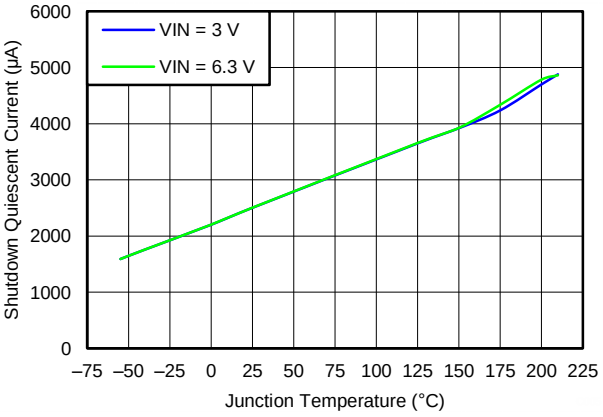


Figure 5.

EN PIN HYSTERESIS CURRENT vs TEMPERATURE

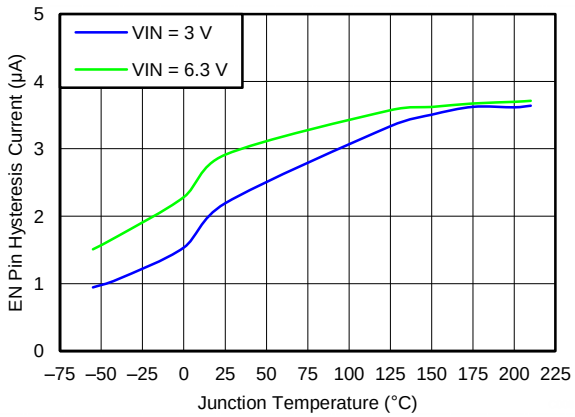


Figure 6.

EN PIN PULL-UP CURRENT vs TEMPERATURE

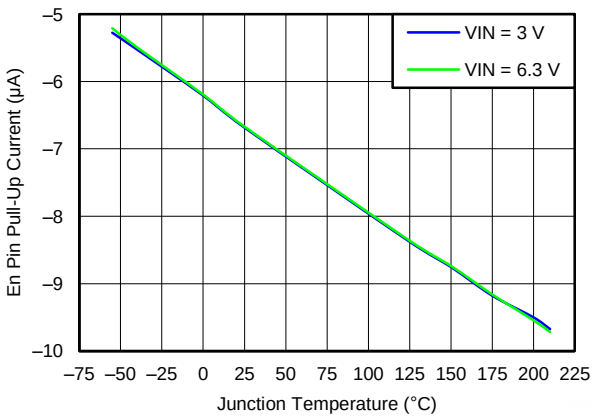


Figure 7.

EN PIN UVLO THRESHOLD vs TEMPERATURE

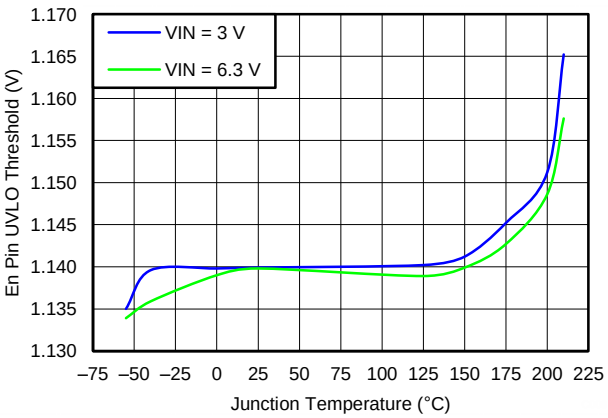


Figure 8.

TYPICAL CHARACTERISTICS (continued)

NON-SWITCHING OPERATING QUIESCENT CURRENT (VIN) vs TEMPERATURE

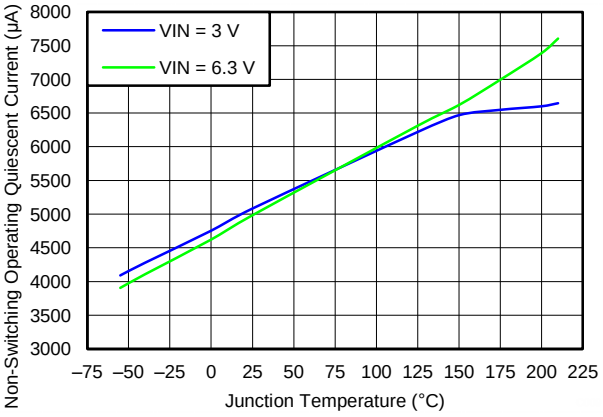


Figure 9.

SLOW START CHARGE CURRENT vs TEMPERATURE

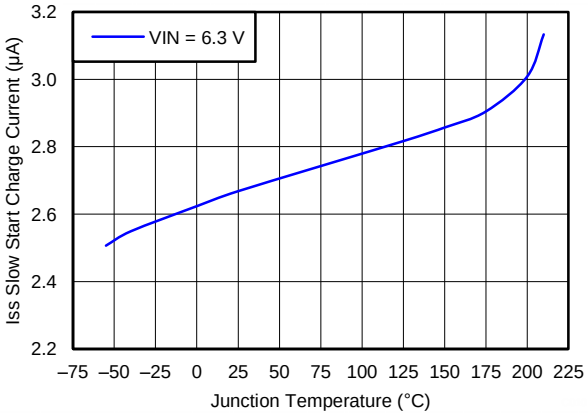


Figure 10.

(SS-V_{SENSE}) OFFSET vs TEMPERATURE

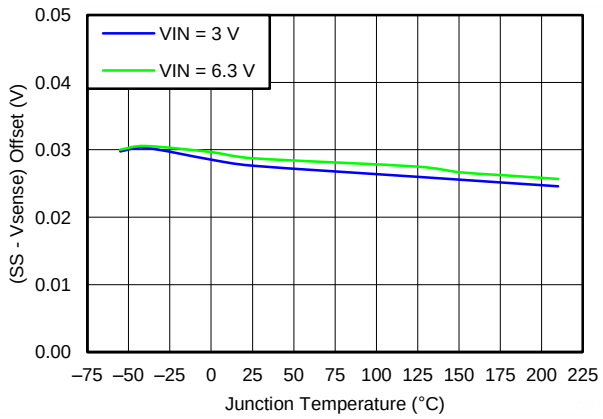


Figure 11.

HIGH-SIDE CURRENT LIMIT THRESHOLD vs TEMPERATURE

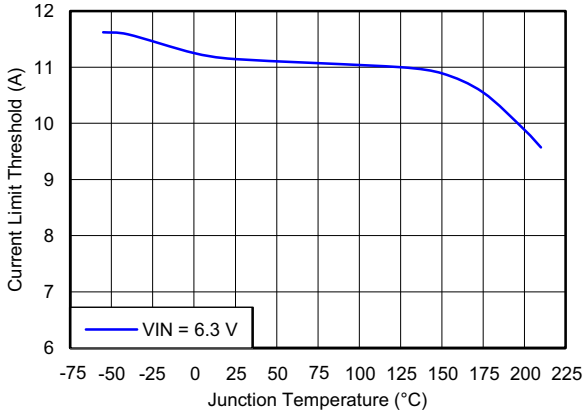


Figure 12.

LOW-SIDE $R_{DS(ON)}$ vs TEMPERATURE

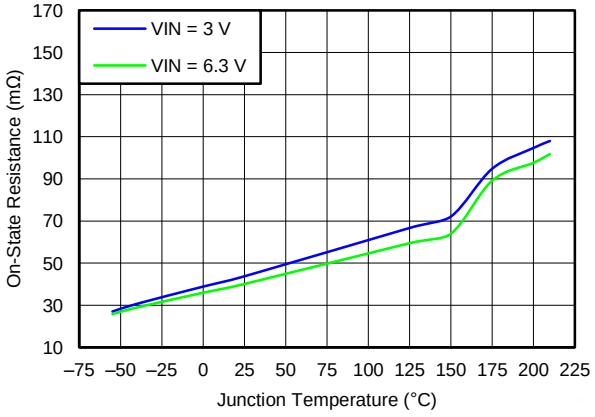


Figure 13.

HIGH-SIDE $R_{DS(ON)}$ vs TEMPERATURE

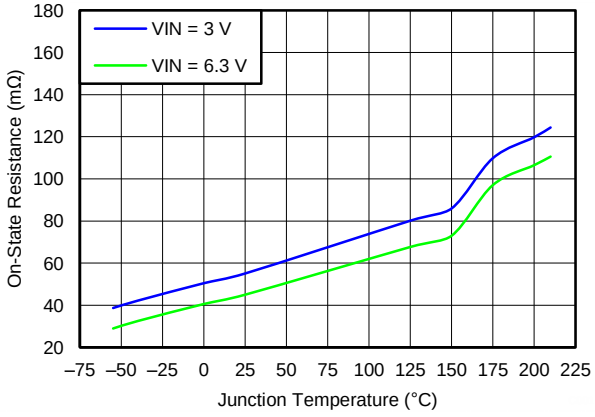


Figure 14.

TYPICAL CHARACTERISTICS (continued)

MINIMUM CONTROLLABLE ON TIME vs TEMPERATURE

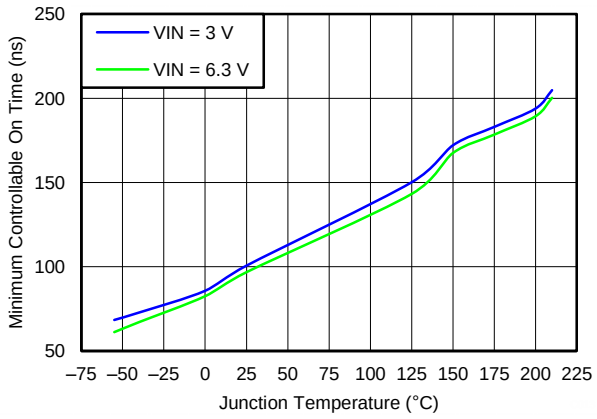


Figure 15.

MINIMUM CONTROLLABLE DUTY RATIO vs TEMPERATURE

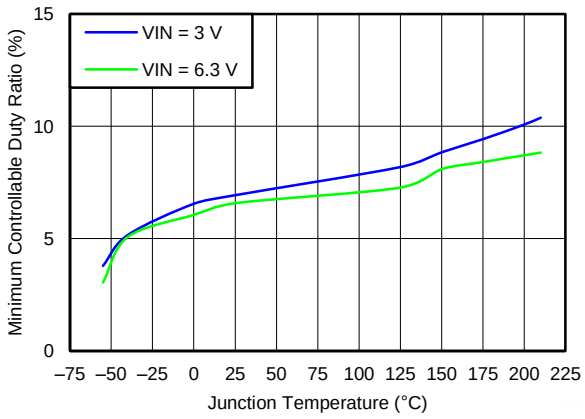


Figure 16.

DETAILED DESCRIPTION

Fixed Frequency PWM Control

The device uses fixed frequency, peak current mode control. The output voltage is compared through external resistors on the VSENSE pin to an internal voltage reference by an error amplifier which drives the COMP pin. An internal oscillator initiates the turn on of the high-side power switch. The error amplifier output is converted into a current reference which compares to the high-side power switch current. When the power switch current reaches current reference generated by the COMP voltage level the high-side power switch is turned off and the low-side power switch is turned on.

Continuous Current Mode Operation (CCM)

As a synchronous buck converter, the device normally works in CCM (Continuous Conduction Mode) under all load conditions.

VIN and Power VIN Pins (VIN and PVIN)

The device allows for a variety of applications by using the VIN and PVIN pins together or separately. The VIN pin voltage supplies the internal control circuits of the device. The PVIN pin voltage provides the input voltage to the power converter system.

If tied together, the input voltage for VIN and PVIN can range from 3 V to 6.3 V. If using the VIN separately from PVIN, the VIN pin must be between 3 V and 6.3 V, and the PVIN pin can range from as low as 1.6 V to 6.3 V. A voltage divider connected to the EN pin can adjust the input voltage UVLO appropriately. Adjusting the input voltage UVLO on the PVIN pin helps to provide consistent power up behavior.

PVIN vs Frequency

With V_{IN} tied to PV_{IN} minimum off-time determines what output voltage is achievable over frequency range.

Voltage Reference

The voltage reference system produces a precise voltage reference as indicated in TPS50301 ELECTRICAL CHARACTERISTICS and TPS50601 ELECTRICAL CHARACTERISTICS.

Adjusting the Output Voltage

The output voltage is set with a resistor divider from the output (VOUT) to the VSENSE pin. It is recommended to use 1% tolerance or better divider resistors. Start with a 10 kΩ for R15 (top resistor) and use Equation 1 to calculate R38 (bottom reisitor divider). To improve efficiency at light loads consider using larger value resistors. If the values are too high the regulator is more susceptible to noise and voltage errors from the VSENSE input current are noticeable.

$$R38 = \frac{Vref}{Vo - Vref} R15 \quad (1)$$

Where Vref = 0.795 V

The minimum output voltage and maximum output voltage can be limited by the minimum on time of the high-side MOSFET and bootstrap voltage (BOOT-PH voltage) respectively. More discussion is located in Bootstrap Voltage (BOOT) and Low Dropout Operation.

Maximum Duty Cycle Limit

The TPS50601 can operate at duty cycle per Equation 2 and Equation 3 as long as the boot capacitor voltage is higher than the preset BOOT-PH UVLO threshold which is typically 2.2 V.

Duty cycle can be calculated based on Equation 2:

$$D(V_{IN}) = \frac{V_{OUT} + I_{OUT\_max} \bullet R_{Tesr} + I_{OUT\_max} \bullet R_{ds\_low}}{V_{IN} - I_{OUT\_max} \bullet R_{ds\_high} + I_{OUT\_max} \bullet R_{ds\_low}} \quad (2)$$

Where

$R_{Tesr} = R_{dcr} + R_{trace}$
R_{dcr} is the DC resistance of the inductor.
R_{trace} is the DC trace resistance (miscellaneous drop).
R_{ds_high} is the maximum R_{DS} of the high side MOSFET.
R_{ds_low} is the maximum R_{DS} of the low side MOSFET.

PVIN vs Frequency

With V_{IN} tied to PVIN minimum off-time will determine the output voltage that is achievable over frequency range. For V_{IN} = PVIN must be greater than or equal to 3 V. For V_{IN} = 3 V, PVIN can vary from 1.6 V to 6.3 V as highlighted in Electrical Characteristics.

This is given by equation below.

$$PV_{in\_min}(f_{SW}) = \frac{V_O + I_O(R_{ds\_onLS} + R_{misc})}{1 - T_{off\_min} \bullet f_{SW}} \quad (3)$$

Where

R_{ds_onLS} - low side $R_{ds\text{-}on}$
R_{misc} - Miscellaneous trace drops
T_{off_min} – minimum off time

Using the above approach one can calculate minimum PVIN required for specific V_{OUT} as indicated below as an example.

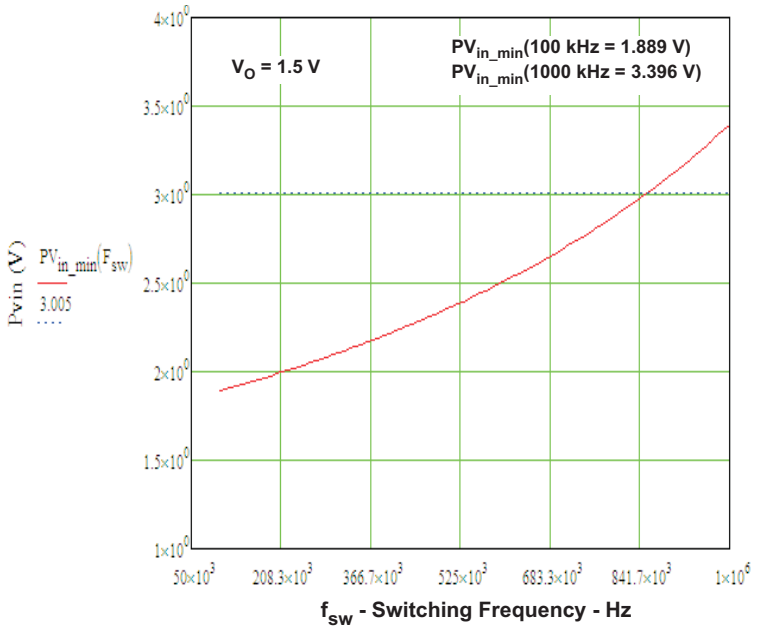


Figure 17. PV_{IN} vs Frequency

Safe Start-up into Pre-Biased Outputs

The device has been designed to prevent the low-side MOSFET from discharging a pre-biased output. During monotonic pre-biased startup, the low-side MOSFET is not allowed to sink current until the SS/TR pin voltage is higher than 1.4 V.

Error Amplifier

The device uses a transconductance error amplifier. The error amplifier compares the VSENSE pin voltage to the lower of the SS/TR pin voltage or the internal 0.795 V voltage reference. The transconductance of the error amplifier is 1300 µA/V during normal operation. The frequency compensation network is connected between the COMP pin and ground. Error amplifier DC gain is typically 39000 V/V with minimum value of 22000 V/V per design.

Slope Compensation

The device adds a compensating ramp to the switch current signal. This slope compensation prevents sub-harmonic oscillations. The available peak inductor current remains constant over the full duty cycle range. Minimum peak-to-peak inductor current should be greater than 1 A.

Enable and Adjusting Under-Voltage Lockout

The EN pin provides electrical on/off control of the device. Once the EN pin voltage exceeds the threshold voltage, the device starts operation. If the EN pin voltage is pulled below the threshold voltage, the regulator stops switching and enters low Iq state. If an external Schottky diode is used from V_{IN} to Boot, then a bleeder may be required < 1 mA to ensure output is low when unit is disabled via Enable pin.

The EN pin has an internal pull-up current source, allowing the user to float the EN pin for enabling the device. If an application requires controlling the EN pin, use open drain or open collector output logic to interface with the pin.

The device implements internal UVLO circuitry on the VIN pin. The device is disabled when the VIN pin voltage falls below the internal VIN UVLO threshold. The internal VIN UVLO threshold has a hysteresis of 150 mV.

If an application requires either a higher UVLO threshold on the VIN pin or a secondary UVLO on the PVIN, in split rail applications, then the EN pin can be configured as shown in Figure 18, Figure 19 and Figure 20. When using the external UVLO function it is recommended to set the hysteresis to be greater than 500 mV.

The EN pin has a small pull-up current Ip which sets the default state of the pin to enable when no external components are connected. The pull-up current is also used to control the voltage hysteresis for the UVLO function since it increases by I_h once the EN pin crosses the enable threshold. The UVLO thresholds can be calculated using Equation 4 and Equation 5.

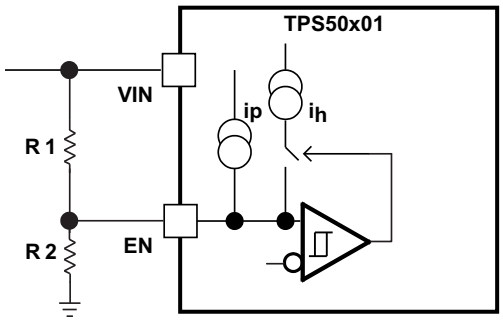


Figure 18. Adjustable VIN Under Voltage Lock Out

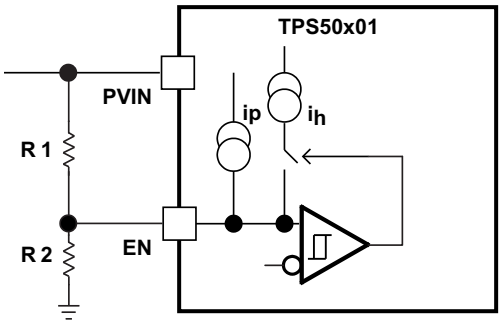


Figure 19. Adjustable PVIN Under Voltage Lock Out, VIN ≥ 3 V

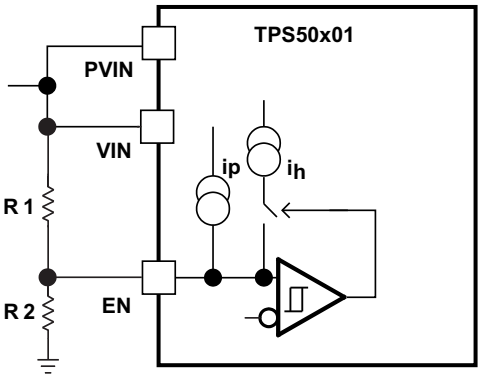


Figure 20. Adjustable VIN and PVIN Under Voltage Lock Out

$$R1 = \frac{V_{START}\left(\frac{V_{ENFALLING}}{V_{ENRISING}}\right) - V_{STOP}}{I_p\left(1 - \frac{V_{ENFALLING}}{V_{ENRISING}}\right) + I_h} \quad (4)$$

$$R2 = \frac{R1 \times V_{ENFALLING}}{V_{STOP} - V_{ENFALLING} + R1(I_p + I_h)} \quad (5)$$

Where I_h = 3 µA, I_p = 3.2 µA, $V_{ENRISING}$ = 1.131 V, $V_{ENFALLING}$ = 1.09 V

Adjustable Switching Frequency and Synchronization (SYNC)

The switching frequency of the device supports three modes of operations. The modes of operation are set by the conditions on the RT and Sync pins. At a high level these modes can be described as master, internal oscillator and external synchronization modes.

In master mode, the RT pin should be left floating, the internal oscillator is set to 500 kHz and the Sync pin is set as an output clock. The Sync output is in phase with respect to the internal oscillator. Sync out signal level is same as V_{IN} level with 50% duty cycle. Sync signal feeding the slave module which is in phase with the master clock gets internally inverted (180 degrees out of phase with the master clock) internally in the slave module.

In internal oscillator mode, a resistor is connected between the RT pin and GND. The Sync pin requires a 10-kΩ resistor to GND for this mode to be effective. The switching frequency of the device is adjustable from 100 kHz to 1 MHz by placing a maximum of 510 kΩ and a minimum of 47 kΩ respectively. To determine the RT resistance for a given switching frequency, use Equation 6 or the curve in Figure 21. To reduce the solution size one would set switching frequency as high as possible, but tradeoffs of supply efficiency and minimum controllable on time should be considered.

$$RT(F_{SW}) = 67009 \times F_{SW}^{-1.0549} \quad (6)$$

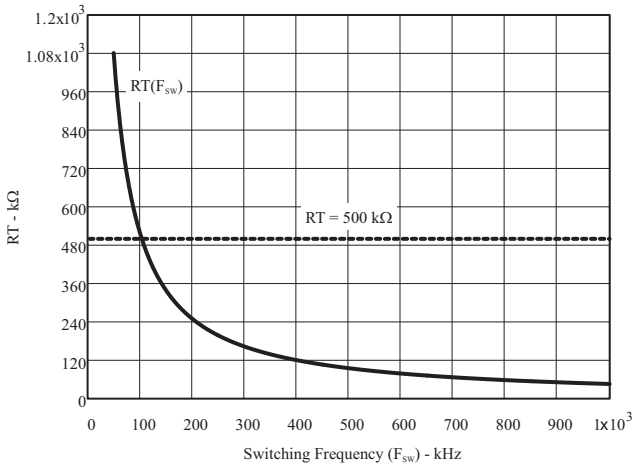


Figure 21. RT vs Switching Frequency

When operating the converter in internal oscillator mode (internal oscillator determines the switching frequency (500 kHz) default), the synchronous pin becomes the output and there is a phase inversion. When trying to parallel with another converter, the RT pin of the second (slave) converter must have its RT pin populated such that the converter frequency of the slave converter must be within ±5% of the master converter. This is required because the RT pin also sets the proper operation of slope compensation.

In external synchronization mode, a resistor is connected between the RT pin and GND. The Sync pin requires a toggling signal for this mode to be effective. The switching frequency of the device goes 1:1 with that of Sync pin. External system clock-user supplied sync clock signal determines the switching frequency. If no external clock signal is detected for 20 µs, then TPS50601-SP transitions to its internal clock which is typically 500 kHz. An external synchronization using an inverter to obtain phase inversion is necessary. RT values of master and slave converter must be within ±5% of the external synchronization frequency. This is necessary for proper slope compensation. A resistance in the RT pin required for proper operation of the slope compensation circuit. To determine the RT resistance for a given switching frequency, use Equation 6 or the curve in Figure 21. To reduce the solution size one would set switching frequency as high as possible, but tradeoffs of supply efficiency and minimum controllable on time should be considered.

These modes are described in Table 3.

Table 3. Switching Frequency, SYNC and RT Pins Usage Table

RT PIN	SYNC PIN	SWITCHING FREQUENCY	DESCRIPTION/NOTES
Float	Generates an output signal	500 kHz	Sync pin behaves as an output. Sync output signal is 180° out of phase to the internal 500-kHz switching frequency.
47-kΩ to 485-kΩ resistor to AGND	10-kΩ resistor to AGND	100 kHz to 1 MHz	Internally generated switching frequency is based upon the resistor value present at the RT pin.
	User supplied sync clock or TPS50601 master device sync output	Internally synchronized to external clock	Set value of RT that corresponds to the externally supplied sync frequency.

Slow Start (SS/TR)

The device uses the lower voltage of the internal voltage reference or the SS/TR pin voltage as the reference voltage and regulates the output accordingly. A capacitor on the SS/TR pin to ground implements a slow start time. The device has an internal pull-up current source of 5 mA that charges the external slow start capacitor. The calculations for the slow start time (Tss, 10% to 90%) and slow start capacitor (Css) are shown in Equation 7. The voltage reference (Vref) is 0.795 V and the slow start charge current (Iss) is 2.5 µA.

$$Tss(ms) = \frac{Css(nF) \times Vref(V)}{Iss(\mu A)} \quad (7)$$

When the input UVLO is triggered, the EN pin is pulled below 1.032 V, or a thermal shutdown event occurs the device stops switching and enters low current operation. At the subsequent power up, when the shutdown condition is removed, the device does not start switching until it has discharged its SS/TR pin to ground ensuring proper soft start behavior.

Power Good (PWRGD)

The PWRGD pin is an open drain output. Once the VSENSE pin is between 94% and 106% of the internal voltage reference the PWRGD pin pull-down is de-asserted and the pin floats. It is recommended to use a pull-up resistor between the values of 10 kΩ and 100 kΩ to a voltage source that is 5.5 V or less. The PWRGD is in a defined state once the VIN input voltage is greater than 1 V but with reduced current sinking capability. The PWRGD achieves full current sinking capability once the VIN input voltage is above 3 V.

The PWRGD pin is pulled low when VSENSE is lower than 91% or greater than 109% of the nominal internal reference voltage. Also, the PWRGD is pulled low, if the input UVLO or thermal shutdown are asserted, the EN pin is pulled low or the SS/TR pin is below 1.4 V.

Bootstrap Voltage (BOOT) and Low Dropout Operation

The device has an integrated boot regulator, and requires a small ceramic capacitor between the BOOT and PH pins to provide the gate drive voltage for the high-side MOSFET. The boot capacitor is charged when the BOOT pin voltage is less than VIN and BOOT-PH voltage is below regulation. The value of this ceramic capacitor should be 0.1 µF. A ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 10 V or higher is recommended because of the stable characteristics over temperature and voltage.

To improve drop out, the device is designed to operate at a high duty cycle as long as the BOOT to PH pin voltage is greater than the BOOT-PH UVLO threshold which is typically 2.1 V. When the voltage between BOOT and PH drops below the BOOT-PH UVLO threshold the high-side MOSFET is turned off and the low-side MOSFET is turned on allowing the boot capacitor to be recharged. In applications with split input voltage rails, high duty cycle operation can be achieved as long as (VIN – PVIN) > 4 V.

Maximum switching frequency is also limited by minimum on time (specified in Electrical Characteristics table) as indicated by Equation 8. Switching frequency will be worse case at no load conditions.

$$F_{SW} = \frac{1}{T} = \frac{V_O + R_{ds\_on} \bullet (I_O)}{V_{IN} \bullet (T_{on\_max})} \quad (8)$$

Sequencing (SS/TR)

Many of the common power supply sequencing methods can be implemented using the SS/TR, EN and PWRGD pins.

The sequential method is illustrated in Figure 22 using two TPS50601 devices. The power good of the first device is coupled to the EN pin of the second device which enables the second power supply once the primary supply reaches regulation.

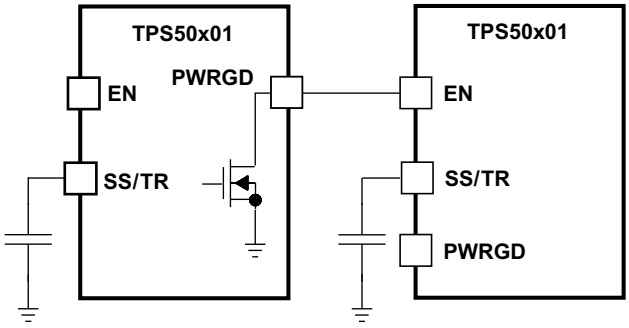


Figure 22. Sequential Start Up Sequence

Figure 23 shows the method implementing ratio-metric sequencing by connecting the SS/TR pins of two devices together. The regulator outputs ramp up and reach regulation at the same time. When calculating the slow start time the pull-up current source must be doubled in Equation 7.

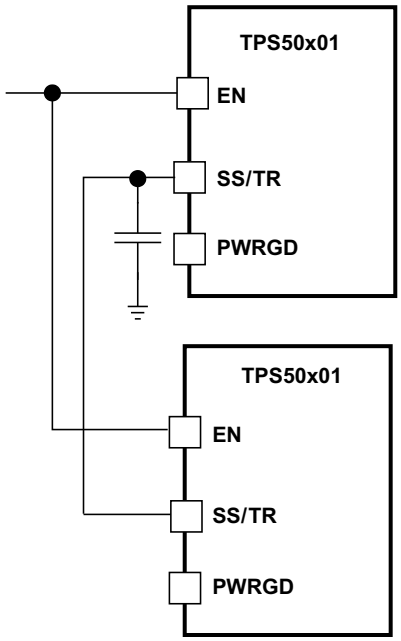


Figure 23. Ratiometric Start Up Sequence

Ratio-metric and simultaneous power supply sequencing can be implemented by connecting the resistor network of R1 and R2 shown in Figure 24 to the output of the power supply that needs to be tracked or another voltage reference source. Using Equation 9 and Equation 10, the tracking resistors can be calculated to initiate the Vout2 slightly before, after or at the same time as Vout1. Equation 11 is the voltage difference between Vout1 and Vout2.

To design a ratio-metric start up in which the Vout2 voltage is slightly greater than the Vout1 voltage when Vout2 reaches regulation, use a negative number in Equation 9 and Equation 10 for ΔV. Equation 11 results in a positive number for applications where the Vout2 is slightly lower than Vout1 when Vout2 regulation is achieved.

The ΔV variable is zero volt for simultaneous sequencing. To minimize the effect of the inherent SS/TR to VSENSE offset (Vssoffset, 29 mV) in the slow start circuit and the offset created by the pull-up current source (Iss, 2 μA) and tracking resistors, the Vssoffset and Iss are included as variables in the equations.

To ensure proper operation of the device, the calculated R1 value from Equation 9 must be greater than the value calculated in Equation 12.

$$R1 = \frac{Vout2 + \Delta V}{Vref} \times \frac{Vssoffset}{Iss} \quad (9)$$

$$R2 = \frac{Vref \times R1}{Vout2 + \Delta V - Vref} \quad (10)$$

$$\Delta V = Vout1 - Vout2 \quad (11)$$

$$R1 > 2800 \times Vout1 - 180 \times \Delta V \quad (12)$$

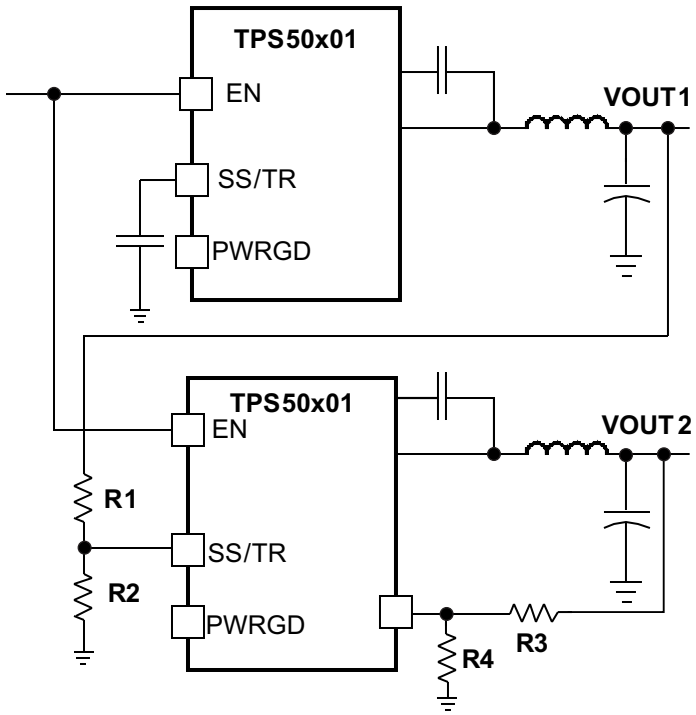


Figure 24. Ratiometric and Simultaneous Startup Sequence

Output Overvoltage Protection (OVP)

The device incorporates an output overvoltage protection (OVP) circuit to minimize output voltage overshoot. For example, when the power supply output is overloaded the error amplifier compares the actual output voltage to the internal reference voltage. If the VSENSE pin voltage is lower than the internal reference voltage for a considerable time, the output of the error amplifier demands maximum output current. Once the condition is removed, the regulator output rises and the error amplifier output transitions to the steady state voltage. In some applications with small output capacitance, the power supply output voltage can respond faster than the error amplifier. This leads to the possibility of an output overshoot. The OVP feature minimizes the overshoot by comparing the VSENSE pin voltage to the OVP threshold. If the VSENSE pin voltage is greater than the OVP threshold the high-side MOSFET is turned off preventing current from flowing to the output and minimizing output overshoot. When the VSENSE voltage drops lower than the OVP threshold, the high-side MOSFET is allowed to turn on at the next clock cycle.

Overcurrent Protection

The device is protected from overcurrent conditions by cycle-by-cycle current limiting on both the high-side MOSFET and the low-side MOSFET.

High-side MOSFET overcurrent protection

The device implements current mode control which uses the COMP pin voltage to control the turn off of the high-side MOSFET and the turn on of the low-side MOSFET on a cycle by cycle basis. Each cycle the switch current and the current reference generated by the COMP pin voltage are compared, when the peak switch current intersects the current reference the high-side switch is turned off.

Low-side MOSFET overcurrent protection

While the low-side MOSFET is turned on its conduction current is monitored by the internal circuitry. During normal operation the low-side MOSFET sources current to the load. At the end of every clock cycle, the low-side MOSFET sourcing current is compared to the internally set low-side sourcing current limit. If the low-side sourcing current is exceeded the high-side MOSFET is not turned on and the low-side MOSFET stays on for the next cycle. The high-side MOSFET is turned on again when the low-side current is below the low-side sourcing current limit at the start of a cycle.

The low-side MOSFET may also sink current from the load. If the low-side sinking current limit is exceeded the low-side MOSFET is turned off immediately for the rest of that clock cycle. In this scenario both MOSFETs are off until the start of the next cycle.

When the low-side MOSFET turns off, switch node increases and forward biases the high-side MOSFET parallel diode (high-side MOSFET is still off at this stage).

TPS50601 Thermal Shutdown

The internal thermal shutdown circuitry forces the device to stop switching if the junction temperature exceeds 175°C typically. The device reinitiates the power up sequence when the junction temperature drops below 165°C typically.

Turn-On Behavior

Minimum on-time specification determines the maximum operating frequency of the design. As the unit starts up and goes through its soft start process, the required duty-cycle is less than the minimum controllable on-time. This can cause the converter to skip pulses. Thus, instantaneous output pulses can be higher or lower than the desired voltage. This behavior is shown in and is only evident when operating at high frequency with high bandwidth. Once the minimum on-pulse is greater than the minimum controllable on-time, the turn-on behavior is normal. When operating at low frequencies (100 kHz or less), the turn-on behavior does not exhibit any ringing at initial startup.

Small Signal Model for Loop Response

Figure 25 shows an equivalent model for the device control loop which can be modeled in a circuit simulation program to check frequency response and transient responses. The error amplifier is a transconductance amplifier with a gm of 1300 µA/V. The error amplifier can be modeled using an ideal voltage controlled current source. The resistor Roea (30 MΩ) and capacitor Coea (20.7 pF) model the open loop gain and frequency response of the error amplifier. The 1-mV ac voltage source between the nodes a and b effectively breaks the control loop for the frequency response measurements. Plotting a/c and c/b show the small signal responses of the power stage and frequency compensation respectively. Plotting a/b shows the small signal response of the overall loop. The dynamic loop response can be checked by replacing the R_L with a current source with the appropriate load step amplitude and step rate in a time domain analysis.

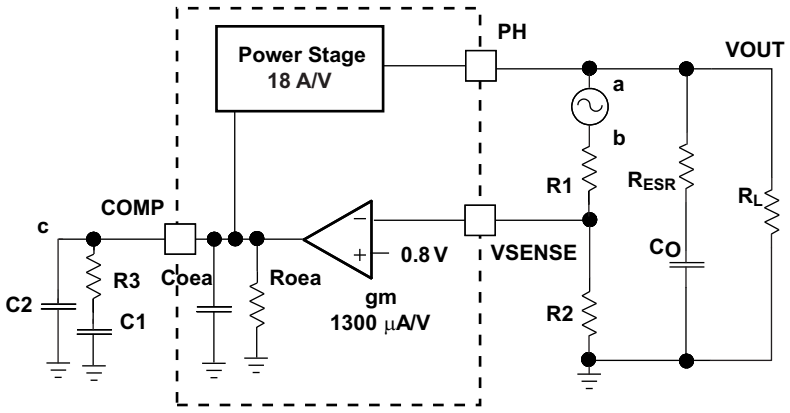


Figure 25. Small Signal Model for Loop Response

Simple Small Signal Model for Peak Current Mode Control

Figure 26 is a simple small signal model that can be used to understand how to design the frequency compensation. The device power stage can be approximated to a voltage controlled current source (duty cycle modulator) supplying current to the output capacitor and load resistor. The control to output transfer function is shown in Equation 13 and consists of a dc gain, one dominant pole and one ESR zero. The quotient of the change in switch current and the change in COMP pin voltage (node c in Figure 25) is the power stage transconductance (gm_{ps}) which is 18 A/V for the device. The DC gain of the power stage is the product of gm_{ps} and the load resistance R_L) as shown in Equation 14 with resistive loads. As the load current increases, the DC gain decreases. This variation with load may seem problematic at first glance, but fortunately the dominant pole moves with load current (see Equation 15). The combined effect is highlighted by the dashed line in Figure 27. As the load current decreases, the gain increases and the pole frequency lowers, keeping the 0-dB crossover frequency the same for the varying load conditions which makes it easier to design the frequency compensation.

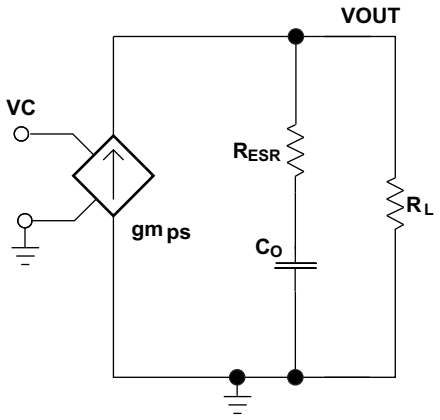


Figure 26. Simplified Small Signal Model for Peak Current Mode Control

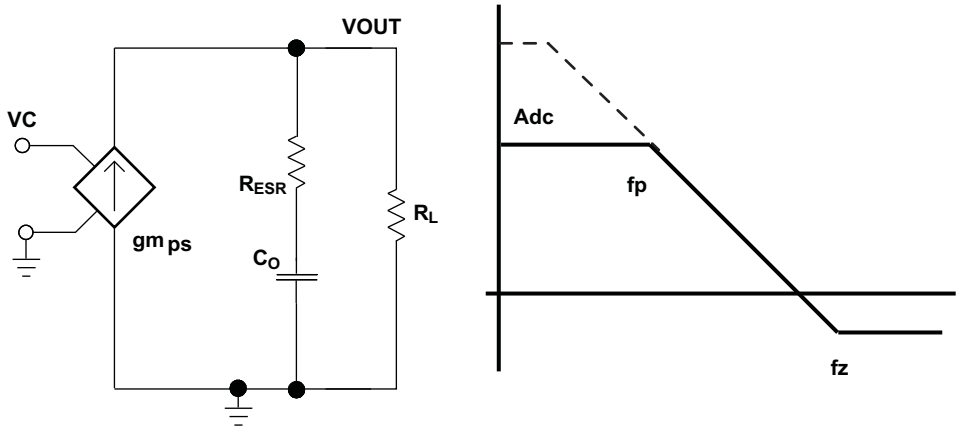


Figure 27. Simplified Frequency Response for Peak Current Mode Control

$$\frac{VOUT}{VC} = Adc \times \frac{\left(1+\frac{s}{2\pi \times fz}\right)}{\left(1+\frac{s}{2\pi \times fp}\right)} \quad (13)$$

$$Adc = gm_{ps} \times R_L \quad (14)$$

$$fp = \frac{1}{C_O \times R_L \times 2\pi} \quad (15)$$

$$fz = \frac{1}{C_O \times R_{ESR} \times 2\pi} \quad (16)$$

Where

gm_{ea} is the GM amplifier gain (1300 µA/V)
gm_{ps} is the power stage gain (18 A/V).
R_L is the load resistance
C_O is the output capacitance.
R_{ESR} is the equivalent series resistance of the output capacitor.

Small Signal Model for Frequency Compensation

The device uses a transconductance amplifier for the error amplifier and readily supports two of the commonly used frequency compensation circuits shown in Figure 28. In Type 2A, one additional high frequency pole is added to attenuate high frequency noise.

The design guideline below are provided for advanced users who prefer to compensate using the general method. The step-by-step design procedure described in the application section may also be used.

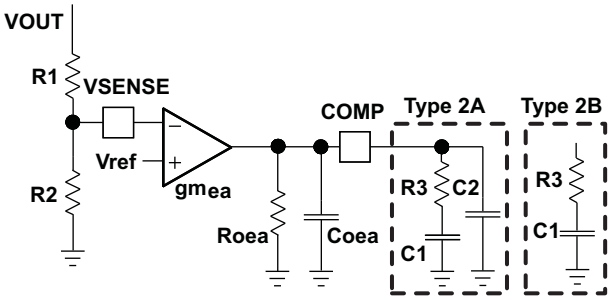


Figure 28. Types of Frequency Compensation

The general design guidelines for device loop compensation are as follows

1. Determine the crossover frequency fc. A good starting point is 1/10th of the switching frequency, f_{SW}.
2. R3 can be determined by

$$R3 = \frac{2\pi \times fc \times VOUT \times Co}{gm_{ea} \times Vref \times gm_{ps}} \quad (17)$$

   Where

   gm_{ea} is the GM amplifier gain (1300 µA/V)
   gm_{ps} is the power stage gain (18 A/V).
   Vref is the reference voltage (0.795 V)

3. Place a compensation zero at the dominant pole $\left(fp = \frac{1}{C_O \times R_L \times 2\pi} \right)$.
   C1 can be determined by

$$C1 = \frac{R_L \times Co}{R3} \quad (18)$$

4. C2 is optional. It can be used to cancel the zero from the ESR (Equivalent Series Resistance) of the output capacitor Co.

$$C2 = \frac{R_{ESR} \times Co}{R3} \quad (19)$$

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-1022101VSC	ACTIVE	CFP	HKH	20	1	TBD	AU	N / A for Pkg Type	-55 to 125	5962-1022101VS C TPS50601MHKHV	Samples
TPS50301SHKH	ACTIVE	CFP	HKH	20	1	TBD	AU	N / A for Pkg Type	-55 to 210	TPS50301SHKH	Samples
TPS50601MHKHV	ACTIVE	CFP	HKH	20	1	TBD	AU	N / A for Pkg Type	-55 to 125	5962-1022101VS C TPS50601MHKHV	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

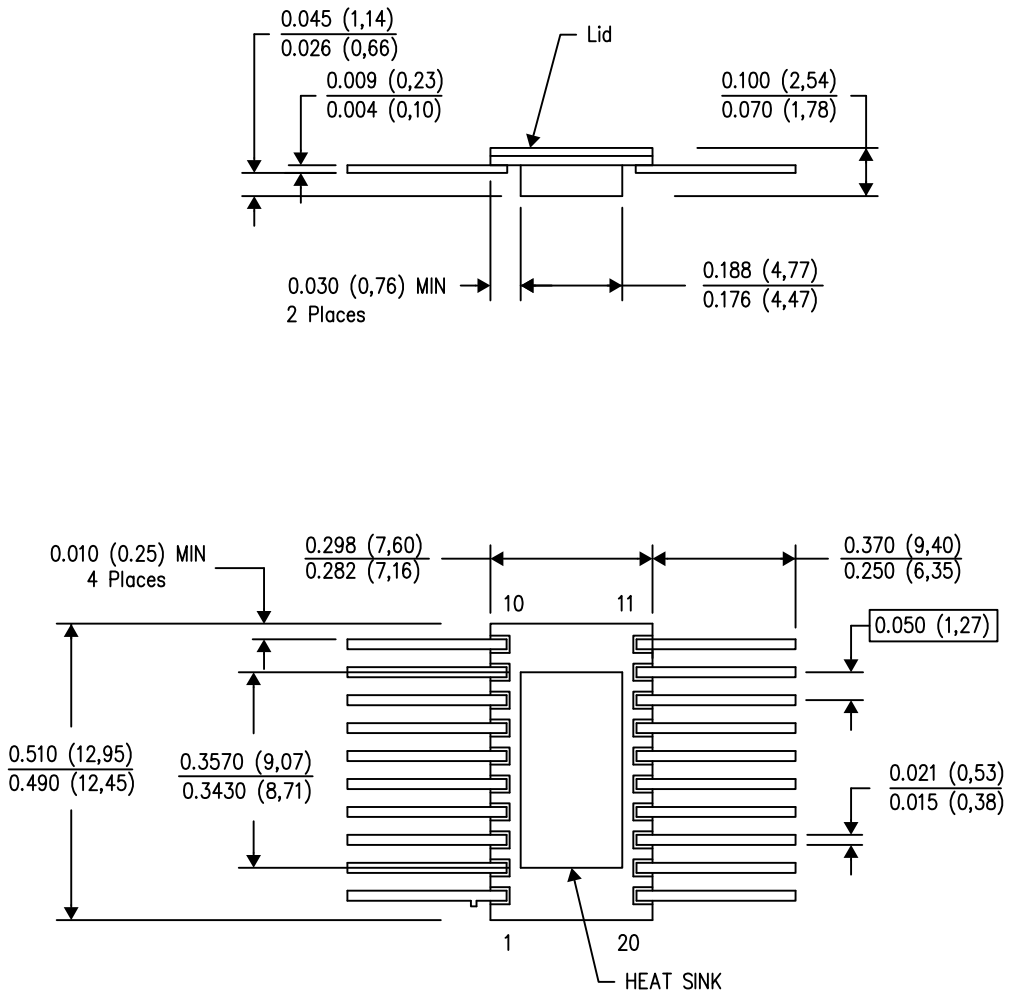
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

HKH (R–CDFP–F20) CERAMIC DUAL FLATPACK



4209648/B 12/12

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals will be gold plated.
E. Falls within MIL STD 1835 CDFP3–F20.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265