300-mA 40-V LOW-DROPOUT REGULATOR WITH 25-μA QUIESCENT CURRENT

Check for Samples: TPS7A6533-Q1, TPS7A6550-Q1

FEATURES

- **Low Dropout Voltage**
  - **300 mV at I_{OUT} = 150 mA**
- **4-V to 40-V Wide Input Voltage Range With up to 45-V Transients**
- **300-mA Maximum Output Current**
- **25-μA (Typ) Ultralow Quiescent Current at Light Loads**
- **3.3-V and 5-V Fixed Output Voltage With ±2% Tolerance**
- **Low-ESR Ceramic Output Stability Capacitor**
- **Integrated Fault Protection**
  - **Short-Circuit and Overcurrent Protection**
  - **Thermal Shutdown**
- **Low Input-Voltage Tracking**
- **Thermally Enhanced Power Package**
  - **3-Pin TO-252 (KVU /DPAK)**

APPLICATIONS

- **Qualified for Automotive Applications**
- **Infotainment Systems With Sleep Mode**
- **Body Control Modules**
- **Always-On Battery Applications**
  - **Gateway Applications**
  - **Remote Keyless Entry Systems**
  - **Immobilizers**

DESCRIPTION

The TPS7A65xx-Q1 is a family of low-dropout linear voltage regulators designed for low power consumption and quiescent current less than 25 μA in light-load applications. These devices feature integrated overcurrent protection and a design to achieve stable operation even with low-ESR ceramic output capacitors. A low-voltage tracking feature allows for a smaller input capacitor and can possibly eliminate the need of using a boost converter during cold crank conditions. Because of these features, these devices are well-suited in power supplies for various automotive applications.

TYPICAL REGULATOR STABILITY

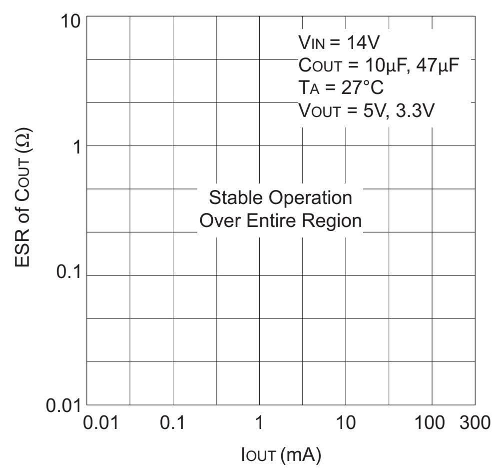


Figure 1. ESR versus Load Current for TPS7A6550-Q1

TYPICAL APPLICATION SCHEMATIC

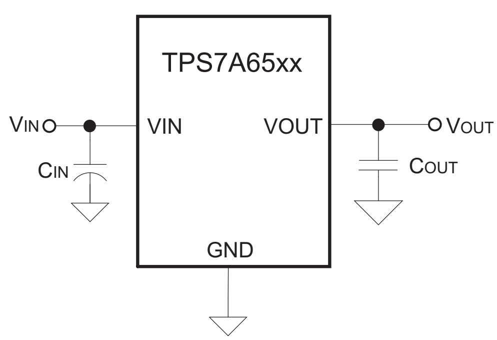


Figure 2. Application Schematic

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

OUTPUT VOLTAGE	PACKAGE		TOP-SIDE MARKING	ORDERABLE PART NUMBER
5 V	3-pin KVU	Tube of 70	7A6550Q1	TPS7A6550QKVUQ1
		Reel of 2500	7A6550Q1	TPS7A6550QKVURQ1
3.3 V	3-pin KVU	Reel of 2500	7A6533Q1	TPS7A6533QKVURQ1

(1) For the most-current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

NO.	DESCRIPTION		VALUE	UNIT
1.1	V_{IN}	Unregulated input(2)(3)	45	V
1.2	V_{OUT}	Regulated output	7	V
1.3	θ_{JP}	Thermal impedance junction to exposed pad KVU (DPAK) package	1.2	°C/W
1.4	θ_{JA}	Thermal impedance junction to ambient KVU (DPAK) package(4)	29.3	°C/W
1.5	θ_{JA}	Thermal impedance junction to ambient KVU (DPAK) package(5)	38.6	°C/W
1.6	ESD	Electrostatic discharge(6)	2	kV
1.7	T_A	Operating ambient temperature	125	°C
1.8	T_{stg}	Storage temperature range	–65 to 150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to GND.
(2) Absolute negative voltage on these pins not to go below –0.3 V.
(3) Absolute maximum voltage for duration less than 480 ms.
(4) The thermal data is based on JEDEC standard high-K profile – JESD 51-5. The copper pad is soldered to the thermal land pattern. Also correct attachment procedure must be incorporated.
(5) The thermal data is based on JEDEC standard low-K profile – JESD 51-3. The copper pad is soldered to the thermal land pattern. Also correct attachment procedure must be incorporated.
(6) The human-body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin.

DISSIPATION RATINGS

NO.	JEDEC STANDARD	PACKAGE	T_A < 25°C POWER RATING (W)	DERATING FACTOR ABOVE T_A = 25°C (°C/W)	T_A = 85°C POWER RATING (W)
2.1	JEDEC Standard PCB - low K, JESD 51-3	3 pin KVU	3.24	38.6	1.68
2.2	JEDEC Standard PCB - high K, JESD 51-5	3 pin KVU	4.27	29.3	2.22

RECOMMENDED OPERATING CONDITIONS

NO.	DESCRIPTION		MIN	MAX	UNIT
3.1	V_{IN}	Unregulated input voltage	4	40	V
3.2	T_J	Operating junction temperature range	–40	150	°C

ELECTRICAL CHARACTERISTICS

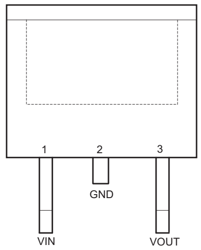
V_{IN} = 14V, T_J = –40ºC to 150ºC (unless otherwise noted)

NO.	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
4. Input Voltage (VIN pin)							
4.1	V_{IN}	Input voltage	Fixed 5-V output, I_{OUT} = 1 mA	5.3		40	V
			Fixed 3.3-V output, I_{OUT} = 1 mA	3.6		40	
4.2	$I_{QUIESCENT}$	Quiescent current	V_{IN} = 8.2 V to 18 V, I_{OUT} = 0.01 mA to 0.75 mA		25	40	µA
4.3	$V_{IN\text{-}UVLO}$	Undervoltage lockout voltage	Ramp V_{IN} down until output is turned OFF		3.16		V
4.4	$V_{IN(POWERUP)}$	Power-up voltage	Ramp V_{IN} up until output is turned ON		3.45		V
5. Regulated Output Voltage (VOUT pin)							
5.1	V_{OUT}	Regulated output voltage	Fixed V_{OUT} value (3.3 V or 5 V as applicable), I_{OUT} = 10 mA, 10 mA to 300 mA, V_{IN} = V_{OUT} + 1 V to 16 V	–2%		2%	
5.2	$\Delta V_{LINE\text{-}REG}$	Line regulation	V_{IN} = 6 V to 28 V, I_{OUT} = 10 mA, V_{OUT} = 5 V			15	mV
			V_{IN} = 6 V to 28 V, I_{OUT} = 10 mA, V_{OUT} = 3.3 V			20	mV
5.3	$\Delta V_{LOAD\text{-}REG}$	Load regulation	I_{OUT} = 10 mA to 300 mA, V_{IN}= 14 V, V_{OUT} = 5 V			25	mV
			I_{OUT} = 10 mA to 300 mA,V_{IN} = 14 V, V_{OUT} = 3.3 V			35	mV
5.4	$V_{DROPOUT}$ (1)	Dropout voltage (V_{IN} – V_{OUT})	I_{OUT} = 250 mA			500	mV
			I_{OUT} = 150 mA			300	mV
5.5	R_{SW} (2)	Switch resistance	VIN to VOUT resistance			2	Ω
5.6	I_{OUT}	Output current	V_{OUT} in regulation	0		300	mA
5.7	I_{CL}	Output current limit	V_{OUT} = 0 V (VOUT pin is shorted to ground)	350		1000	mA
5.8	PSRR (2)	Power-supply ripple rejection	$V_{IN\text{-}RIPPLE}$ = 0.5 Vpp, I_{OUT} = 300 mA, frequency = 100 Hz, V_{OUT} = 5 V, and V_{OUT} = 3.3 V		60		dB
			$V_{IN\text{-}RIPPLE}$ = 0.5 Vpp, I_{OUT} = 300 mA, frequency = 150 kHz, V_{OUT} = 5 V, and V_{OUT} = 3.3 V		30		
6. Operating Temperature Range							
6.1	T_J	Operating junction temperature		-40		150	ºC
6.2	$T_{SHUTDOWN}$	Thermal shutdown trip point			165		ºC
6.3	T_{HYST}	Thermal shutdown hysteresis			10		ºC

(1) This test is done with V_{OUT} in regulation and V_{IN} – V_{OUT} parameter is measured when V_{OUT} (3.3 V or 5 V) drops by 100 mV at specified loads.
(2) Specified by design – not tested

DEVICE INFORMATION

**KVU PACKAGE
(TOP VIEW)**



TERMINAL FUNCTIONS

NO.	NAME	TYPE	DESCRIPTION
1	VIN	I	Input voltage pin: The unregulated input voltage is supplied to this pin. A bypass capacitor is connected between VIN pin and GND pin to dampen input line transients.
2	GND	I/O	Ground pin: This is signal ground pin of the IC.
3	VOUT	O	Regulated output voltage pin: This is a regulated voltage output (V_{OUT} = 3.3 V or 5 V, as applicable) pin with a limitation on maximum output current. In order to achieve stable operation and prevent oscillation, an external output capacitor (C_{OUT}) with low ESR is connected between this pin and the GND pin.

FUNCTIONAL BLOCK DIAGRAM

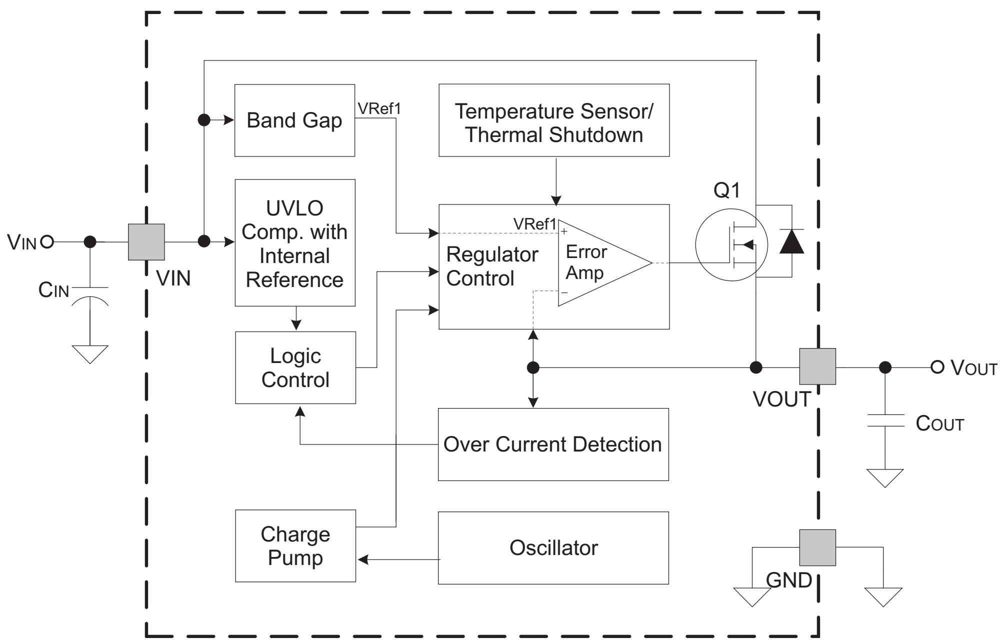
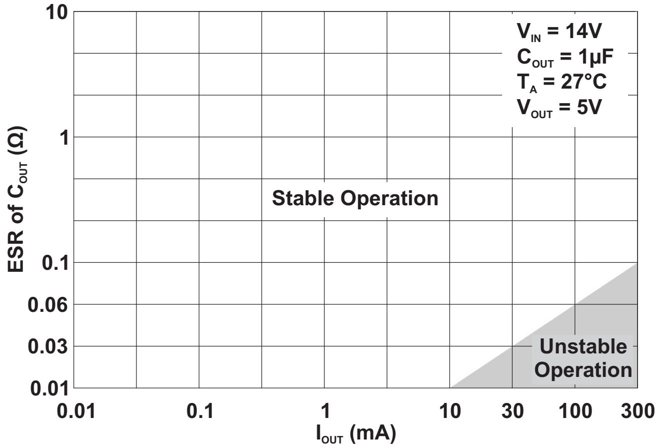


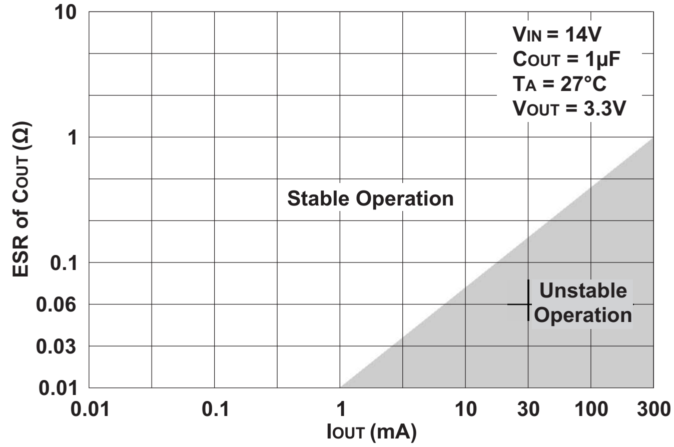
Figure 3. TPS7A65xx-Q1 Functional Block Diagram

TYPICAL CHARACTERISTICS

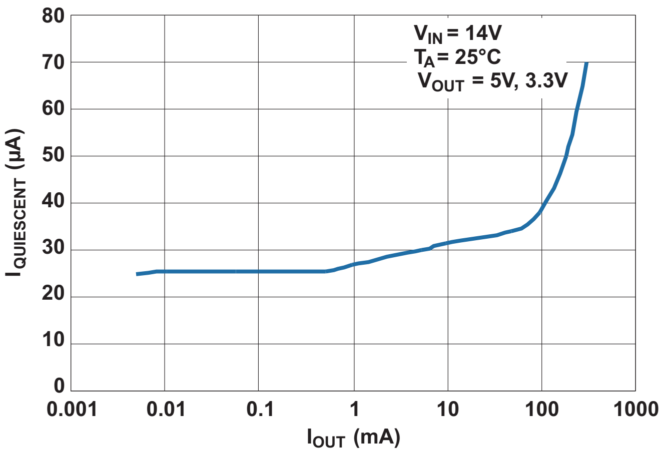
ESR vs LOAD CURRENT



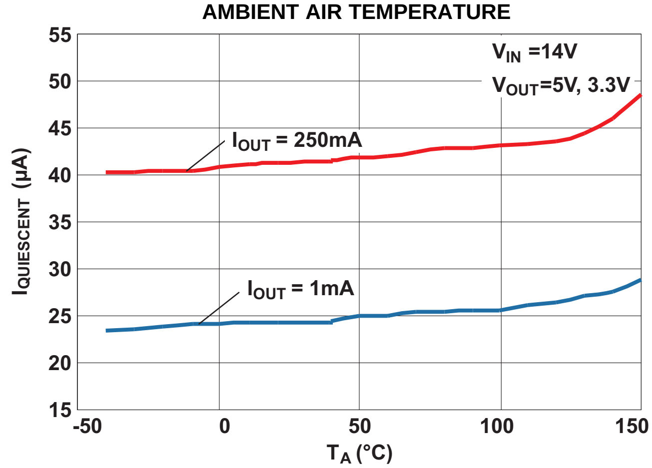
ESR vs LOAD CURRENT



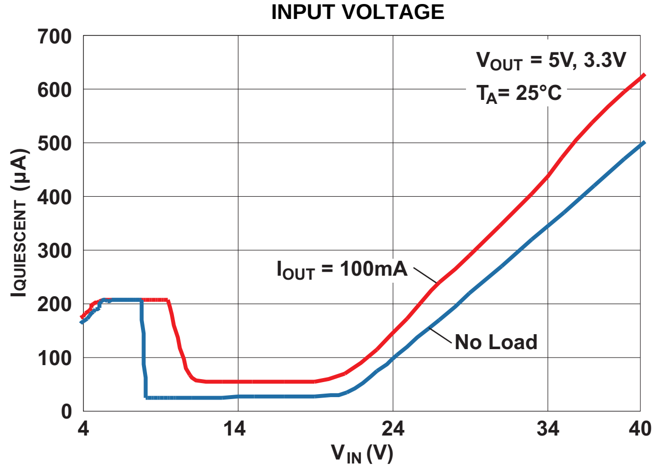
QUIESCENT CURRENT vs LOAD CURRENT



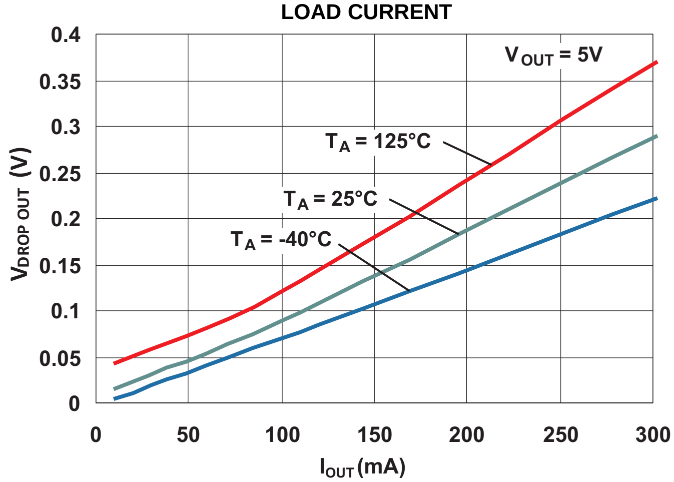
QUIESCENT CURRENT vs AMBIENT AIR TEMPERATURE



QUIESCENT CURRENT vs INPUT VOLTAGE



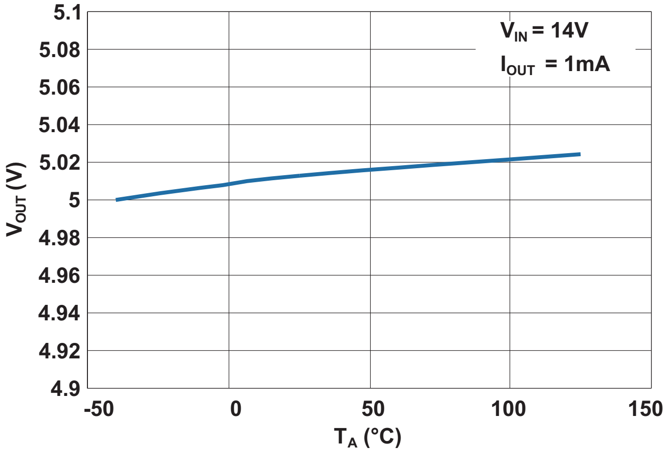
DROPOUT VOLTAGE (1) vs LOAD CURRENT



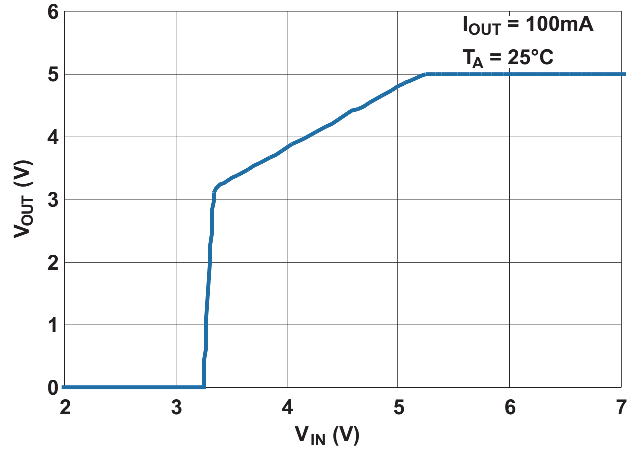
(1) Dropout voltage is measured when the output voltage drops by 100mV from the regulated output voltage level. (For example, the drop out voltage for TPS7A6550 is measured when the output voltage drops down to 4.9V from 5V.)

TYPICAL CHARACTERISTICS (continued)

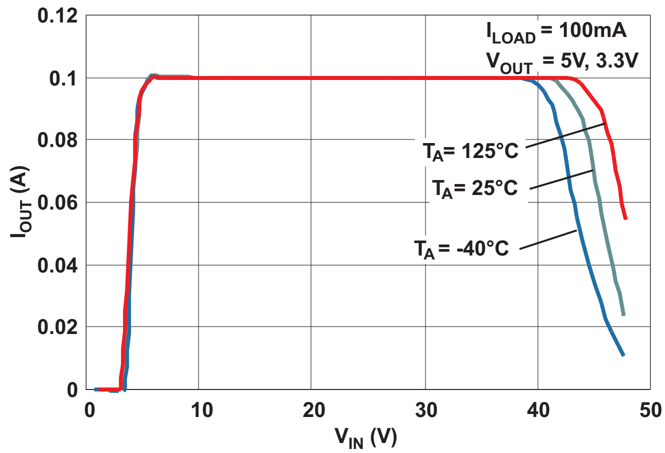
OUTPUT VOLTAGE vs AMBIENT AIR TEMPERATURE



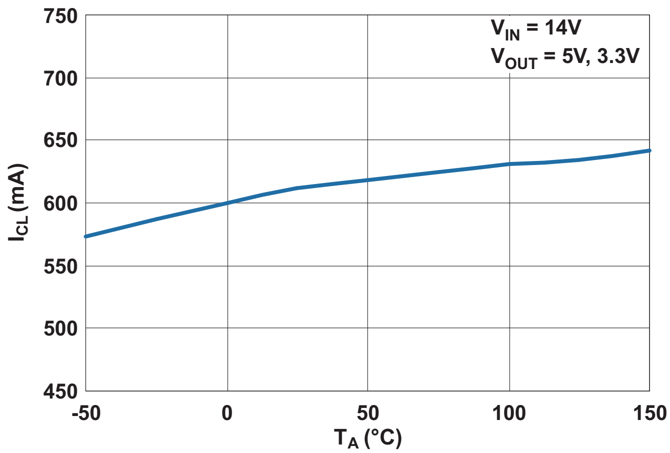
OUTPUT VOLTAGE vs INPUT VOLTAGE



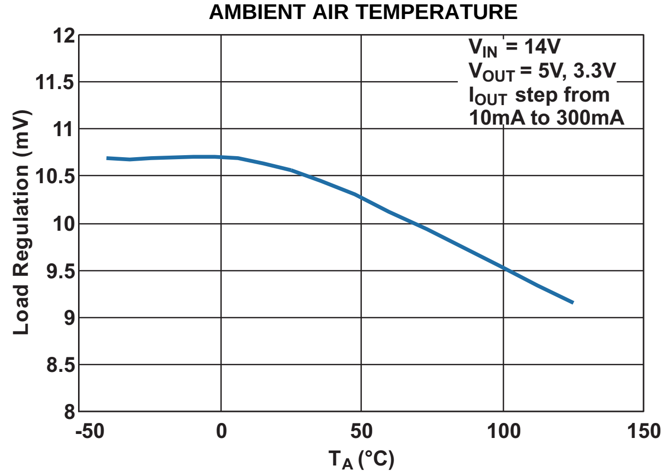
OUTPUT CURRENT vs INPUT VOLTAGE



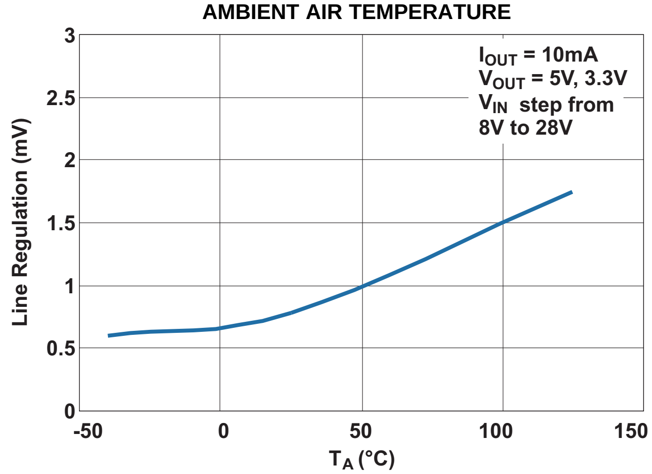
OUTPUT CURRENT LIMIT vs AMBIENT AIR TEMPERATURE



LOAD REGULATION vs AMBIENT AIR TEMPERATURE

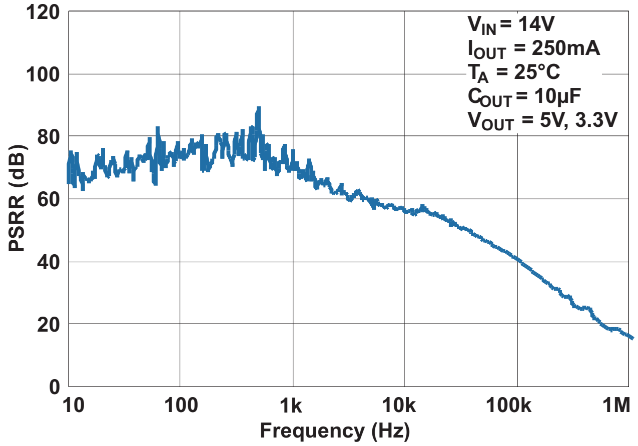


LINE REGULATION vs AMBIENT AIR TEMPERATURE

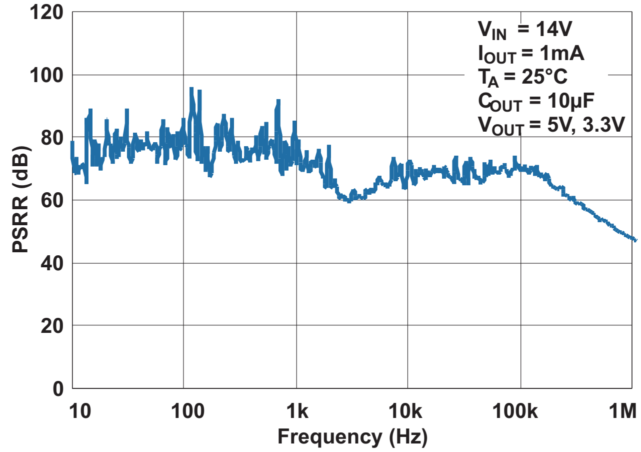


TYPICAL CHARACTERISTICS (continued)

PSRR AT HEAVY LOAD CURRENT



PSRR AT LIGHT LOAD CURRENT



DETAILED DESCRIPTION

TPS7A65xx-Q1 is a family of monolithic low-dropout linear voltage regulators designed for low power consumption and quiescent current less than 25 µA in light-load applications. Because of an integrated fault protection, these devices are well-suited in power supplies for various automotive applications.

These devices are available in two fixed-output-voltage versions as follows:

- 5-V output version (TPS7A6550-Q1)
- 3.3-V output version (TPS7A6533-Q1)

The following section describes the features of TPS7A65xx-Q1 voltage regulators in detail.

Power Up

During power up, the regulator incorporates a protection scheme to limit the current through the pass element and output capacitor. When the input voltage exceeds a certain threshold ($V_{IN(POWERUP)}$) level, the output voltage begins to ramp up; see Figure 4.

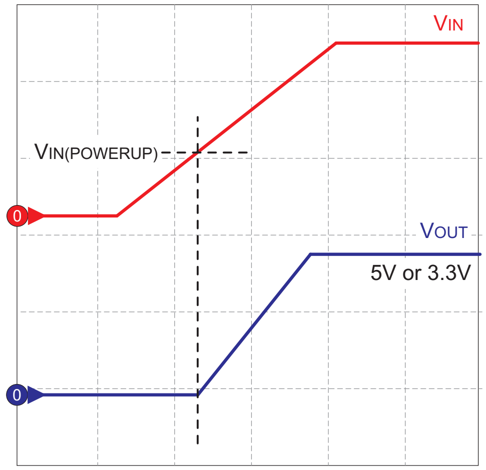


Figure 4. Power-Up Sequence

Charge-Pump Operation

These devices have an internal charge pump which turns on or off depending on the input voltage and the output current. The charge pump switching circuitry does not cause conducted emissions to exceed required thresholds on the input voltage line. For a given output current, the charge pump stays on at lower input voltages and turns off at higher input voltages. The charge-pump switching thresholds are hysteretic. Figure 5 and Figure 6 show typical switching thresholds for the charge pump at light (I_{OUT} < approximately 2 mA) and heavy (I_{OUT} > approximately 2 mA) loads, respectively.

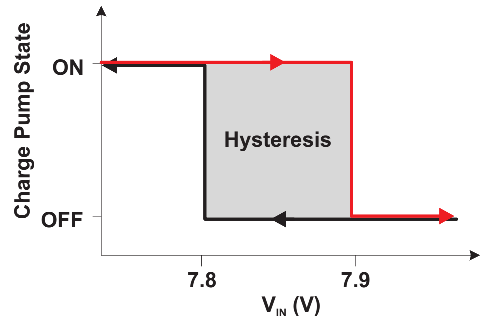


Figure 5. Charge-Pump Operation at Light Loads

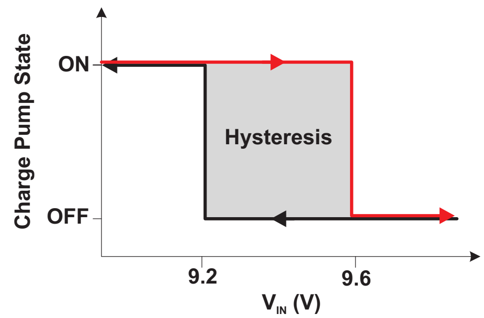


Figure 6. Charge-Pump Operation at Heavy Loads

Low-Power Mode

At light loads and high input voltages (V_{IN} > approximately 8 V such that charge pump is off) the device operates in the low-power mode and the quiescent current consumption decreases to 25 µA (typical) as shown in Table 1.

Table 1. Typical Quiescent Current Consumption

I_{OUT}	Charge Pump ON	Charge Pump OFF
I_{OUT} < approximately 2 mA (light load)	250 µA	25 µA (low-power mode)
I_{OUT} > approximately 2 mA (heavy load)	280 µA	70 µA

Undervoltage Shutdown

These devices have an integrated undervoltage lockout (UVLO) circuit to shut down the output if the input voltage (V_{IN}) falls below an internally fixed UVLO threshold level ($V_{IN\text{-}UVLO}$) as shown in Figure 7. This ensures that the regulator does not latch into an unknown state during low input-voltage conditions. The regulator normally powers up when the input voltage exceeds the $V_{IN(POWERUP)}$ threshold.

Low-Voltage Tracking

At low input voltages, the regulator drops out of regulation, and the output voltage tracks input minus a voltage based on the load current (I_{OUT}) and switch resistance (R_{SW}) as shown in Figure 7. This allows for a smaller input capacitor and can possibly eliminate the need of using a boost convertor during cold crank conditions.

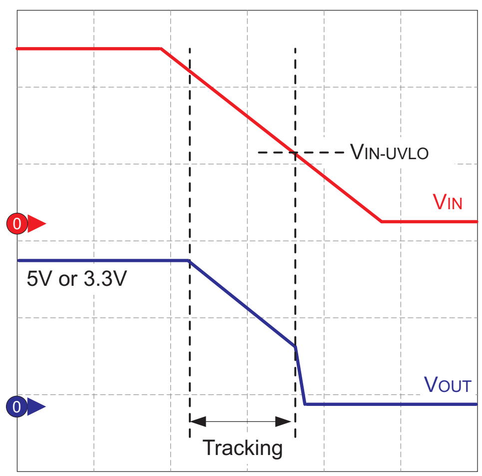


Figure 7. Undervoltage Shutdown and Low-Voltage Tracking

Integrated Fault Protection

These devices feature integrated fault protection to make them ideal for use in automotive applications. In order to keep them in a safe area of operation during certain fault conditions, they use internal current-limit protection and current-limit foldback to limit the maximum output current. This protects them from excessive power dissipation. For example, during a short-circuit condition on the output; limiting current through the pass element to I_{CL} protects the device from excessive power dissipation.

Thermal Shutdown

These devices incorporate a thermal shutdown (TSD) circuit as a protection from overheating. For continuous normal operation, the junction temperature should not exceed the TSD trip point. If the junction temperature exceeds the TSD trip point, the output turns off. When the junction temperature falls below the TSD trip point, the output turns on again. Figure 8 shows this.

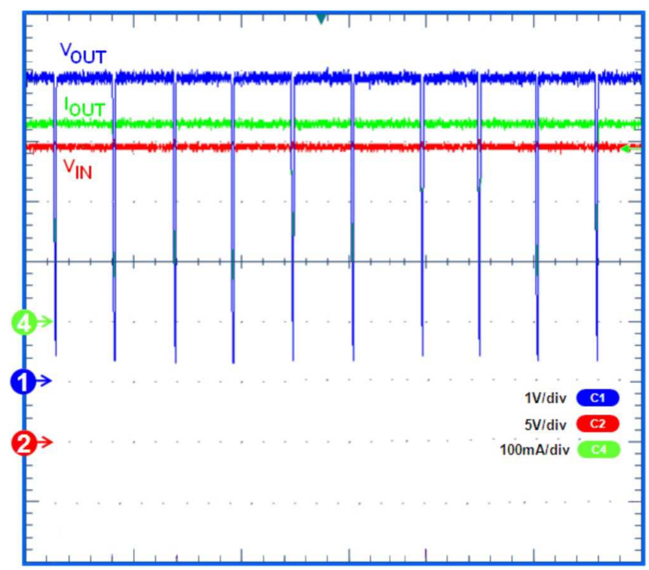


Figure 8. Thermal Cycling Waveform for TPS7A6550-Q1 (V_{IN} = 24 V, I_{OUT} = 300 mA, V_{OUT} = 5 V)

APPLICATION INFORMATION

A typical application circuit for TPS7A65xx-Q1 is Figure 9. Depending on the end application, one may use different values of external components. An application may require a larger output capacitor during fast load steps to prevent the output from temporarily dropping down. TI recommends a low-ESR ceramic capacitor with dielectric of type X5R or X7R. The user can additionally connect a bypass capacitor at the output to decouple high-frequency noise as per the end application.

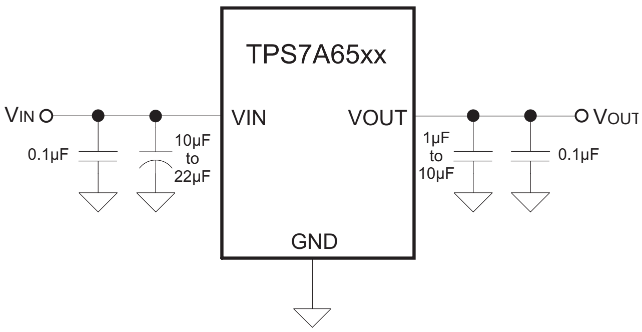


Figure 9. Typical Application Schematic

Power Dissipation and Thermal Considerations

Calculate the power dissipated in the device using Equation 1.

$$P_D = I_{OUT} \times (V_{IN} - V_{OUT}) + I_{QUIESCENT} \times V_{IN} \quad (1)$$

where,

P_D = continuous power dissipation
I_{OUT} = output current
V_{IN} = input voltage
V_{OUT} = output voltage
$I_{QUIESCENT}$ = quiescent current

$I_{QUIESCENT} << I_{OUT}$; therefore, ignore the term $I_{QUIESCENT} \times V_{IN}$ in Equation 1.

For a device under operation at a given ambient air temperature (T_A), calculate the junction temperature (T_J) using Equation 2.

$$T_J = T_A + (\theta_{JA} \times P_D) \quad (2)$$

where,

θ_{JA} = junction-to-ambient air thermal impedance

Calculate the rise in junction temperature due to power dissipation using Equation 3.

$$\Delta T = T_J - T_A = (\theta_{JA} \times P_D) \quad (3)$$

For a given maximum junction temperature ($T_{J\text{-}Max}$), calculate the maximum ambient air temperature ($T_{A\text{-}Max}$) at which the device can operate using Equation 4.

$$T_{A\text{-}Max} = T_{J\text{-}Max} - (\theta_{JA} \times P_D) \quad (4)$$

Example

If I_{OUT} = 100 mA, V_{OUT} = 5 V, V_{IN} = 14 V, $I_{QUIESCENT}$ = 250 µA and θ_{JA} = 30˚C/W, the continuous power dissipated in the device is 0.9 W. The rise in junction temperature due to power dissipation is 27˚C. For a maximum junction temperature of 150˚C, maximum ambient air temperature at which the device can operate is 123˚C.

For adequate heat dissipation, TI recommends soldering the power pad (exposed heat sink) to the thermal land pad on the PCB. Doing this provides a heat conduction path from the die to the PCB and reduces overall package thermal resistance. Figure 10 shows power derating curves for the TPS7A65xx-Q1 family of devices in the KVU (DPAK) package.

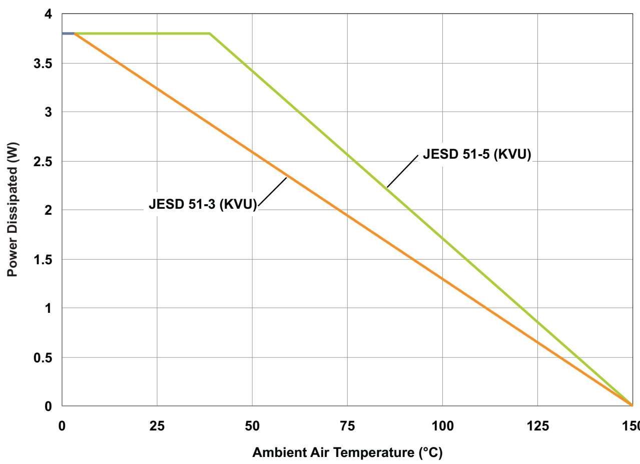


Figure 10. Power Derating Curves

For optimum thermal performance, TI recommends using a high-K PCB with thermal vias between the ground plane and solder pad or thermal land pad. Figure 11 (a) and (b) show this. Further, a design can improve the heat-spreading capabilities of a PCB considerably by using a thicker ground plane and a thermal land pad with a larger surface area.

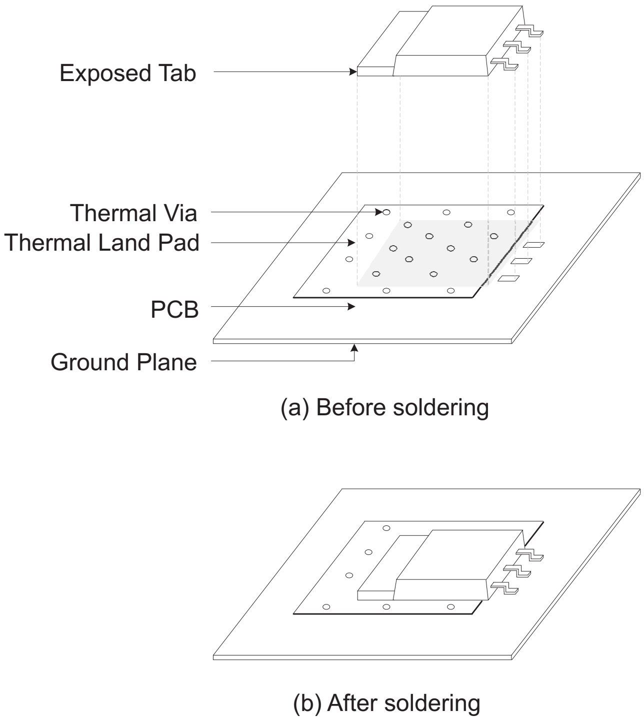


Figure 11. Using a Multilayer PCB and Thermal Vias For Adequate Heat Dissipation

Keeping other factors constant, the surface area of the thermal land pad contributes to heat dissipation only to a certain extent. Figure 12 shows the variation of θ_{JA} with surface area of the thermal land pad (soldered to the exposed pad) for the KVU package.

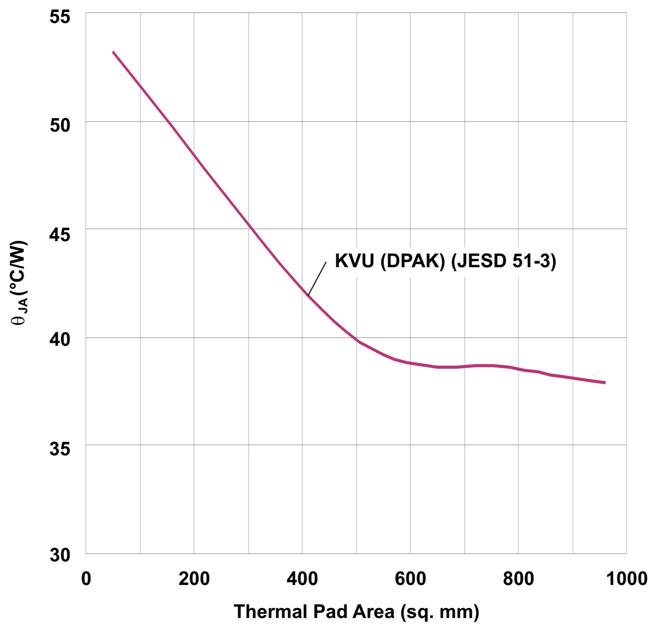


Figure 12. θ_{JA} versus Thermal Pad Area

REVISION HISTORY

Changes from Original (May 2010) to Revision A	Page
• Removed all KKT information.	2

Changes from Revision A (November 2011) to Revision B	Page
• Changed the θ_{JP} value in the Abs Max Table From: 12.7 To: 1.2°C/W	2

Changes from Revision B (November 2011) to Revision C	Page
• Deleted the TPS7A6533-Q1 device	1
• Changed the Regulated Output Voltage (5.1). Added to Test Conditions "10mA to 300mA, $V_{IN} = V_{OUT}$ + 1V to 16V"	3

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7A6533QKVURQ1	ACTIVE	TO-252	KVU	3	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	7A6533Q1	Samples
TPS7A6550QKVURQ1	ACTIVE	TO-252	KVU	3	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	7A6550Q1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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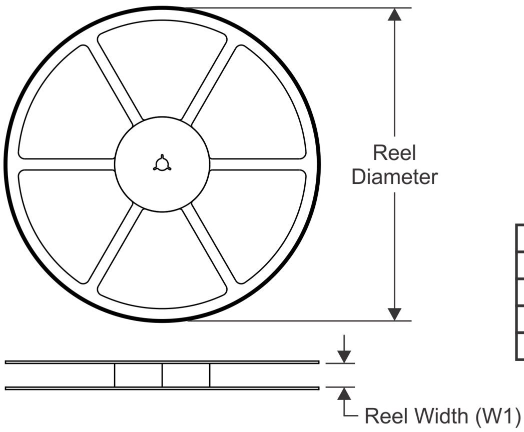
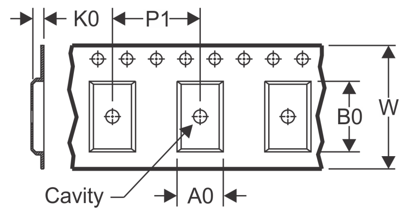
TAPE AND REEL INFORMATION

REEL DIMENSIONS

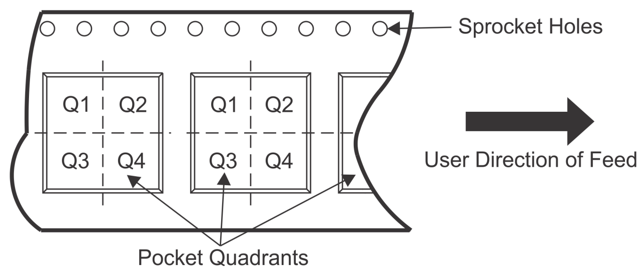


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

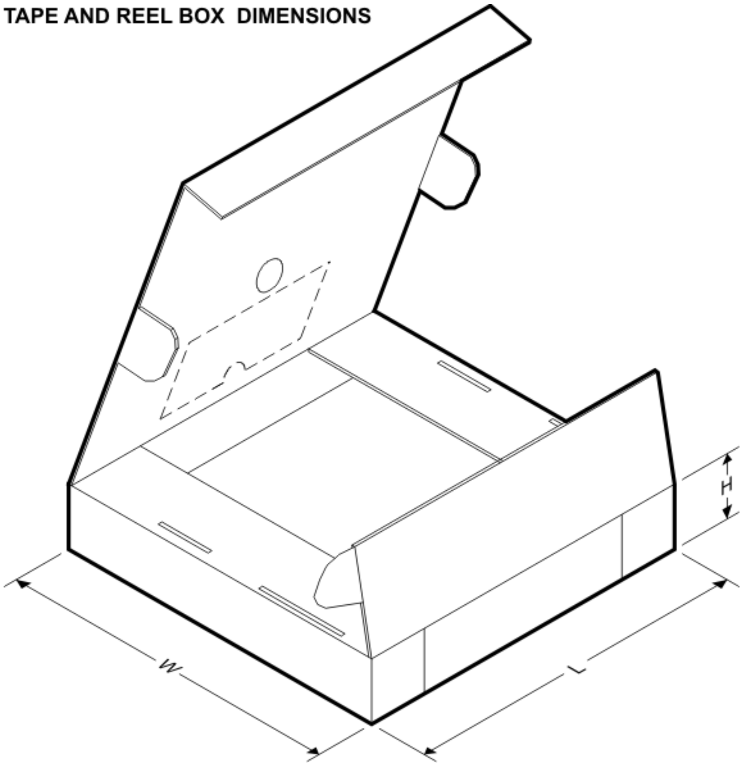
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A6533QKVURQ1	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TPS7A6550QKVURQ1	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2

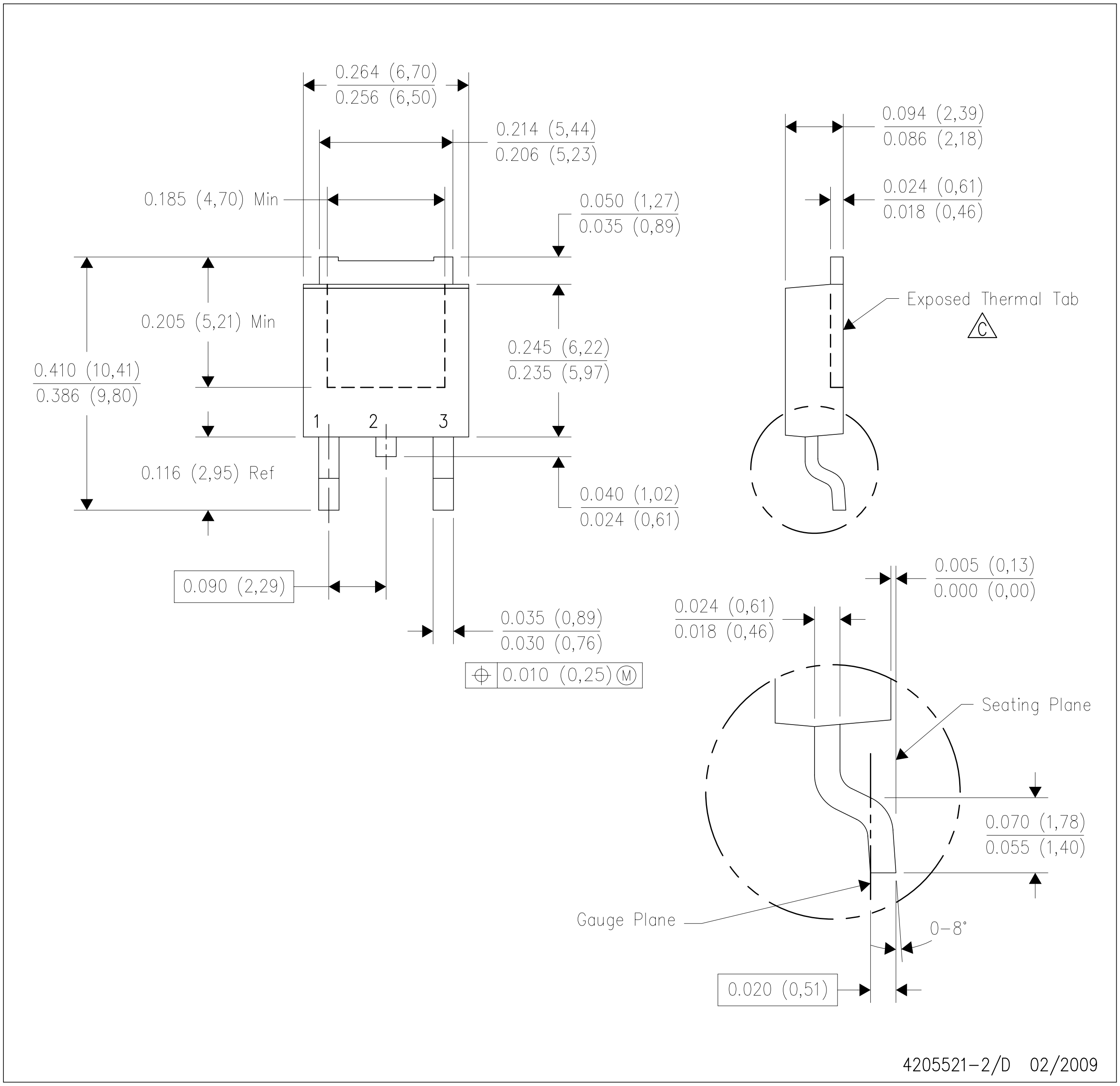
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

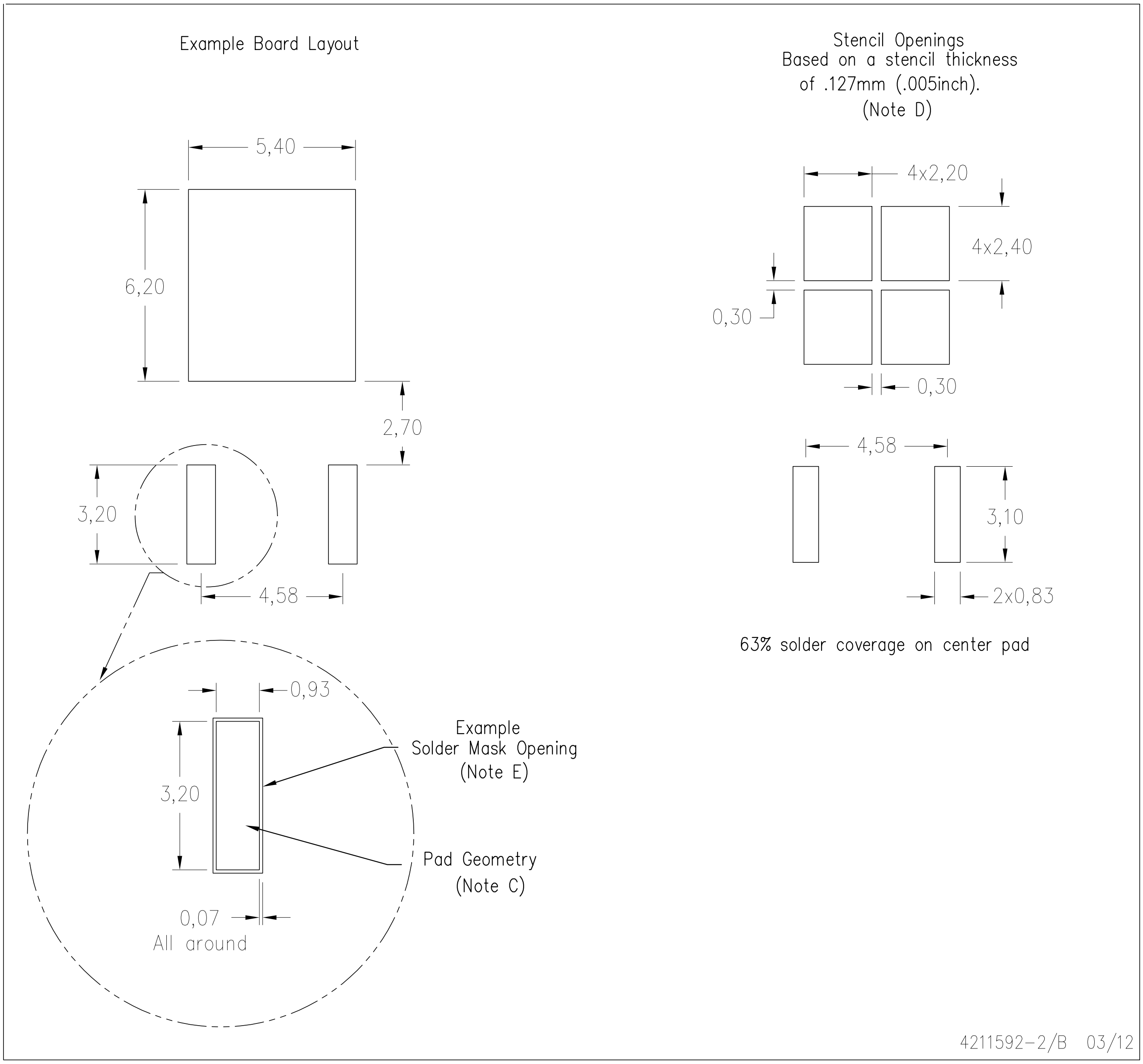
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A6533QKVURQ1	TO-252	KVU	3	2500	340.0	340.0	38.0
TPS7A6550QKVURQ1	TO-252	KVU	3	2500	340.0	340.0	38.0

KVU (R–PSFM–G3) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. The center lead is in electrical contact with the exposed thermal tab.
- D. Body Dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.006 (0,15) per side.
- E. Falls within JEDEC TO–252 variation AA.

KVU (R-PSFM-G3) PLASTIC FLANGE MOUNT PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-SM-782 is an alternate information source for PCB land pattern designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

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