0.8-V INPUT SYNCHRONOUS BOOST CONVERTER WITH 100-mA OUTPUT CURRENT

FEATURES

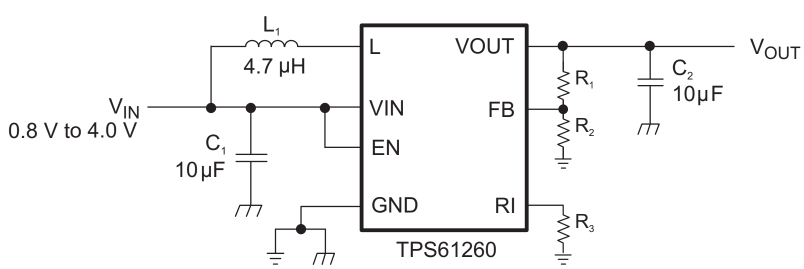
- **Up to 95% Efficiency**
- **100 mA Output Current at 3.3 V_{out} (VIN > 1 V)**
- **Input Voltage Range from 0.8 V to 4.0 V**
- **Fixed and Adjustable Output Voltage Options from 1.8 V to 4.0 V**
- **Programmable Average Output Current from 10 mA to 100 mA**
- **Adjustable Output Current Limit for Smallest Inductor**
- **Power Save Mode for Improved Efficiency at Low Output Power**
- **29 µA Quiescent Current**
- **Advanced Softstart**
- **Quasi Fixed Frequency Operation at 2.5 MHz**
- **Output Overvoltage Protection**
- **Load Disconnect During Shutdown**
- **Undervoltage Lockout**
- **Available in a 2 × 2 mm, 6-pin SON Package**

APPLICATIONS

- **All single or dual cell Alkaline, NiCd or NiMH Battery Powered Products**
- **High Output Impedance Battery (Coin Cells) Powered Products**
- **Personal Medical Products**
- **LED Driver**
- **Laser Pointer**
- **Wireless Headsets**
- **Industrial Metering Equipment**

DESCRIPTION

The TPS6126x devices provide a power supply solution for products powered by either single or dual cell alkaline, NiCd or NiMH batteries. Its unique advanced softstart makes it also suitable for products powered by high output impedance battery types, like coin cells. Output currents can go as high as 100 mA while using a single cell alkaline battery, and discharge it down to 0.8 V or lower. The boost converter is based on a quasi fixed frequency, pulse-width-modulation (PWM) controller using synchronous rectification to obtain maximum efficiency. At low load currents, the converter enters Power Save Mode to ensure high efficiency over a wide load current range. The maximum average current in the switches is limited to a programmable value which can go as high as 700 mA. The output voltage is programmable using an external resistor divider, or is fixed internally on the chip. In addition, the average output current can be programmed as well. The converter then regulates the programmed output voltage or the programmed output current, which ever demands lower output power. The converter can be disabled to minimize battery drain. During shutdown, the load is disconnected from the battery. The device is packaged in a 6-pin SON package measuring 2 × 2 mm (DRV).



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

AVAILABLE DEVICE OPTIONS[1]

T_A	OUTPUT VOLTAGE	PACKAGE MARKING	PACKAGE	PART NUMBER[2]
–40°C to 85°C	Adjustable	QWD	6-Pin SON	TPS61260DRV
	3.3 V	QWE		TPS61261DRV

(1) Contact the factory to check availability of other fixed output voltage versions.
(2) For detailed ordering information please check the PACKAGE OPTION ADDENDUM section at the end of this datasheet.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Voltage range[2]	VIN, L, VOUT, EN, FB	–0.3	5.0	V
	RI	–0.3	3.6	V
Temperature range	Operating junction, T_J	–40	150	°C
	Storage, T_{stg}	–65	150	°C
ESD rating[3]	Human Body Model - (HBM)		2	kV
	Charge Device Model - (CDM)		0.5	kV

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.
(2) All voltages are with respect to network ground terminal.
(3) ESD testing is performed according to the respective JESD22 JEDEC standard.

THERMAL INFORMATION

THERMAL METRIC[1]		TPS61260, TPS61261	UNITS
		DRV	
		6 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	89	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	100	
θ_{JB}	Junction-to-board thermal resistance	35	
ψ_{JT}	Junction-to-top characterization parameter	2	
ψ_{JB}	Junction-to-board characterization parameter	36	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Input Supply voltage at VIN	0.8		4.0	V
Operating free air temperature range, T_A	–40		85	°C
Operating junction temperature range, T_J	–40		125	°C

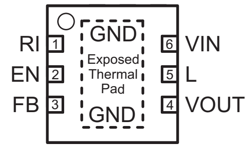
ELECTRICAL CHARACTERISTICS

over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC/DC STAGE						
V_{IN}	Input voltage range		0.8		4.0	V
V_{IN}	Minimum input voltage for startup				0.8	V
V_{OUT}	TPS61260 output voltage range		1.8		4.0	V
V_{FB}	TPS61260 feedback voltage	-40°C < T_J < 85°C	495	500	505	mV
V_{OUT}	TPS61261 output voltage		3.27	3.3	3.33	V
I_{LIM}	Average switch current limit			7 x I_{OUT}		mA
$R_{DS(on)}$	High side switch on resistance	V_{IN} = 1.2 V, V_{OUT} = 3.3 V		1000		mΩ
$R_{DS(on)}$	Low side switch on resistance	V_{IN} = 1.2 V, V_{OUT} = 3.3 V		250		mΩ
	Output voltage line regulation	PWM mode		0.5%		
	Output voltage load regulation	PWM mode		0.5%		
I_{OUT}	Average output current programming range		10		100	mA
	Average output current	R_I = 10 kΩ, T_A = 25 °C, V_{IN} < V_{OUT}	19	20	21	mA
	Average output current	R_I = 10 kΩ, 0°C < T_J < 60°C, V_{IN} < V_{OUT}	18	20	22	mA
	Average output current line regulation			0.5%		
	Average output current load regulation			0.5%		
I_Q	Quiescent current, VIN	I_O = 0 mA, V_{EN} = V_{IN} = 1.2 V, V_{OUT} = 3.3 V, Device not switching		4	7	μA
I_Q	Quiescent current, VOUT	I_O = 0 mA, V_{EN} = V_{IN} = 1.2 V, V_{OUT} = 3.3 V, Device not switching		25	40	μA
	TPS61261 FB pin input impedance	V_{EN} = HIGH		1		MΩ
I_{SD}	Shutdown current	V_{EN} = 0 V, V_{IN} = 1.2 V		0.1	1.5	μA
CONTROL STAGE						
V_{UVLO}	Under voltage lockout threshold	Falling V_{IN}	0.6	0.7	0.8	V
V_{UVLO}	Under voltage lockout threshold hysteresis			200		mV
V_{IL}	Low level input threshold voltage (EN)	V_{IN} ≤ 1.8 V, -40°C < T_J < 85°C			0.2 × V_{IN}	V
V_{IL}	Low level input threshold voltage (EN)	V_{IN} > 1.8 V, -40°C < T_J < 85°C			0.36	V
V_{IH}	High level input threshold voltage (EN)	V_{IN} ≤ 1.5 V	0.8 × V_{IN}			V
V_{IH}	High level input threshold voltage (EN)	V_{IN} > 1.5 V	1.2			V
I_{LKG}	Input leakage current (EN)	EN = GND or VIN		0.01	0.1	μA
V_{OVP}	Output overvoltage protection		4.0		4.5	V

PIN ASSIGNMENTS

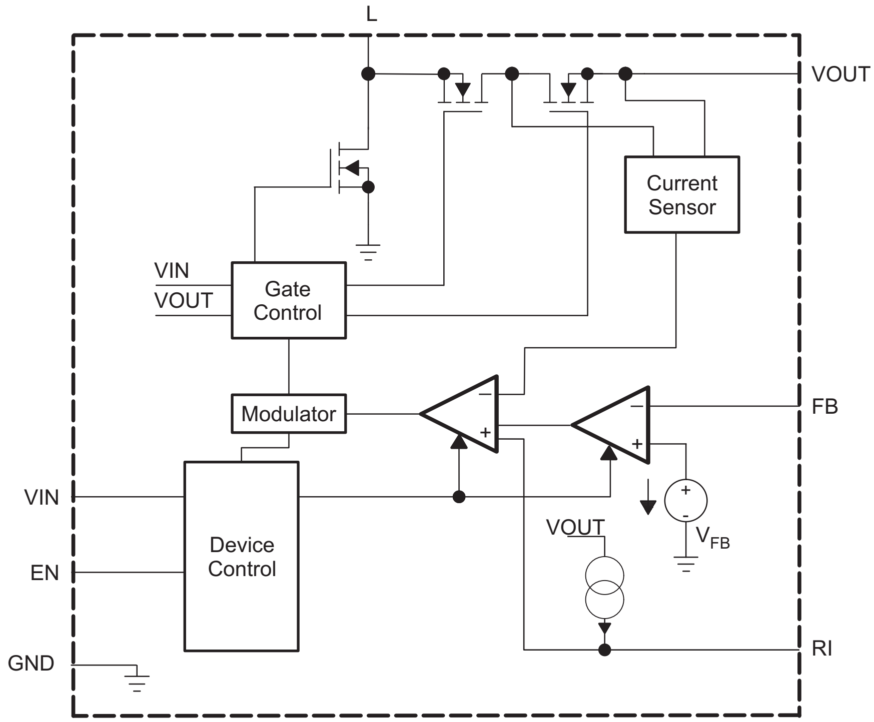
DRV PACKAGE
(TOP VIEW)



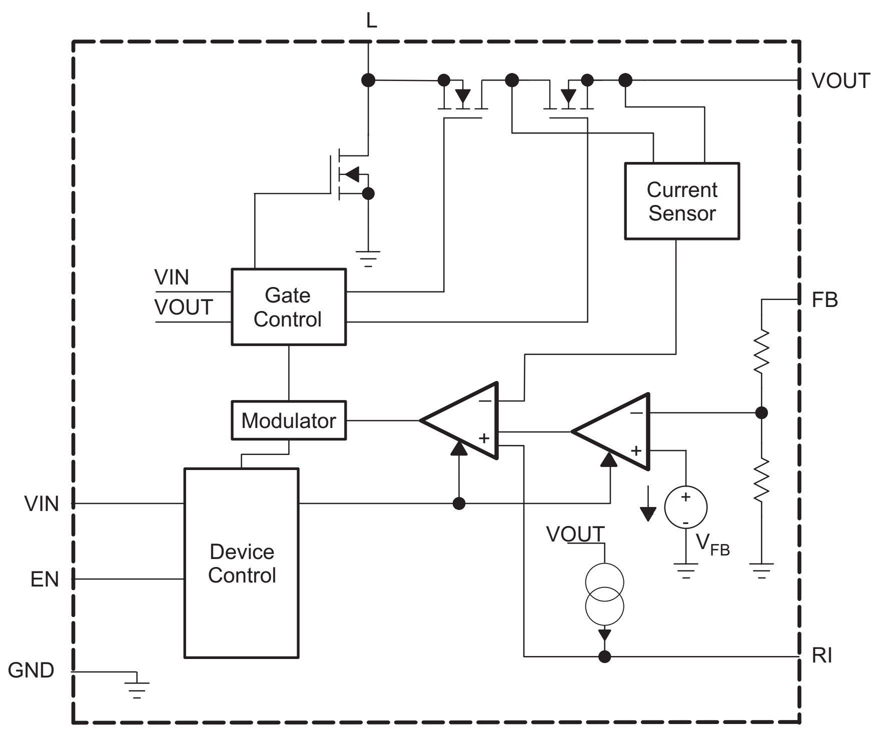
Pin Functions

PIN NAME	PIN NO.	I/O	DESCRIPTION
EN	2	I	Enable input. (High = enabled, Low = disabled). Do not leave floating.
FB	3	I	Voltage feedback of adjustable versions. Must be connected to VOUT on fixed output voltage versions.
L	5	I	Connection for Inductor
RI	1	I	Average output current programming input. A resistor with a value between 2 kΩ and 20 kΩ must be connected between the RI pin and GND.
VIN	6	I	Supply voltage for control stage
VOUT	4	O	Boost converter output
GND	Exposed Thermal Pad		Must be soldered to achieve appropriate power dissipation and mechanical reliability. Must be connected to GND.

FUNCTIONAL BLOCK DIAGRAM (TPS61260)



FUNCTIONAL BLOCK DIAGRAM (TPS61261)



TYPICAL CHARACTERISTICS

TABLE OF GRAPHS

DESCRIPTION		FIGURE
Maximum output current	vs Input voltage (TPS61260, VOUT = {1.8 V; 2.5 V; 4.0 V})	1
	vs Input voltage (TPS61261, VOUT = 3.3 V)	2
Efficiency	vs Output current (TPS61260, VOUT = {1.8 V; 2.5 V; 4.0 V})	3
	vs Output current (TPS61261, VOUT = 3.3 V)	4
	vs Input voltage (TPS61260, VOUT = 1.8 V, IOUT = {10; 20; 50 mA})	5
	vs Input voltage (TPS61260, VOUT = 2.5 V, IOUT = {10; 20; 50 mA})	6
	vs Input voltage (TPS61260, VOUT = 4.0 V, IOUT = {10; 20; 50; 100 mA})	7
	vs Input voltage (TPS61261, VOUT = 3.3V, IOUT = {10; 20; 50 mA})	8
Output current	vs Resistance at RI	9
Output voltage	vs Output current (TPS61260, VOUT = 1.8 V)	10
	vs Output current (TPS61260, VOUT = 2.5 V)	11
	vs Output current (TPS61260, VOUT = 4.0 V)	12
	vs Output current (TPS61261, VOUT = 3.3V)	13
Output current	vs Output voltage	14
Waveforms	Load transient response (TPS61261, Load change from 5 mA to 45 mA)	15
	Line transient response (TPS61261, Iout = 50 mA, VIN change from 1.0 V to 1.5 V)	16
	Startup after enable (TPS61261, VOUT = 3.3V, VIN = 1.2 V, Iout = 10 mA)	17
	Startup after enable (TPS61261, VOUT = 3.3V, VIN = 2.5 V, Iout = 10 mA)	18

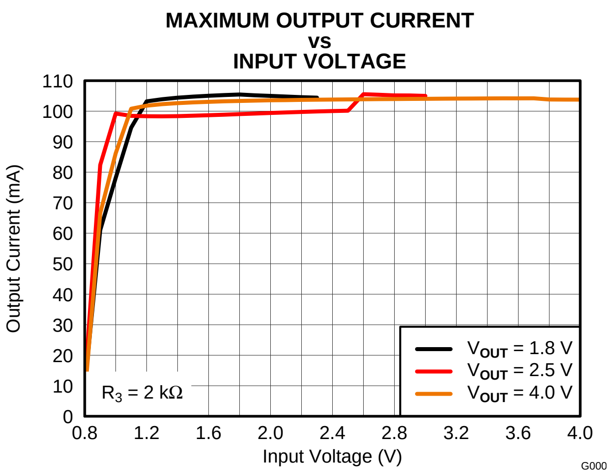


Figure 1.

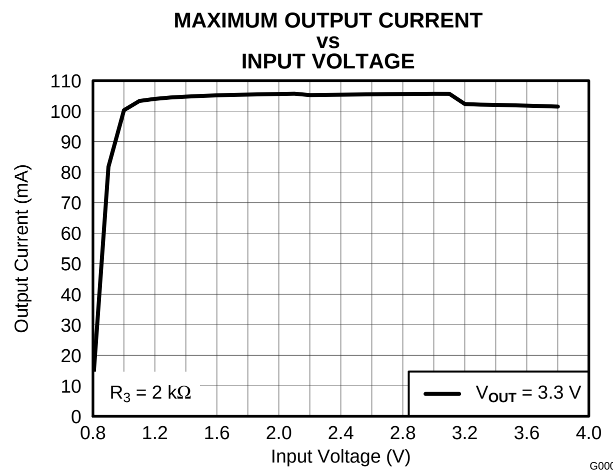


Figure 2.

EFFICIENCY vs OUTPUT CURRENT

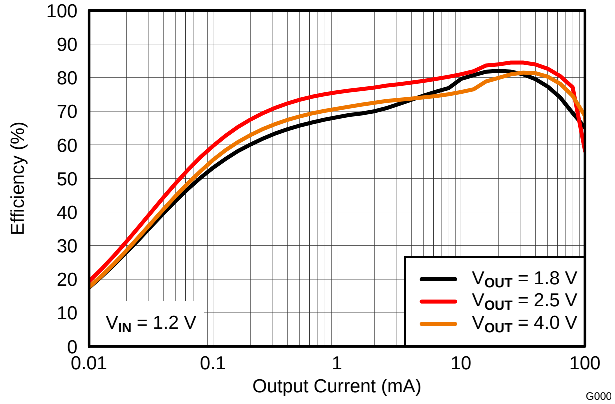


Figure 3.

EFFICIENCY vs OUTPUT CURRENT

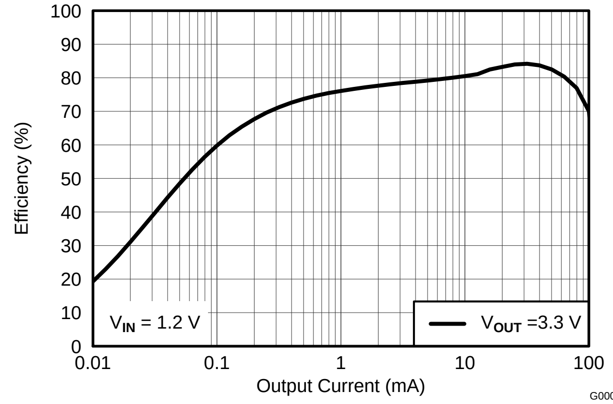


Figure 4.

EFFICIENCY vs INPUT VOLTAGE

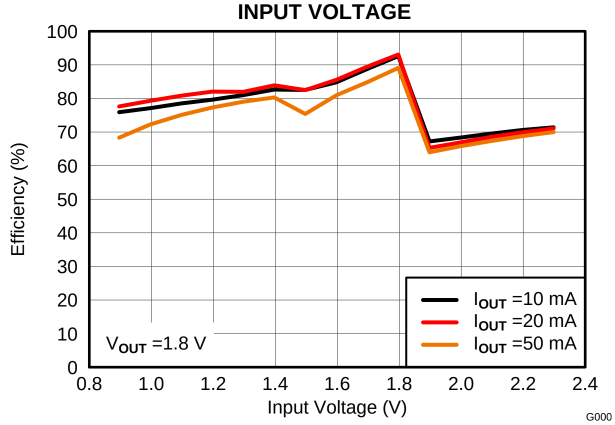


Figure 5.

EFFICIENCY vs INPUT VOLTAGE

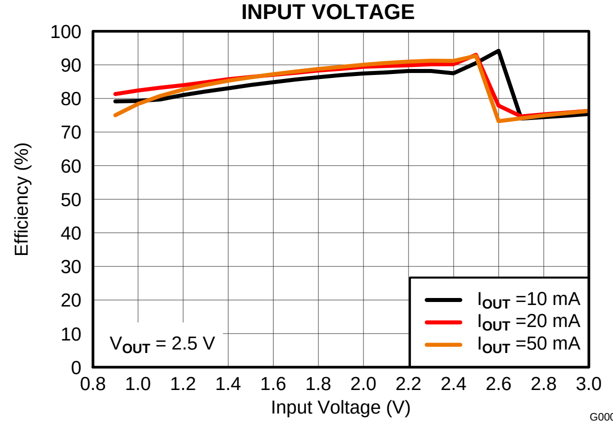


Figure 6.

EFFICIENCY vs INPUT VOLTAGE

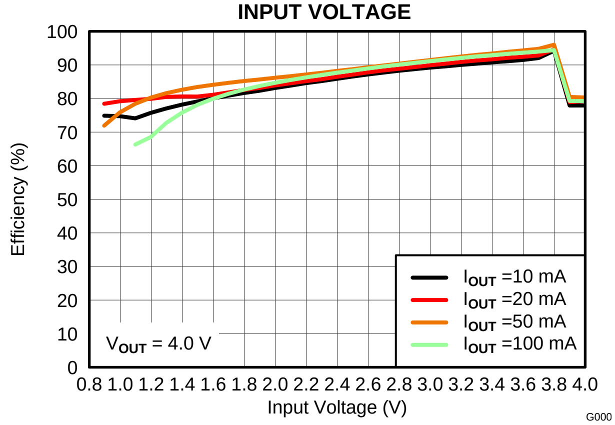


Figure 7.

EFFICIENCY vs INPUT VOLTAGE

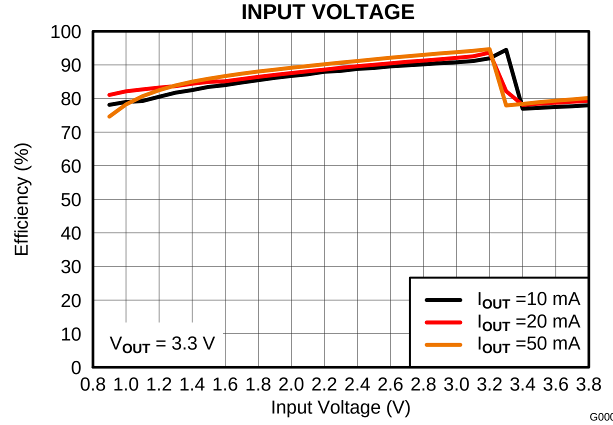


Figure 8.

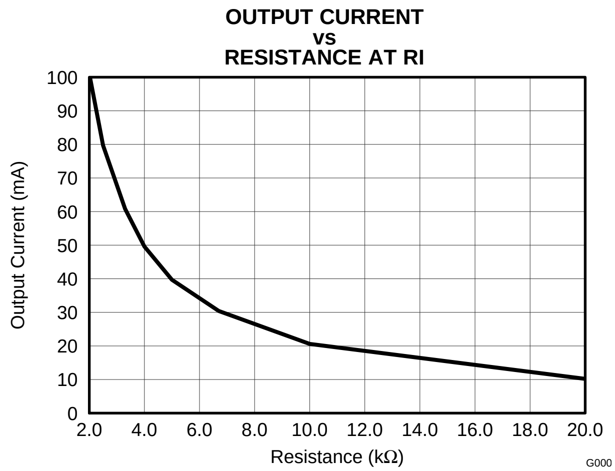


Figure 9.

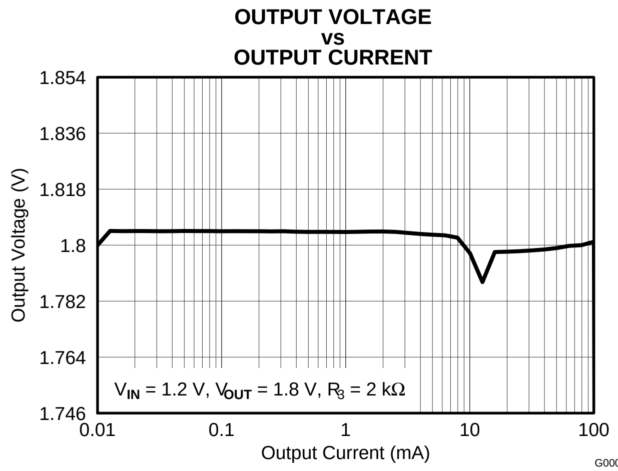


Figure 10.

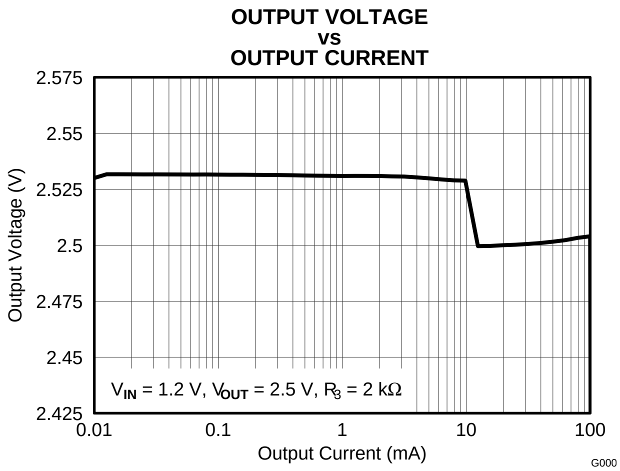


Figure 11.

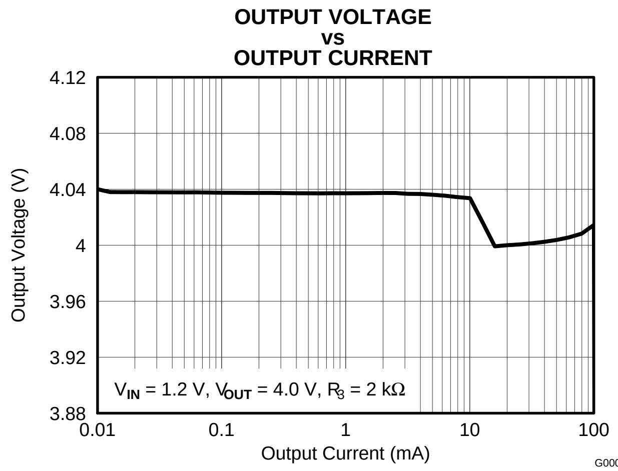


Figure 12.

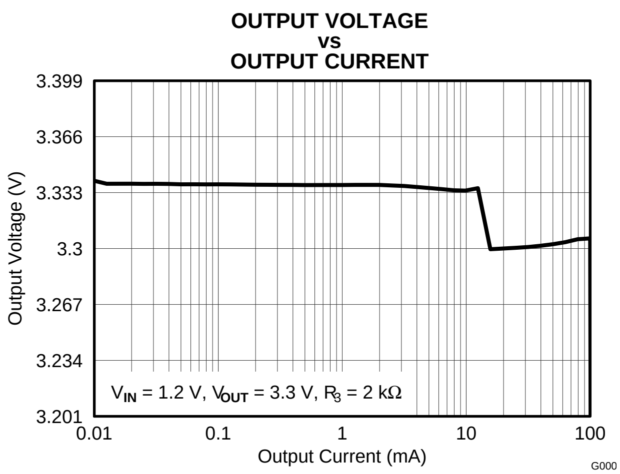


Figure 13.

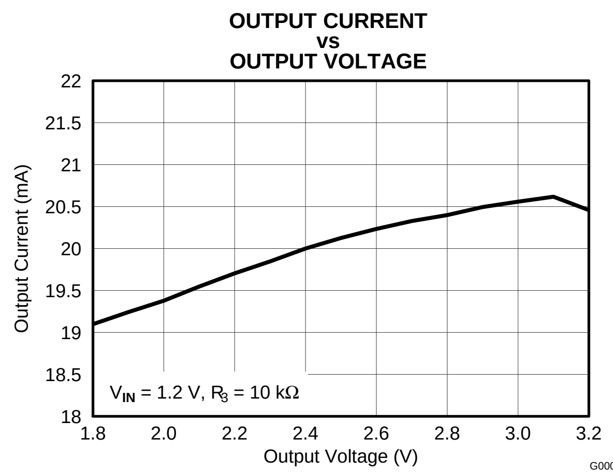
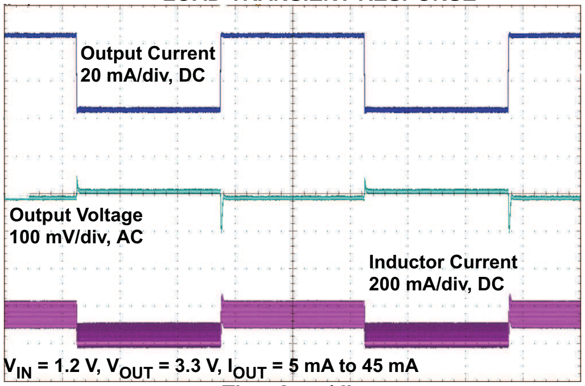


Figure 14.

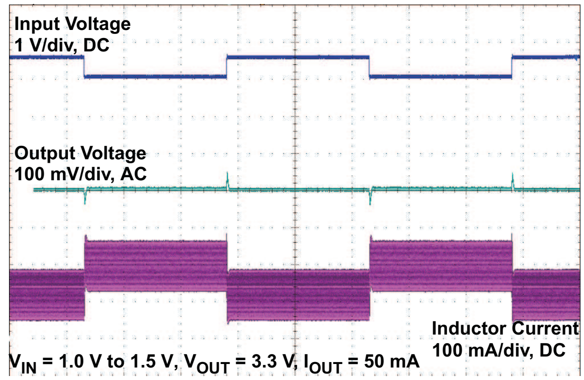
LOAD TRANSIENT RESPONSE



Time 2 ms/div

Figure 15.

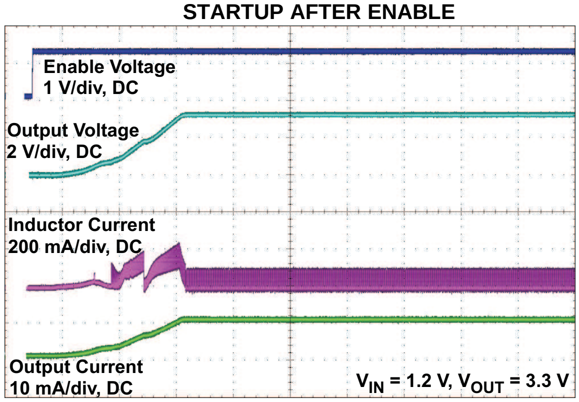
LINE TRANSIENT RESPONSE



Time 2 ms/div

Figure 16.

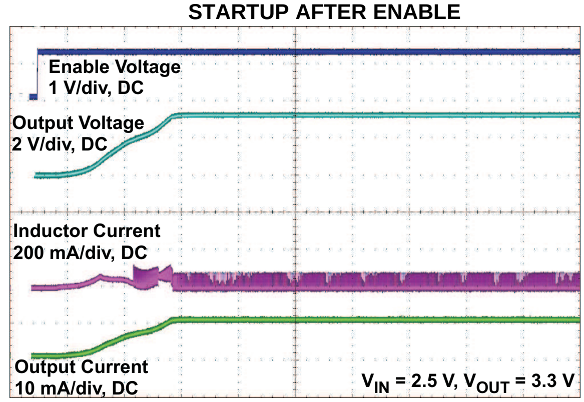
STARTUP AFTER ENABLE



Time 400 µs/div

Figure 17.

STARTUP AFTER ENABLE



Time 400 µs/div

Figure 18.

PARAMETER MEASUREMENT INFORMATION

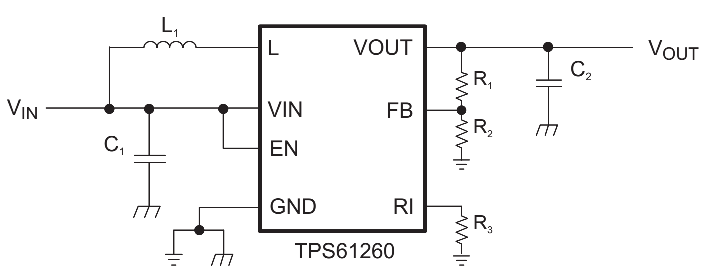


Table 1. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER
	TPS61260 / 1	Texas Instruments
L1	4.7 µH, 2.5 mm x 2 mm	LQM2HPN4R7MG0, Murata
C1	10 µF 6.3V, 0603, X5R ceramic	GRM188R60J106KME84D, Murata
C2	10 µF 6.3V, 0603, X5R ceramic	GRM188R60J106KME84D, Murata
R1	Depending on the output voltage at TPS61260. 0 Ω at TPS61261	
R2	Depending on the output voltage at TPS61260. Not used at TPS61261	
R3	Depending on the output current	

DETAILED DESCRIPTION

Controller Circuit

The controlling circuit of the device is based on a current mode topology. The inductor current is regulated by a fast current regulator loop which is controlled by either a voltage control loop or a reference current. The controller also uses input and output voltage feedforward. Changes of input and output voltage are monitored and immediately change the duty cycle in the modulator to achieve a fast response to those errors. The voltage error amplifier gets its feedback input from the FB pin. For the adjustable output voltage version, a resistive voltage divider must be connected to that pin. For the fixed output voltage version, the FB pin must be connected to the output voltage to directly sense the voltage. Fixed output voltage versions use a trimmed internal resistive divider. The feedback voltage is compared with the internal reference voltage to generate a stable and accurate output voltage. The reference current for average output current control is programmed with a resistor connected between the RI pin and GND.

The programming of the average output current also affects the maximum switch current in the main switch which basically is the input current. The lower the average output current is programmed, the lower the maximum input current is. Now, maximum input power is controlled as well as the maximum peak current to achieve a safe and stable operation under all possible conditions. Smaller inductors with lower saturation current ratings can be used, when lower average output currents are programmed.

Synchronous Boost Operation

The device uses 3 internal N-channel MOSFETs to maintain synchronous power conversion at all possible operating conditions. This enables the device to keep high efficiency over a wide input voltage and output power range. Using 2 rectifying switches also enables the device to control the output voltage and current during startup conditions when the input voltage is higher than the output voltage. During startup, the rectifying switch works in a linear mode until the output voltage is near the input voltage. Once in regulation, operating with input voltage greater than the output voltage may cause either the output voltage or current to exceed its regulation value. Though this operating point is not recommended, the device will not be damaged by this as long as absolute maximum ratings are not violated.

As opposed to a standard boost converter, the implemented 3 switch topology enables the output to be disconnected from the input during device shutdown when disabled. Current does not flow from output to input or from input to output.

Power Save Mode

At normal load conditions with continuous inductor current, the device operates at a quasi fixed frequency. If the load gets lower, the inductor current decreases and becomes discontinuous. If this happens and the load is further decreased, the device lowers the switching frequency and turns off parts of the control to minimize internal power consumption. The output voltage is controlled by a low power comparator at a level about 1% higher than the nominal output voltage. If the output voltage reaches the nominal value or drops below it, the device control is turned on again to handle the new load condition. The boundary between power save mode and PWM mode is when the inductor current becomes discontinuous.

Accurate average output current regulation requires continuous inductor current. This means that there is no power save mode during current regulation.

Device Enable

The device is put into operation, when EN is set high. It is put into a shutdown mode, when EN is set to GND. In shutdown mode, the regulator stops switching, all internal control circuitry is switched off, and the load is disconnected from the input. This means that the output voltage can drop below the input voltage during shutdown.

Softstart and Short Circuit Protection

During startup of the converter, the duty cycle and the peak current are limited in order to avoid high peak currents flowing from the input. After being enabled, the device starts operating. Until the output voltage reaches about 0.4 V, the average output current ramps up from zero to the programmed value, as the output voltage increases. As soon as the output current has reached the programmed value, it stays regulated at that value until the load conditions demand less current. This typically happens when the output capacitor is charged and the output voltage is regulated.

During startup, the device can seamlessly change modes of operation. When the input voltage is higher than the output voltage, the device operates in a linear mode using the rectifying switches for control. If the input voltage is lower than the output voltage it operates in a standard boost conversion mode. The boost conversion is non-synchronous when the output voltage is below approximately 1.8 V and it is synchronous if the output voltage is higher than approximately 1.8 V.

At short circuit conditions at the output, the output current is limited to the programmed average current. If the short at the output causes the output voltage to drop below 0.4 V, the average current decreases approximately linearly with the output voltage down to zero.

The device can monotonically start into a pre-bias on the output.

Undervoltage Lockout

An undervoltage lockout function prevents device startup if the supply voltage on VIN is lower than the undervoltage lockout threshold defined in the ELECTRICAL CHARACTERISTICS table. When in operation, the device automatically shuts down the power stage if the voltage on VIN drops below the undervoltage lockout threshold. The device automatically restarts if the input voltage recovers to the minimum operating input voltage.

Output Overvoltage Protection

If, for any reason, the output voltage of the device (as measured at the VOUT pin) exceeds its maximum recommended value, the device stops operating. It continues operating as soon as the output voltage has dropped below this threshold.

APPLICATION INFORMATION

PROGRAMMING THE OUTPUT VOLTAGE

Within the TPS6126x family, there are fixed and adjustable output voltage versions available. To properly configure the fixed output voltage devices, the FB pin is used to sense the output voltage. This means that it must be connected directly to VOUT. For the adjustable output voltage version, an external resistor divider is used to adjust the output voltage. The resistor divider must be connected between the VOUT, FB and GND pins. When the output voltage is regulated properly, the typical value of the voltage at the FB pin is 500 mV. The maximum recommended value for the output voltage is 4.0 V. The current through the resistive divider should be about 100 times greater than the current into the FB pin. The typical current into the FB pin is 0.01 µA, and the voltage across the resistor between the FB and GND pins, R_2, is typically 500 mV. Based on these two values, the recommended value for R2 should be lower than 500 kΩ, in order to set the divider current at 1 µA or higher. It is also recommended to keep the total value for the resistor divider, **R1 + R2**, in the range of 1 MΩ. From that, the value of the resistor connected between VOUT and FB, R1, depending on the needed output voltage (V_{OUT}), can be calculated using Equation 1:

$$R1 = R2 \cdot \left(\frac{V_{OUT}}{V_{FB}} - 1 \right) \quad (1)$$

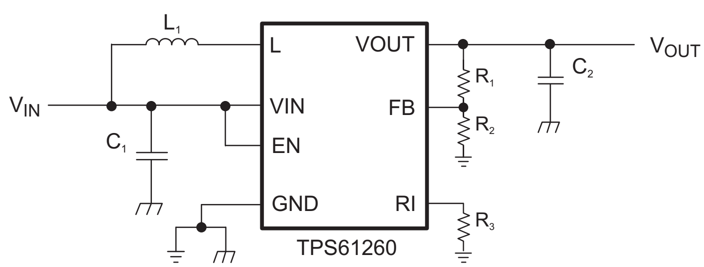


Figure 19. Typical Application Circuit for Adjustable Output Voltage Option

PROGRAMMING THE OUTPUT CURRENT

The devices of the TPS6126x family also support average output current regulation. An external resistor is used to program the average output current. The resistor must be connected between the RI and GND pins. When the average output current is regulated properly, the typical value of the voltage at the RI pin is 400 mV. The maximum recommended value for the regulated average output current is 100 mA. The value of the resistor R3 should be between 2 kΩ and 20 kΩ. It can be calculated, depending on the needed average output current (I_{OUT}), using Equation 2:

$$R3 = \frac{200V}{I_{OUT}} \quad (2)$$

Accurate regulation of the average output current only is possible if the inductor current is continuous. Please check the INDUCTOR SELECTION section to calculate the required parameters for selecting an appropriate inductor.

INDUCTOR SELECTION

To properly configure the TPS6126x devices, an inductor must be connected between the VIN pin and the L pin. To estimate the minimum inductance value for accurate average output current regulation, Equation 3 is used.

$$L_{MIN} = \frac{V_{IN}^2 \cdot \left(V_{OUT} - V_{IN}\right)}{V_{OUT}^2 \cdot I_{OUT}} \cdot 0.2 \cdot \mu s \quad (3)$$

In Equation 3, the minimum inductance value required for accurate average output current regulation is calculated. V_{IN} is the input voltage. For typical applications which require voltage regulation, the recommended inductor value is 4.7 µH. Applications with higher inductance values have lower light load efficiency. The recommended range for the inductor value is from 2.2 µH up to 22 µH. The current rating required for this inductor is I_{LIM} and depends on the programmed output current I_{OUT}. Please refer to the ELECTRICAL CHARACTERISTICS table. Table 2 contains a list of inductors recommended for the TPS6126x:

Table 2. List of Inductors

VENDOR	INDUCTOR SERIES
Murata	LQM2HP_G0
Toko	DFE252012C
Hitachi Metals	KSLI-252010AG

CAPACITOR SELECTION

Input Capacitor

At least a 4.7-µF input capacitor is recommended to improve transient behavior of the regulator and EMI behavior of the total power supply circuit. An X5R or X7R ceramic capacitor placed as close as possible to the VIN and GND pins of the IC is recommended.

Output Capacitor

For the output capacitor, use of a small X5R or X7R ceramic capacitor placed as close as possible to the VOUT and GND pins of the IC is recommended. If, for any reason, the application requires the use of large capacitors which can not be placed close to the IC, use a smaller ceramic capacitor in parallel to the large capacitor. The small capacitor should be placed as close as possible to the VOUT and GND pins of the IC.

The output capacitor should be at least 2.2 µF. There are no additional requirements regarding minimum ESR. There is also no theoretical upper limit for the output capacitance value. The device has been tested with capacitors up to 100 µF. In general, larger capacitors cause lower output voltage ripple as well as lower output voltage drop during load transients. To improve control performance, especially when using high output capacitance values, a feedforward capacitor in parallel to R1 is recommended. The value should be in the range of the value calculated in Equation 4:

$$C_{ff} = 0.3 \cdot \Omega \cdot \frac{C2}{R2} \tag{4}$$

LAYOUT CONSIDERATIONS

For all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground tracks. The input capacitor, output capacitor, and the inductor should be placed as close as possible to the IC. Use a common ground node for power ground and a different one for control ground to minimize the effects of ground noise. Connect these ground nodes at any place close to the ground pin of the IC.

The feedback divider should be placed as close as possible to the control ground connection. To lay out the control ground, short traces are recommended as well, separated from the power ground traces. This avoids ground shift problems, which can occur due to superimposition of power ground current and control ground current. See Figure 20 for the recommended layout:

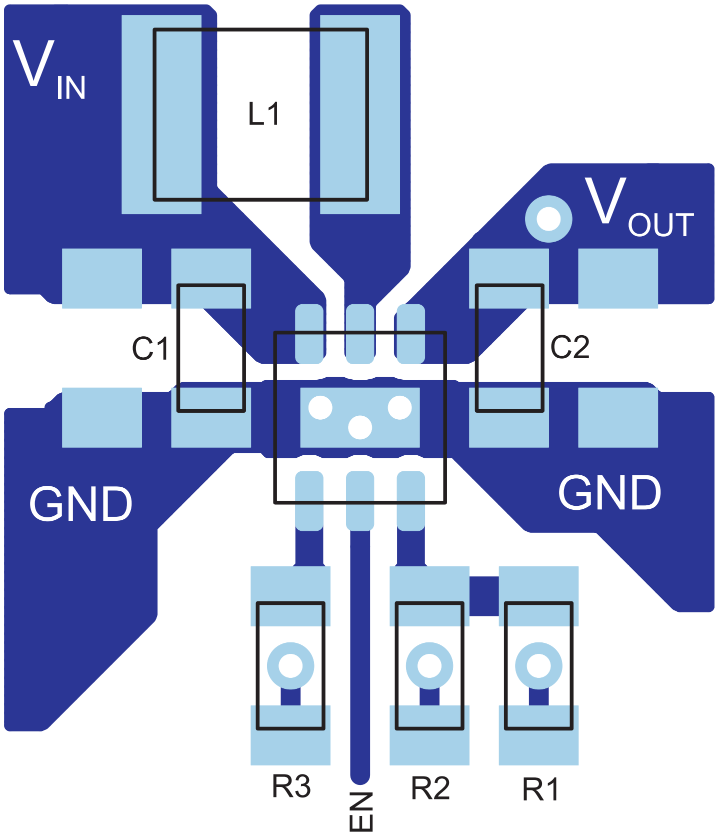


Figure 20. PCB Layout Suggestion

THERMAL INFORMATION

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below.

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB by soldering the Exposed Thermal Pad
- Introducing airflow in the system

For more details on how to use the thermal parameters in the dissipation ratings table, please check the Thermal Characteristics Application Note (SZZA017) and the IC Package Thermal Metrics Application Note (SPRA953).

APPLICATION EXAMPLE AS LED DRIVER

Figure 21 shows the TPS61261 configured to drive an LED with analog and/or PWM dimming. This circuit does not require an external current sensing resistor and so provides high efficiency, as shown in Figure 22. See SLVA562 for details. This design is available as the TPS61261EVM-208.

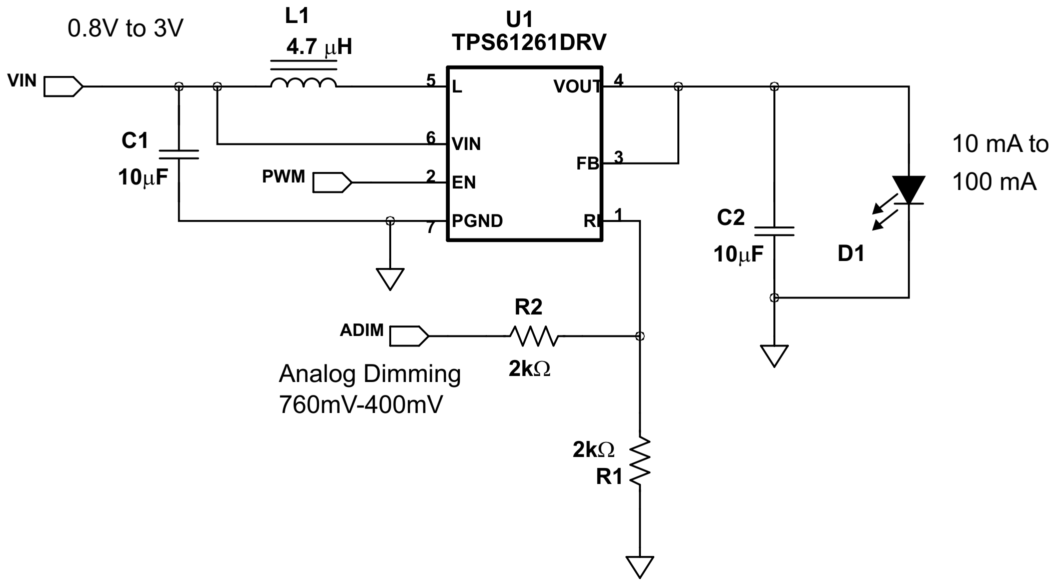


Figure 21. LED Driver

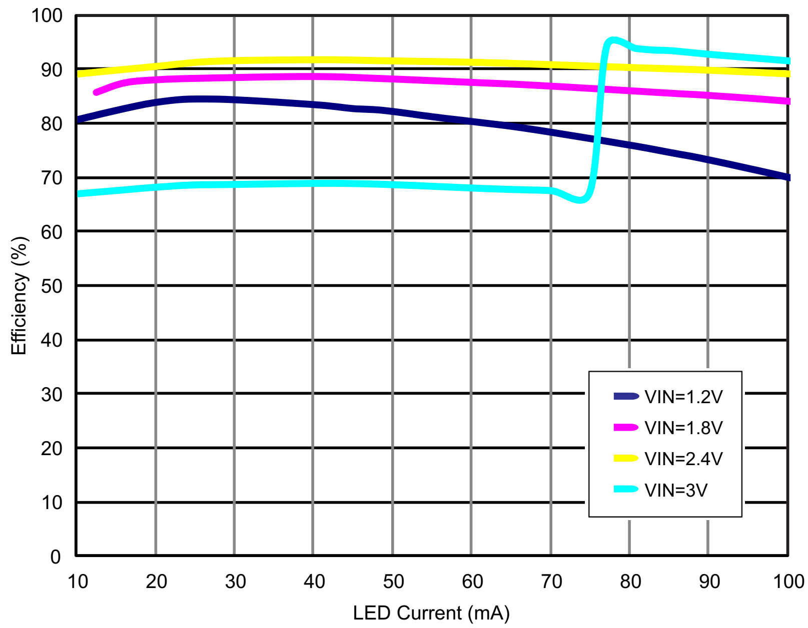


Figure 22. LED Driver Efficiency

REVISION HISTORY

Changes from Original (May 2011) to Revision A **Page**

- Changed Synchronous Boost Operation section 10
- Deleted Dynamic Current Limit section 10
- Changed PowerPAD™ to Exposed Thermal Pad 14
- Added APPLICATION EXAMPLE AS LED DRIVER 14

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS61260DRVR	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	QWD	Samples
TPS61260DRVT	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	QWD	Samples
TPS61261DRVR	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	QWE	Samples
TPS61261DRVT	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	QWE	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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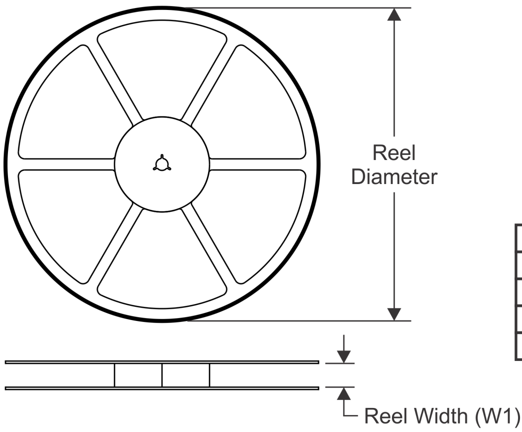
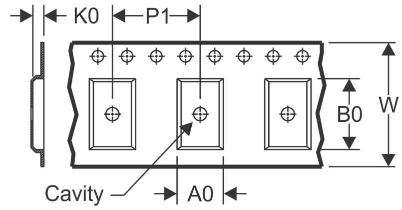
TAPE AND REEL INFORMATION

REEL DIMENSIONS

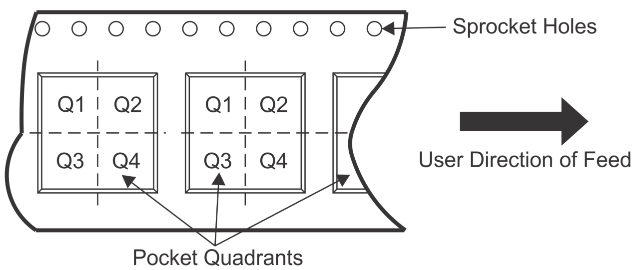


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

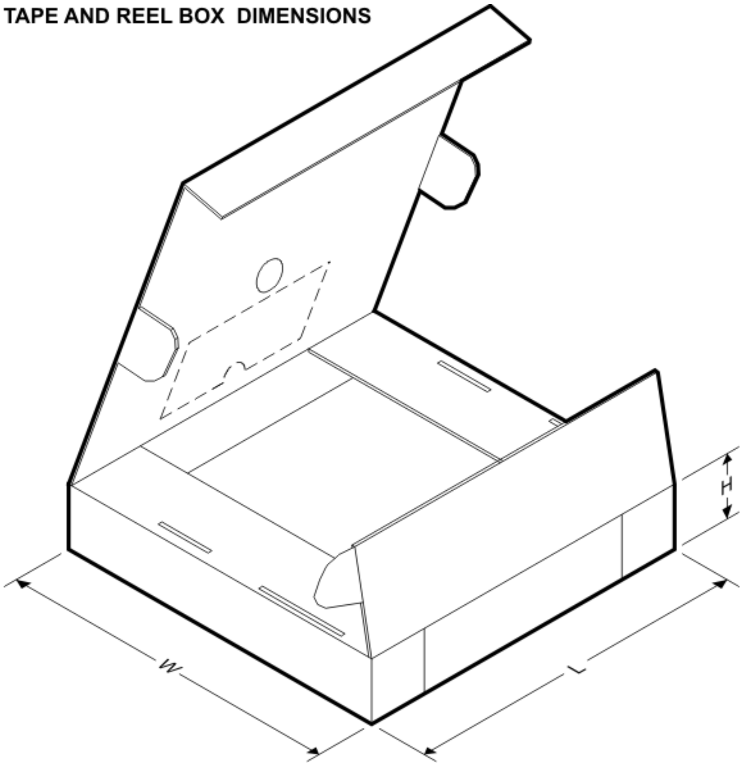
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61260DRVR	SON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS61260DRVT	SON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

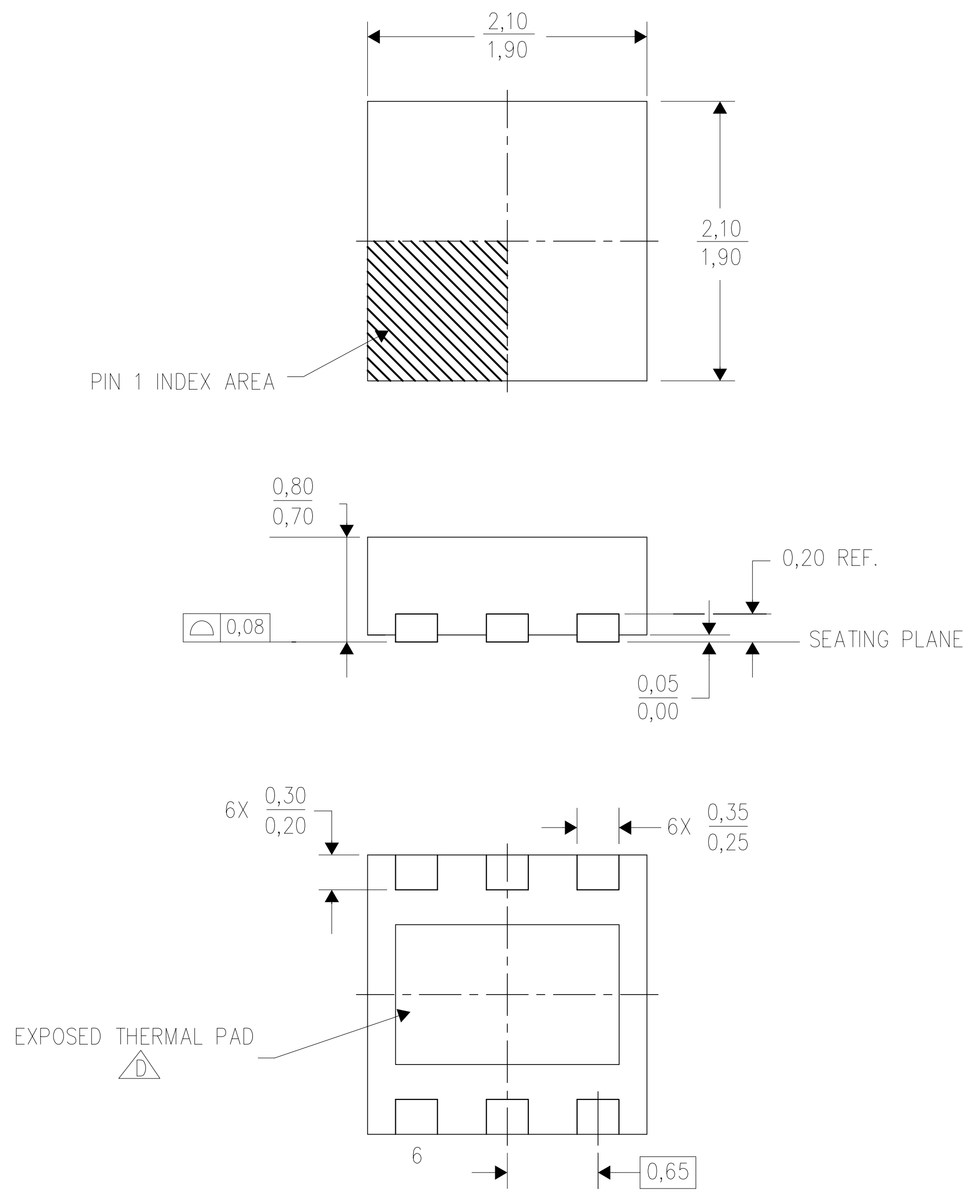
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61260DRVR	SON	DRV	6	3000	210.0	185.0	35.0
TPS61260DRVT	SON	DRV	6	250	210.0	185.0	35.0

DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



4206925/E 10/10

NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Small Outline No–Lead (SON) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

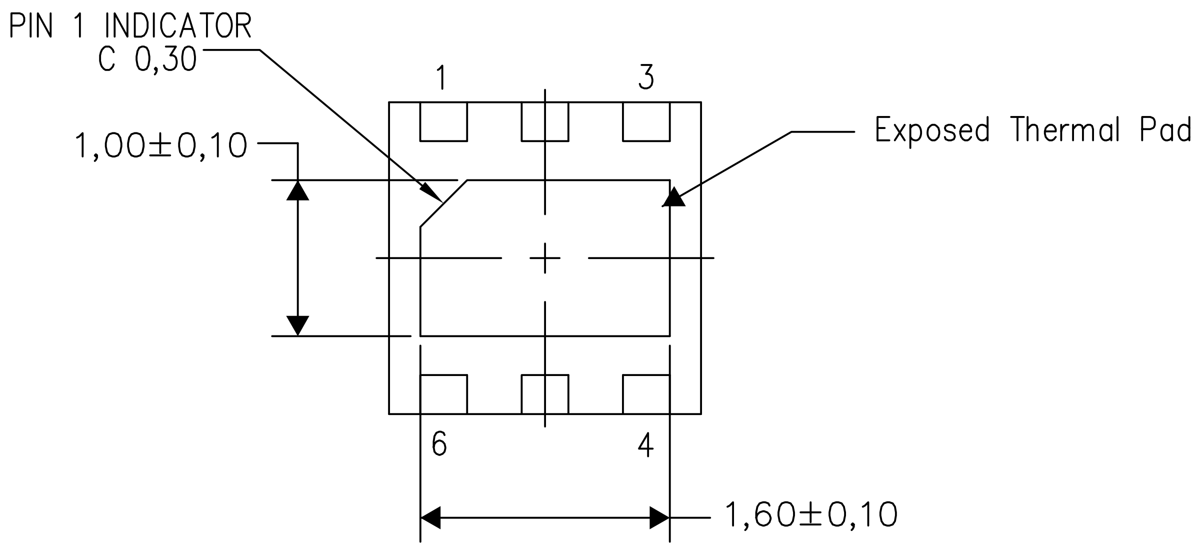
DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



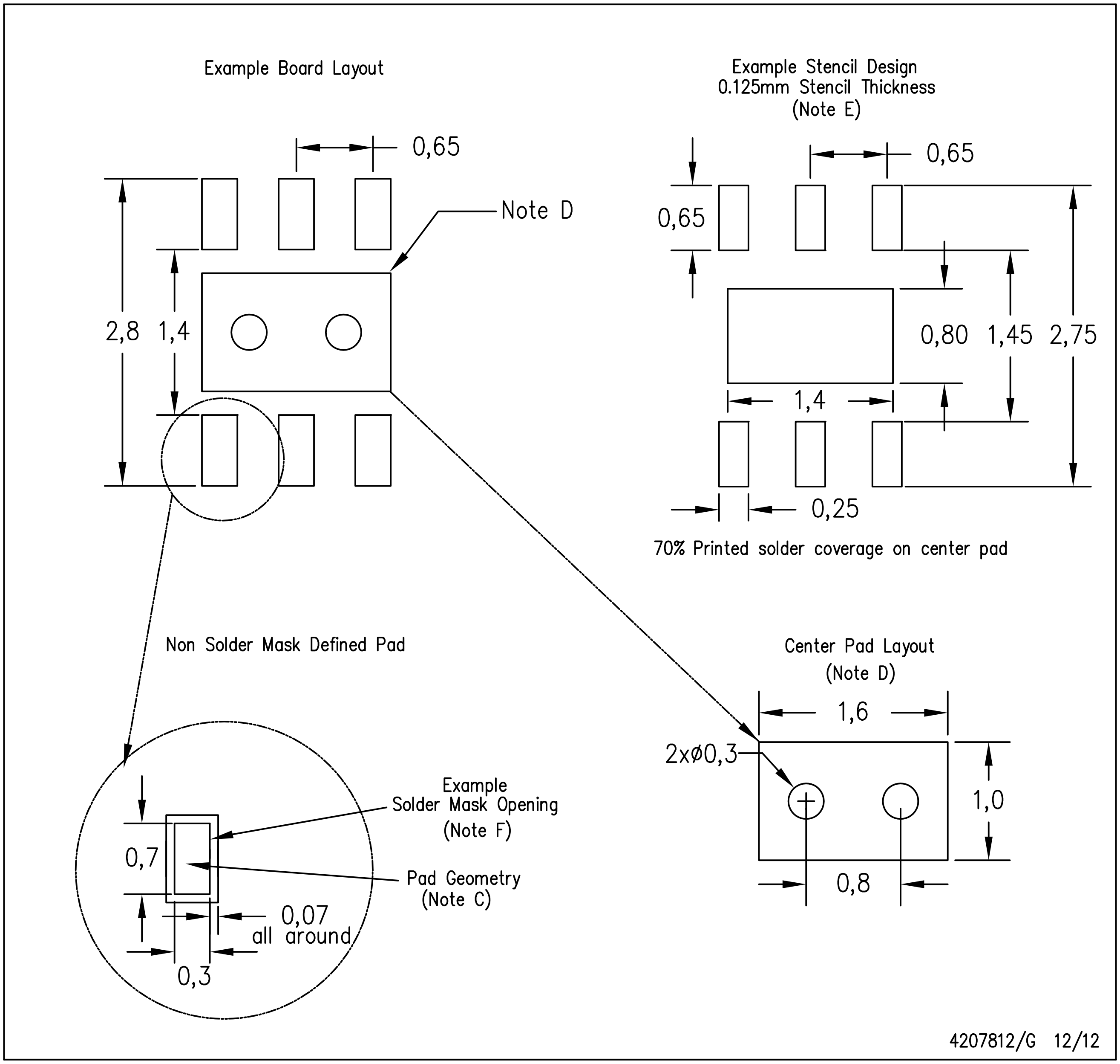
Bottom View

Exposed Thermal Pad Dimensions

4206926/N 03/13

NOTE: All linear dimensions are in millimeters

DRV (S-PWSON-N6) PLASTIC SMALL OUTLINE NO-LEAD



NOTES:

A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Publication IPC-7351 is recommended for alternate designs.

D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.

E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.

F. Customers should contact their board fabrication site for solder mask tolerances.

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