300-mA 40-V LOW-DROPOUT REGULATOR WITH 25-µA QUIESCENT CURRENT

Check for Samples: TPS7A6201-Q1

FEATURES

- **Low Dropout Voltage**
  - **300mV at I_{OUT} = 150mA**
- **4-V to 40-V Wide Input Voltage Range With up to 45-V Transients**
- **300-mA Maximum Output Current**
- **Ultra Low Quiescent Current**
  - **$I_{QUIESCENT}$ = 25 µA (Typ) at Light Loads**
  - **I_{SLEEP} < 2 µA when EN = Low**
- **2.5-V to 7-V Programmable Output Voltage**
- **Low-ESR Ceramic Output Stability Capacitor**
- **Integrated Fault Protection**
  - **Short-Circuit/Over-Current Protection**
  - **Thermal Shutdown**
- **Low Input Voltage Tracking**
- **Thermally Enhanced Power Package**
 - **5-pin TO-263 (KTT /D2PAK)**

APPLICATIONS

- **Qualified for Automotive Applications**
- **Infotainment Systems with Sleep Mode**
- **Body Control Modules**
- **Always ON Battery Applications**
  - **Gateway Applications**
 - **Remote Keyless Entry Systems**
  - **Immobilizers**

DESCRIPTION

The TPS7A6201 is a low dropout linear voltage regulator designed for low power consumption and quiescent current less than 25 µA in light load applications. This device features an integrated over-current protection, and is designed to achieve stable operation even with low-ESR ceramic output capacitors. The output voltage can be programmed using external resistors. Low voltage tracking feature allows for a smaller input capacitor and can possibly eliminate the need of using a boost converter during cold crank conditions. Because of these features, this device is well suited in power supplies for various automotive applications.

TYPICAL REGULATOR STABILITY
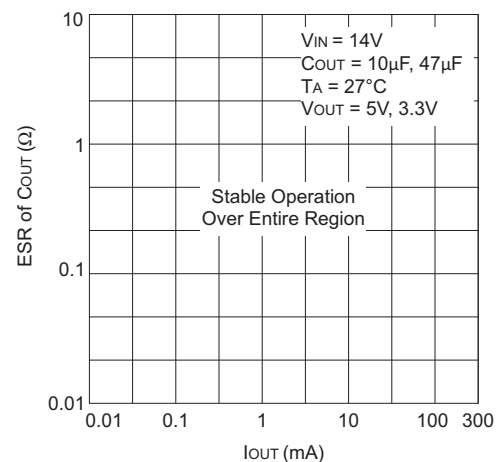
Figure 1. ESR vs Load Current for TPS7A6201

TYPICAL APPLICATION SCHEMATIC
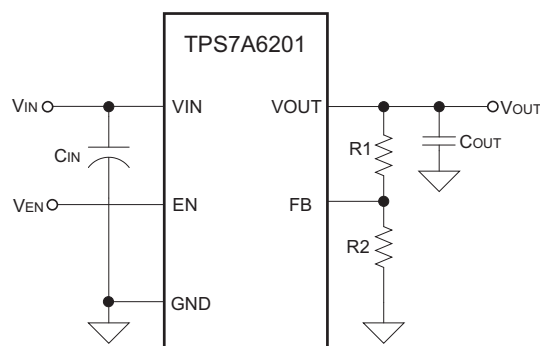
Figure 2. Application Schematic

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ORDERING INFORMATION[1]

PACKAGE		TOP SIDE MARKING	ORDERABLE PART NUMBER[2]
5 pin KTT	Reel of 500	7A6201Q1	TPS7A6201QKTTRQ1

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

ABSOLUTE MAXIMUM RATINGS[1]

over operating free-air temperature range (unless otherwise noted)

NO.		DESCRIPTION	VALUE	UNIT
1.1	V_{IN}, V_{EN}	Unregulated inputs[2]	-0.3 to 45	V
1.2	V_{OUT}	Regulated output	7	V
1.3	V_{FB}	Feedback voltage	-0.3 to 7	V
1.4	θ_{JP}	Thermal impedance junction to exposed pad KTT (D2PAK) package	10.4	°C/W
1.5	θ_{JA}	Thermal impedance junction to ambient KTT (D2PAK) package[3]	30.2	°C/W
1.6	θ_{JA}	Thermal impedance junction to ambient KTT (D2PAK) package[4]	34.4	°C/W
1.7	ESD	Electrostatic discharge (Human Body Model)[5]	2	kV
1.8	T_{OP}	Operating ambient temperature	-40 to +125	°C
1.9	T_S	Storage temperature range	-65 to +150	°C
1.10	T_{LEAD}	Lead temperature (soldering, 10sec)	260	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to GND.
(2) Absolute maximum voltage for duration less than 480ms.
(3) The thermal data is based on JEDEC standard high K profile – JESD 51-5. The copper pad is soldered to the thermal land pattern. Also correct attachment procedure needs to be incorporated.
(4) The thermal data is based on JEDEC standard low K profile – JESD 51-3. The copper pad is soldered to the thermal land pattern. Also correct attachment procedure needs to be incorporated.
(5) Tested in accordance with JEDEC Standard 22, Test Method A114-A (100pF capacitor discharged through a 1.5kΩ resistor into each pin).

DISSIPATION RATINGS

NO.	JEDEC STANDARD	PACKAGE	$T_A < 25°C$ POWER RATING (W)	DERATING FACTOR ABOVE $T_A = 25°C$ (°C/W)	$T_A = 85°C$ POWER RATING (W)
2.1	JEDEC Standard PCB - low K, JESD 51-3	5 pin KTT	3.63	34.4	1.89
2.2	JEDEC Standard PCB - high K, JESD 51-5	5 pin KTT	4.14	30.2	2.15

RECOMMENDED OPERATING CONDITIONS

NO.		DESCRIPTION	MIN	MAX	UNIT
3.1	V_{IN}, V_{EN}	Unregulated input voltage	4	40	V
3.2	T_J	Operating junction temperature range	-40	150	°C

ELECTRICAL CHARACTERISTICS

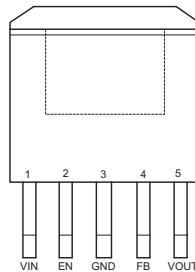V_{IN} = 14V, T_J = -40ºC to 150ºC (unless otherwise noted)

NO.	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
4. Input Voltage (VIN pin)							
4.1	V_{IN}	Input voltage		4		40	V
4.2	$I_{QUIESCENT}$	Quiescent current	V_{IN} = 8.2V to 18V, V_{EN} = 5V, I_{OUT} = 0.01mA to 0.75mA		25	40	µA
4.3	I_{SLEEP}	Sleep/shutdown current	V_{IN} = 8.2V to 18V, V_{EN} < 0.8V, I_{OUT} = 0mA (no load), T_A = 125°C			3	µA
4.4	$V_{IN-UVLO}$	Under voltage lock out voltage	Ramp V_{IN} down until output is turned OFF		3.16		V
4.5	$V_{IN(POWERUP)}$	Power up voltage	Ramp V_{IN} up until output is turned ON		3.45		V
5. Enable Input (EN pin)							
5.1	V_{IL}	Logic input low level		0		0.8	V
5.2	V_{IH}	Logic input high level		2.5		40	V
6. Regulated Output Voltage (VOUT pin)							
6.1	V_{REF}	Internal Reference Voltage	I_{OUT} = 10mA to 300mA, V_{IN}= V_{OUT} + 1V to 16V	-2		2	%
6.2	$\Delta V_{LINE-REG}$	Line regulation	V_{IN} = 6V to 28V, I_{OUT} = 10mA, V_{OUT} = 7V			15	mV
			[V_{IN} = 6V to 28V, I_{OUT} = 10mA, V_{OUT} = 3.3V][1]			20	mV
6.3	$\Delta V_{LOAD-REG}$	Load regulation	I_{OUT} = 10mA to 300mA, V_{IN} = 14V, V_{OUT} = 7V			25	mV
			[I_{OUT} = 10mA to 300mA, V_{IN} = 14V, V_{OUT} = 3.3V][1]			35	mV
6.4	$V_{DROPOUT}$[2]	Dropout voltage (V_{IN} − V_{OUT})	I_{OUT} = 250mA			500	mV
			I_{OUT} = 150mA			300	mV
6.5	R_{SW}[1]	Switch resistance	VIN to VOUT resistance			2	Ω
6.6	I_{OUT}	Output current	V_{OUT} in regulation	0		300	mA
6.7	I_{CL}	Output current limit	V_{OUT} = 0V (VOUT pin is shorted to ground)	350		1000	mA
6.8	PSRR[1]	Power supply ripple rejection	$V_{IN-RIPPLE}$ = 0.5 Vpp, I_{OUT} = 300mA, frequency = 100 Hz, V_{OUT} = 5V and V_{OUT} = 3.3V		60		dB
			$V_{IN-RIPPLE}$ = 0.5 Vpp, I_{OUT} = 300mA, frequency = 150 kHz, V_{OUT} = 5V and V_{OUT} = 3.3V		30		
7. Operating Temperature Range							
7.1	T_J	Operating junction temperature		-40		150	ºC
7.2	$T_{SHUTDOWN}$	Thermal shutdown trip point			165		ºC
7.3	T_{HYST}	Thermal shutdown hysteresis			10		ºC

(1) Specified by design – not tested
(2) This test is done with V_{OUT} is in regulation and V_{IN} − V_{OUT} parameter is measured when V_{OUT} (programmned output voltage, ex. 5V or 3.3V) drops by 100mV at specified loads.

DEVICE INFORMATION

KTT PACKAGE
(TOP VIEW)

TERMINAL FUNCTIONS

NO.	NAME	TYPE	DESCRIPTION
1	VIN	I	Input voltage pin: The unregulated input voltage is supplied to this pin. A bypass capacitor shall be connected between VIN pin and GND pin to dampen input line transients.
2	EN	I	Enable pin: This is a high voltage tolerant input pin with an internal pull down. A high input to this pin activates the device and turns the regulator ON. This input can be connected to VIN terminal for self bias applications. If this pin is not connected, the device will stay disabled.
3	GND	I/O	Ground pin: This is signal ground pin of the IC.
4	FB	I	Feedback pin: This pin is used to connect external resistors to ground in order to program the output voltage.
5	VOUT	O	Regulated output voltage pin: This is a regulated output voltage pin with a limitation on maximum output current. An external resistor divider is connected at this pin to program the output voltage. In order to achieve stable operation and prevent oscillation, an external output capacitor (C_{OUT}) with low ESR shall be connected between this pin and GND pin.

FUNCTIONAL BLOCK DIAGRAM
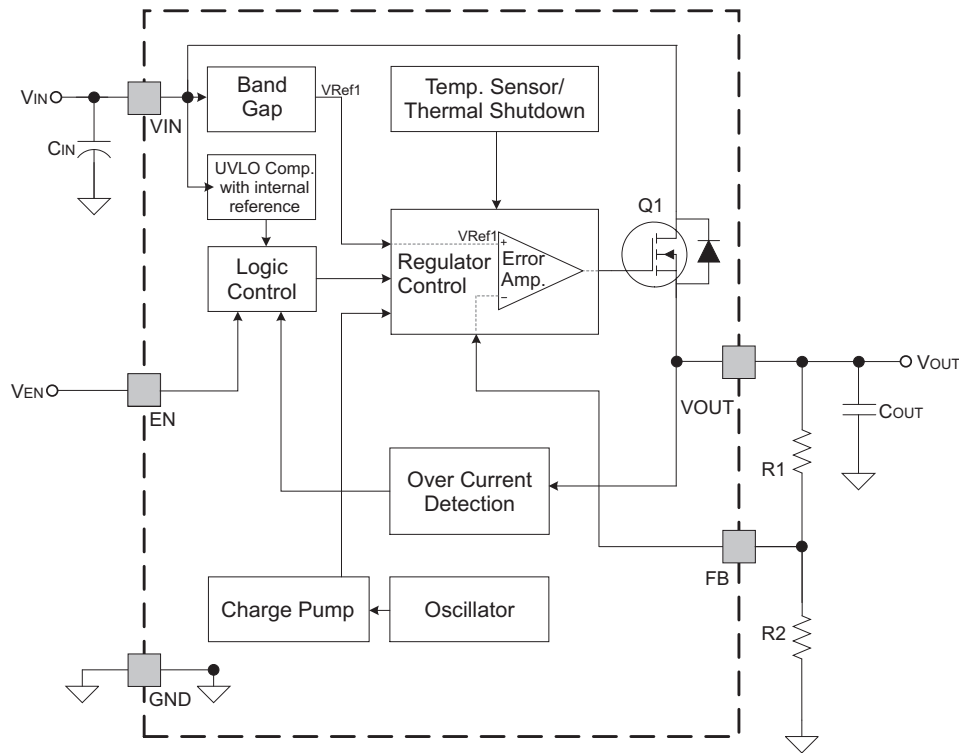
Figure 3. TPS7A6201 Functional Block Diagram

TYPICAL CHARACTERISTICS

Graphs shown in 'Typical Characteristics' section for unreleased devices are for preview only.
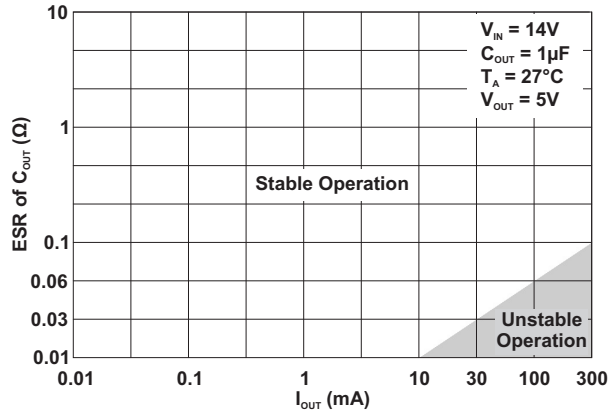
Figure 4. ESR vs Load Current
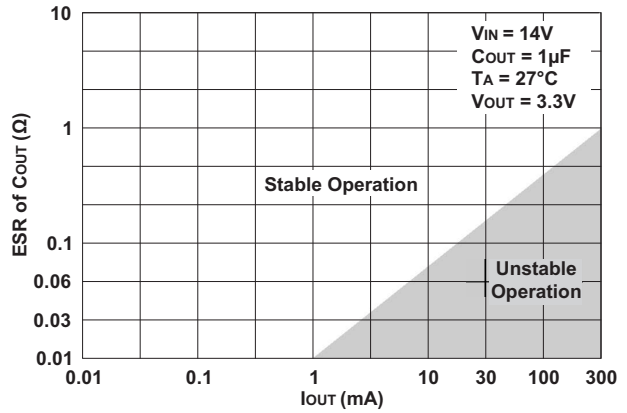
Figure 5. ESR vs Load Current
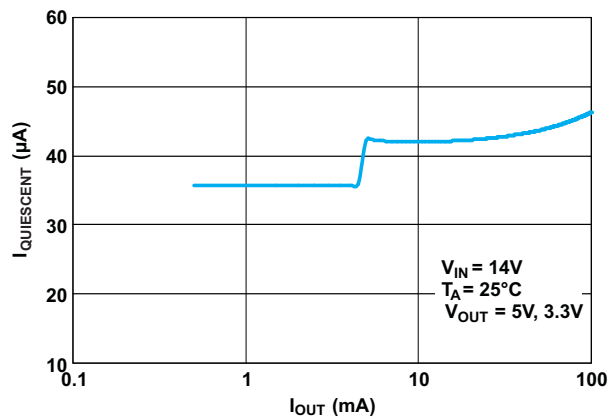
Figure 6. Quiescent Current vs Load Current
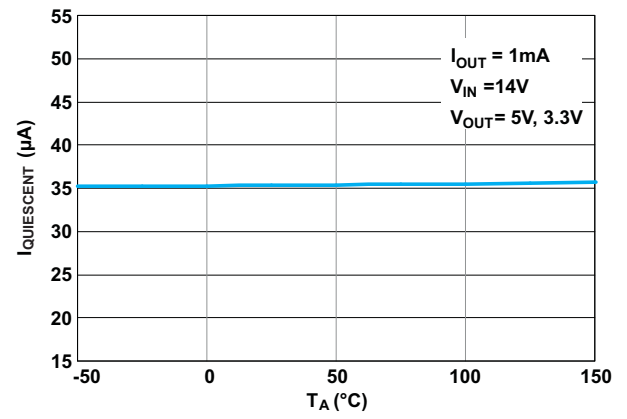
Figure 7. Quiescent Current vs Ambient Air Temperature
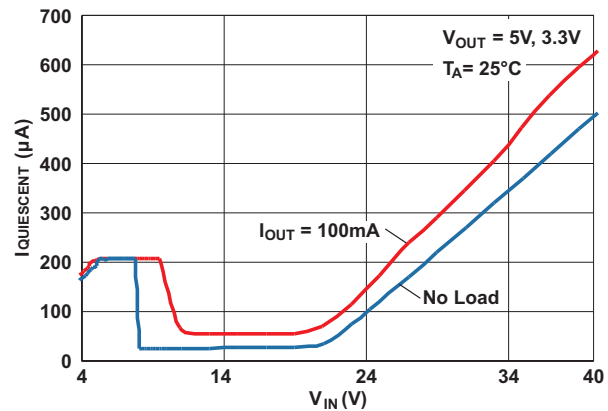
Figure 8. Quiescent Current vs Input Voltage
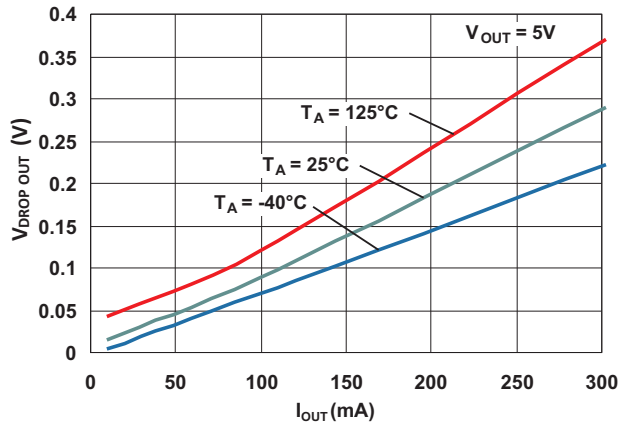
Figure 9. Drop Out Voltage[1] vs Load Current

(1) Drop out voltage is measured when the output voltage drops by 100mV from the regulated output voltage level. (For example, if output voltage is programmed to be 5V, the drop out voltage is measured when the output voltage drops down to 4.9V from 5V.)

TYPICAL CHARACTERISTICS (continued)
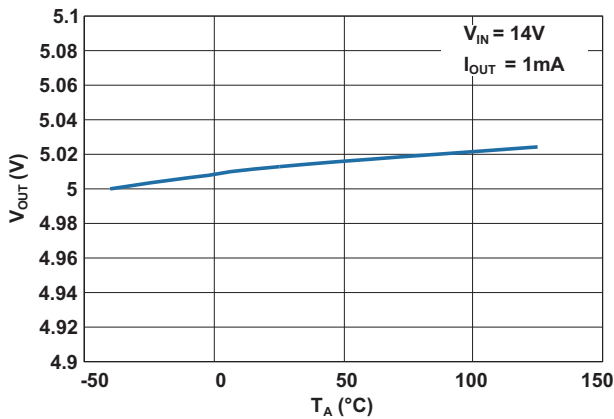
Figure 10. Output Voltage vs Ambient Air Temperature
(V_{OUT} programmed to 5 V)
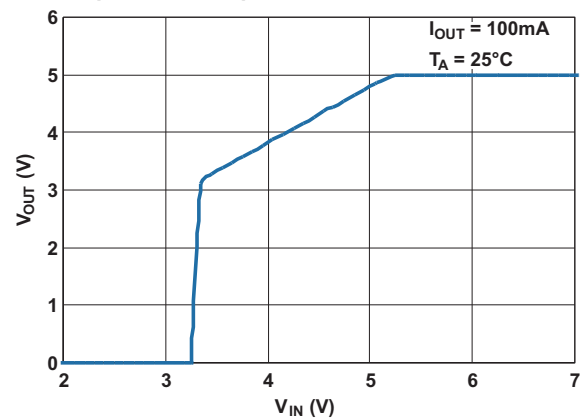
Figure 11. Output Voltage vs Input Voltage
(V_{OUT} programmed to 5 V)
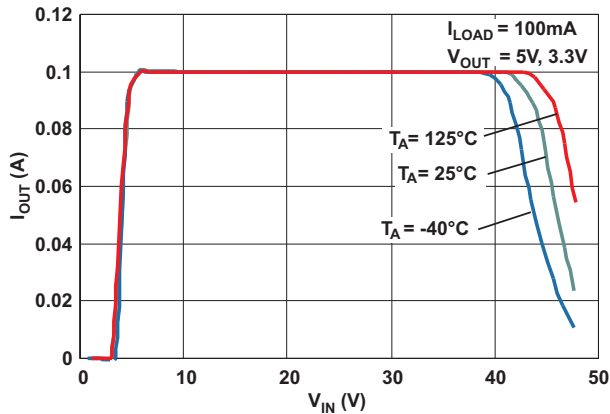
Figure 12. Output Current vs Input Voltage
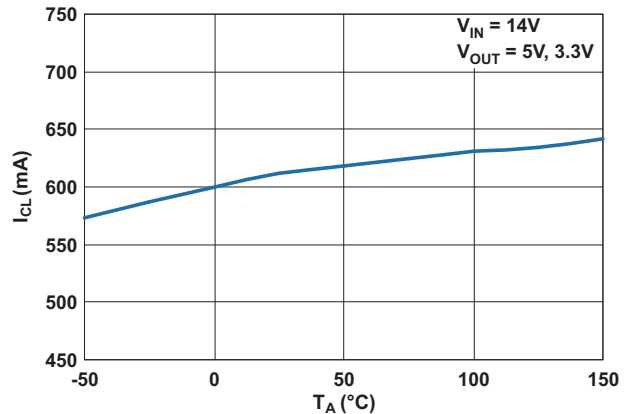
Figure 13. Output Current Limit vs
Ambient Air Temperature
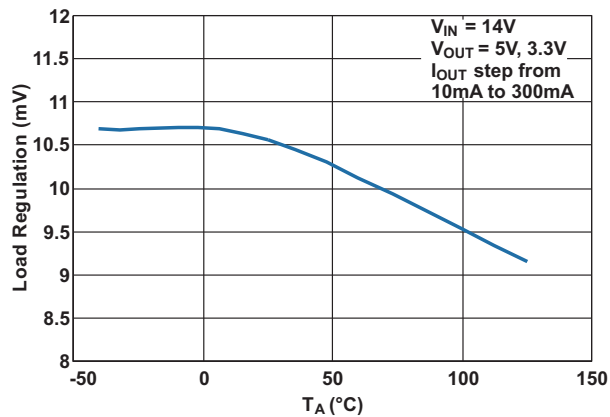
Figure 14. Load Regulation vs Ambient Air Temperature
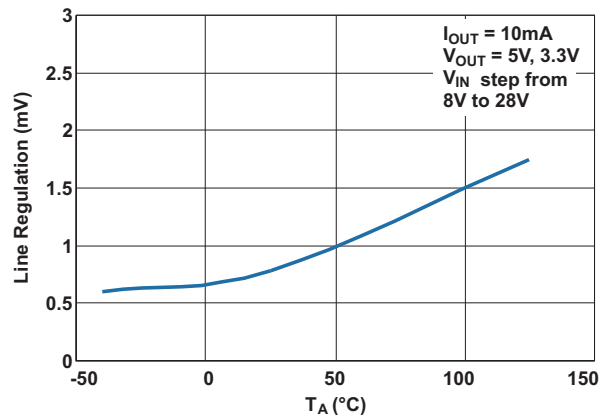
Figure 15. Line Regulation vs Ambient Air Temperature

TYPICAL CHARACTERISTICS (continued)
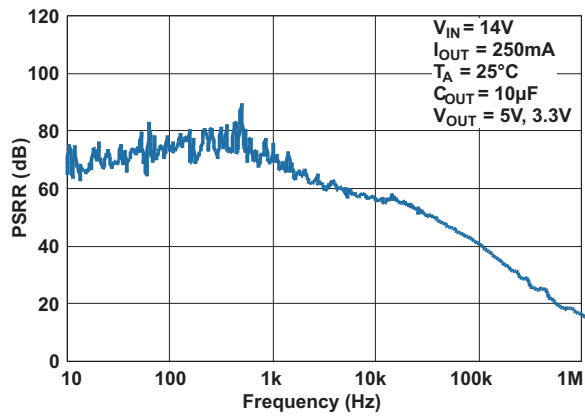
Figure 16. PSRR at Heavy Load Current
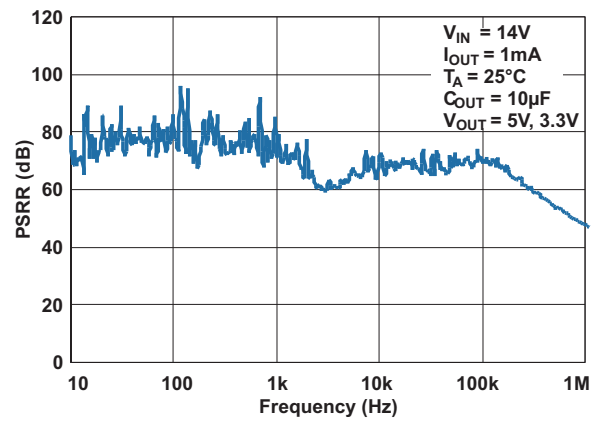
Figure 17. PSRR at Light Load Current

DETAILED DESCRIPTION

TPS7A6201 is a monolithic low dropout linear voltage regulator with programmable output voltage and an integrated fault protection. This voltage regulator is designed for low power consumption and quiescent current less than 25µA in light load applications.

This device is available in two 5 pin package options as follows:

• KTT/ D2PAK

The following section describes the features of TPS7A6201 voltage regulator in detail.

Power Up

During power up, the regulator incorporates a protection scheme to limit the current through pass element and output capacitor. When the input voltage exceeds a certain threshold (VIN$_{(POWERUP)}$) level, the output voltage begins to ramp up as shown in Figure 18.
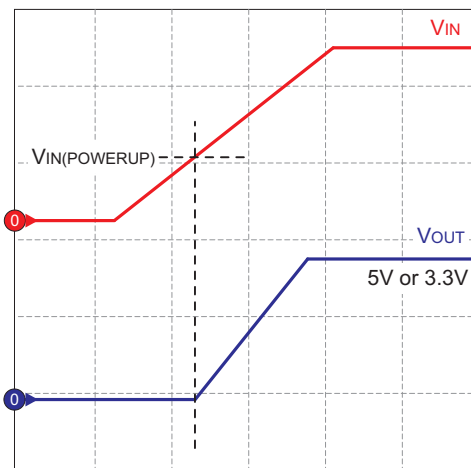
Figure 18.

Adjustable Output Voltage

The regulated output voltage (V$_{OUT}$) can be programmed by connecting external resistors to FB pin. The feedback resistor values can be calculated using Equation 1.

$$V_{OUT} = V_{REF} \left[1 + \frac{R1}{R2} \right]$$

(1)

Where,

V$_{OUT}$=desired output voltage

V$_{REF}$ = reference voltage (V$_{REF}$= 1.23 V typically)

R1, R2 = feedback resistors (see Figure 3)

The overall tolerance of the regulated output voltage depends on the tolerance of internal reference voltage and external feedback resistors, and is given by Equation 2.

$$tol_{V_{OUT}} = tol_{V_{REF}} + \left[\frac{R1}{R1 + R2} \right] \left[tol_{R1} + tol_{R2} \right]$$

(2)

Where,

tol$_{VOUT}$ = tolerance of output voltage

tol$_{VREF}$ = tolerance of internal reference voltage (tol$_{VREF}$ = ± 1.5% typically)

tol$_{R1}$,tol$_{R2}$ = tolerance of feedback resistors R1, R2

For a tighter tolerance on V$_{OUT}$, lower-value feedback resistors can be selected. It is recommended to select feedback resistors such that the sum of R1 and R2 is between 20kΩ and 200kΩ.

Enable Input

This device has a high voltage tolerant EN pin that can be used to enable and disable a device from an external microcontroller or a digital control circuit. A high input to this pin activates the device and turns the regulator on. This input can also be connected to V$_{IN}$ terminal for self bias applications. An internal pull down resistor is connected to this pin, and therefore if this pin is left unconnected, the device will stay disabled.

Charge Pump Operation

This device has an internal charge pump which turns on or off depending on the input voltage and the output current. The charge pump switching circuitry shall not cause conducted emissions to exceed required thresholds on the input voltage line. For a given output current, the charge pump stays on at lower input voltages and turns off at higher input voltages. The charge pump switching thresholds are hysteretic. Figure 19 and Figure 20 shows typical switching thresholds for the charge pump at light (I$_{OUT}$ < ~2mA) and heavy (I$_{OUT}$ > ~2mA) loads respectively.
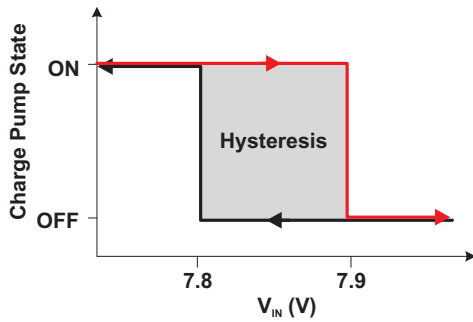
Figure 19. Charge Pump Operation at Light Loads
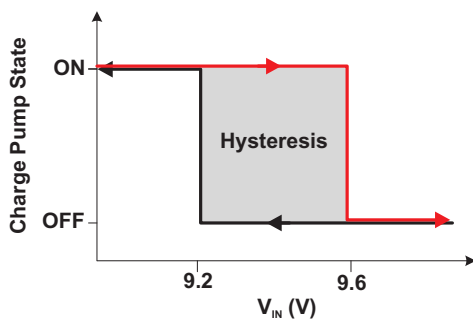
Figure 20. Charge Pump Operation at Heavy Loads

Low Power Mode

At light loads and high input voltages (V_{IN}>~8V such that charge pump is off) the device operates in Low Power Mode and the quiescent current consumption is reduced to 25µA (typical) as shown in Table 1.

Table 1. Typical Quiescent Current Consumption

I_{OUT}	Charge Pump ON	Charge Pump OFF
I_{OUT} < ~2mA (Light load)	250 µA	25 µA (Low Power Mode)
I_{OUT} > ~2mA (Heavy load)	280 µA	70 µA

Under Voltage Shutdown

This device has an integrated under voltage lock out (UVLO) circuit to shutdown the output if the input voltage (V_{IN}) falls below an internally fixed UVLO threshold level ($V_{IN-UVLO}$) as shown in Figure 21. This ensures that the regulator is not latched into an unknown state during low input voltage conditions. The regulator will normally power up when the input voltage exceeds $V_{IN(POWERUP)}$ threshold.

Low Voltage Tracking

At low input voltages the regulator drops out of regulation, the output voltage tracks input minus a voltage based on the load current (I_{OUT}) and switch resistance (R_{SW}) as shown in Figure DDD. This allows for a smaller input capacitor and can possibly eliminate the need of using a boost convertor during cold crank conditions.
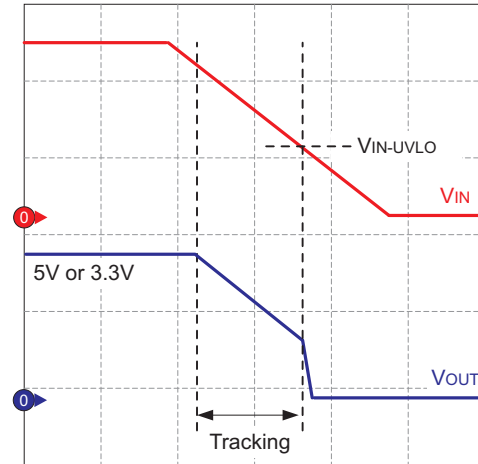
Figure 21.

Integrated Fault Protection

The device features integrated fault protection to make it ideal for use in automotive applications. In order to keep the device in safe area of operation during certain fault conditions, internal current limit protection and current limit fold back are used to limit the maximum output current. This protects the device from excessive power dissipation. For example, during a short circuit condition on the output; current through the pass element is limited to I_{CL} to protect the device from excessive power dissipation.

Thermal Shutdown

The device incorporates a thermal shutdown (TSD) circuit as a protection from overheating. For continuous normal operation, the junction temperature should not exceed TSD trip point. If the junction temperature exceeds TSD trip point, the output is turned off. When the junction temperature falls below TSD trip point, the output is turned on again. This is shown in Figure 22.
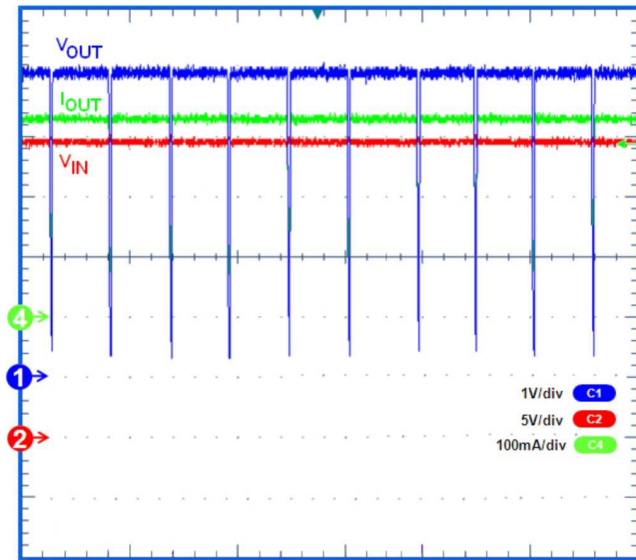
Figure 22. Thermal Cycling Waveform for TPS7A6201 (V_{IN} = 24 V, I_{OUT} = 300 mA, V_{OUT} = 5 V)

APPLICATION INFORMATION

Typical application circuit for TPS7A6201 is shown in Figure 23. Depending upon an end application, different values of external components may be used. In order to program the output voltage, feedback resistors (R1 and R2) should be carefully selected. Using small resistors will result in higher current consumption, where as, using very large resistors will impact the sensitivity of the regulator. Therefore, It is recommended to select feedback resistors such that the sum of R1 and R2 is between 20kΩ and 200kΩ. Also, the overall tolerance of the regulated output voltage depends on the tolerance of internal reference voltage and external feedback resistors.

A larger output capacitor may be required during fast load steps to prevent output from temporarily dropping down. A low ESR ceramic capacitor with dielectric of type X5R or X7R is recommended. Additionally, a bypass capacitor can be connected at the output to decouple high frequency noise as per the end application.

Example

If the desired regulated output voltage is 5V, upon selecting R2; R1 can be calculated using Equation 1 (and vice versa). Knowing V_{REF} = 1.23V (typical), V_{OUT} = 5V, selecting R2 = 20kΩ, R1 is calculated to be 61.3kΩ.
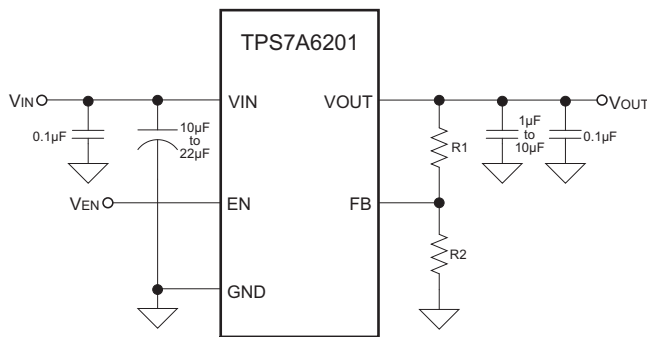
Figure 23. Typical Application Schematic for TPS7A6201

Power Dissipation and Thermal Considerations

Power dissipated in the device can be calculated using Equation 3.

$$P_D = I_{OUT} \times (V_{IN} - V_{OUT)} + I_{QUIESCENT} \times V_{IN} \tag{3}$$

Where,

P_D = continuous power dissipation

I_{OUT} = output current

V_{IN} = input voltage

V_{OUT} = output voltage

$I_{QUIESCENT}$ = quiescent current

As $I_{QUIESCENT}$ << I_{OUT}, therefore, the term $I_{QUIESCENT} \times V_{IN}$ in Equation 3 can be ignored.

For device under operation at a given ambient air temperature (T_A), the junction temperature (T_J) can be calculated using Equation 4.

$$T_J = T_A + (\theta_{JA} \times P_D) \tag{4}$$

Where,

θ_{JA} = junction to ambient air thermal impedance

The rise in junction temperature due to power dissipation can be calculated using Equation 5.

$$\Delta T = T_J - T_A = (\theta_{JA} \times P_D) \tag{5}$$

For a given maximum junction temperature (T_{J-Max}), the maximum ambient air temperature (T_{A-Max}) at which the device can operate can be calculated using Equation 6.

$$T_{A-Max} = T_{J-Max} - (\theta_{JA} \times P_D) \tag{6}$$

Example

If I_{OUT} = 100mA, V_{OUT} = 5V, V_{IN} = 14V, $I_{QUIESCENT}$ = 250µA and θ_{JA}= 30°C/W, the continuous power dissipated in the device is 0.9W. The rise in junction temperature due to power dissipation is 27°C. For a maximum junction temperature of 150°C, maximum ambient air temperature at which the device can operate is 123°C.

For adequate heat dissipation, it is recommended to solder the thermal pad (exposed heat sink) to thermal land pad on the PCB. Doing this provides a heat conduction path from die to the PCB and reduces overall package thermal resistance. Power derating curves for TPS7A6201 device in the KTT (D2PAK) package is shown in Figure 24.
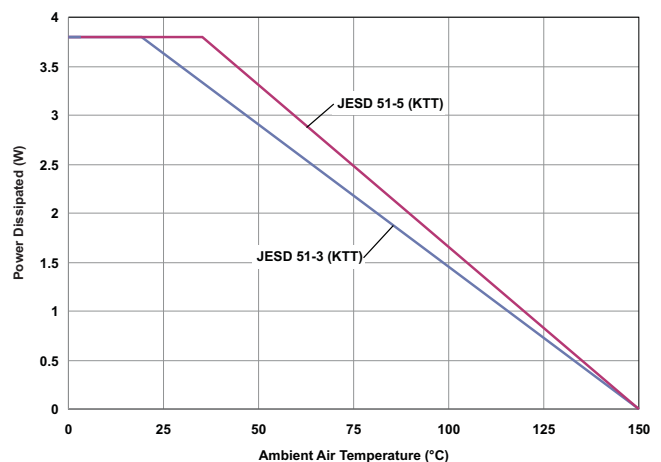
Figure 24. Power Derating Curves

For optimum thermal performance, it is recommended to use a high K PCB with thermal vias between ground plane and solder pad/ thermal land pad. This is shown in Figure 25 (a) and (b). Further, heat spreading capabilities of a PCB can be considerably improved by using a thicker ground plane and a thermal land pad with a larger surface area.

Keeping other factors constant, surface area of the thermal land pad contributes to heat dissipation only to a certain extent. Figure 26 shows variation of θ_{JA} with surface area of the thermal land pad (soldered to the exposed pad) for KTT package.

Exposed Tab

Thermal Via
Thermal Land Pad

PCB

Ground Plane

(a) Before soldering

(b) After soldering
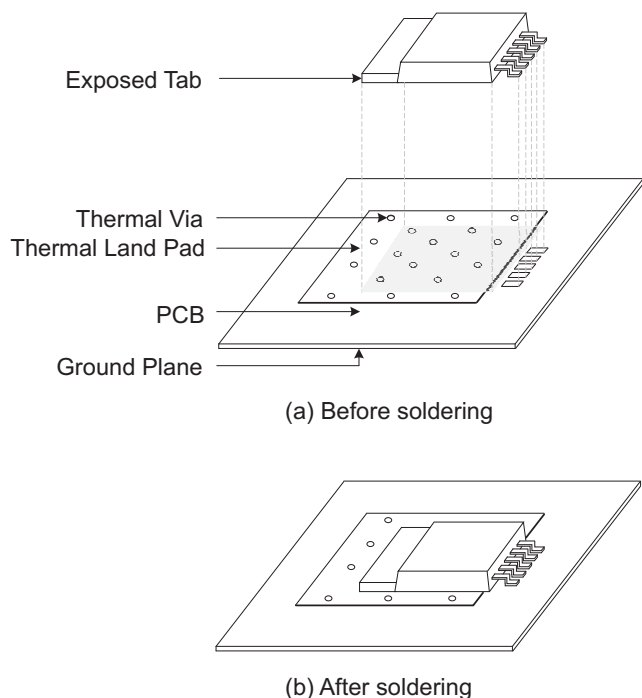
Figure 25. Using Multilayer PCB and Thermal Vias For Adequate Heat Dissipation

KTT (D2PAK) (JESD 51-3)

Thermal Pad Area (sq. mm)
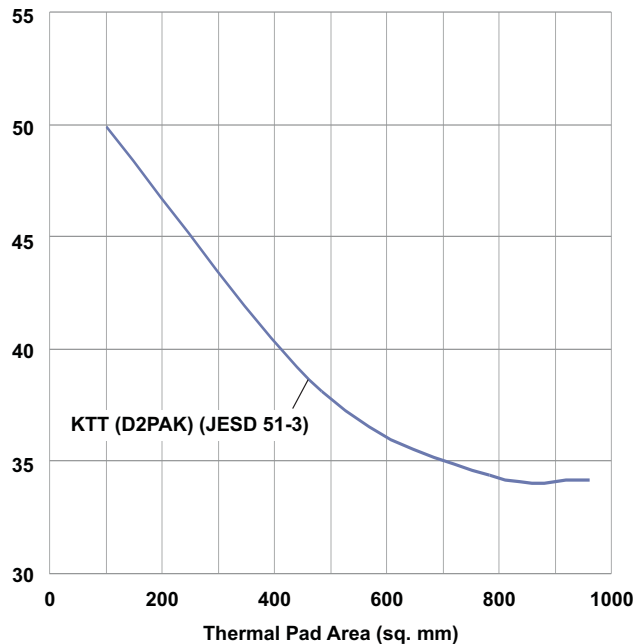
Figure 26. θ_{JA} vs Thermal Pad Area

REVISION HISTORY

Changes from Revision A (December 2011) to Revision B   **Page**

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]	Samples (Requires Login)
TPS7A6201QKTTRQ1	ACTIVE	DDPAK/TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS
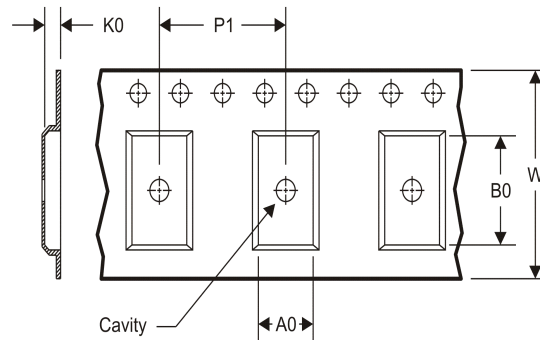
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A6201QKTTRQ1	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.6	15.8	4.9	16.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A6201QKTTRQ1	DDPAK/TO-263	KTT	5	500	340.0	340.0	38.0

KTT (R−PSFM−G5)   PLASTIC FLANGE−MOUNT PACKAGE

10,67
9,65

1,68
1,14

6,22 Min

4,83
4,06

1,40
1,14

6,86 Min

Exposed Thermal Tab

9,65
8,20

⟨D⟩

0,30
0,00

15,88
14,60

1 2 3 4 5

0,91
0,66

1,70

0,58
0,30

⟨D⟩

⊕ | 0,25 Ⓜ

2,79
1,78

Gauge Plane

2,79
1,78

Gauge Plane

0−8°

0−8°

0,25

0,25

OPTIONAL LEAD FORM
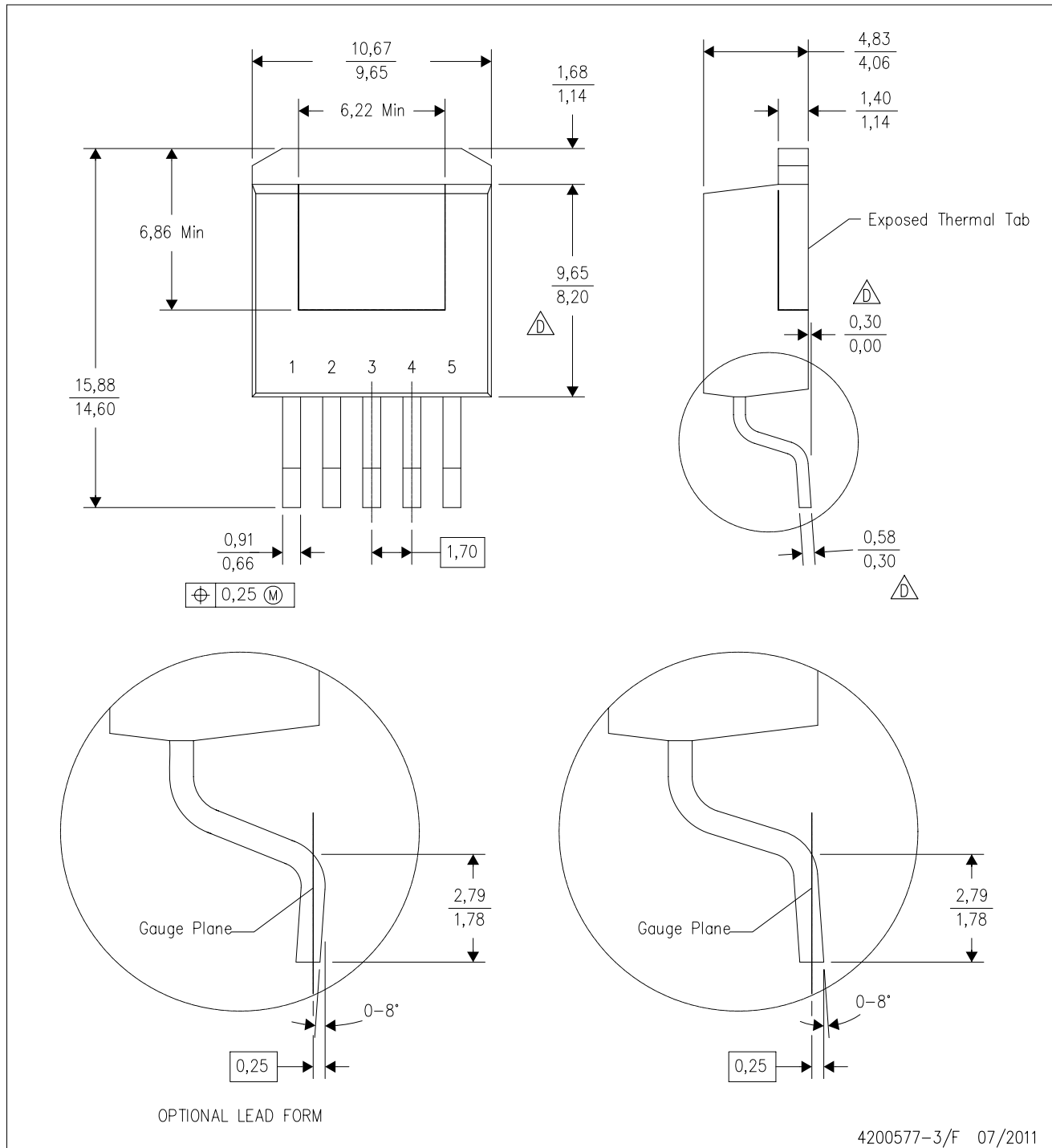
4200577−3/F   07/2011

NOTES: A. All linear dimensions are in millimeters.
         B. This drawing is subject to change without notice.
         C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0,13) per side.
         ⟨D⟩ Falls within JEDEC TO−263 variation BA, except minimum lead thickness, maximum seating height,
             and minimum body length.

KTT (R−PSFM−G5)   PLASTIC FLANGE−MOUNT PACKAGE

Example Board Layout
(Note C)

10,7

Copper Area
(Note F)

8,6

10,6

4,6

1,0

3,4

4x1,7

Non Solder Mask Defined Pad

Example Stencil Design
(Note D)

10,6

8,5

10,6

4,65

0,90

3,3

4x1,7

Example
Solder Mask Opening
(Note E)

1,0

3,4

0,07
All Around

Pad Geometry
(Note C)

4208208−3/C 08/12

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
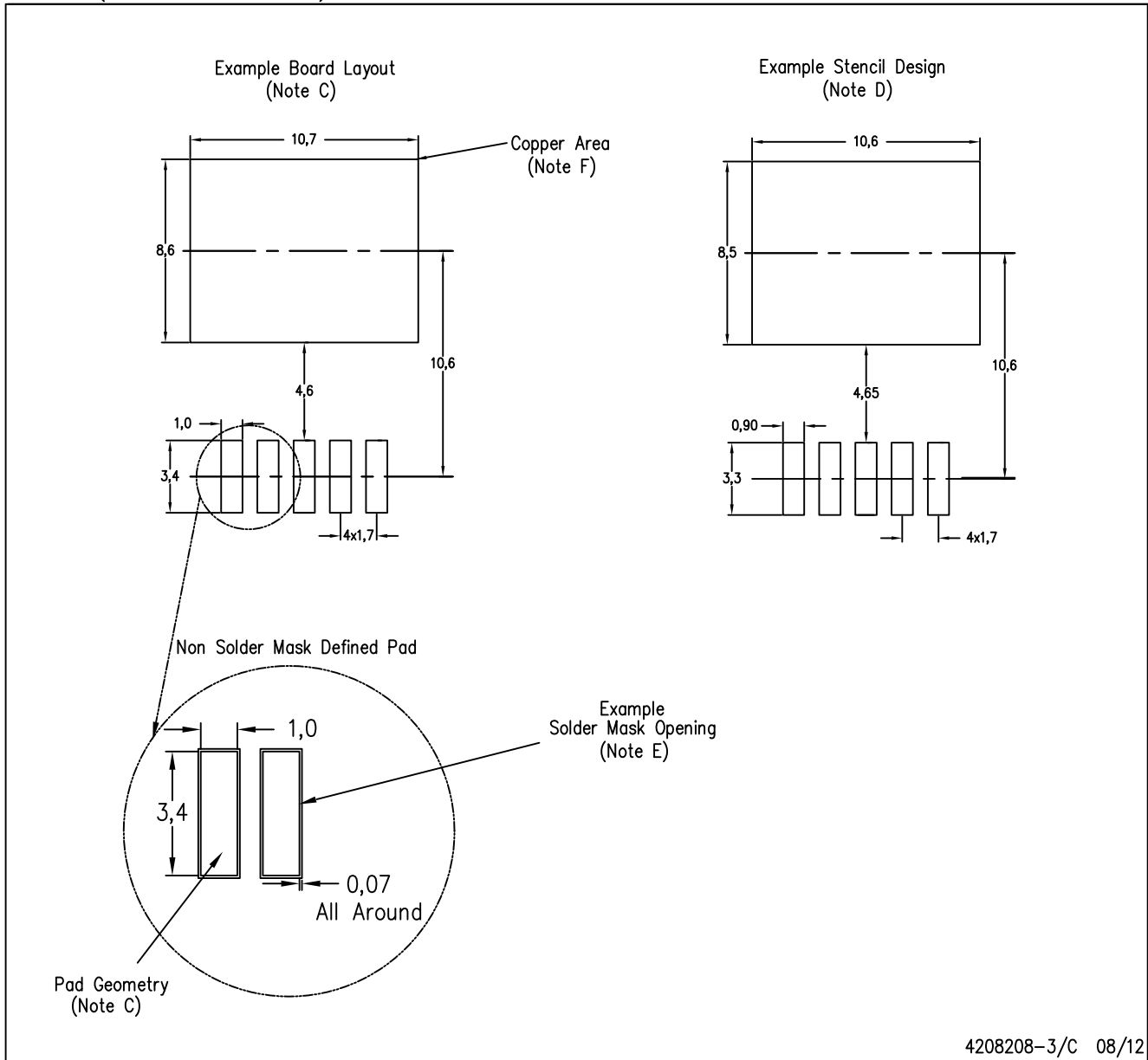   C.   Publication IPC−SM−782 is recommended for alternate designs.
         D.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release.
              Customers should contact their board assembly site for stencil design recommendations. Refer to IPC−7525.
         E.   Customers should contact their board fabrication site for solder mask tolerances between and around
              signal pads.
         F.   This package is designed to be soldered to a thermal pad on the board. Refer to the Product Datasheet
              for specific thermal information, via requirements, and recommended thermal pad size. For thermal pad
              sizes larger than shown a solder mask defined pad is recommended in order to maintain the solderable
              pad geometry while increasing copper area.

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