4.5-V TO 18-V INPUT, HIGH CURRENT, SYNCHRONOUS STEP DOWN THREE BUCK SWITCHER WITH INTEGRATED FET

Check for Samples: TPS65251

FEATURES

- **Wide Input Supply Voltage Range (4.5 V - 18 V)**
- **0.8 V, 1% Accuracy Reference**
- **Continuous Loading: 3 A (Buck 1), 2 A (Buck 2 and 3)**
- **Maximum Current: 3.5 A (Buck 1), 2.5 A (Buck 2 and 3)**
- **Adjustable Switching Frequency 300 kHz - 2.2 MHz Set By External Resistor**
- **Dedicated Enable for Each Buck**
- **External Synchronization Pin for Oscillator**
- **External Enable/Sequencing and Soft Start Pins**
- **Adjustable Current Limit Set By External Resistor**
- **Soft Start Pins**
- **Current-Mode Control With Simple Compensation Circuit**
- **Power Good**
- **Optional Low Power Mode Operation for Light Loads**
- **QFN Package, 40-Pin 6 mm x 6 mm RHA**

APPLICATIONS

- **Set Top Boxes**
- **Blu-ray DVD**
- **DVR**
- **DTV**
- **Car Audio/Video**
- **Security Camera**

DESCRIPTION/ORDERING INFORMATION

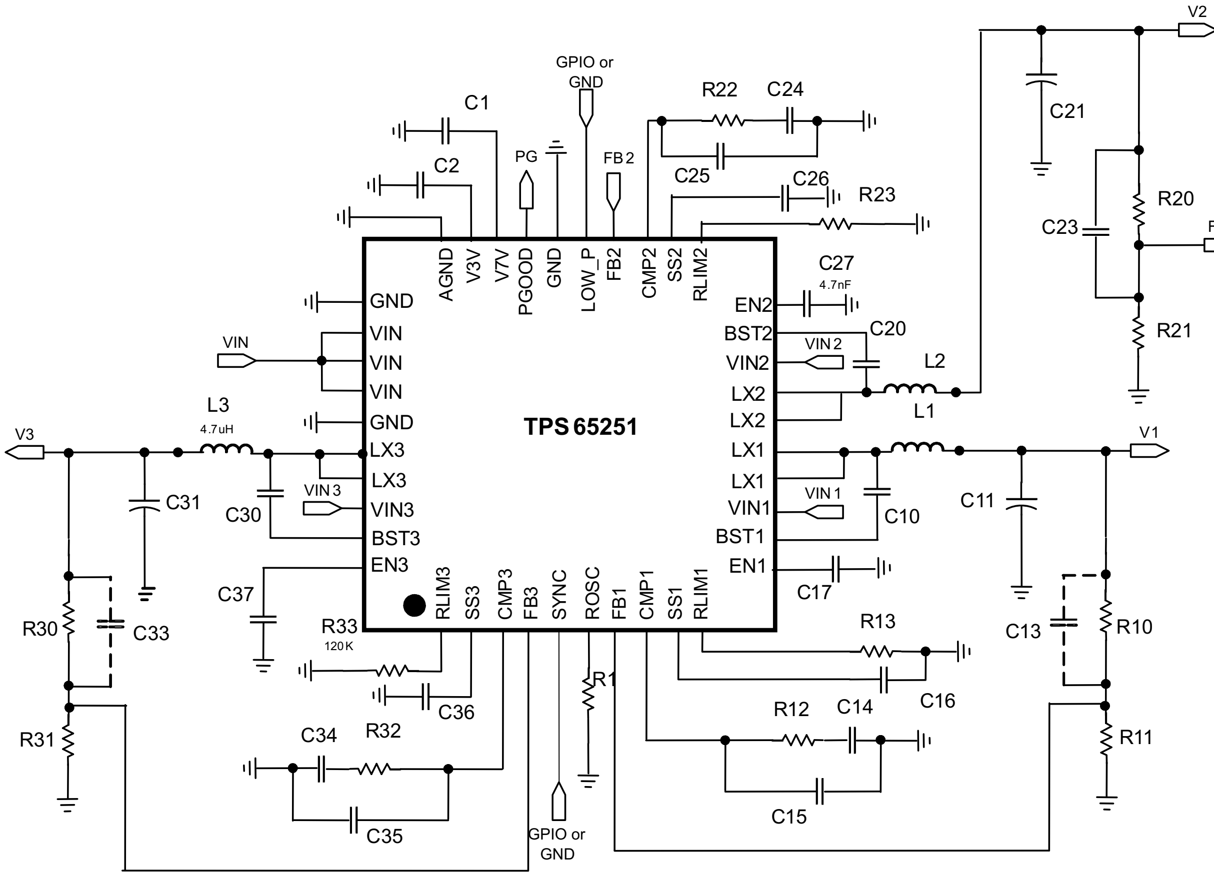
The TPS65251 features three synchronous wide input range high efficiency buck converters. The converters are designed to simplify its application while giving the designer the option to optimize their usage according to the target application.

The converters can operate in 5-, 9-, 12- or 15-V systems and have integrated power transistors. The output voltage can be set externally using a resistor divider to any value between 0.8 V and close to the input supply. Each converter features enable pin that allows a delayed start-up for sequencing purposes, soft start pin that allows adjustable soft-start time by choosing the soft-start capacitor, and a current limit (RLIMx) pin that enables designer to adjust current limit by selecting an external resistor and optimize the choice of inductor. The current mode control allows a simple RC compensation.

The switching frequency of the converters can either be set with an external resistor connected to ROSC pin or can be synchronized to an external clock connected to SYNC pin if needed. The switching regulators are designed to operate from 300 kHz to 2.2 MHz. 180° out of phase operation between Buck 1 and Buck 2, 3 (Buck 2 and 3 run in phase) minimizes the input filter requirements.

TPS65251 features a supervisor circuit that monitors each converter output. The PGOOD pin is asserted once sequencing is done, all PG signals are reported and a selectable end of reset time lapses. The polarity of the PGOOD signal is active high.

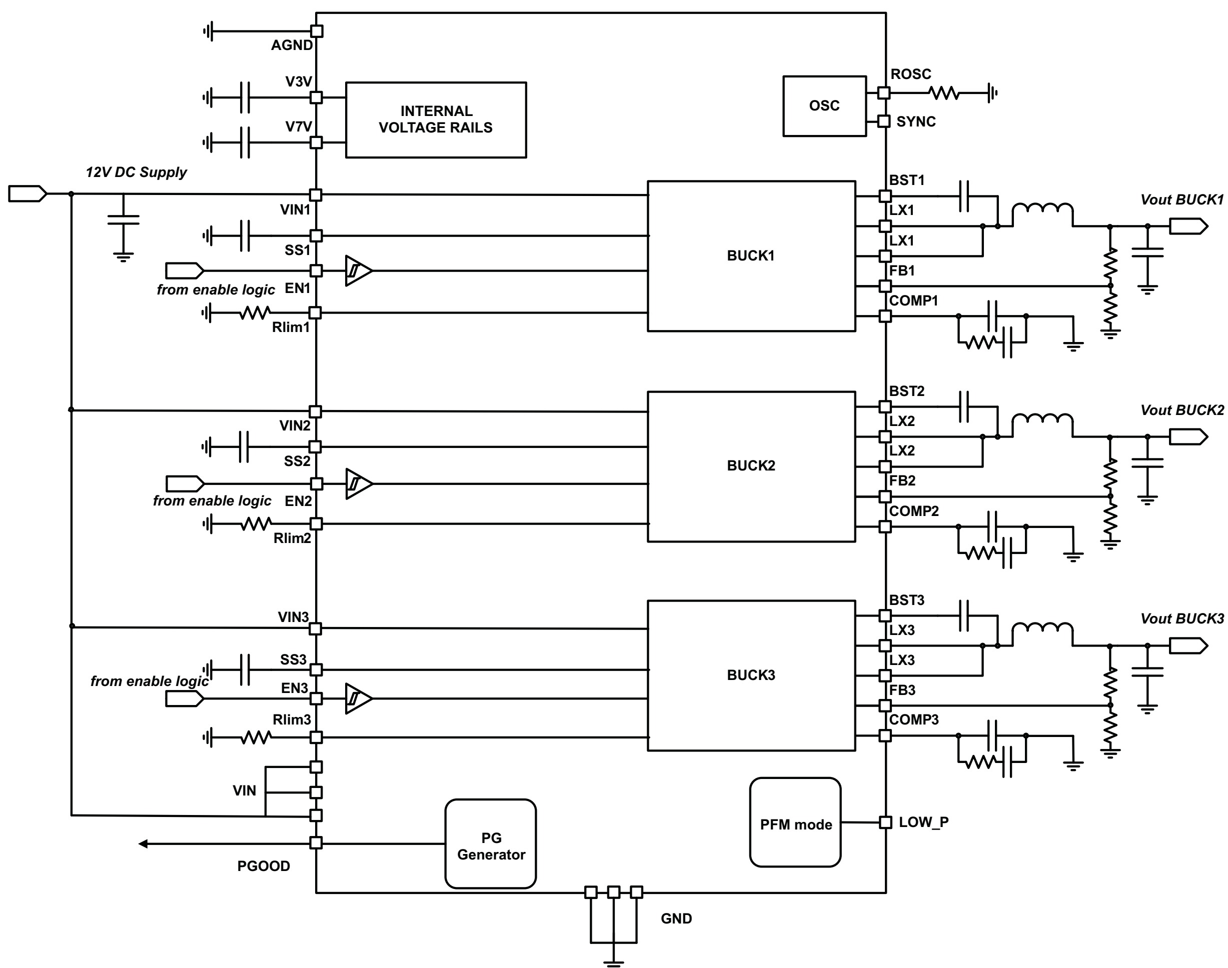
TPS65251 also features a light load pulse skipping mode (PSM) by allowing the LOW_P pin tied to V3V. The PSM mode allows for a reduction on the input power supplied to the system when the host processor is in stand-by (low activity) mode.


TPS 65251
GPIO or GND
C1
C2
PG
FB 2
R22
C24
C25
C26
R23
V2
C21
R20
C23
FB 2
R21
C27
4.7nF
C20
VIN 2
L2
L1
AGND
V3V
V7V
PGOOD
GND
LOW_P
FB2
CMP2
SS2
RLIM2
GND
VIN
VIN
VIN
GND
LX3
LX3
VIN3
BST3
EN3
EN2
BST2
VIN2
LX2
LX2
LX1
LX1
VIN1
BST1
EN1
VIN
L3
4.7uH
V3
C31
C30
VIN 3
C37
R33
120 K
R30
C33
R31
RLIM3
SS3
CMP3
FB3
SYNC
ROSC
FB1
CMP1
SS1
RLIM1
V1
VIN 1
C10
C11
C17
R13
C13
R10
C16
R12
C14
R11
C36
R1
C34
R32
C35
GPIO or GND
C15

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

FUNCTIONAL BLOCK DIAGRAM

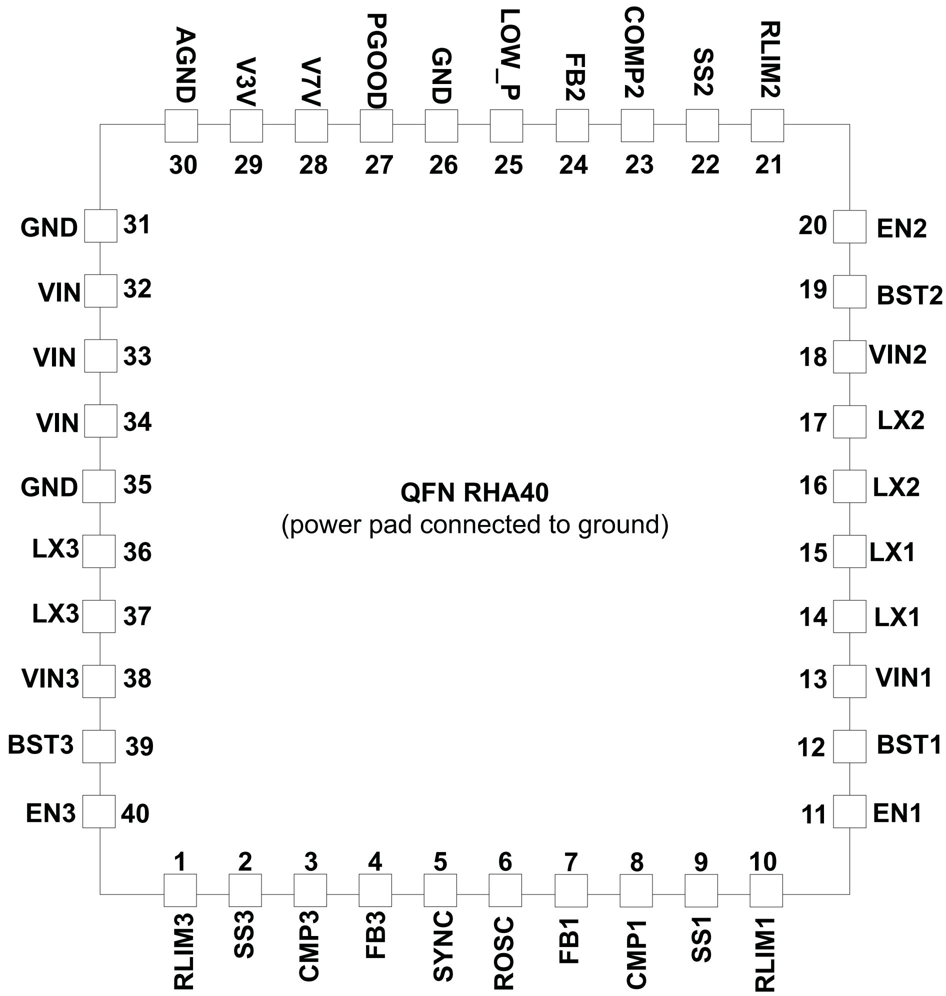


ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	40-pin (QFN) - RHA	Reel of 2500	TPS65251RHAR	TPS65251
		Reel of 250	TPS65251RHAT	

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

PIN OUT


AGND
V3V
V7V
PGOOD
GND
LOW_P
FB2
COMP2
SS2
RLIM2
30
29
28
27
26
25
24
23
22
21
GND 31
VIN 32
VIN 33
VIN 34
GND 35
LX3 36
LX3 37
VIN3 38
BST3 39
EN3 40
20 EN2
19 BST2
18 VIN2
17 LX2
16 LX2
15 LX1
14 LX1
13 VIN1
12 BST1
11 EN1
QFN RHA40
(power pad connected to ground)
1
2
3
4
5
6
7
8
9
10
RLIM3
SS3
CMP3
FB3
SYNC
ROSC
FB1
CMP1
SS1
RLIM1

TERMINAL FUNCTIONS (DCA)

NAME	NO.	I/O	DESCRIPTION
RLIM3	1	I	Current limit setting for Buck 3. Fit a resistor from this pin to ground to set the peak current limit on the output inductor.
SS3	2	I	Soft start pin for Buck 3. Fit a small ceramic capacitor to this pin to set the converter soft start time.
COMP3	3	O	Compensation for Buck 3. Fit a series RC circuit to this pin to complete the compensation circuit of this converter.
FB3	4	I	Feedback input for Buck 3. Connect a divider set to 0.8V from the output of the converter to ground.
SYNC	5	I	Synchronous clock input. If there is a sync clock in the system, connect to the pin. When not used connect to GND.
ROSC	6	I	Oscillator set. This resistor sets the frequency of internal autonomous clock. If external synchronization is used resistor should be fitted and set to ~70% of external clock frequency.
FB1	7	I	Feedback pin for Buck 1. Connect a divider set to 0.8 V from the output of the converter to ground.
COMP1	8	O	Compensation pin for Buck 1. Fit a series RC circuit to this pin to complete the compensation circuit of this converter.
SS1	9	I	Soft start pin for Buck 1. Fit a small ceramic capacitor to this pin to set the converter soft start time.
RLIM1	10	I	Current limit setting pin for Buck 1. Fit a resistor from this pin to ground to set the peak current limit on the output inductor.
EN1	11	I	Enable pin for Buck 1. A low level signal on this pin disables it. If pin is left open a weak internal pull-up to V3V will allow for automatic enable. For a delayed start-up add a small ceramic capacitor from this pin to ground.
BST1	12	I	Bootstrap capacitor for Buck 1. Fit a 47-nF ceramic capacitor from this pin to the switching node.
VIN1	13	I	Input supply for Buck 1. Fit a 10-µF ceramic capacitor close to this pin.
LX1	14, 15	O	Switching node for Buck 1
LX2	16, 17	O	Switching node for Buck 2
VIN2	18	I	Input supply for Buck 2. Fit a 10-µF ceramic capacitor close to this pin.
BST2	19	I	Bootstrap capacitor for Buck 2. Fit a 47-nF ceramic capacitor from this pin to the switching node.
EN2	20	I	Enable pin for Buck 2. A low level signal on this pin disables it. If pin is left open a weak internal pull-up to V3V will allow for automatic enable. For a delayed start-up add a small ceramic capacitor from this pin to ground.
RLIM2	21	I	Current limit setting for Buck 2. Fit a resistor from this pin to ground to set the peak current limit on the output inductor.
SS2	22	I	Soft start pin for Buck 2. Fit a small ceramic capacitor to this pin to set the converter soft start time.
COMP2	23	O	Compensation pin for Buck 2. Fit a series RC circuit to this pin to complete the compensation circuit of this converter
FB2	24	I	Feedback input for Buck 2. Connect a divider set to 0.8 V from the output of the converter to ground.
LOW_P	25	I	Low power operation mode(active high) input for TPS65251
GND	26		Ground pin
PGOOD	27	O	Power good. Open drain output asserted after all converters are sequenced and within regulation. Polarity is factory selectable (active high default).
V7V	28	O	Internal supply. Connect a 10-µF ceramic capacitor from this pin to ground.
V3V	29	O	Internal supply. Connect a 3.3-µF to 10-µF ceramic capacitor from this pin to ground.
AGND	30		Analog ground. Connect all GND pins and the power pad together.
GND	31		Ground pin

TERMINAL FUNCTIONS (DCA) (continued)

NAME	NO.	I/O	DESCRIPTION
VIN	32	I	Input supply
VIN	33	I	Input supply
VIN	34	I	Input supply
GND	35		Ground pin
LX3	36, 37	O	Switching node for Buck 3
VIN3	38		Input supply for Buck 3. Fit a 10-µF ceramic capacitor close to this pin.
BST3	39	I	Bootstrap capacitor for Buck 3. Fit a 47-nF ceramic capacitor from this pin to the switching node.
EN3	40	I	Enable pin for Buck 3. A low level signal on this pin disables it. If pin is left open a weak internal pull-up to V3V will allow for automatic enable. For a delayed start-up add a small ceramic capacitor from this pin to ground.
PAD			Power pad. Connect to ground.

ABSOLUTE MAXIMUM RATINGS (1)

over operating free-air temperature range (unless otherwise noted)

	Voltage range at VIN1,VIN2, VIN3, LX1, LX2, LX3	–0.3 to 18	V
	Voltage range at LX1, LX2, LX3 (maximum withstand voltage transient < 10 ns)	–1 to 18	V
	Voltage at BST1, BST2, BST3, referenced to Lx pin	–0.3 to 7	V
	Voltage at V7V, COMP1, COMP2, COMP3	–0.3 to 7	V
	Voltage at V3V, RLIM1, RLIM2, RLIM3, EN1,EN2,EN3, SS1, SS2,SS3, FB1, FB2, FB3, PGOOD, SYNC, ROSC, LOW_P	–0.3 to 3.6	V
	Voltage at AGND, GND	–0.3 to 0.3	V
T_J	Operating virtual junction temperature range	–40 to 125	°C
T_{STG}	Storage temperature range	–55 to 150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VIN	Input operating voltage	4.5		18	V
T_J	Junction temperature	–40		125	°C

ELECTROSTATIC DISCHARGE (ESD) PROTECTION

	MIN	MAX	UNIT
Human body model (HBM)	2000		V
Charge device model (CDM)	500		V

PACKAGE DISSIPATION RATINGS(1)

PACKAGE	θ_{JA} (°C/W)	T_A = 25°C POWER RATING (W)	T_A = 55°C POWER RATING (W)	T_A = 85°C POWER RATING (W)
RHA	30	3.33	2.3	1.3

(1) Based on JEDEC 51.5 HIGH K environment measured on a 76.2 x 114 x .6-mm board with the following layer arrangement:
(a) Top layer: 2 Oz Cu, 6.7% coverage
(b) Layer 2: 1 Oz Cu, 90% coverage
(c) Layer 3: 1 Oz Cu, 90% coverage
(d) Bottom layer: 2 Oz Cu, 20% coverage

ELECTRICAL CHARACTERISTICS

T_J = -40°C to 125°C, VIN = 12 V, f_{SW} = 1 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY UVLO AND INTERNAL SUPPLY VOLTAGE						
V_{IN}	Input Voltage range		4.5		18	V
IDD_{SDN}	Shutdown	EN pin = low for all converters		1.3		mA
IDD_{Q}	Quiescent, low power disabled (Lo)	Converters enabled, no load Buck 1 = 3.3 V, Buck 2 = 2.5 V, Buck 3 = 7.5 V, L = 4.7 µH , f_{SW} = 800 kHz		20		mA
$IDD_{Q\_LOW\_P}$	Quiescent, low power enabled (Hi)	Converters enabled, no load Buck 1 = 3.3 V, Buck 2 = 2.5 V, Buck 3 = 7.5 V, L = 4.7 µH , f_{SW} = 800 kHz		1.5		mA
$UVLO_{VIN}$	V_{IN} under voltage lockout	Rising V_{IN}		4.22		V
		Falling V_{IN}		4.1		
$UVLO_{DEGLITCH}$		Both edges		110		µs
V_{3V}	Internal biasing supply	I_{LOAD} = 0 mA	3.2	3.3	3.4	V
I_{3V}	Biasing supply output current	V_{IN} = 12 V			10	mA
V_{7V}	Internal biasing supply	I_{LOAD} = 0 mA	5.63	6.25	6.88	V
I_{7V}	Biasing supply output current	V_{IN} = 12 V			10	mA
$V7V_{UVLO}$	UVLO for internal V7V rail	Rising V7V		3.8		V
		Falling V7V		3.6		
$V7V_{UVLO\_DEGLITCH}$		Falling edge		110		µs
BUCK CONVERTERS (ENABLE CIRCUIT, CURRENT LIMIT, SOFT START, SWITCHING FREQUENCY AND SYNC CIRCUIT, LOW POWER MODE)						
V_{IH}	Enable threshold high	V3p3 = 3.2 V - 3.4 V, V_{ENX} rising	1.55		1.82	V
	Enable high level	External GPIO, V_{ENX} rising	0.66 x V_{3V}			
V_{IL}	Enable threshold low	V3p3 = 3.2 V - 3.4 V, V_{ENX} falling	0.98		1.24	V
	Enable low level	External GPIO, V_{ENX} falling			0.33 x V_{3V}	
R_{EN_DIS}	Enable discharge resistor		-10%	2.1	10%	kΩ
ICH_{EN}	Pull up current enable pin			1.1		µA
t_D	Discharge time enable pins	Power-up		10		ms
I_{SS}	Soft start pin current source			5		µA
F_{SW_BK}	Converter switching frequency range	Set externally with resistor	0.3		2.2	MHz
R_{FSW}	Frequency setting resistor	Depending on set frequency	50		600	kΩ
f_{SW_TOL}	Internal oscillator accuracy	f_{SW} = 800 kHz	-10		10	%
V_{SYNCH}	External clock threshold high	V3p3 = 3.3 V	1.55			V
V_{SYNCL}	External clock threshold Low	V3p3 = 3.3 V			1.24	V
$SYNC_{RANGE}$	Synchronization range		0.2		2.2	MHz
$SYNC_{CLK\_MIN}$	Sync signal minimum duty cycle		40			%
$SYNC_{CLK\_MAX}$	Sync signal maximum duty cycle				60	%
VIH_{LOW_P}	Low power mode threshold high	V3p3 = 3.3 V, V_{ENX} rising	1.55			V
VIL_{LOW_P}	Low power mode threshold Low	V3p3 = 3.3 V, V_{ENX} falling	0.98		1.24	V

ELECTRICAL CHARACTERISTICS (continued)

T_J = -40°C to 125°C, VIN = 12 V, f_{SW} = 1 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FEEDBACK, REGULATION, OUTPUT STAGE						
V_{FB}	Feedback voltage	V_{IN} = 12V T_J = 25°C	-1%	0.8	1%	V
		V_{IN} = 4.5 to 18V	-2%	0.8	2%	
I_{FB}	Feedback leakage current				50	nA
t_{ON_MIN}	Minimum on time (current sense blanking)			80	120	ns
$V_{LINEREG}$	Line regulation - DC $\Delta V_{OUT}/\Delta V_{INB}$	V_{INB} = 4.5 V to 18 V, I_{OUT} = 1000 mA		0.5		% V_{OUT}
$V_{LOADREG}$	Load regulation - DC $\Delta V_{OUT}/\Delta I_{OUT}$	I_{OUT} = 10 % - 90% $I_{OUT,MAX}$		0.5		% V_{OUT}/A
MOSFET (BUCK 1)						
H.S. Switch	Turn-On resistance high side FET on CH1	V_{IN} = 12 V, T_J = 25°C		95		mΩ
L.S. Switch	Turn-On resistance low side FET on CH1	V_{IN} = 12 V, T_J = 25°C		50		mΩ
MOSFET (BUCK 2)						
H.S. Switch	Turn-On resistance high side FET on CH2	V_{IN} = 12 V, T_J = 25°C		120		mΩ
L.S. Switch	Turn-On resistance low side FET on CH2	V_{IN} = 12 V, T_J = 25°C		80		mΩ
MOSFET (BUCK 3)						
H.S. Switch	Turn-On resistance high side FET on CH3	V_{IN} = 12 V, T_J = 25°C		120		mΩ
L.S. Switch	Turn-On resistance low side FET on CH3	V_{IN} = 12 V, T_J = 25°C		80		mΩ
ERROR AMPLIFIER						
g_M	Error amplifier transconductance	–2 µA < I_{COMP} < 2 µA		130		µmhos
gm_{PS}	COMP to ILX g_M	ILX = 0.5 A		10		A/V
POWER GOOD RESET GENERATOR						
VUV_{BUCKX}	Threshold voltage for buck under voltage	Output falling (device will be disabled after t_{ON_HICCUP})		85		%
		Output rising (PG will be asserted)		90		
$t_{UV\_deglitch}$	Deglitch time (both edges)	Each buck		11		ms
t_{ON_HICCUP}	Hiccup mode ON time	VUV_{BUCKX} asserted		12		ms
t_{OFF_HICCUP}	Hiccup mode OFF time before re-start is attempted	All converters disabled. Once t_{OFF_HICCUP} elapses, all converters will go through sequencing again.		15		ms
VOV_{BUCKX}	Threshold voltage for buck over voltage	Output rising (high side fet will be forced off)		109		%
		Output falling (high side fet will be allowed to switch)		107		
t_{RP}	minimum reset period	Measured after minimum reset period of all bucks power-up successfully		1		s
THERMAL SHUTDOWN						
T_{TRIP}	Thermal shut down trip point	Rising temperature		160		°C
T_{HYST}	Thermal shut down hysteresis	Device re-starts		20		°C
$T_{TRIP\_DEGLITCH}$	Thermal shut down deglitch			110		µs
CURRENT LIMIT PROTECTION						
$RLIM_1$	Limit resistance range Buck 1		75		300	kΩ
$RLIM_{2\&3}$	Limit resistance range Bucks 2 and 3		100		300	kΩ
$ILIM_1$	Buck 1 adjustable current limit range	V_{IN} = 12 V, f_{SW} = 500 kHz, see Figure 24	1.2		5.5	A
$ILIM_2$	Buck 2 adjustable current limit range	V_{IN} = 12 V, f_{SW} = 500 kHz, see Figure 25	1		4.1	A
$ILIM_3$	Buck 3 adjustable current limit range	V_{IN} = 12 V, f_{SW} = 500 kHz, see Figure 26	1.3		4.4	A

TYPICAL CHARACTERISTICS

Buck 1

T_A = 25°C, V_{IN} = 12 V, f_{SW} = 1.1 MHz (unless otherwise noted)

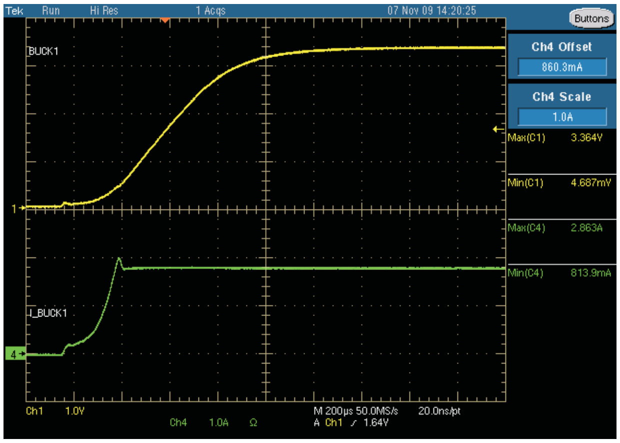


Figure 1. Start-Up
L_O = 4.7 µH, C_O = 22 µF, V_{OUT} = 3.3 V, 2 A

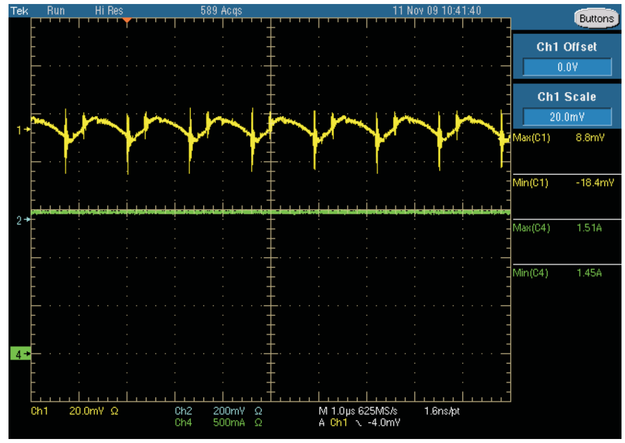


Figure 2. Ripple
V_{OUT} = 3.3 V, 1.5 A, f_{SW} = 800 kHz, 20 mV/div

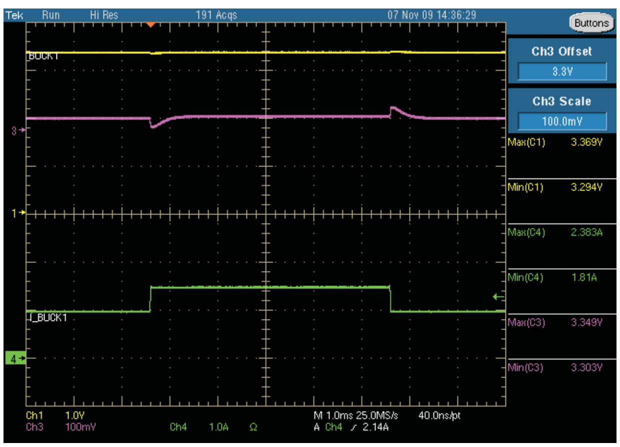


Figure 3. Transient Load Response
L_O = 4.7 µH, C_O = 22 µF, V_{OUT} = 3.3 V, ΔI = 1 A to 1.5 A, 100 mV/div

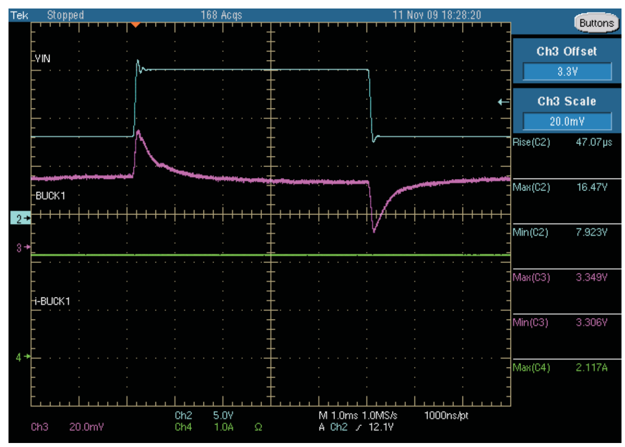


Figure 4. Transient Supply Response
L_O = 4.7 µH, C_O = 22 µF, V_{OUT} = 3.3 V, ΔV_{IN} = 8 V to 16.5 V, 20 mV/div

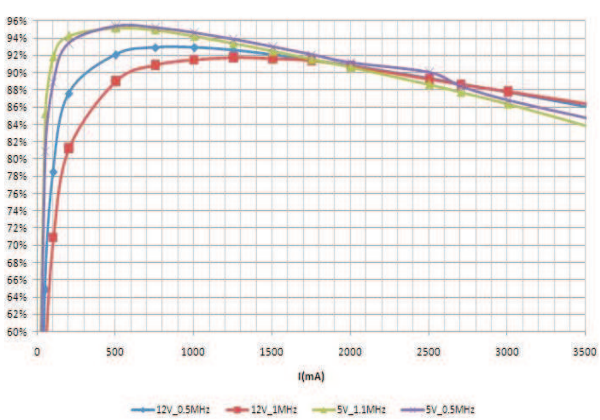


Figure 5. Efficiency
f_{SW} = 500 kHz, V_{OUT} = 3.3 V, L= 4.7 µH, DCR = 28 mΩ

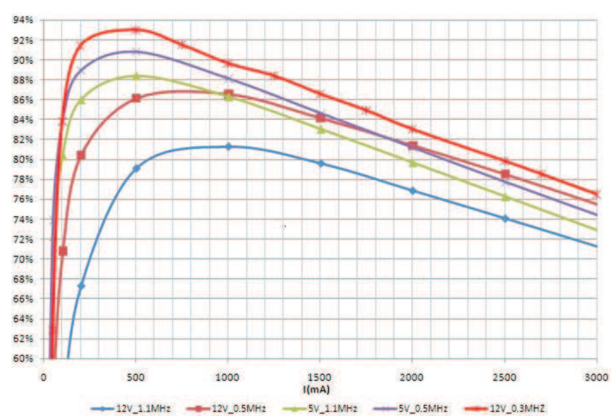


Figure 6. Efficiency
f_{SW} = 500 kHz, V_{OUT} = 1.2 V, L = 4.7 µH, DCR = 28 mΩ

TYPICAL CHARACTERISTICS (continued)

Buck 1

T_A = 25°C, V_{IN} = 12 V, f_{SW} = 1.1 MHz (unless otherwise noted)

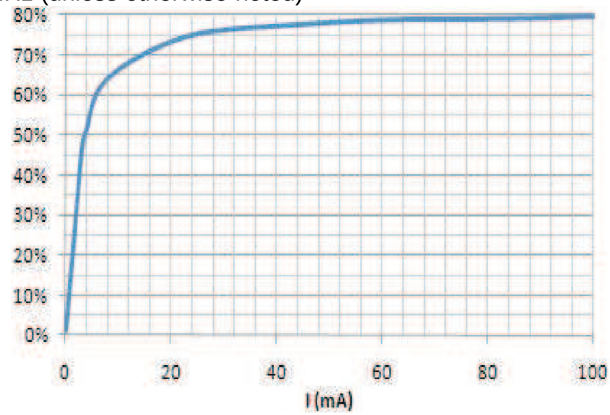


Figure 7. Efficiency Low Power Enabled
C_O = 22 µF, V_{OUT} = 3.3 V, L = 4.7 µH

TYPICAL CHARACTERISTICS

Buck 2

T_A = 25°C, V_{IN} = 12 V, f_{SW} = 1.14 MHz (unless otherwise noted)

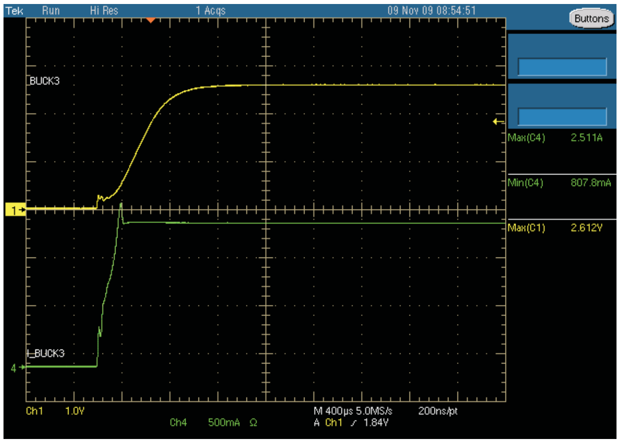


Figure 8. Start-Up
L_O = 4.7 µH, C_O = 22 µF, V_{OUT} = 2.5 V, 1.5 A

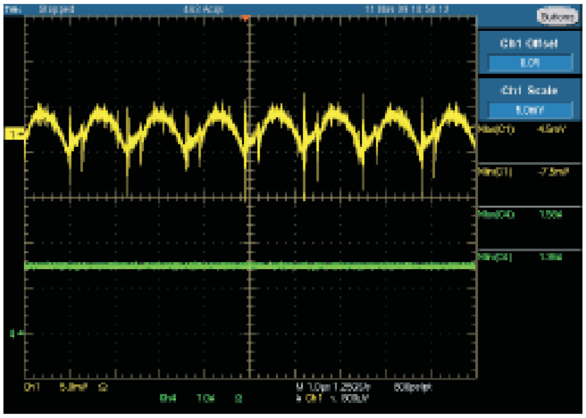


Figure 9. Ripple
V_{OUT} = 2.5 V, 1.5 A, f_{SW} = 800 kHz, 5 mV/div

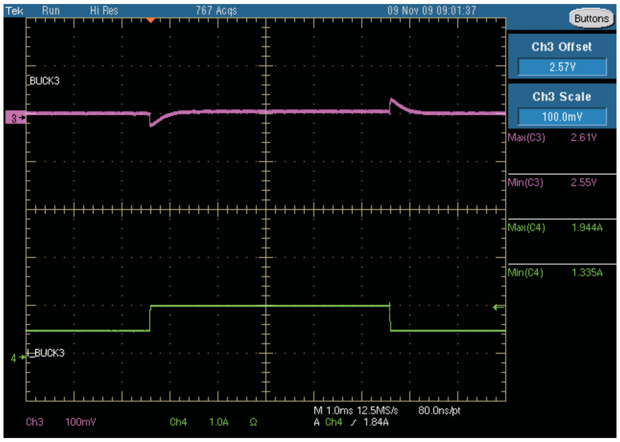


Figure 10. Transient Load Response
L_O = 4.7 µH, C_O = 22 µF, V_{OUT} = 2.5 V, ΔI = 1 A to 1.5 A

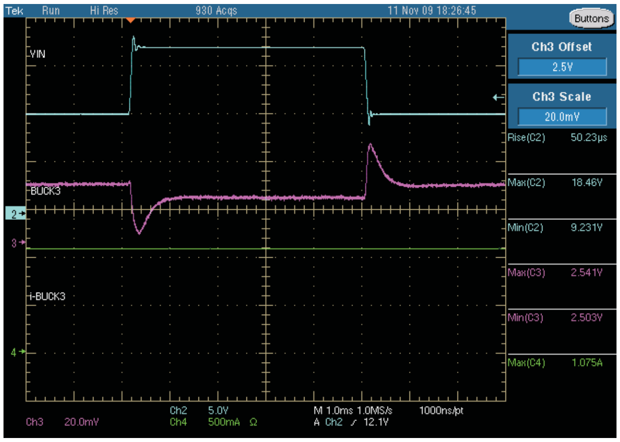


Figure 11. Transient Supply Response
L_O = 4.7 µH, C_O = 22 µF, V_{OUT} = 2.5 V, ΔV_{IN} = 9 V to 8 V

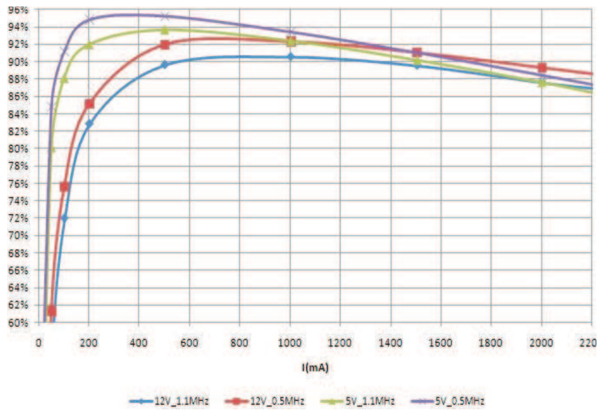


Figure 12. Efficiency
f_{SW} = 500 kHz, V_{OUT} = 3.3 V, L = 4.7 µH, DCR = 28 mΩ (Also Applies to Buck 3)

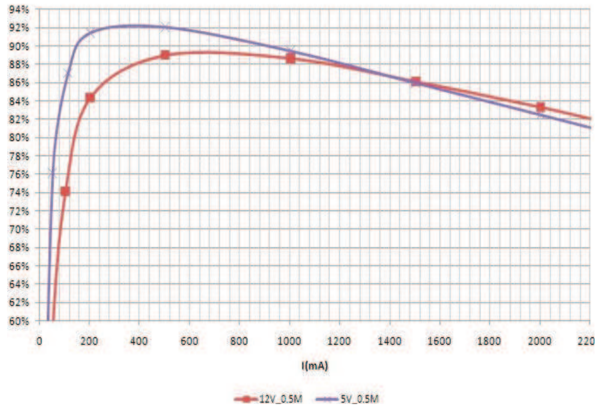


Figure 13. Efficiency
f_{SW} = 500 kHz, V_{OUT} = 1.8 V, L = 4.7 µH, DCR = 28 mΩ (Also Applies to Buck 3)

TYPICAL CHARACTERISTICS (continued)

Buck 2

T_A = 25°C, V_{IN} = 12 V, f_{SW} = 1.14 MHz (unless otherwise noted)

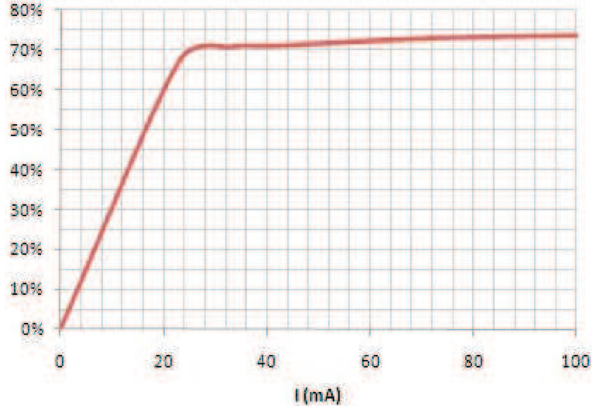


Figure 14. Efficiency Low Power Enabled
V_{OUT} = 2.5 V, L = 4.7 μF

TYPICAL CHARACTERISTICS

Buck 3

T_A = 25°C, V_{IN} = 12 V, f_{SW} = 1.14 MHz (unless otherwise noted)

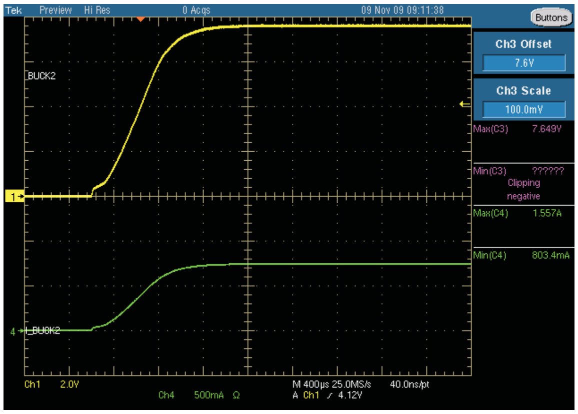


Figure 15. Start-Up
V_{OUT} = 7.5 V, 0.7 A

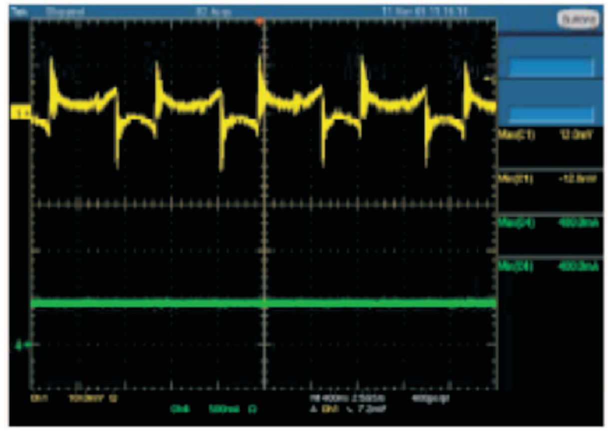


Figure 16. Ripple
V_{OUT} = 7.5 V, 0.5 A, f_{SW} = 800 kHz 5 mV/div

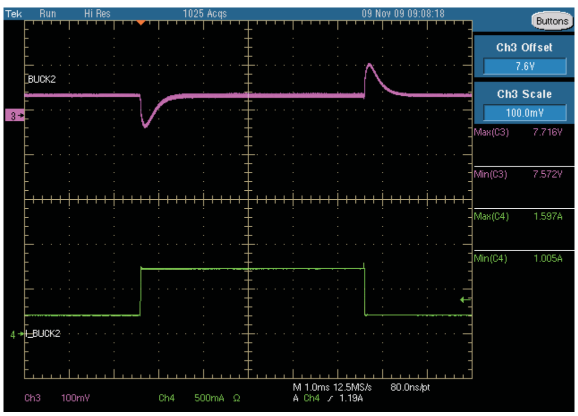


Figure 17. Transient Load Response
L_O = 4.7 µH, C_O = 22 µF, V_{OUT} = 7.5 V, ΔI = 1 A to 1.5 A

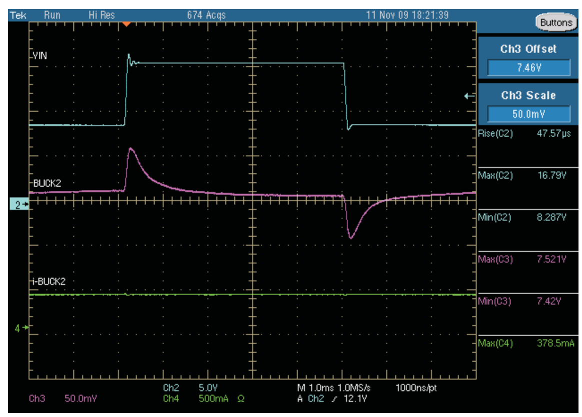


Figure 18. Transient Supply Response
V_{OUT} = 2.5 V, ΔV_{IN} = 9 V to 8 V

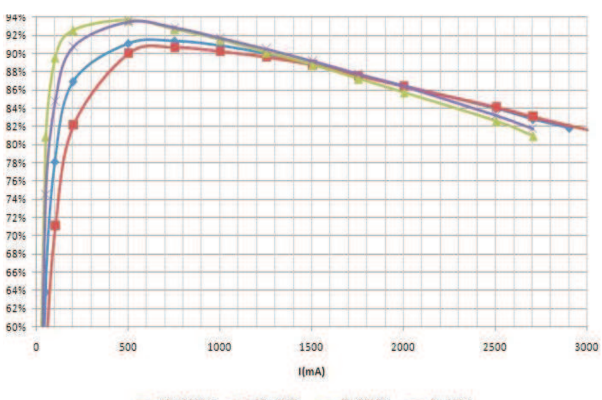


Figure 19. Efficiency
V_{OUT} = 2.5 V, L = 4.7 µH, DCR = 28 mΩ (Also Applies to Buck 2)

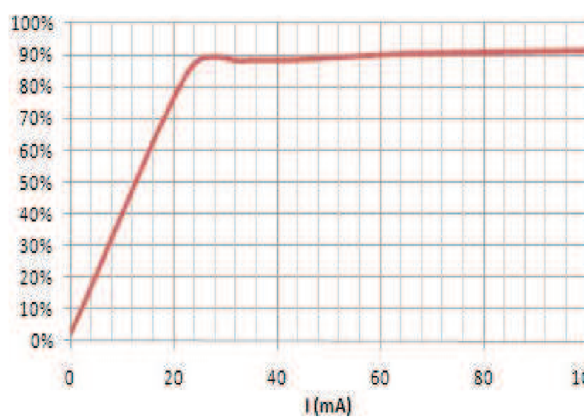
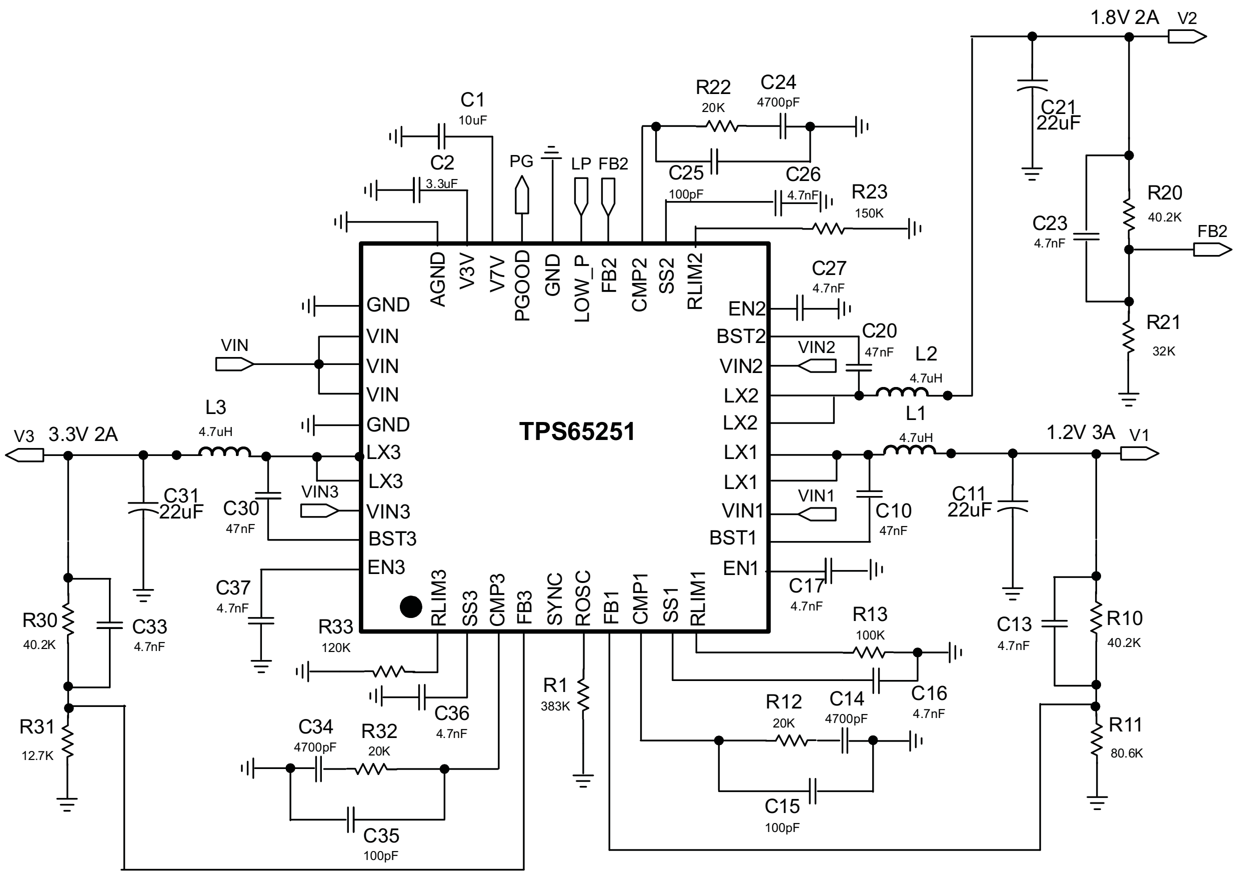


Figure 20. Efficiency Low Power Enabled
V_{OUT} = 2.5 V, L = 4.7 µF

TYPICAL APPLICATION CIRCUIT



A. VIN pins require local decoupling capacitors.

OVERVIEW

TPS65251 is a power management IC with three step-down buck converters. Both high-side and low-side MOSFETs are integrated to provide fully synchronous conversion with higher efficiency. TPS65251 can support 4.5-V to 18-V input supply, high load current, 300-kHz to 2.2-MHz clocking. The buck converters have an optional PSM mode, which can improve power dissipation during light loads. Alternatively, the device implements a constant frequency mode by connecting the LOW_P pin to ground. The wide switching frequency of 300 kHz to 2.2 MHz allows for efficiency and size optimization. The switching frequency is adjustable by selecting a resistor to ground on the ROSC pin. The SYNC pin also provides a means to synchronize the power converter to an external signal. Input ripple is reduced by 180 degree out-of-phase operation between Buck 1 and Buck 2. Buck 3 operates in phase with Buck 2.

All three buck converters have peak current mode control which simplifies external frequency compensation. A traditional type II compensation network can stabilize the system and achieve fast transient response. Moreover, an optional capacitor in parallel with the upper resistor of the feedback divider provides one more zero and makes the crossover frequency over 100 kHz.

Each buck converter has an individual current limit, which can be set up by a resistor to ground from the RLIM pin. The adjustable current limiting enables high efficiency design with smaller and less expensive inductors.

The device has two built-in LDO regulators. During a standby mode, the 3.3-V LDO and the 6.5-V LDO can be used to drive MCU and other active loads. By this, the system is able to turn off the three buck converters and improve the standby efficiency.

The device has a power good comparator monitoring the output voltage. Each converter has its own soft start and enable pins, which provide independent control and programmable soft start.

DETAILED DESCRIPTION

Adjustable Switching Frequency

To select the internal switching frequency connect a resistor from ROSC to ground. Figure 21 shows the required resistance for a given switching frequency.

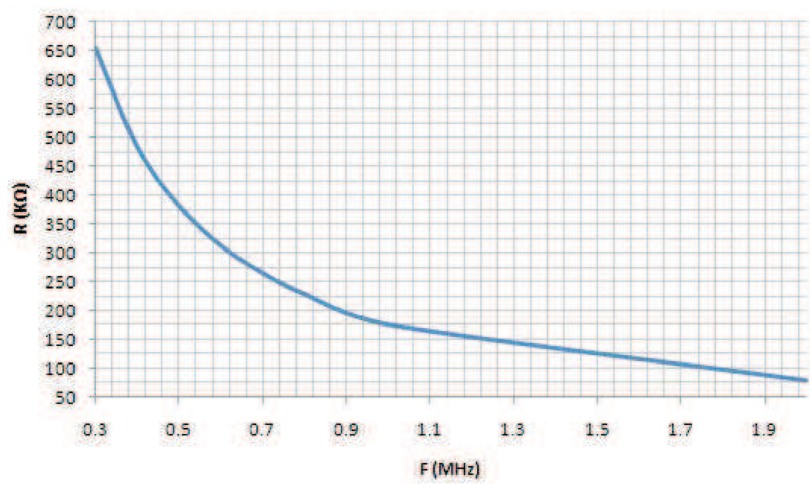


Figure 21. ROSC vs Switching Frequency

$$R_{OSC}(k\Omega) = 174 \bullet f(MHz)^{-1.122} \quad (1)$$

For operation at 800 kHz a 230-kΩ resistor is required.

Synchronization

The status of the SYNC pin will be ignored during start-up and the TPS65251's control will only synchronize to an external signal after the PGOOD signal is asserted. The status of the SYNC pin will be ignored during start-up and the TPS65251 will only synchronize to an external clock if the PGOOD signal is asserted. When synchronization is applied, the PWM oscillator frequency must be lower than the sync pulse frequency to allow the external signal trumping the oscillator pulse reliably. When synchronization is not applied, the SYNC pin should be connected to ground.

Out-of-Phase Operation

Buck 1 has a low conduction resistance compared to Buck 2 and 3. Normally Buck 1 is used to drive higher system loads. Buck 2 and 3 are used to drive some peripheral loads like I/O and line drivers . The combination of Buck 2 and 3's loads may be on par with Buck 1's. In order to reduce input ripple current, Buck 2 operates in phase with Buck 3; Buck 1 and Buck 2 operate 180 degrees out-of-phase. This enables the system, having less input ripple, to lower component cost, save board space and reduce EMI.

Delayed Start-Up

If a delayed start-up is required on any of the buck converters fit a ceramic capacitor to the ENx pins. The delay added is ~1.67 ms per nF connected to the pin. Note that the EN pins have a weak 1-µA pull-up to the 3V3 rail.

Soft Start Time

The device has an internal pull-up current source of 5 µA that charges an external slow start capacitor to implement a slow start time. Equation 2 shows how to select a slow start capacitor based on an expected slow start time. The voltage reference (V_{REF}) is 0.8 V and the slow start charge current (I_{SS}) is 5 µA. The soft start circuit requires 1 nF per 200 µS to be connected at the SS pin. A 1-ms soft-start time is implemented for all converters fitting 4.7 nF to the relevant pins.

$$T_{ss}(ms) = V_{REF}(V) \bullet \left(\frac{C_{ss}(nF)}{I_{ss}(\mu A)} \right) \tag{2}$$

Adjusting the Output Voltage

The output voltage is set with a resistor divider from the output node to the FB pin. It is recommended to use 1% tolerance or better divider resistors. In order to improve efficiency at light load, start with 40.2 kΩ for the R1 resistor and use the Equation 3 to calculate R2.

$$R2 = R1 \cdot \left(\frac{0.8V}{V_O - 0.8V} \right) \tag{3}$$

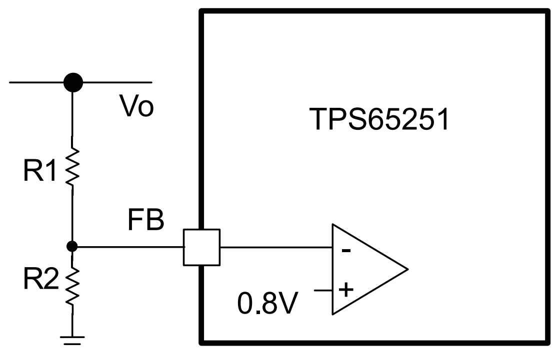


Figure 22. Voltage Divider Circuit

Input Capacitor

Use 10-µF X7R/X5R ceramic capacitors at the input of the converter inputs. These capacitors should be connected as close as physically possible to the input pins of the converters.

Bootstrap Capacitor

The device has three integrated boot regulators and requires a small ceramic capacitor between the BST and LX pin to provide the gate drive voltage for the high side MOSFET. The value of the ceramic capacitor should be 0.047 µF. A ceramic capacitor with an X7R or X5R grade dielectric is recommended because of the stable characteristics over temperature and voltage.

Error Amplifier

The device has a transconductance error amplifier. The frequency compensation network is connected between the COMP pin and ground.

Loop Compensation

TPS65251 is a current mode control dc/dc converter. The error amplifier is a transconductance amplifier with a of 130 µA/V.

A typical compensation circuit could be type II (R_c and C_c) to have a phase margin between 60 and 90 degrees, or type III (R_c, C_c and C_{ff}) to improve the converter transient response. C_{Roll} adds a high frequency pole to attenuate high-frequency noise when needed. . It may also prevent noise coupling from other rails if there is possibility of cross coupling in between rails when layout is very compact.

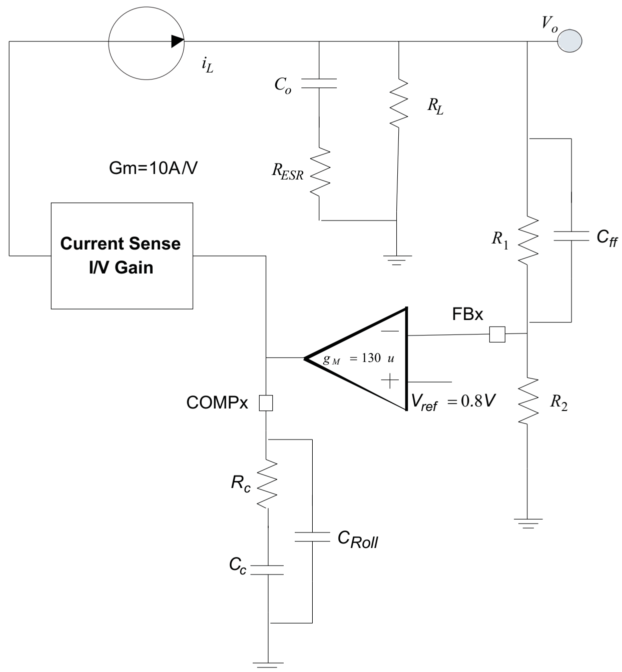


Figure 23. Loop Compensation

To calculate the external compensation components follow the following steps:

	TYPE II CIRCUIT	TYPE III CIRCUIT
Select switching frequency that is appropriate for application depending on L, C sizes, output ripple, EMI concerns and etc. Switching frequencies between 500 kHz and 1 MHz give best trade off between performance and cost. When using smaller L and Cs, switching frequency can be increased. To optimize efficiency, switching frequency can be lowered.		Type III circuit recommended for switching frequencies higher than 500 kHz.
Select cross over frequency (fc) to be less than 1/5 to 1/10 of switching frequency.	Suggested fc = fs/10	Suggested fc = fs/10
Set and calculate R_c.	$R_C = \frac{2\pi \cdot fc \cdot Vo \cdot Co}{g_M \cdot Vref \cdot gm_{ps}}$	$R_C = \frac{2\pi \cdot fc \cdot Co}{g_M \cdot gm_{ps}}$
Calculate C_c by placing a compensation zero at or before the converter dominant pole $fp = \frac{1}{C_O \cdot R_L \cdot 2\pi}$	$C_c = \frac{R_L \cdot Co}{R_c}$	$C_c = \frac{R_L \cdot Co}{R_c}$
Add C_{Roll} if needed to remove large signal coupling to high impedance COMP node. Make sure that $fp_{Roll} = \frac{1}{2 \cdot \pi \cdot R_C \cdot C_{Roll}}$ is at least twice the cross over frequency.	$C_{Roll} = \frac{\mathrm{Re}sr \cdot Co}{R_C}$	$C_{Roll} = \frac{\mathrm{Re}sr \cdot Co}{R_C}$
Calculate C_{ff} compensation zero at low frequency to boost the phase margin at the crossover frequency. Make sure that the zero frequency (fz_{ff} is smaller than soft start equivalent frequency ($1/T_{ss}$).	NA	$C_{ff} = \frac{1}{2 \cdot \pi \cdot fz_{ff} \cdot R_1}$

Slope Compensation

The device has a built-in slope compensation ramp. The slope compensation can prevent sub harmonic oscillations in peak current mode control.

Power Good

The PGOOD pin is an open drain output. The PGOOD pin is pulled low when any buck converter is pulled below 85% of the nominal output voltage. The PGOOD is pulled up when all three buck converters' outputs are more than 90% of its nominal output voltage and reset time of 1 second elapses. The polarity of the PGOOD is active high.

Current Limit Protection

Figure 24 shows the (peak) inductor current limit for Buck 1. The typical limit can be approximated with the following graph.

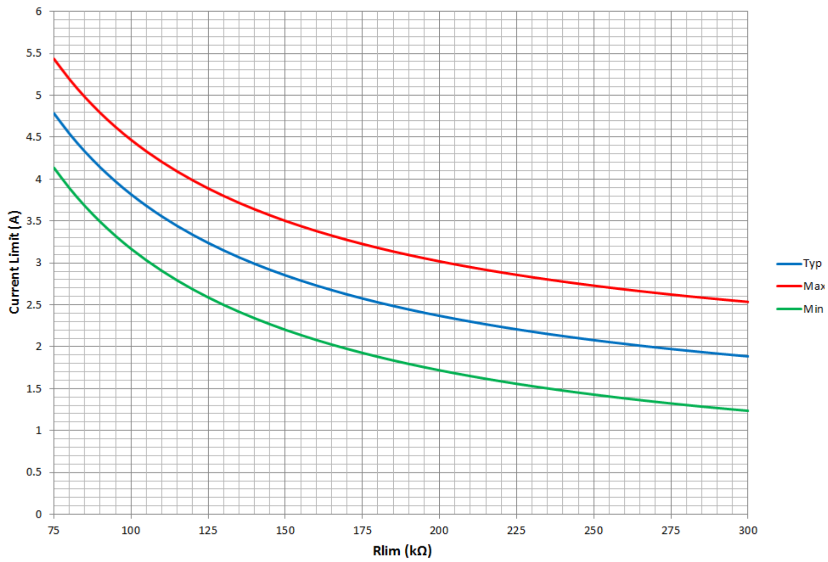


Figure 24. Buck 1

Figure 25 shows the (peak) inductor current limit for Buck 2. The typical limit can be approximated with the following graph.

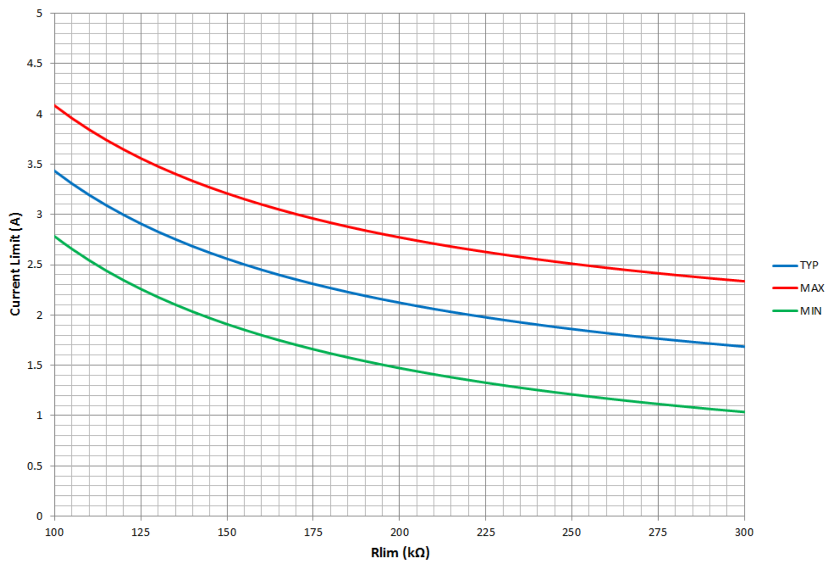


Figure 25. Buck 2

Figure 26 shows the (peak) inductor current limit for Buck 3. The typical limit can be approximated with the following graph.

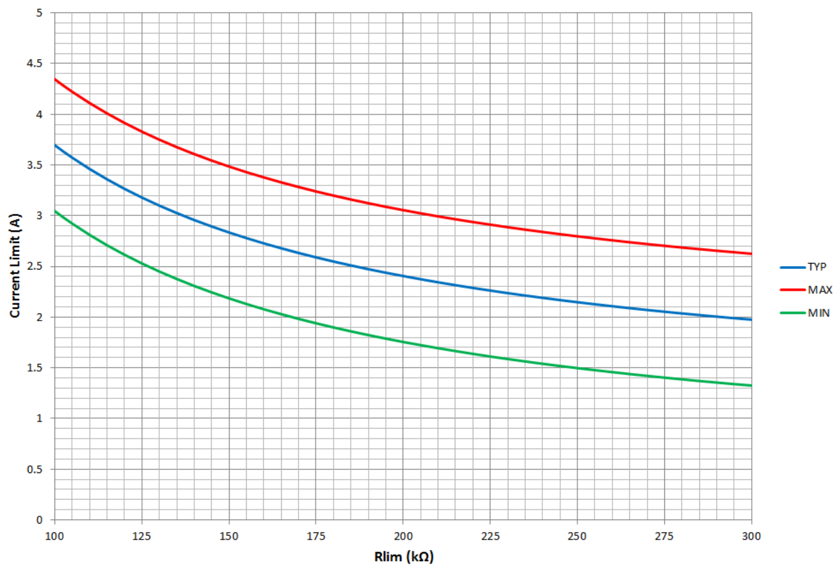


Figure 26. Buck 3

All converters operate in hiccup mode: Once an over-current lasting more than 10 ms is sensed in any of the converters, all the converters will shut down for 10 ms and then the start-up sequencing will be tried again. If the overload has been removed, the converter will ramp up and operate normally. If this is not the case the converter will see another over-current event and shuts-down again repeating the cycle (hiccup) until the failure is cleared.

If an overload condition lasts for less than 10 ms, only the relevant converter affected will go into and out of under-voltage and no global hiccup mode will occur. The converter will be protected by the cycle-by-cycle current limit during that time.

Overvoltage Transient Protection

The device incorporates an overvoltage transient protection (OVP) circuit to minimize voltage overshoot. The OVP feature minimizes the output overshoot by implementing a circuit to compare the FB pin voltage to OVP threshold which is 109% of the internal voltage reference. If the FB pin voltage is greater than the OVP threshold, the high side MOSFET is disabled preventing current from flowing to the output and minimizing output overshoot. When the FB voltage drops below the lower OVP threshold which is 107%, the high side MOSFET is allowed to turn on the next clock cycle.

Thermal Shutdown

The device implements an internal thermal shutdown to protect itself if the junction temperature exceeds 160°C. The thermal shutdown forces the device to stop switching when the junction temperature exceeds thermal trip threshold. Once the die temperature decreases below 140°C, the device reinitiates the power up sequence. The thermal shutdown hysteresis is 20°C.

Power Dissipation

The total power dissipation inside TPS65251 should not to exceed the maximum allowable junction temperature of 125°C. The maximum allowable power dissipation is a function of the thermal resistance of the package (R_{JA}) and ambient temperature.

To calculate the temperature inside the device under continuous loading use the following procedure.

1. Define the set voltage for each converter.
2. Define the continuous loading on each converter. Make sure do not exceed the converter maximum loading.
3. Determine from the graphs below the expected losses (Y axis) in watts per converter inside the device. The losses depend on the input supply, the selected switching frequency, the output voltage and the converter chosen.
4. To calculate the maximum temperature inside the IC use the following formula:

$$T_{HOT\_SPOT} = T_A + P_{DIS} \bullet \theta_{JA} \quad (4)$$

Where:

T_A is the ambient temperature

P_{DIS} is the sum of losses in all converters

θ_{JA} is the junction to ambient thermal impedance of the device and it is heavily dependant on board layout

BUCK 1 LOSSES (W)
vs
OUTPUT CURRENT
V_{IN} = 12 V, f_{SW} = 500 kHz
V_O (From Top to Bottom) = 5 V , 3.3 V, 2.5 V, 1.8 V, 1.2 V

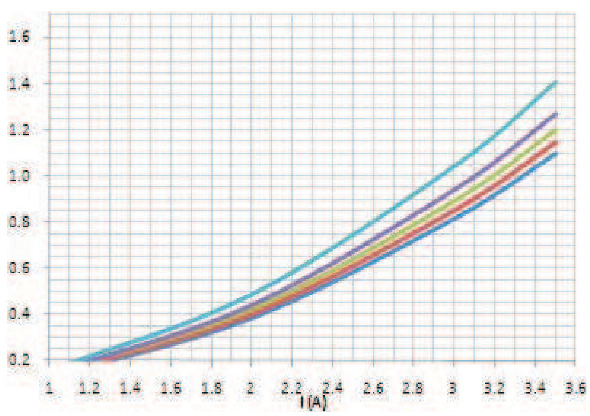


Figure 27.

BUCK 1 LOSSES (W)
vs
OUTPUT CURRENT
V_{IN} = 12 V, f_{SW} = 1.1 MHz
V_O (From Top to Bottom) = 5 V , 3.3 V, 2.5 V, 1.8 V, 1.2 V

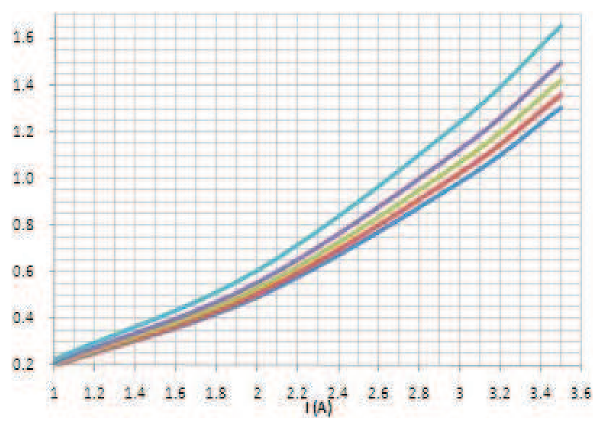


Figure 28.

BUCK 2 AND 3 LOSSES (W)
vs
OUTPUT CURRENT
V_{IN} = 12 V, f_{SW} = 500 kHz
V_O (From Top to Bottom) = 5 V , 3.3 V, 2.5 V, 1.8 V, 1.2 V

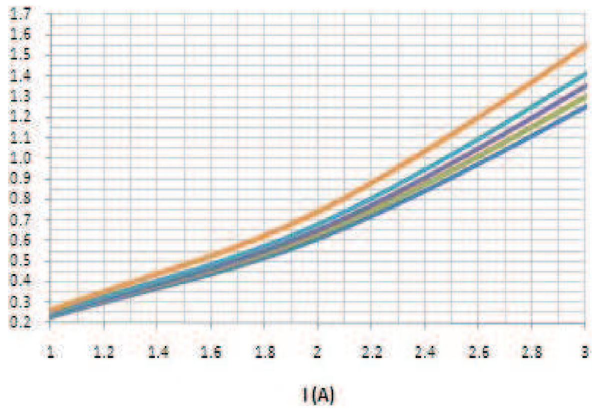


Figure 29.

BUCK 2 AND 3 LOSSES (W)
vs
OUTPUT CURRENT
V_{IN} = 12 V, f_{SW} = 1.1 MHz
V_O (From Top to Bottom) = 5 V , 3.3 V, 2.5 V, 1.8 V, 1.2 V

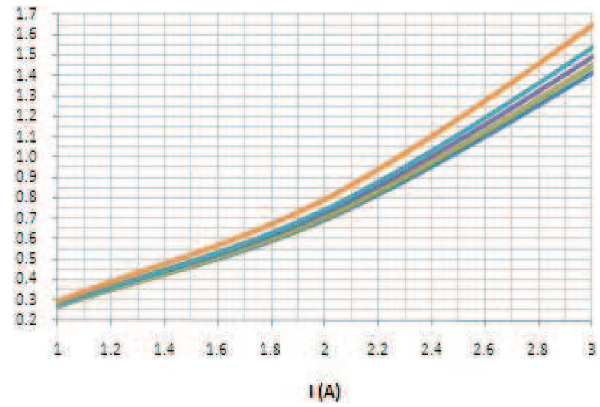


Figure 30.

Low Power Mode Operation

By pulling the Low_p pin high all converters will operate in pulse-skipping mode, greatly reducing the overall power consumption at light and no load conditions. Although each buck converter has a skip comparator that makes sure regulation is not lost when a heavy load is applied and low power mode is enabled, system design needs to make sure that the LP pin is pulled low for continuous loading in excess of 100 mA.

When low power is implemented, the peak inductor current used to charge the output capacitor is:

$$I_{LIMIT} = 0.25 \bullet T_{SLEEP\_CLK} \bullet \frac{V_{IN} - V_{OUT}}{L} \quad (5)$$

Where T_{SLEEP_CLK} is half of the converter switching period, $2/f_{SW}$.

The size of the additional ripple added to the output is:

$$\Delta V_{OUT} = \frac{1}{C} \bullet \left(\frac{L \bullet I_{LIMIT}{}^{2}}{2} \bullet \frac{V_{IN}}{V_{OUT} \bullet (V_{IN} - V_{OUT})} - \frac{I_{LOAD}}{f_{SLEEP\_CLK}} \right) \quad (6)$$

And the peak output voltage during low power operation is:

$$V_{OUT\_PK} = V_{OUT} + \frac{\Delta V_{OUT}}{2} \quad (7)$$

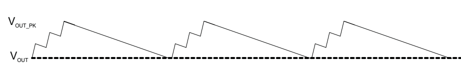


Figure 31. Peak Output Voltage During Low Power Operation

APPLICATION INFORMATION

Design Guide - Step-By-Step Design Procedure

The following example illustrates the design procedure for selecting external components for the three buck converters. The example focuses on Buck 1, but the procedure can be directly applied to Buck 2 and 3 as well. The design goal parameters are given in Table 1.

Table 1. Design Parameters

Output voltage	1.2 V
Transient response 0.5-A to 2-A load step	120 mV
Maximum output current	3 A
Input voltage	12 V nom, 9.6 V to 14.4 V
Output voltage ripple	< 30 mV p-p
Switching frequency	500 kHz

Typical Buck 1 Application Schematic

The application schematic of Buck 1 is shown in Figure 32. The design procedure is given below.

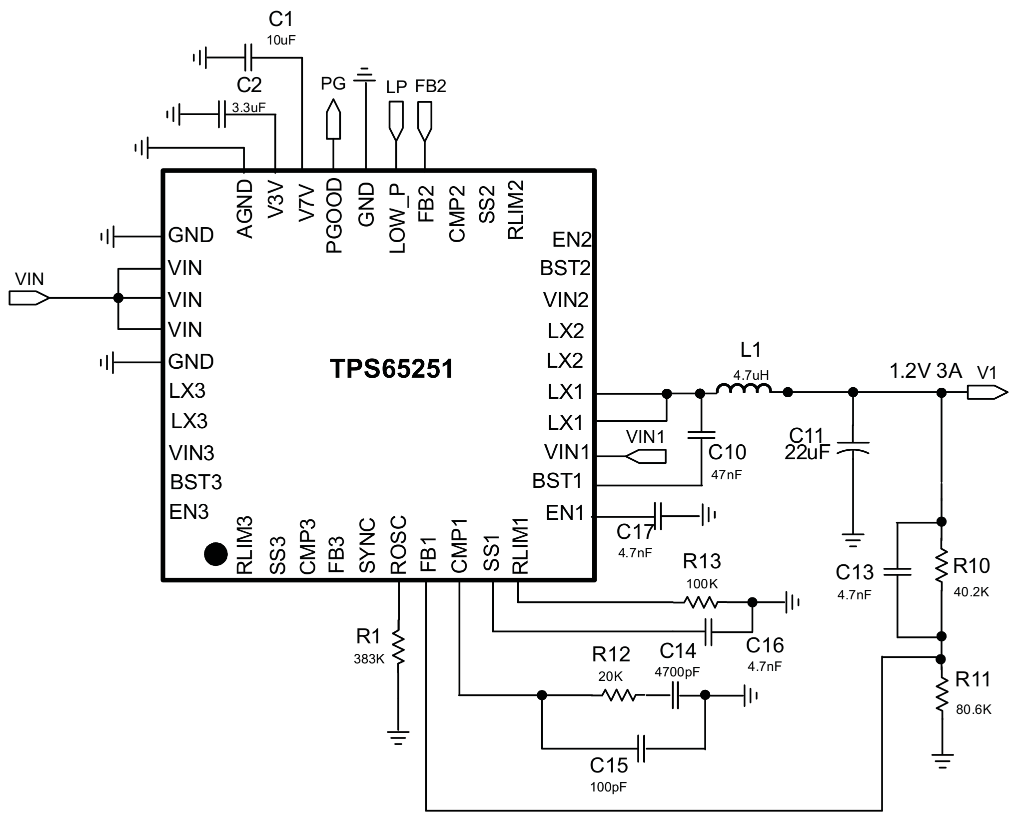


Figure 32. Typical Buck 1 Application Circuit

Selecting the Switching Frequency

The first step is to decide on a switching frequency for the regulator. Typically, you will want to choose the highest switching frequency possible since this will produce the smallest solution size. The high switching frequency allows for lower valued inductors and smaller output capacitors compared to a power supply that switches at a lower frequency. However, the highest switching frequency causes extra switching losses, which hurt the converter's performance. The converter is capable of running from 300 kHz to 2.2 MHz. Unless a small solution size is an ultimate goal, a moderate switching frequency of 500 kHz is selected to achieve both a small solution size and a high efficiency operation. Using Figure 21, R1 is determined to be 383 kΩ

Output Inductor Selection

To calculate the value of the output inductor, use Equation 8. KIND is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. In general, KIND is normally from 0.1 to 0.3 for the majority of applications.

For this design example, use KIND = 0.2 and the inductor value is calculated to be 3.6 µH. For this design, a nearest standard value was chosen: 4.7 µH. For the output filter inductor, it is important that the RMS current and saturation current ratings not be exceeded. The RMS and peak inductor current can be found from Equation 9 and Equation 10.

$$Lo = \frac{Vin - Vout}{Io \cdot K_{ind}} \cdot \frac{Vout}{Vin \cdot fsw} \tag{8}$$

$$Iripple = \frac{Vin - Vout}{Lo} \cdot \frac{Vout}{Vin \cdot fsw} \tag{9}$$

$$ILrms = \sqrt{Io^2 + \frac{1}{12} \cdot \left(\frac{Vo \cdot (Vin\max - Vo)}{Vin\max \cdot Lo \cdot fsw} \right)^2} \tag{10}$$

$$ILpeak = Iout + \frac{Iripple}{2} \tag{11}$$

Output Capacitor

There are two primary considerations for selecting the value of the output capacitor. The output capacitors are selected to meet load transient and output ripple's requirements.

Equation 12 gives the minimum output capacitance to meet the transient specification. For this example, L_O = 4.7 µH, ΔI_{OUT} = 1.5 A – 0.75 A = 0.75 A and ΔV_{OUT} = 120 mV. Using these numbers gives a minimum capacitance of 18 µF. A standard 22-µF ceramic capacitor is chose in the design.

$$Co > \frac{\Delta I_{OUT}{}^2 \cdot L_o}{V_{out} \cdot \Delta Vout} \tag{12}$$

Equation 13 calculates the minimum output capacitance needed to meet the output voltage ripple specification. Where fsw is the switching frequency, V_{RIPPLE} is the maximum allowable output voltage ripple, and I_{RIPPLE} is the inductor ripple current. In this case, the maximum output voltage ripple is 30 mV. From Equation 9, the output current ripple is 0.46 A. From Equation 13, the minimum output capacitance meeting the output voltage ripple requirement is 1.74 µF.

$$Co > \frac{1}{8 \cdot fsw} \cdot \frac{1}{\dfrac{Vripple}{Iripple}} \tag{13}$$

Additional capacitance de-rating for aging, temperature and DC bias should influence this minimum value. For this example, one 22-µF, 6.3-V X7R ceramic capacitor with 3 mΩ of ESR will be used.

Input Capacitor

A minimum 10-µF X7R/X5R ceramic input capacitor is recommended to be added between VIN and GND. These capacitors should be connected as close as physically possible to the input pins of the converters as they handle the RMS ripple current shown in Equation 14. For this example, I_{OUT} = 3 A, V_{OUT} = 1.2 V, V_{INmin} = 9.6 V, from Equation 14, the input capacitors must support a ripple current of 0.99 A RMS.

$$Icirms = Iout \cdot \sqrt{\frac{Vout}{Vin\min} \cdot \frac{(Vin\min - Vout)}{Vin\min}} \tag{14}$$

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 15. Using the design example values, I_{OUTmax} = 3 A, C_{IN} = 10 µF, f_{SW} = 500 kHz, yields an input voltage ripple of 150 mV.

$$\Delta Vin = \frac{Iout\max \cdot 0.25}{Cin \cdot fsw} \tag{15}$$

Soft Start Capacitor

The soft start capacitor determines the minimum amount of time it will take for the output voltage to reach its nominal programmed value during power up. This is useful if the output capacitance is very large and would require large amounts of current to quickly charge the capacitor to the output voltage level.

The soft start capacitor value can be calculated using Equation 16. In this example, the converter's soft start time is 0.8 ms. In TPS65251, Iss is 5 µA and Vref is 0.8 V. From Equation 16, the soft start capacitance is 5 nF. A standard 4.7-nF ceramic capacitor is chosen in this design. In this example, C16 is 4.7nF

$$Css(nF) = \frac{Tss(ms) \cdot Iss(uA)}{Vref(V)} \tag{16}$$

Bootstrap Capacitor Selection

A 0.047-µF ceramic capacitor must be connected between the BST to LX pin for proper operation. It is recommended to use a ceramic capacitor with X5R or better grade dielectric. The capacitor should have 10-V or higher voltage rating.

Adjustable Current Limiting Resistor Selection

The converter uses the voltage drop on the high-side MOSFET to measure the inductor current. The over current protection threshold can be optimized by changing the trip resistor. Figure 24 governs the threshold of over current protection for Buck 1. When selecting a resistor, do not exceed the graph limits. In this example, the over current threshold is 3.2 A. In order to prevent a premature limit trip, the minimum line is used and the resistor is 100 kΩ.

When setting high-side current limit to large current values, ensure that the additional load immediately prior to an overcurrent condition will not cause the switching node voltage to exceed 20 V. Additionally, ensure during worst case operation, with all bucks loaded immediately prior to current limit, the maximum virtual junction temperature of the device does not exceed 125°C.

Output Voltage and Feedback Resistors Selection

For the example design, 40.2 kΩ was selected for R10. Vout is 1.2 V, Vref = 0.8 V. Using Equation 17, R11 is calculated as 80.4 kΩ. A standard 80.6-kΩ resistor is chose in this design.

$$R11 = \frac{Vout - Vref}{Vref} R10 \tag{17}$$

Compensation

A type-II compensation circuit is adequate for the converter to have a phase margin between 60 and 90 degrees. The following equations show the procedure of designing a peak current mode control dc/dc converter.

The compensation design takes the following steps:

1. Set up the anticipated cross-over frequency. In this example, the anticipated cross-over frequency (fc) is 65 kHz. The power stage gain (gm_{PS}) is 10 A/V and the GM amplifier gain (g_M) is 130 µA/V.

$$R12 = \frac{2\pi \cdot fc \cdot Vo \cdot Co}{g_M \cdot Vref \cdot gm_{ps}} \tag{18}$$

2. Place compensation zero at low frequency to boost the phase margin at the crossover frequency. From the procedures above, the compensation network includes a 20-kΩ resistor (R12) and a 4700-pF capacitor (C1).
3. An additional pole can be added to attenuate high frequency noise.

From the procedures above, the compensation network includes a 20-kΩ resistor (R12) and a 4700-pF capacitor (C14).

3.3-V and 6.5-V LDO Regulators

The following ceramic capacitor (X7R/X5R) should be connected as close as possible to the described pins:

- 10 µF for V7V pin 28
- 3.3 µF to 10 µF for V3V pin 29

Layout Recommendation

Layout is a critical portion of PMIC designs.

- Place VOUT, and LX on the top layer and an inner power plane for VIN.
- Fit also on the top layer connections for the remaining pins of the PMIC and a large top side area filled with ground.
- The top layer ground area sould be connected to the internal ground layer(s) using vias at the input bypass capacitor, the output filter cpacitor and directly under the TPS65251 device to provide a thermal path from the Powerpad land to ground.
- The AGND pin should be tied directly to the power pad under the IC and the power pad.
- For operation at full rated load, the top side ground area together with the internal ground plane, must provide adequate heat dissipating area.
- There are several signals paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance. To help eliminate these problems, the VIN pin should be bypassed to ground with a low ESR ceramic bypass capacitor with X5R or X7R dielectric. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VIN pins, and the ground connections. Since the LX connection is the switching node, the output inductor should be located close to the LX pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling.
- The output filter capacitor ground should use the same power ground trace as the VIN input bypass capacitor. Try to minimize this conductor length while maintaining adequate width.
- The compensation should be as close as possible to the COMP pins. The COMP and OSC pins are sensitive to noise so the components associated to these pins should be located as close as possible to the IC and routed with minimal lengths of trace.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TPS65251RHAR	ACTIVE	VQFN	RHA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
TPS65251RHAT	ACTIVE	VQFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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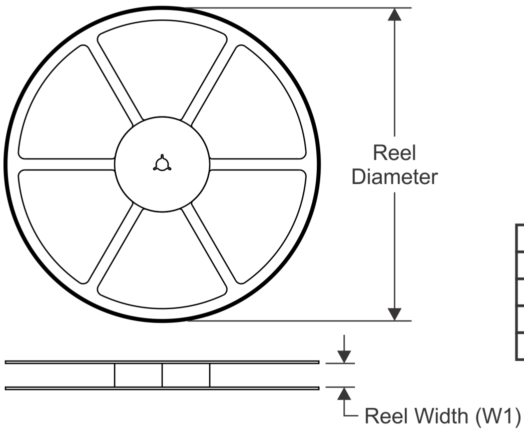
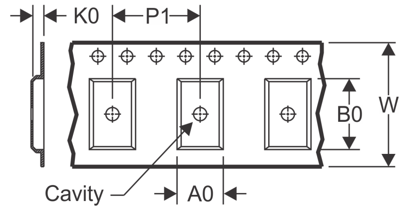
TAPE AND REEL INFORMATION

REEL DIMENSIONS

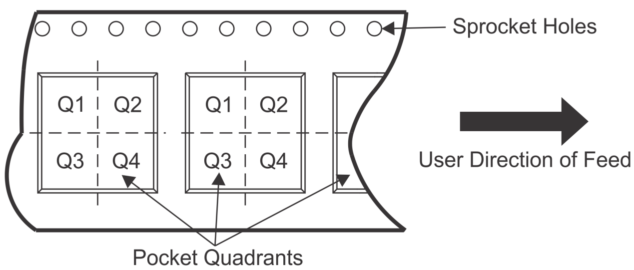


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

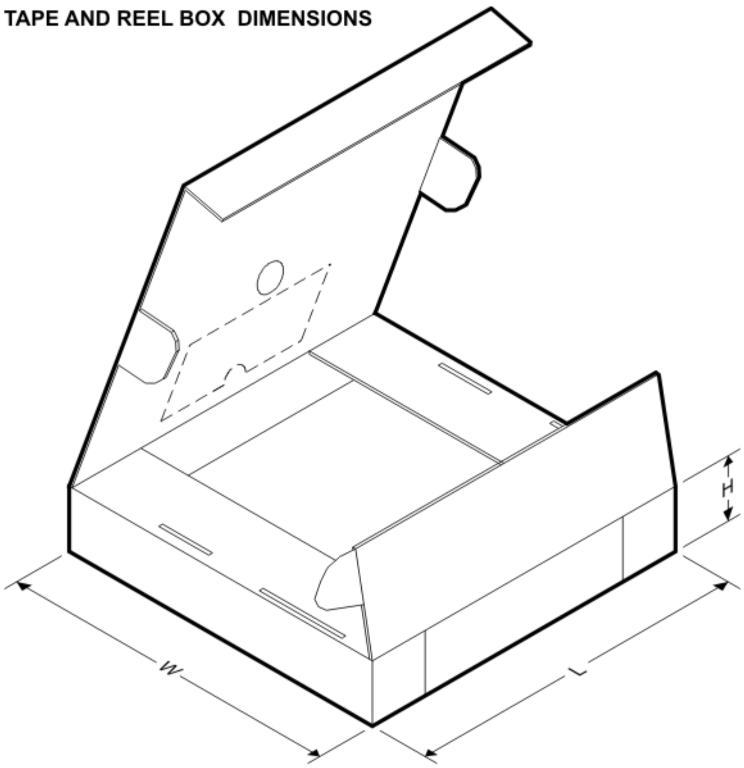
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65251RHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q2
TPS65251RHAT	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.5	12.0	16.0	Q2

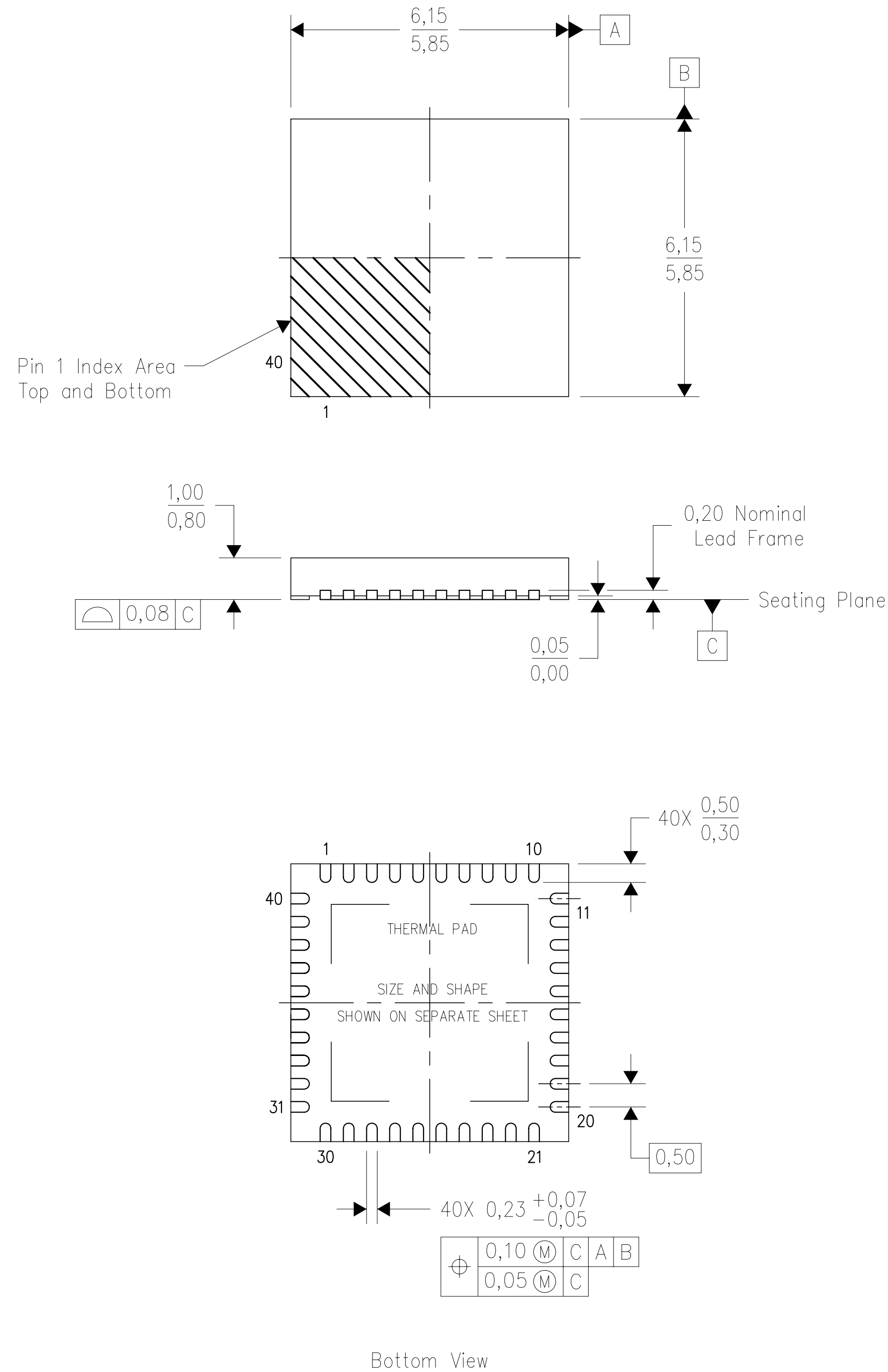
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65251RHAR	VQFN	RHA	40	2500	367.0	367.0	38.0
TPS65251RHAT	VQFN	RHA	40	250	210.0	185.0	35.0

RHA (S-PVQFN-N40) PLASTIC QUAD FLATPACK NO-LEAD



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NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No−Lead) Package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Package complies to JEDEC MO−220 variation VJJD−2.

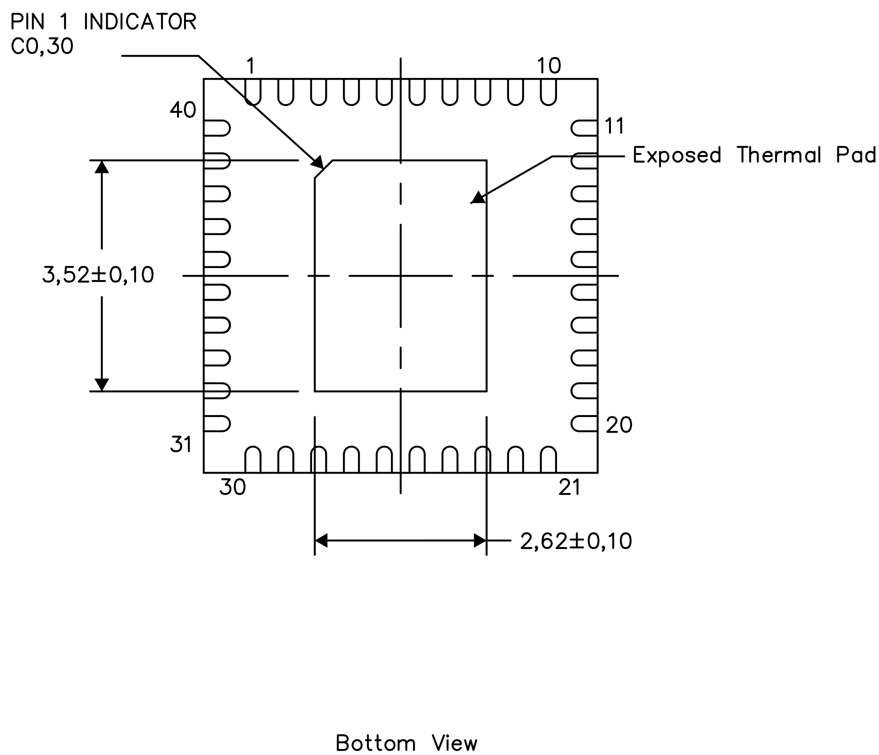
RHA (S–PVQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

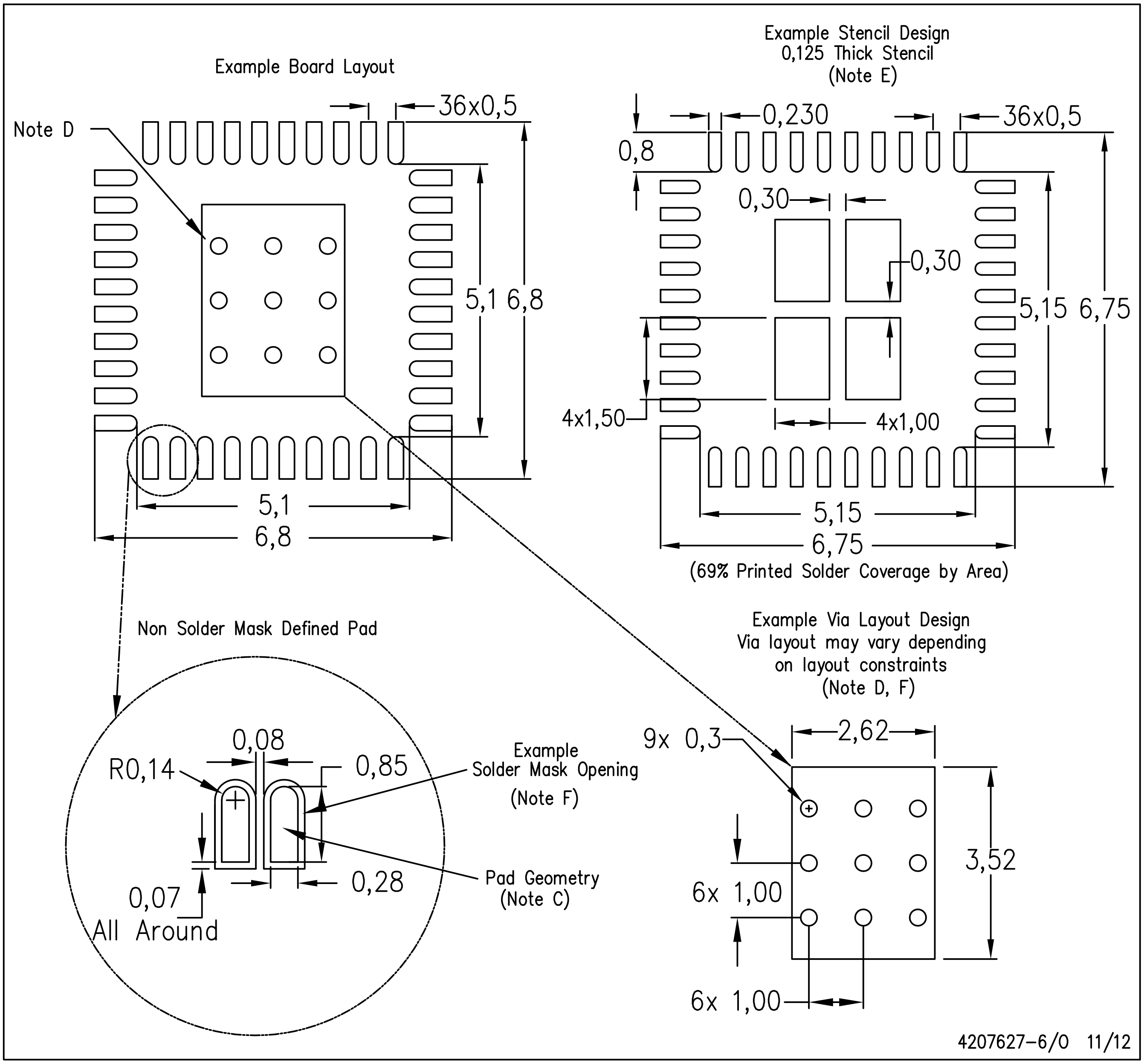


Exposed Thermal Pad Dimensions

4206355–9/T 11/12

NOTES: A. All linear dimensions are in millimeters

RHA (S-PVQFN-N40) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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