# 1.5-A 42-V STEP-DOWN SWIFT™ DC-DC CONVERTER WITH Eco-mode™ CONTROL

**Check for Samples: TPS57140-Q1**

## FEATURES

- **Qualified for Automotive Applications**
- **3.5-V to 42-V Input Voltage Range**
- **200-mΩ High-Side MOSFET**
- **High Efficiency at Light Loads With Pulse-Skipping Eco-mode™ Control Scheme**
- **116-µA Operating Quiescent Current**
- **1.5-µA Shutdown Current**
- **100-kHz to 2.5-MHz Switching Frequency**
- **Synchronizes to External Clock**
- **Adjustable Slow Start and Sequencing**
- **Undervoltage and Overvoltage Power-Good Output**
- **Adjustable Undervoltage Lockout Voltage and Hysteresis**
- **0.8-V Internal Voltage Reference**
- **Supported by SwitcherPro™ Software Tool (http://focus.ti.com/docs/toolsw/folders/print/switcherpro.html)**
- **For SWIFT™ Documentation, See the TI Web site at http://www.ti.com/swift**

## APPLICATIONS

- **12-V and 24-V Industrial and Commercial Low-Power Systems**
- **Aftermarket Automotive Accessories: Video, GPS, Entertainment**

## DESCRIPTION

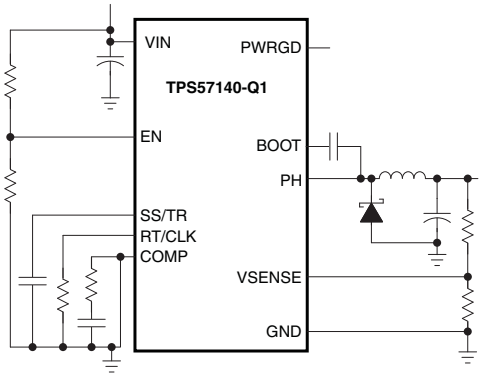
The TPS57140-Q1 device is a 42-V, 1.5-A step-down regulator with an integrated high-side MOSFET. Current-mode control provides simple external compensation and flexible component selection. A low-ripple pulse-skip mode reduces the no-load, regulated output supply current to 116 µA. Using the enable pin reduces the shutdown supply current to 1.5 µA.

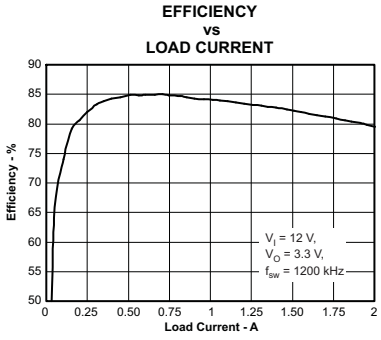
Undervoltage lockout is internally set at 2.5 V, but can be increased using the enable pin. The slow-start pin, which is also configurable for sequencing or tracking, controls the output voltage start-up ramp. An open-drain power-good signal indicates the output is within 92% to 109% of its nominal voltage.

A wide switching-frequency range allows optimizaton of efficiency and external component size. Frequency foldback and thermal shutdown protect the part during an overload condition.

The TPS57140-Q1 is available in a 10-pin thermally enhanced MSOP PowerPAD™ package (DGQ) and a 10-pin SON package (DRC).

**SIMPLIFIED SCHEMATIC**




Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE AND ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

## ABSOLUTE MAXIMUM RATINGS(1)

over operating temperature range (unless otherwise noted)

| | | | | VALUE |
|---|---|---|---|---|
| $V_{IN}$ | Input voltage | VIN | | –0.3 V to 47 V |
| | | EN(2) | | –0.3 V to 5 V |
| | | BOOT | | 55 V |
| | | VSENSE | | –0.3 V to 3 V |
| | | COMP | | –0.3 V to 3 V |
| | | PWRGD | | –0.3 V to 6 V |
| | | SS/TR | | –0.3 V to 3 V |
| | | RT/CLK | | –0.3 V to 3.6 V |
| $V_{OUT}$ | Output voltage | PH to BOOT | | 8 V |
| | | PH | | –0.6 V to 47 V |
| | | | 200 ns | –1 V to 47 V |
| | | | 30 ns | –2 V to 47 V |
| | | | Maximum dc voltage, $T_J$ = –40°C | -0.85 V |
| $V_{DIFF}$ | Differential voltage | PAD to GND | | ±200 mV |
| $I_{SOURCE}$ | Source current | EN | | 100 µA |
| | | BOOT | | 100 mA |
| | | VSENSE | | 10 µA |
| | | PH | | Current limit |
| | | RT/CLK | | 100 µA |
| $I_{SINK}$ | Sink current | VIN | | Current limit |
| | | COMP | | 100 µA |
| | | PWRGD | | 10 mA |
| | | SS/TR | | 200 µA |
| $T_J$ | Operating junction temperature range | | | –40°C to 150°C |
| $T_{stg}$ | Storage temperature range | | | –65°C to 150°C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) See Enable and Adjusting Undervoltage Lockout for details.

## THERMAL INFORMATION

| THERMAL METRIC(1)(2) | | DGQ | DRC | UNIT |
|---|---|---|---|---|
| | | 10 PINS | 10 PINS | |
| $\theta_{JA}$ | Junction-to-ambient thermal resistance (standard board) | 62.5 | 56.5 | °C/W |
| $\theta_{JA}$ | Junction-to-ambient thermal resistance (custom board)(3) | 57 | 61.5 | °C/W |
| $\theta_{JCtop}$ | Junction-to-case (top) thermal resistance | 83 | 52.1 | °C/W |
| $\theta_{JB}$ | Junction-to-board thermal resistance | 28 | 20.8 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 1.7 | 0.9 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 20.1 | 20.8 | °C/W |
| $\theta_{JCbot}$ | Junction-to-case (bottom) thermal resistance | 21 | 5.2 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) Power rating at a specific ambient temperature $T_A$ should be determined with a junction temperature of 150°C. This is the point where distortion starts to increase substantially. See the power dissipation estimate in the application section of this data sheet for more information.
(3) Test-board conditions:
(a) 3 inches (7.62 cm) × 3 inches (7.62 cm), 2 layers, thickness: 0.062 inch (1.57 mm)
(b) 2-oz. (0.071-mm thick) copper traces located on the top of the PCB
(c) 2-oz. (0.071-mm thick) copper ground plane, bottom layer
(d) 6 thermal vias (13-mil, 0.o254-mm)) located under the device package

## ELECTRICAL CHARACTERISTICS

$T_J$ = –40°C to 150°C, VIN = 3.5 V to 42 V (unless otherwise noted)

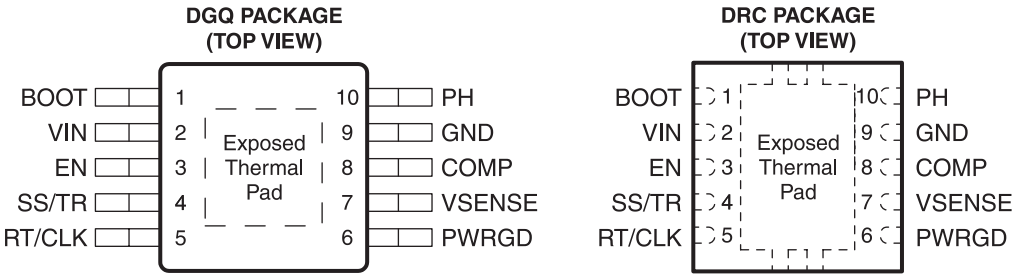
| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SUPPLY VOLTAGE (VIN PIN)** | | | | | | |
| | Operating input voltage | | 3.5 | | 42 | V |
| | Internal undervoltage lockout threshold | No voltage hysteresis, rising and falling | | 2.5 | | V |
| | Shutdown supply current | EN = 0 V, 25°C, 3.5 V ≤ $V_{IN}$ ≤ 60 V | | 1.5 | 4 | μA |
| | | EN = 0 V, 125°C, 3.5 V ≤ $V_{IN}$ ≤ 60 V | | 1.9 | 6.5 | |
| | Operating: nonswitching supply current | $V_{SENSE}$ = 0.83 V, $V_{IN}$ = 12 V, 25°C | | 116 | 136 | |
| **ENABLE AND UVLO (EN PIN)** | | | | | | |
| | Enable threshold voltage | No voltage hysteresis, rising and falling, 25°C | 1.15 | 1.25 | 1.36 | V |
| | Input current | Enable threshold 50 mV | | –3.8 | | μA |
| | | Enable threshold –50 mV | | –0.9 | | |
| | Hysteresis current | | | –2.9 | | μA |
| **VOLTAGE REFERENCE** | | | | | | |
| | Voltage reference | $T_J$ = 25°C | 0.792 | 0.8 | 0.808 | V |
| | | | 0.784 | 0.8 | 0.816 | |
| **HIGH-SIDE MOSFET** | | | | | | |
| | On-resistance | $V_{IN}$ = 3.5 V, BOOT-PH = 3 V | | 300 | | mΩ |
| | | $V_{IN}$ = 12 V, BOOT-PH = 6 V | | 200 | 410 | |
| **ERROR AMPLIFIER** | | | | | | |
| | Input current | | | 50 | | nA |
| | Error amplifier transconductance (gm) | –2 μA < $I_{COMP}$ < 2 μA, $V_{COMP}$ = 1 V | | 97 | | μS |
| | Error amplifier transconductance (gm) during slow start | –2 μA < $I_{COMP}$ < 2 μA, $V_{COMP}$ = 1 V, $V_{VSENSE}$ = 0.4 V | | 26 | | μS |
| | Error amplifier dc gain | $V_{VSENSE}$ = 0.8 V | | 10 000 | | V/V |
| | Error amplifier bandwidth | | | 2700 | | kHz |
| | Error amplifier source/sink | $V_{(COMP)}$ = 1 V, 100 mV overdrive | | ±7 | | μA |
| | COMP to switch current transconductance | | | 6 | | S |

## ELECTRICAL CHARACTERISTICS (continued)

$T_J$ = –40°C to 150°C, VIN = 3.5 V to 42 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **CURRENT LIMIT** | | | | | | |
| | Current-limit threshold | VIN = 12 V, $T_J$ = 25°C | 1.8 | 2.7 | | A |
| **THERMAL SHUTDOWN** | | | | | | |
| | Thermal shutdown | | | 182 | | °C |
| **TIMING RESISTOR AND EXTERNAL CLOCK (RT/CLK PIN)** | | | | | | |
| | Switching-frequency range using RT mode | $V_{IN}$ = 12 V | 100 | | 2500 | kHz |
| $f_{SW}$ | Switching frequency | $V_{IN}$ = 12 V, $R_T$ = 200 kΩ | 450 | 581 | 720 | kHz |
| | Switching-frequency range using CLK mode | $V_{IN}$ = 12 V | 300 | | 2200 | kHz |
| | Minimum CLK pulse duration | | | 40 | | ns |
| | RT/CLK high threshold | $V_{IN}$ = 12 V | | 1.9 | 2.2 | V |
| | RT/CLK low threshold | $V_{IN}$ = 12 V | 0.45 | 0.7 | | V |
| | RT/CLK falling-edge to PH rising-edge delay | Measured at 500 kHz with RT resistor in series | | 60 | | ns |
| | PLL lock in time | Measured at 500 kHz | | 100 | | µs |
| **SLOW START AND TRACKING (SS/TR)** | | | | | | |
| | Charge current | $V_{SS/TR}$ = 0.4 V | | 2 | | µA |
| | SS/TR-to-VSENSE matching | $V_{SS/TR}$ = 0.4 V | | 45 | | mV |
| | SS/TR-to-reference crossover | 98% nominal | | 1 | | V |
| | SS/TR discharge current (overload) | $V_{SENSE}$ = 0 V, $V_{(SS/TR)}$ = 0.4 V | | 112 | | µA |
| | SS/TR discharge voltage | $V_{SENSE}$ = 0 V | | 54 | | mV |
| **POWER GOOD (PWRGD PIN)** | | | | | | |
| $V_{VSENSE}$ | VSENSE threshold | $V_{SENSE}$ falling | | 92% | | |
| | | $V_{SENSE}$ rising | | 94% | | |
| | | $V_{SENSE}$ rising | | 109% | | |
| | | $V_{SENSE}$ falling | | 107% | | |
| | Hysteresis | $V_{SENSE}$ falling | | 2% | | |
| | Output-high leakage | $V_{SENSE}$ = $V_{REF}$, $V_{(PWRGD)}$ = 5.5 V, 25°C | | 10 | | nA |
| | On-resistance | $I_{(PWRGD)}$ = 3 mA, $V_{SENSE}$ < 0.79 V | | 50 | | Ω |
| | Minimum VIN for defined output | $V_{(PWRGD)}$ < 0.5 V, $I_{I(PWRGD)}$ = 100 µA | | 0.95 | 1.5 | V |

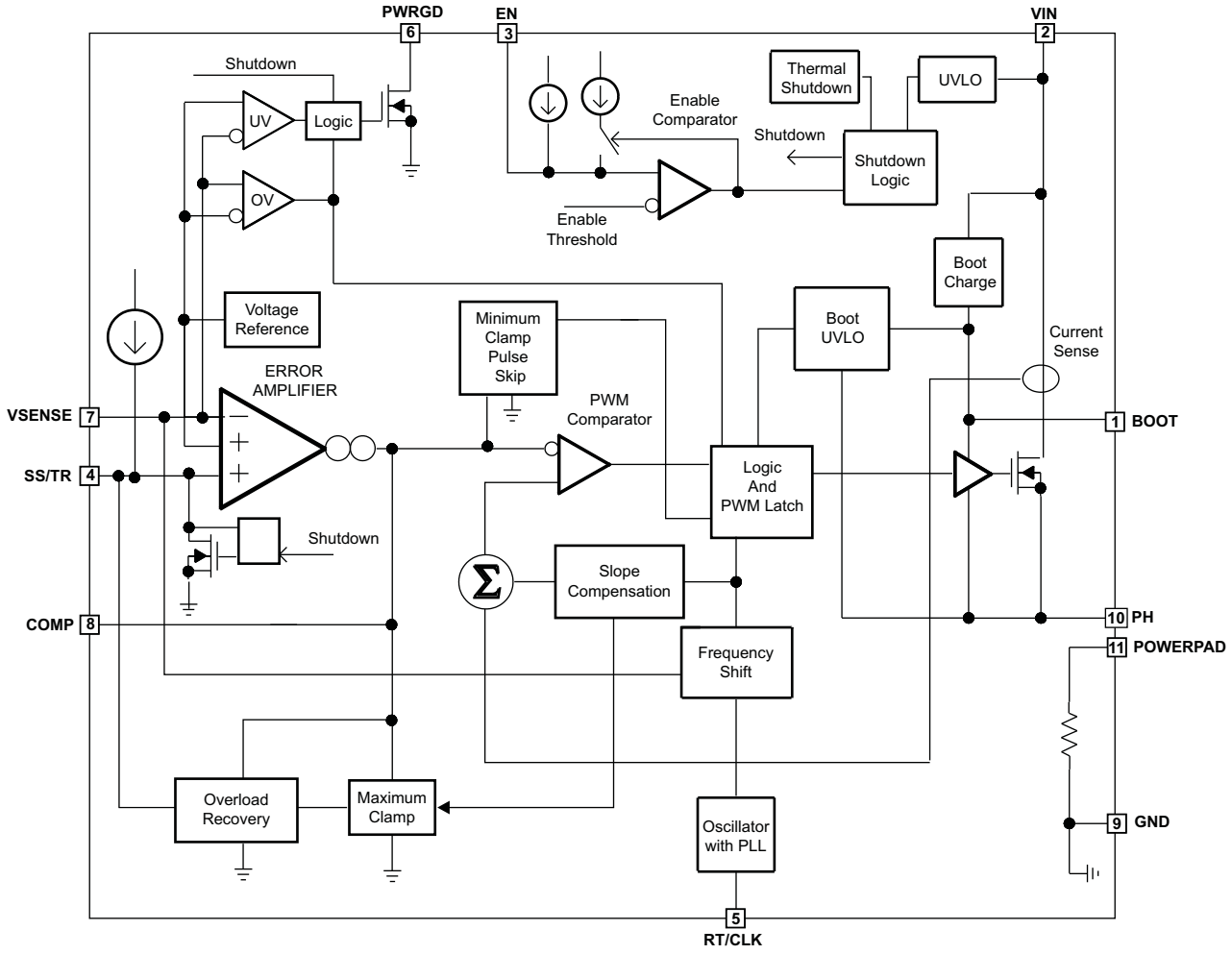
## DEVICE INFORMATION




## PIN FUNCTIONS

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| BOOT | 1 | O | The device requires a bootstrap capacitor between BOOT and PH. A voltage on this capacitor below the minimum required by the output device forces the output is forced to switch off pending a referesh of the capacitor. |
| COMP | 8 | O | Error-amplifier output, and input to the output-switch current comparator. Connect frequency-compensation components to this pin. |
| EN | 3 | I | Enable pin, internal pullup current source. Pull below 1.2 V to disable. Float to enable. Adjust the input undervoltage lockout with two resistors. |
| GND | 9 | – | Ground |
| PH | 10 | I | The source of the internal high-side power MOSFET |
| PWRGD | 6 | O | An open-drain output, asserts low if output voltage is low due to thermal shutdown, dropout, overvoltage, or EN shutdown. |
| RT/CLK | 5 | I | Resistor timing and external clock. An internal amplifier holds this pin at a fixed voltage when using an external resistor to ground to set the switching frequency. Pulling the pin above the PLL upper threshold causes a mode change whereby the pin becomes a synchronization input. Disabling of the internal amplifier occurs, and the pin is a high-impedance clock input to the internal PLL. If clocking edges stop, re-enabling of the internal amplifier occurs, and the mode returns to a resistor-set function. |
| SS/TR | 4 | I | Slow-start and tracking. An external capacitor connected to this pin sets the output rise time. The voltage on this pin overrides the internal reference, allowing use of the pin for tracking and sequencing. |
| VIN | 2 | I | Input supply voltage, 3.5 V to 42 V |
| VSENSE | 7 | I | Inverting node of the transconductance (gm) error amplifier |
| Thermal pad | | – | GND pin must have an electrical connection to the exposed pad on the printed-circuit board for proper operation. |

## FUNCTIONAL BLOCK DIAGRAM



## TYPICAL CHARACTERISTICS

**ON RESISTANCE vs JUNCTION TEMPERATURE**

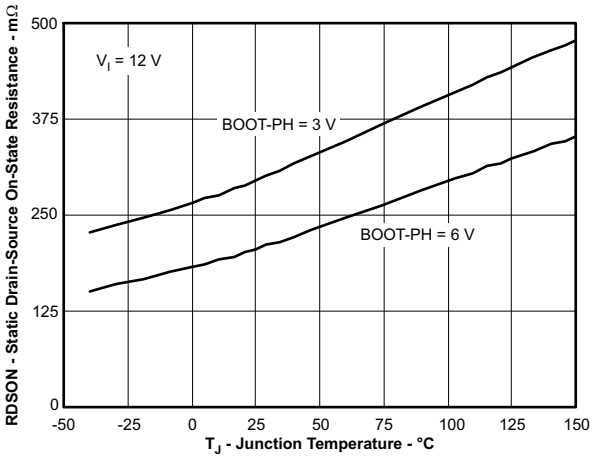



**Figure 1.**

**VOLTAGE REFERENCE versus JUNCTION TEMPERATURE**

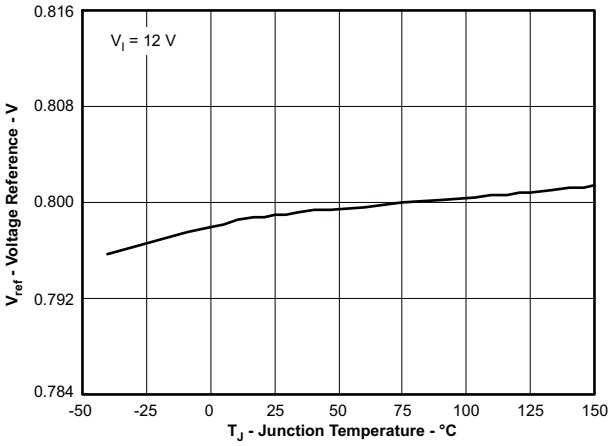



**Figure 2.**

**SWITCH CURRENT LIMIT versus JUNCTION TEMPERATURE**

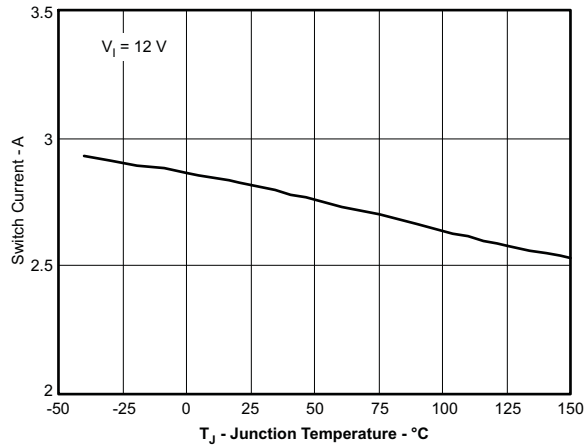



**Figure 3.**

**SWITCHING FREQUENCY versus JUNCTION TEMPERATURE**

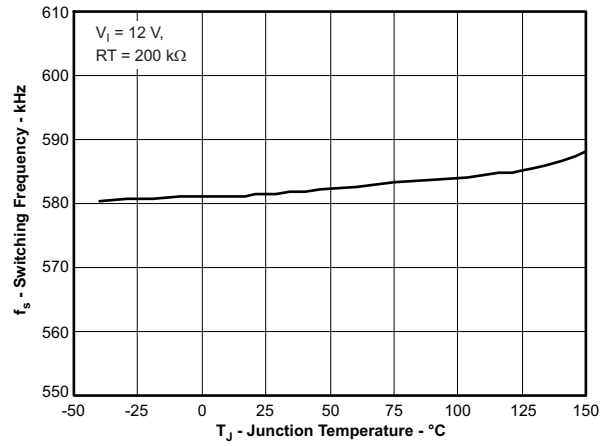



**Figure 4.**

**SWITCHING FREQUENCY versus RT/CLK RESISTANCE, HIGH-FREQUENCY RANGE**

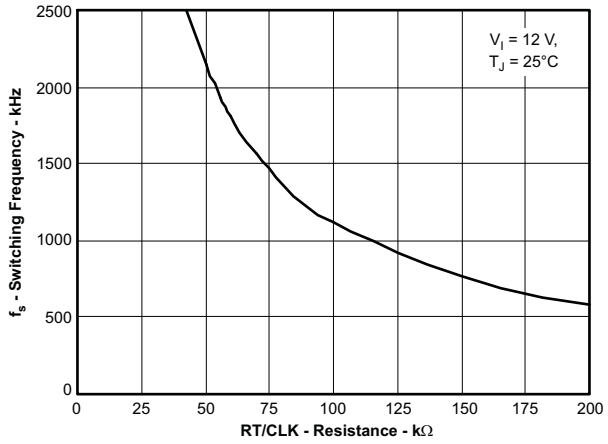



**Figure 5.**

**SWITCHING FREQUENCY versus RT/CLK RESISTANCE, LOW-FREQUENCY RANGE**

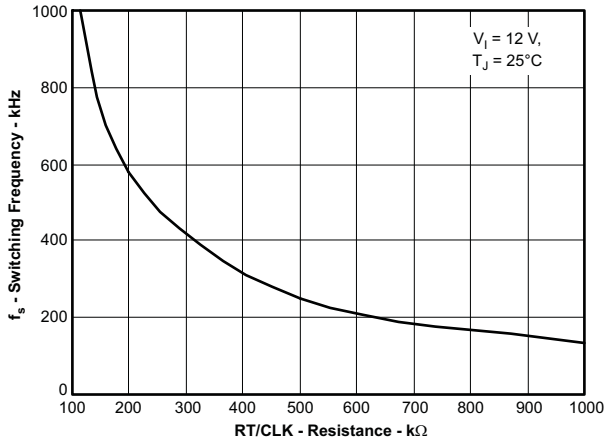



**Figure 6.**

## TYPICAL CHARACTERISTICS (continued)

EA TRANSCONDUCTANCE DURING SLOW START versus JUNCTION TEMPERATURE

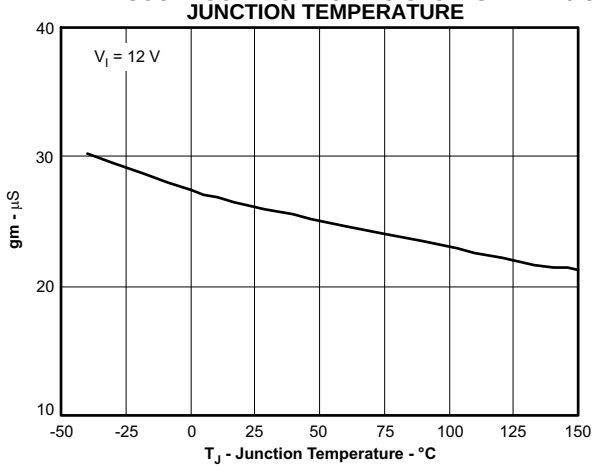



Figure 7.

EA TRANSCONDUCTANCE versus JUNCTION TEMPERATURE

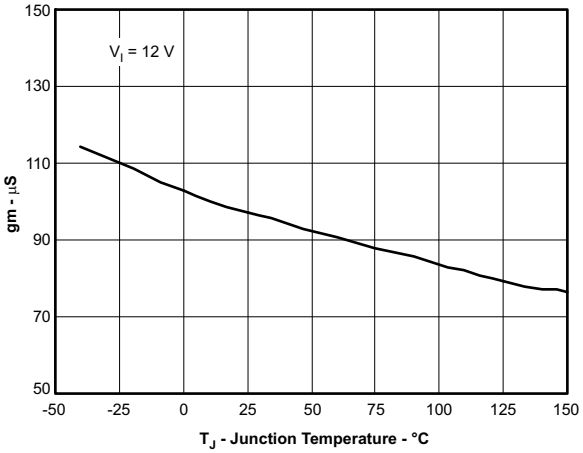



Figure 8.

EN PIN VOLTAGE versus JUNCTION TEMPERATURE

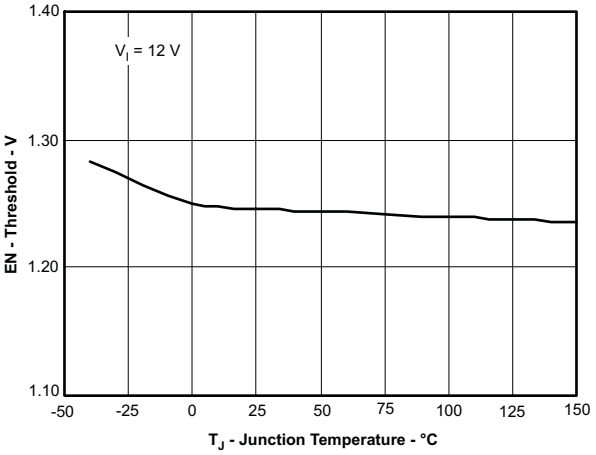



Figure 9.

EN PIN CURRENT versus JUNCTION TEMPERATURE

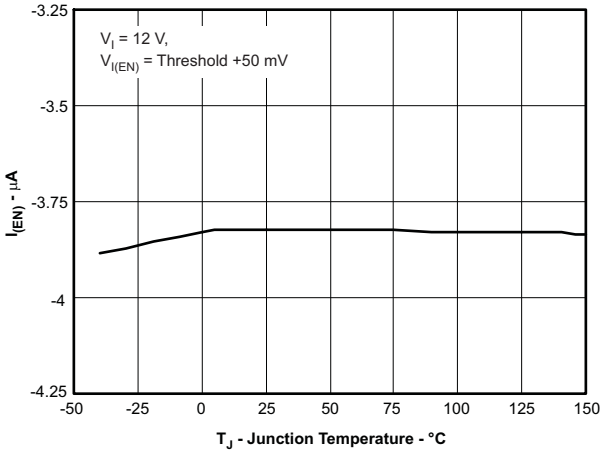



Figure 10.

EN PIN CURRENT versus JUNCTION TEMPERATURE

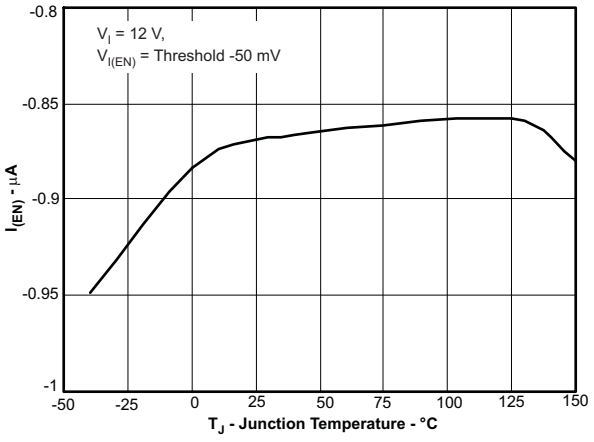



Figure 11.

SS/TR CHARGE CURRENT versus JUNCTION TEMPERATURE

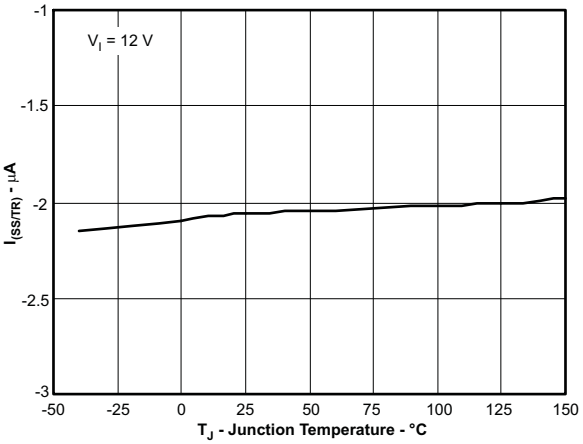



Figure 12.

## TYPICAL CHARACTERISTICS (continued)

**SS/TR DISCHARGE CURRENT versus JUNCTION TEMPERATURE**

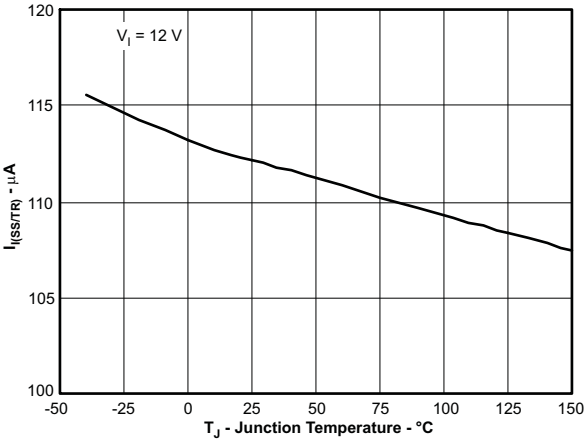



**Figure 13.**

**SWITCHING FREQUENCY versus VSENSE**

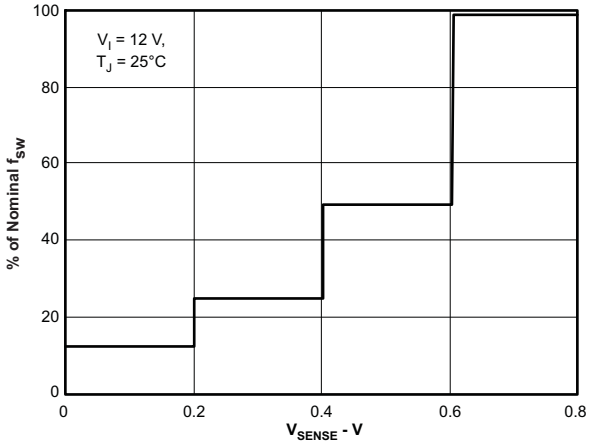



**Figure 14.**

**SHUTDOWN SUPPLY CURRENT versus JUNCTION TEMPERATURE**

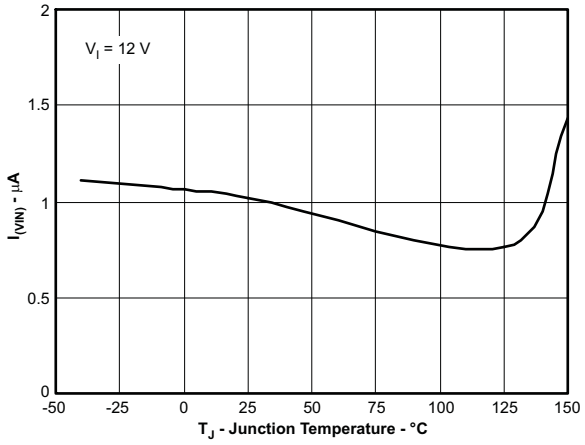



**Figure 15.**

**SHUTDOWN SUPPLY CURRENT versus INPUT VOLTAGE ($V_{IN}$)**

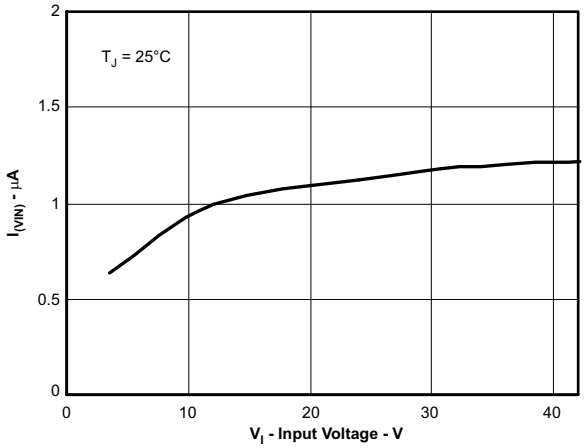



**Figure 16.**

**VIN SUPPLY CURRENT versus JUNCTION TEMPERATURE**

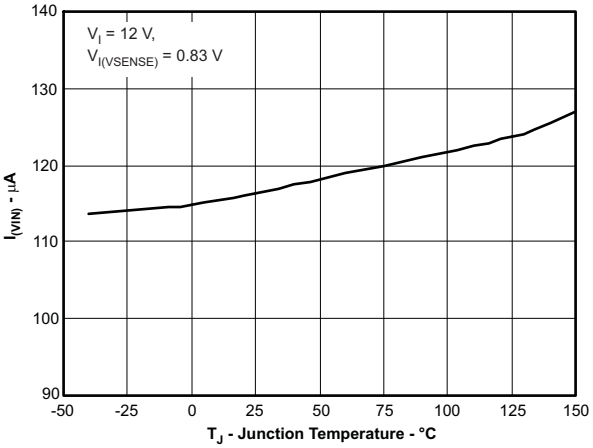



**Figure 17.**

**VIN SUPPLY CURRENT versus INPUT VOLTAGE**

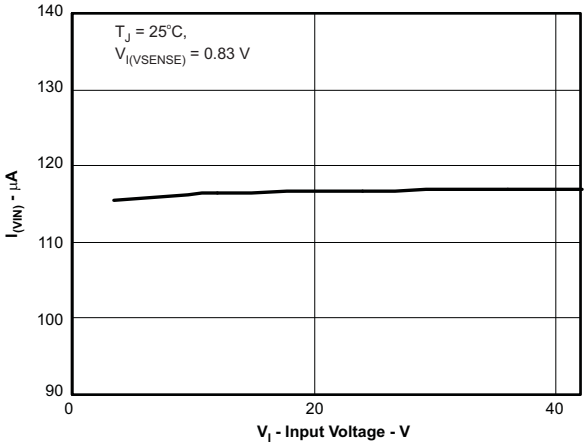



**Figure 18.**

## TYPICAL CHARACTERISTICS (continued)

PWRGD ON RESISTANCE versus JUNCTION TEMPERATURE

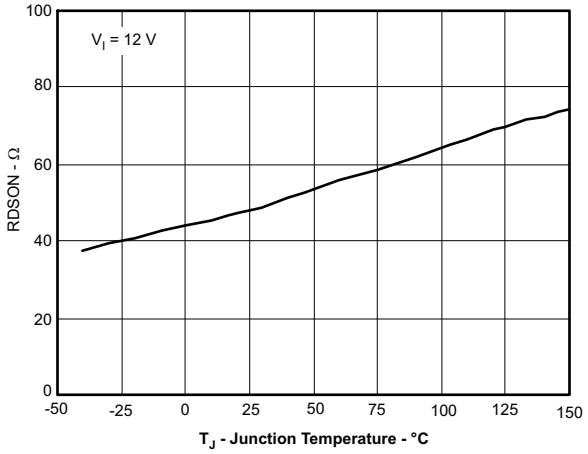



Figure 19.

PWRGD THRESHOLD versus JUNCTION TEMPERATURE

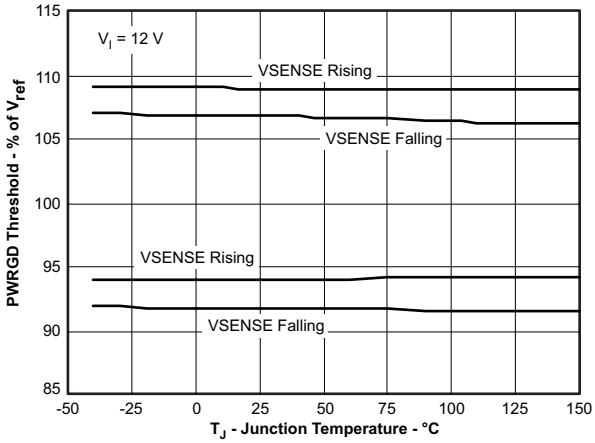



Figure 20.

BOOT-PH UVLO versus JUNCTION TEMPERATURE

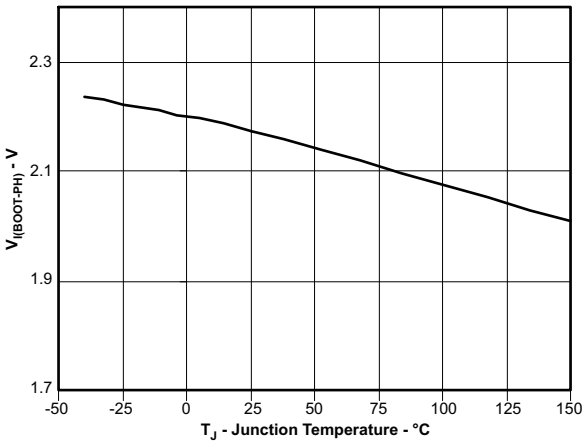



Figure 21.

INPUT VOLTAGE (UVLO) versus JUNCTION TEMPERATURE

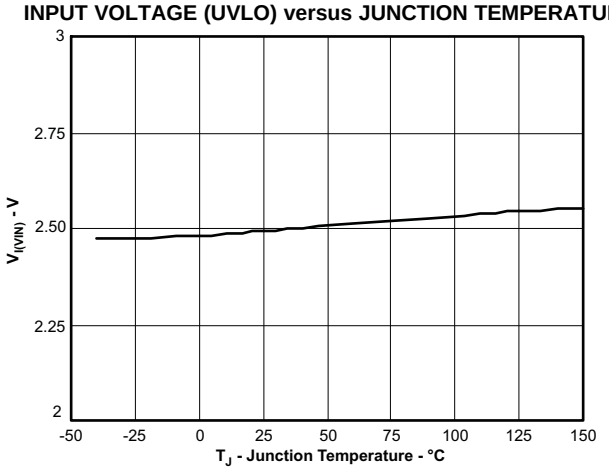



Figure 22.

SS/TR TO VSENSE OFFSET versus VSENSE

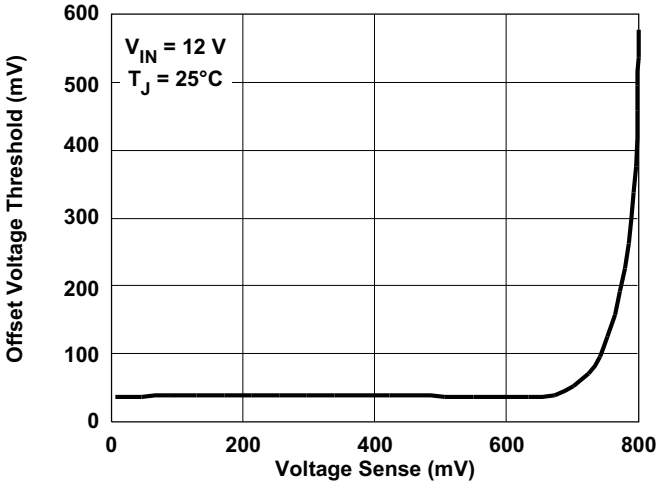



Figure 23.

SS/TR TO VSENSE OFFSET versus TEMPERATURE

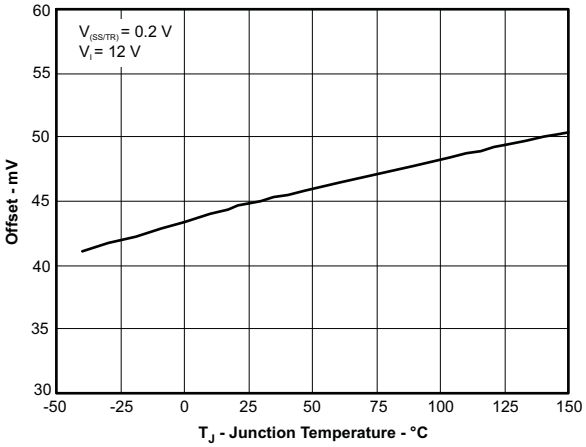



Figure 24.

## OVERVIEW

The TPS57140-Q1 device is a 42-V, 1.5-A, step-down (buck) regulator with an integrated high-side n-channel MOSFET. To improve performance during line and load transients, the device implements a constant-frequency, current-mode control which reduces output capacitance and simplifies external frequency-compensation design. The wide switching frequency of 100 kHz to 2500 kHz allows for efficiency and size optimization when selecting the output-filter components. Using a resistor to ground on the RT/CLK pin adjusts the switching frequency. The device has an internal phase-lock loop (PLL) on the RT/CLK pin that synchronizes the power-switch turnon to a falling edge of an external system clock.

The TPS57140-Q1 has a default start-up voltage of approximately 2.5 V. The EN pin has an internal pullup current source that one can use to adjust the input-voltage undervoltage-lockout (UVLO) threshold with two external resistors. In addition, the pullup current provides a default condition. When the EN pin is floating the device operates. The operating current is 116 µA when not switching and under no load. With the device disabled, the supply current is 1.5 µA.

The integrated 200-mΩ high-side MOSFET allows for high-efficiency power-supply designs capable of delivering 1.5 amperes of continuous current to a load. The TPS57140-Q1 reduces the external component count by integrating the boot recharge diode. A capacitor between the BOOT and PH pins supplies the bias voltage for the integrated high-side MOSFET. A UVLO circuit monitors the boot-capacitor voltage and turns the high-side MOSFET off when the boot voltage falls below a preset threshold. The TPS57140-Q1 can operate at high duty cycles because of the boot UVLO. Stepping down of the output voltage can extend down to as low as the 0.8-V reference.

The TPS57140-Q1 has a power-good comparator (PWRGD) which asserts when the regulated output voltage is less than 92% or greater than 109% of the nominal output voltage. The PWRGD pin is an open-drain output which deasserts when the VSENSE pin voltage is between 94% and 107% of the nominal output voltage, allowing the pin to transition high when a pullup resistor is used.

The TPS57140-Q1 minimizes excessive output overvoltage (OV) transients by taking advantage of the OV power-good comparator. With the OV comparator activated, the high-side MOSFET turns off and remains masked from turning on until the output voltage is lower than 107%.

Use the SS/TR (slow start/tracking) pin to minimize inrush currents or provide power-supply sequencing during power up. Couple a small-value capacitor to the pin to adjust the slow-start time. One can couple a resistor divider to the pin for critical power-supply sequencing requirements. Discharge of the SS/TR pin occurs before the output powers up. This discharging ensures a repeatable restart after an overtemperature fault, UVLO fault, or a disabled condition.

The TPS57140-Q1 also discharges the slow-start capacitor during overload conditions with an overload-recovery circuit. The overload-recovery circuit slow-starts the output from the fault voltage to the nominal regulation voltage on removal of a fault condition. A frequency-foldback circuit reduces the switching frequency during start-up and overcurrent fault conditions to help control the inductor current.

## DETAILED DESCRIPTION

### Fixed Frequency PWM Control

The TPS57140-Q1 uses an adjustable fixed-frequency, peak-current mode control. External resistors on the VSENSE pin compare the output voltage to an internal voltage reference by an error amplifier which drives the COMP pin. An internal oscillator initiates the turnon of the high-side power switch. The device compares the error-amplifier output to the high-side power-switch current. When the power-switch current reaches the COMP voltage level, the power switch turns off. The COMP pin voltage increases and decreases as the output current increases and decreases. The device implements a current limit by clamping the COMP pin voltage to a maximum level. A minimum clamp on the COMP pin implements the Eco-mode control scheme.

### Slope-Compensation Output Current

The TPS57140-Q1 adds a compensating ramp to the switch-current signal. This slope compensation prevents sub-harmonic oscillations. The available peak inductor current remains constant over the full duty-cycle range.

### Pulse-Skip Eco-mode Control Scheme

The TPS57140-Q1 enters the pulse-skip mode when the voltage on the COMP pin is the minimum clamp value. The TPS57140-Q1 operates in a pulse-skip mode at light load currents to improve efficiency. The peak switch current during the pulse-skip mode is the greater value of 50 mA or the peak inductor current that is a function of the minimum on-time, input voltage, output voltage, and inductance value. When the load current is low and the output voltage is within regulation, the device enters a sleep mode and draws only 116 µA of input quiescent current. While the device is in sleep mode, the output capacitor delivers the output power. As the load current decreases, the time the output capacitor supplies the load current increases and the switching frequency decreases, reducing gate-drive and switching losses. As the output voltage drops, the TPS57140-Q1 wakes up from the sleep mode and the power switch turns on to recharge the output capacitor, see Figure 25. The internal PLL remains operating when in sleep mode. When operating at light load currents in the pulse-skip mode, the switching transitions occur synchronously with the external clock signal.

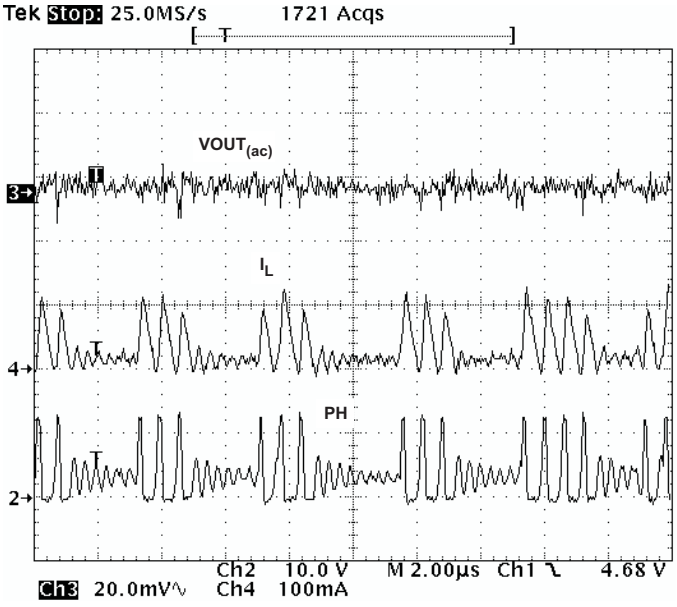



**Figure 25. Operation in Pulse-Skip Mode**

## DETAILED DESCRIPTION (continued)

### Bootstrap Voltage (BOOT)

The TPS57140-Q1 has an integrated boot regulator and requires a small ceramic capacitor between the BOOT and PH pins to provide the gate-drive voltage for the high-side MOSFET. The value of the ceramic capacitor should be 0.1 µF. TI recommends a ceramic capacitor with an X7R or X5R grade dielectric because of the stable characteristics over temperature and voltage. To improve dropout, the TPS57140-Q1 operates at 100% duty cycle as long as the BOOT-to-PH pin voltage is greater than 2.1 V. When the voltage from BOOT to PH drops below 2.1 V, the high-side MOSFET turns off using a UVLO circuit, allowing for the low-side diode to conduct, which allows refreshing of the BOOT capacitor. Because the supply current sourced from the BOOT capacitor is low, the high-side MOSFET can remain on for more switching cycles than it refreshes; thus, the effective duty-cycle limitation attributed to the boot regulator system is high.

### Low-Dropout Operation

The voltage drops across the power MOSFET, inductor, low-side diode, and printed-circuit-board resistance mainly determine the duty cycle during dropout of the regulator. During operating conditions in which the input voltage drops, the high-side MOSFET can remain on for 100% of the duty cycle to maintain output regulation until the BOOT-to-PH voltage falls below 2.1 V.

Once the high side is off, the low-side diode conducts and the BOOT capacitor recharges. During this boot-capacitor recharge time, the inductor current ramps down until the high-side MOSFET turns on. The recharge time is longer than the typical high-side off-time of previous switching cycles, and thus the inductor-current ripple is larger, resulting in more ripple voltage on the output. The recharge time is a function of the input voltage, boot-capacitor value, and the impedance of the internal boot-recharge diode.

Pay attention in maximum-duty-cycle applications which experience extended time periods without a load current. When the voltage across the BOOT capacitors falls below the 2.1-V threshold in applications that have a difference in the input voltage and output voltage that is less than 3 V, the high-side MOSFET turns off, but there is not enough current in the inductor to pull the PH pin down to recharge the boot capacitor. The regulator does not switch because the boot capacitor is less than 2.1 V, and the output capacitor decays until the difference between the input voltage and output voltage is 2.1 V. At this time, the boot undervoltage lockout is exceeded and the device switches until reaching the desired output voltage.

Figure 26 and Figure 27 show the start and stop voltages for 3.3-V and 5-V applications. The graphs plot voltages versus the load current. The definition of start voltage is the input voltage needed to regulate within 1%. The definition of stop voltage is the input voltage at which the output drops by 5% or stops switching.

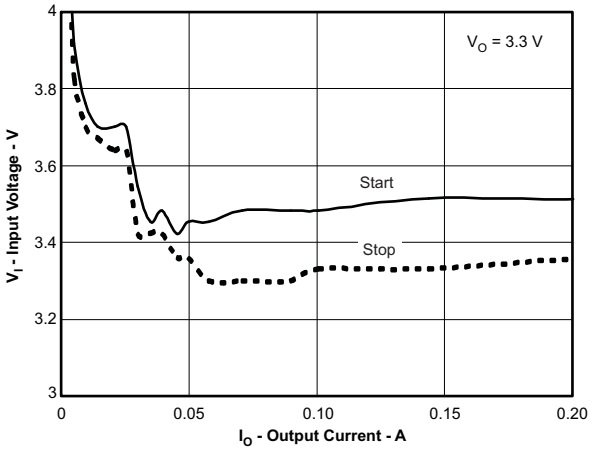



**Figure 26. 3.3-V Start and Stop Voltage**

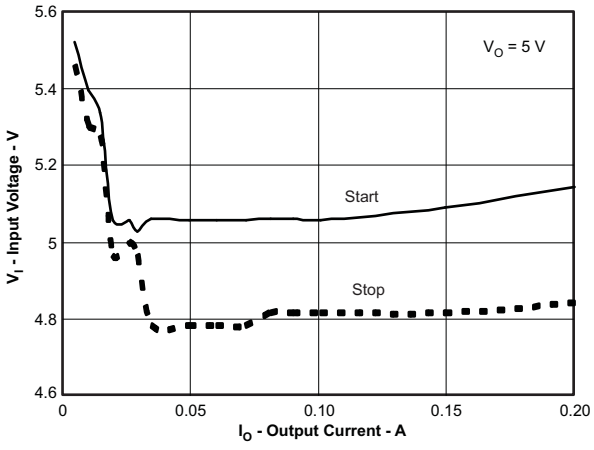



**Figure 27. 5-V Start and Stop Voltage**

## DETAILED DESCRIPTION (continued)

### Error Amplifier

The TPS57140-Q1 has a transconductance amplifier for the error amplifier. The error amplifier compares the VSENSE voltage to the lower of the SS/TR pin voltage or the internal 0.8-V voltage reference. The transconductance (gm) of the error amplifier is 97 µS during normal operation. During the slow-start operation, the transconductance is a fraction of the normal operating gm. When the voltage of the VSENSE pin is below 0.8 V and the device is regulating using the SS/TR voltage, the gm is 25 µS.

The frequency-compensation components (capacitor, series resistor, and capacitor) are added from the COMP pin to ground.

### Voltage Reference

The voltage-reference system produces a precise ±2% voltage reference over temperature by scaling the output of a temperature-stable band-gap circuit.

### Adjusting the Output Voltage

A resistor divider from the output node to the VSENSE pin sets the output voltage. It is recommended to use 1% tolerance or better divider resistors. Start with 10 kΩ for the R2 resistor and use Equation 1 to calculate R1. To improve efficiency at very light loads, consider using larger-value resistors. If the values are too high, the regulator is more susceptible to noise, and voltage errors from the VSENSE input current become noticeable.

$$R1 = R2 \times \left( \frac{Vout - 0.8V}{0.8\ V} \right) \quad (1)$$

### Enable and Adjusting Undervoltage Lockout

The VIN pin voltage falling below 2.5 V disables he TPS57140-Q1. If an application requires a higher undervoltage lockout (UVLO), use the EN pin as shown in Figure 28 to adjust the input-voltage UVLO by using two external resistors. Though it is not necessary to use the UVLO adjust resistors, for operation TI highly recommends providing consistent power-up behavior. The EN pin has an internal pullup current source, I1, of 0.9 µA that provides the default condition of the TPS57140-Q1 operating when the EN pin floats. Once the EN pin voltage exceeds 1.25 V, an additional 2.9 µA of hysteresis, Ihys, is added. This additional current facilitates input-voltage hysteresis. Use Equation 2 to set the external hysteresis for the input voltage. Use Equation 3 to set the input start voltage.

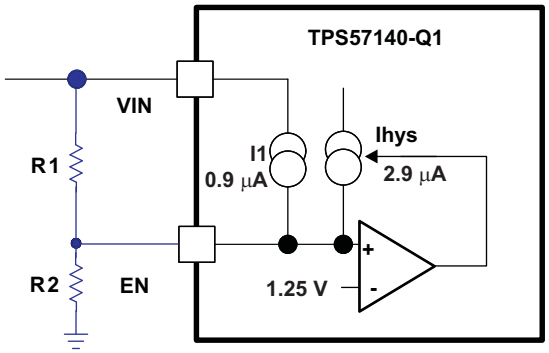



**Figure 28. Adjustable Undervoltage Lockout (UVLO)**

$$R1 = \frac{V_{START} - V_{STOP}}{I_{HYS}} \quad (2)$$

$$R2 = \frac{V_{ENA}}{\frac{V_{START} - V_{ENA}}{R1} + I_1} \quad (3)$$

## DETAILED DESCRIPTION (continued)

Figure 29 shows another technique to add input-voltage hysteresis. One can use this method may be used if the resistance values are high from the previous method and there is a need for a wider voltage hysteresis. Resistor R3 sources additional hysteresis current into the EN pin.

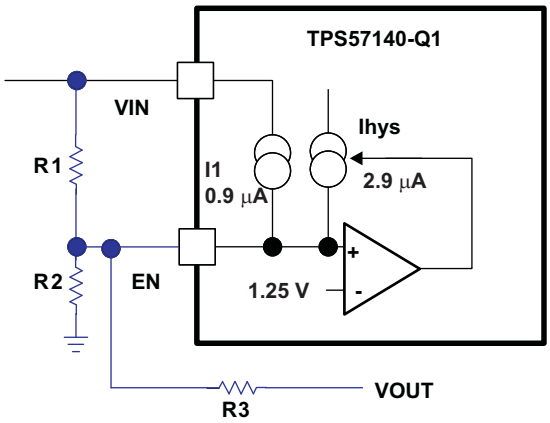



**Figure 29. Adding Additional Hysteresis**

$$R1 = \frac{V_{START} - V_{STOP}}{I_{HYS} + \frac{V_{OUT}}{R3}} \quad (4)$$

$$R2 = \frac{V_{ENA}}{\frac{V_{START} - V_{ENA}}{R1} + I_1 - \frac{V_{ENA}}{R3}} \quad (5)$$

Do not place a low-impedance voltage source with greater than 5 V directly on the EN pin. Do not place a capacitor directly on the EN pin if $V_{EN}$ > 5 V when using a voltage divider to adjust the start and stop voltage. The node voltage, (see Figure 30) must remain equal to or less than 5.8 V. The Zener diode can sink up to 100 µA. The EN pin voltage can be greater than 5 V if the $V_{IN}$ voltage source has a high impedance and does not source more than 100 µA into the EN pin.

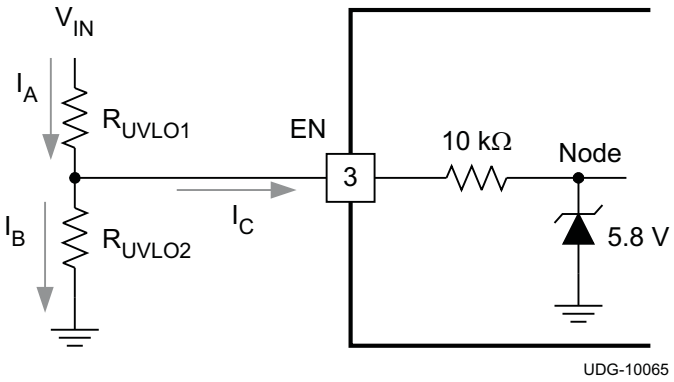



**Figure 30. Node Voltage**

## DETAILED DESCRIPTION (continued)

### Slow-Start or Tracking Pin (SS/TR)

The TPS57140-Q1 effectively uses the lower voltage of the internal voltage reference or the SS/TR pin voltage as the power-supply reference voltage and regulates the output accordingly. A capacitor on the SS/TR pin to ground implements a slow-start time. The TPS57140-Q1 has an internal pullup current source of 2 µA that charges the external slow-start capacitor. The calculations for the slow-start Equation 6 shows the time (10% to 90%). The voltage reference ($V_{REF}$) is 0.8 V and the slow-start current ($I_{SS}$) is 2 µA. The slow-start capacitor should remain lower than 0.47 µF and greater than 0.47 nF.

$$Css(nF) = \frac{Tss(ms) \times Iss(\mu A)}{Vref\ (V) \times 0.8} \quad (6)$$

At power up, the TPS57140-Q1 does not start switching until the slow-start pin discharges to less than 40 mV; to ensure a proper power up, see Figure 31.

Also, during normal operation, the TPS57140-Q1 stops switching and the SS/TR must discharge to 40 mV when the VIN UVLO is exceeded, EN pin is pulled below 1.2 V, or a thermal shutdown event occurs.

The VSENSE voltage follows the SS/TR pin voltage with a 45-mV offset up to 85% of the internal voltage reference. When the SS/TR voltage is greater than 85% of the internal reference voltage, the offset increases as the effective system reference transitions from the SS/TR voltage to the internal voltage reference (see Figure 23). The SS/TR voltage ramps linearly until clamped at 1.7 V.

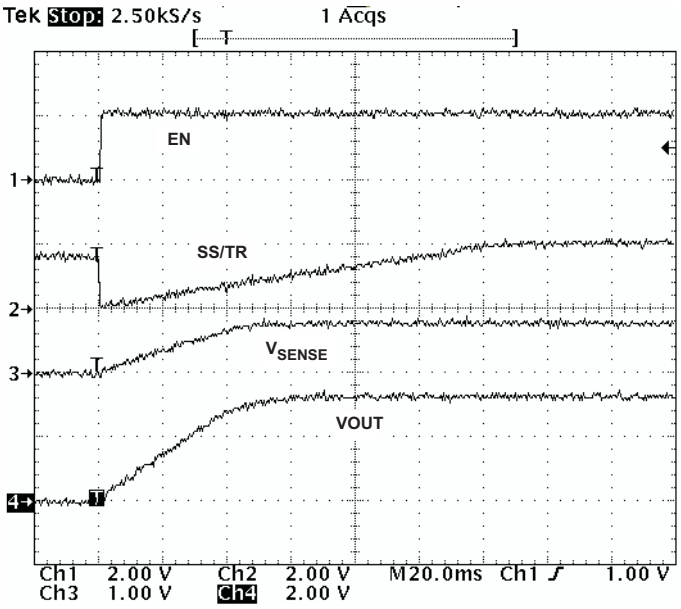



**Figure 31. Operation of SS/TR Pin When Starting**

### Overload Recovery Circuit

The TPS57140-Q1 has an overload recovery (OLR) circuit. The OLR circuit slow-starts the output from the overload voltage to the nominal regulation voltage on removal of the fault condition. The OLR circuit discharges the SS/TR pin to a voltage slightly greater than the VSENSE pin voltage using an internal pulldown of 100 µA when the error amplifier is changed to a high voltage from a fault condition. On removal of the fault condition, the output slow-starts from the fault voltage to the nominal output voltage.

## DETAILED DESCRIPTION (continued)

### Sequencing

One can implement many of the common power-supply sequencing methods using the SS/TR, EN, and PWRGD pins. Implement the sequential method using an open-drain output of a power-on-reset pin of another device. Figure 32 illustrates the sequential method using two TPS57140-Q1 devices. The power-good pin connects to the EN pin on the TPS57140-Q1, which enables the second power supply once the primary supply reaches regulation. If needed, a 1-nF ceramic capacitor on the EN pin of the second power supply provides a 1-ms start-up delay. Figure 33 shows the results of Figure 32.

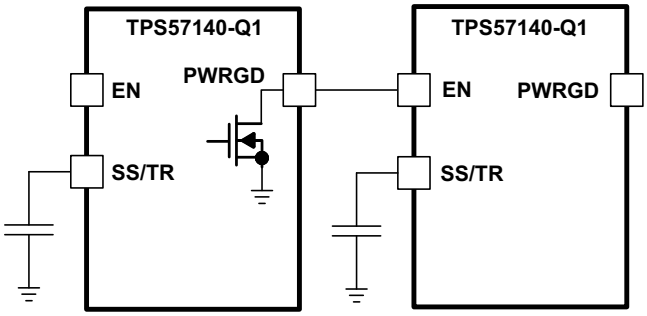



**Figure 32. Schematic for Sequential Start-Up Sequence**

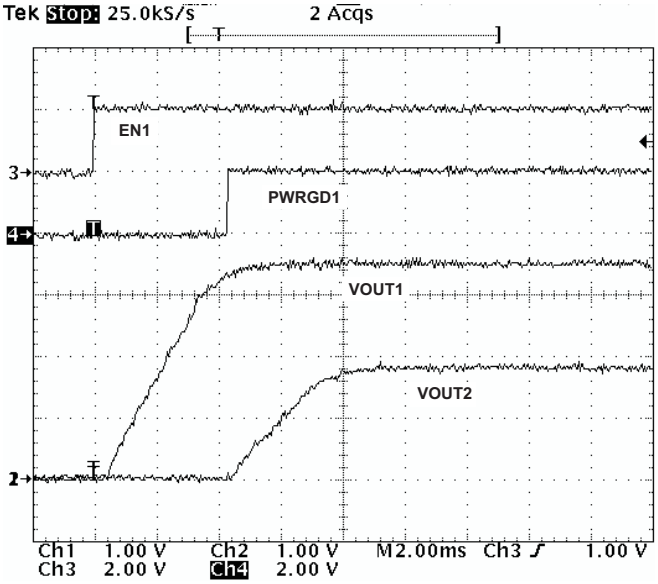



**Figure 33. Sequential Start-Up Using EN and PWRGD**

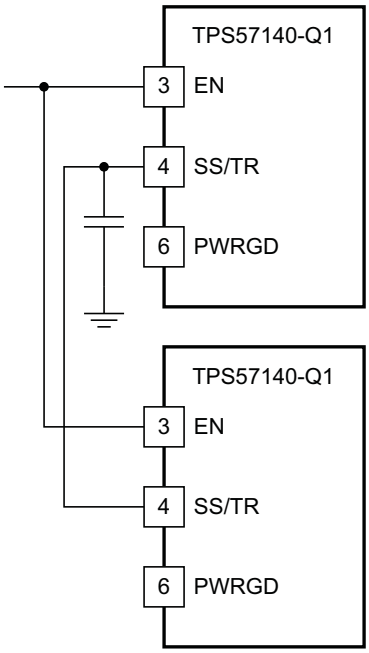



**Figure 34. Schematic for Ratiometric Start-Up Using Coupled SS/TR Pins**

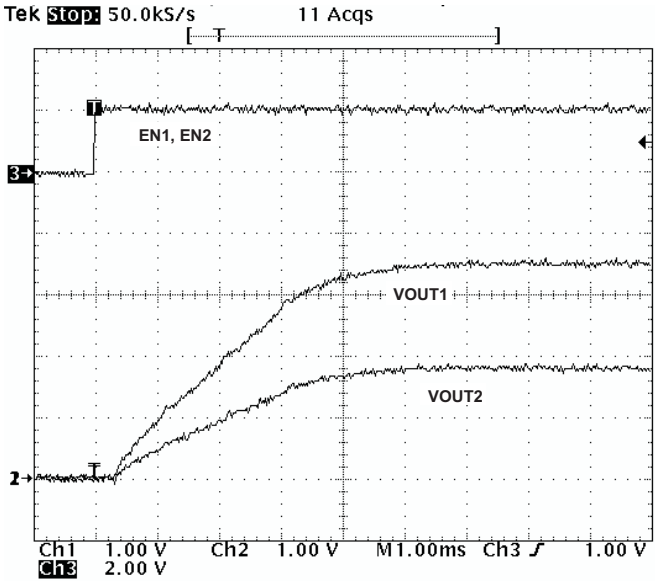



**Figure 35. Ratiometric Start-Up Using Coupled SS/TR Pins**

## DETAILED DESCRIPTION (continued)

Figure 34 shows a method for a ratiometric start-up sequence by connecting the SS/TR pins together. The regulator outputs ramp up and reach regulation at the same time. When calculating the slow-start time, the pullup current source must be doubled in Equation 6. Figure 35 shows the results of Figure 34.

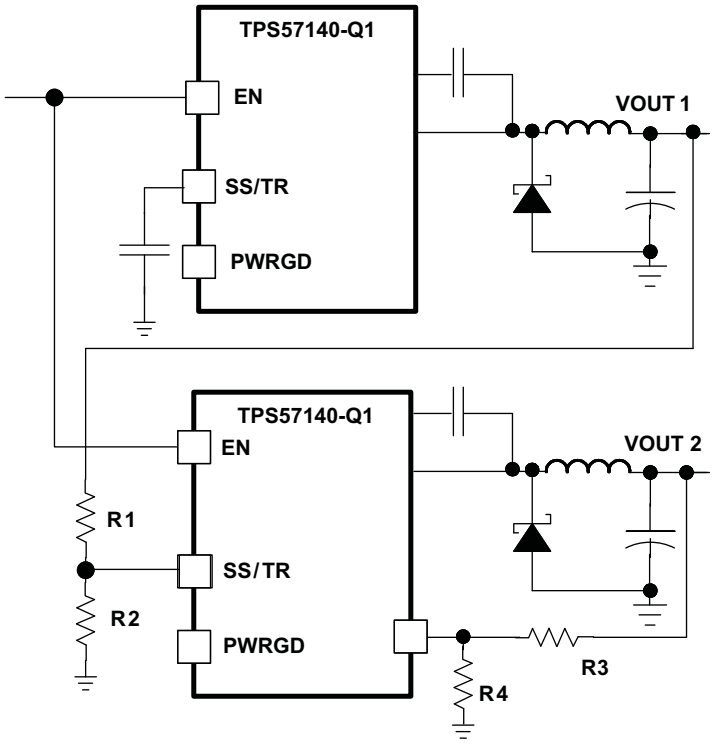



**Figure 36. Schematic for Ratiometric and Simultaneous Start-Up Sequence**

One can implement ratiometric and simultaneous power-supply sequencing by connecting the resistor network of R1 and R2 shown in Figure 36 to the output of the power supply that requires tracking, or to another voltage reference source. Using Equation 7 and Equation 8, calculate values for the tracking resistors to initiate the Vout2 slightly before, after, or at the same time as Vout1. Equation 9 is the voltage difference between Vout1 and Vout2 at 95% of nominal output regulation.

The deltaV variable is zero volts for simultaneous sequencing. To minimize the effect of the inherent SS/TR-to-VSENSE offset (Vssoffset) in the slow-start circuit and the offset created by the pullup current source (Iss) and tracking resistors, the equations include Vssoffset and Iss as variables.

To design a ratiometric start-up in which the Vout2 voltage is slightly greater than the Vout1 voltage when Vout2 reaches regulation, use a negative number in Equation 7 through Equation 9 for deltaV. Equation 9 results in a positive number for applications in which Vout2 is slightly lower than Vout1 when Vout2 regulation is achieved.

Because the SS/TR pin must be below 40 mV before starting after an EN, UVLO, or thermal shutdown fault, a design requires careful selection of the tracking resistors to ensure the device restarts after a fault. Make sure the calculated R1 value from Equation 7 is greater than the value calculated in Equation 10 to ensure the device can recover from a fault.

As the SS/TR voltage becomes more than 85% of the nominal reference voltage, Vssoffset becomes larger as the slow-start circuits gradually hand off the regulation reference to the internal voltage reference. The SS/TR pin voltage must be greater than 1.3 V for a complete handoff to the internal voltage reference as shown in Figure 23.

## DETAILED DESCRIPTION (continued)

$$R1 = \frac{Vout2 + deltaV}{VREF} \times \frac{Vssoffset}{Iss} \quad (7)$$

$$R2 = \frac{VREF \times R1}{Vout2 + deltaV - VREF} \quad (8)$$

$$deltaV = Vout1 - Vout2 \quad (9)$$

$$R1 > 2800 \times Vout1 - 180 \times deltaV \quad (10)$$

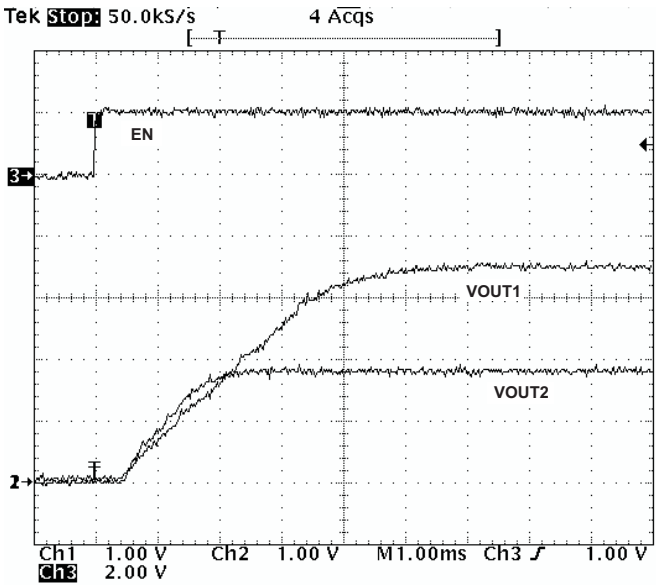



**Figure 37. Ratiometric Start-Up With $V_{OUT2}$ Leading $V_{OUT1}$**

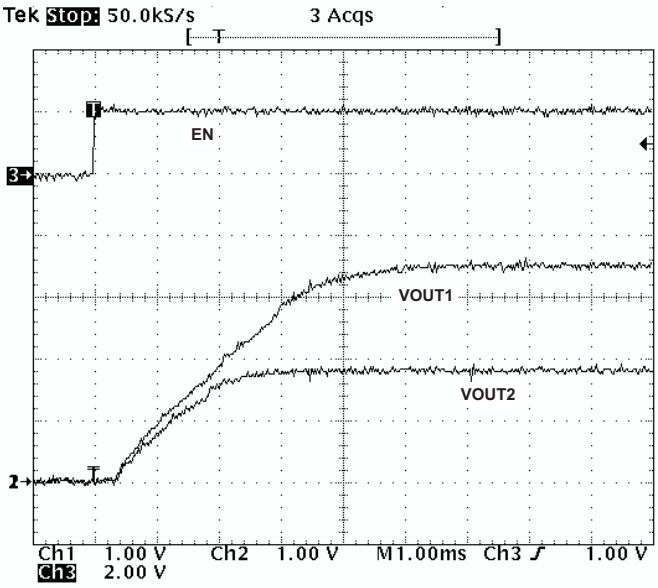



**Figure 38. Ratiometric Start-Up With $V_{OUT1}$ Leading $V_{OUT2}$**

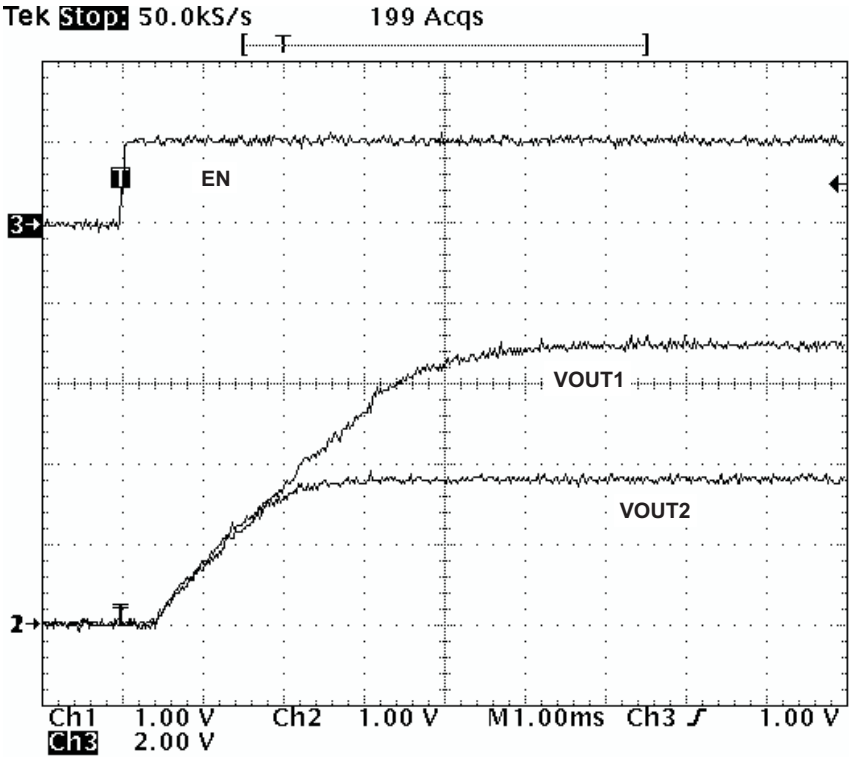



**Figure 39. Simultaneous Start-Up With Tracking Resistor**

## DETAILED DESCRIPTION (continued)

### Constant Switching Frequency and Timing Resistor (RT/CLK Pin)

The switching frequency of the TPS57140-Q1 is adjustable over a wide range from approximately 100-kHz to 2500-kHz by placing a resistor on the RT/CLK pin. The RT/CLK pin voltage is typically 0.5 V and must have a resistor to ground to set the switching frequency. To determine the timing resistance for a given switching frequency, use Equation 11 or the curves in Figure 40 or Figure 41. To reduce the solution size, one would typically set the switching frequency as high as possible, but consider tradeoffs of the supply efficiency, maximum input voltage and minimum controllable on-time.

The minimum controllable on time is typically 130 ns, which limits the maximum operating input voltage.

The frequency-shift circuit also limits the maximum switching frequency. The following contains more discussion on the details of the maximum switching frequency.

$$\text{RT (kOhm)} = \frac{206033}{f\text{sw (kHz)}^{1.0888}} \tag{11}$$

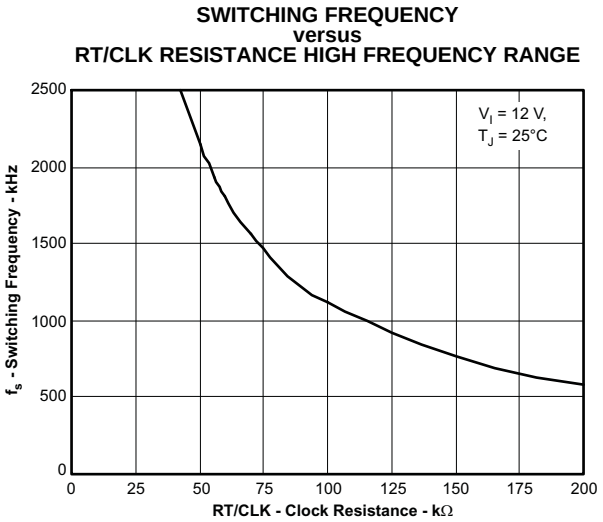



**Figure 40. High-Range RT**

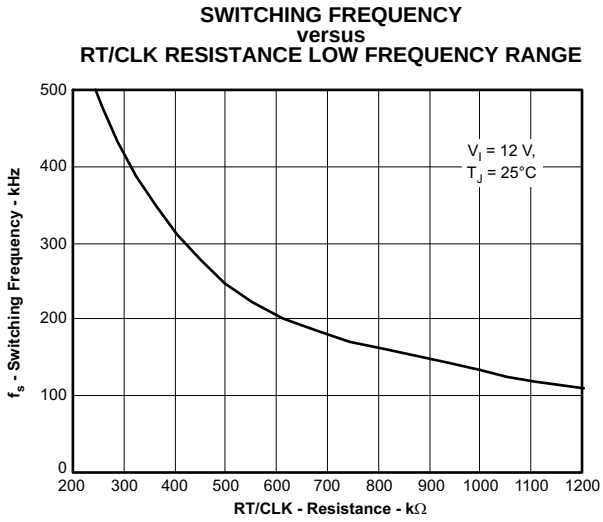



**Figure 41. Low-Range RT**

### Overcurrent Protection and Frequency Shift

The TPS57140-Q1 implements current-mode control, which uses the COMP pin voltage to turn off the high-side MOSFET on a cycle-by-cycle basis. During each cycle, the device compares the switch current and COMP pin voltage. When the peak switch current intersects the COMP voltage, the high side switch turns off. During overcurrent conditions that pull the output voltage low, the error amplifier responds by driving the COMP pin high, increasing the switch current. The internal clamping of the error amplifier output functions as a switch current limit.

To increase the maximum operating switching frequency at high input voltages, the TPS57140-Q1 implements a frequency shift. The divisor of the switching frequency goes to 8, 4, 2, and 1 as the voltage ramps from 0 to 0.8 volts on the VSENSE pin.

The device implements a digital frequency shift to enable synchronizing to an external clock during normal start-up and fault conditions. Because the device can only divide the switching frequency by 8, there is a maximum input voltage limit in which the device operates and still has frequency-shift protection.

During short-circuit events (particularly with high-input-voltage applications), the control loop has a finite minimum controllable on-time and the output has a very low voltage. During the switch on-time, the inductor current ramps to the peak current limit because of the high input voltage and minimum on-time. During the switch off time, the inductor would normally not have enough off-time and output voltage for the inductor to ramp down by the ramp-up amount. The frequency shift effectively increases the off-time, allowing the current to ramp down.

## DETAILED DESCRIPTION (continued)

### Selecting the Switching Frequency

The selected switching frequency should be the lower value of the two equations, Equation 12 and Equation 13. Equation 12 is the maximum switching frequency limitation set by the minimum controllable on-time. Setting the switching frequency above this value causes the regulator to skip switching pulses.

Equation 13 is the maximum switching-frequency limit set by the frequency-shift protection. To have adequate output short-circuit protection at high input voltages, set the switching frequency to be less than the fsw(maxshift) frequency. In Equation 13, to calculate the maximum switching frequency, one must take into account that the output voltage decreases from the nominal voltage to 0 volts, and that the fdiv integer increases from 1 to 8, corresponding to the frequency shift.

In Figure 42, the solid line illustrates a typical safe operating area regarding frequency shift and assumes the output voltage is zero volts, the resistance of the inductor is 0.1 Ω, the FET on-resistance is 0.2 Ω, and the voltage drop of the diode is 0.5 V. The dashed line is the maximum switching frequency to avoid pulse skipping. Enter these equations in a spreadsheet or other software, or use the SwitcherPro design software to determine the switching frequency.

$$f_{SW(max\,skip)} = \frac{1}{t_{ON}} \times \left( \frac{I_L \times R_{dc} + V_{OUT} + V_d}{V_{IN} - I_L \times R_{DS(on)} + V_d} \right) \quad (12)$$

$$f_{SWshift} = \frac{f_{DIV}}{t_{ON}} \times \left( \frac{I_L \times R_{dc} + V_{OUT(sc)} + V_d}{V_{IN} - I_L \times R_{DS(on)} + V_d} \right) \quad (13)$$

| | |
|---|---|
| $I_L$ | Inductor current |
| Rdc | Inductor resistance |
| $V_{IN}$ | Maximum input voltage |
| $V_{OUT}$ | Output voltage |
| $V_{OUTSC}$ | Output voltage during short |
| Vd | Diode voltage drop |
| $r_{DS(on)}$ | Switch on-resistance |
| $t_{ON}$ | Controllable on-time |
| $f_{DIV}$ | Frequency divide (equals 1, 2, 4, or 8) |

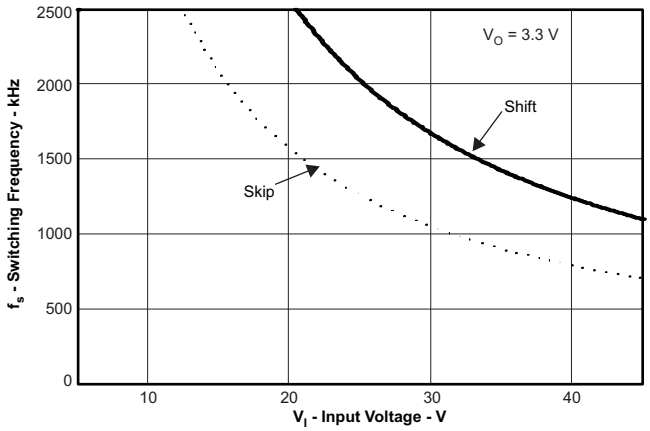



**Figure 42. Maximum Switching Frequency versus Input Voltage**

## DETAILED DESCRIPTION (continued)

### How to Interface to RT/CLK Pin

One can use the RT/CLK pin to synchronize the regulator to an external system clock. To implement the synchronization feature, connect a square wave to the RT/CLK pin through the circuit network shown in Figure 43. The square wave amplitude must transition lower than 0.5 V and higher than 2.2 V on the RT/CLK pin and have an on-time greater than 40 ns and an off-time greater than 40 ns. The synchronization frequency range is 300 kHz to 2200 kHz. The rising edge of PH is synchronizes to the falling edge of the signal on the RT/CLK pin. Design the external synchronization circuit in such a way that the device has the default frequency-set resistor connected from the RT/CLK pin to ground should the synchronization signal turn off. TI recommends using a frequency-set resistor connected as shown in Figure 43 through a 50-Ω resistor to ground. The resistor should set the switching frequency close to the external CLK frequency. TI recommends ac-coupling the synchronization signal through a 10-pF ceramic capacitor and a 4-kΩ series resistor to the RT/CLK pin. The series resistor reduces PH jitter in heavy-load applications when synchronizing to an external clock, and in applications which transition from synchronizing to RT mode. The first time CLK rises above the CLK threshold, the device switches from the RT resistor frequency to PLL mode. The internal 0.5-V voltage source opens and the CLK pin becomes high-impedance as the PLL starts to lock onto the external signal. Because there is a PLL on the regulator, the switching frequency can be higher or lower than the frequency set with the external resistor. The device transitions from the resistor mode to the PLL mode and then increases or decreases the switching frequency until the PLL locks onto the CLK frequency within 100 microseconds.

When the device transitions from the PLL to resistor mode, the switching frequency slows down from the CLK frequency to 150 kHz; then reapply the 0.5-V voltage, and the resistor then sets the switching frequency. The didisor of the switching frequency goes to 8, 4, 2, and 1 as the voltage ramps from 0 to 0.8 volts on the VSENSE pin. The device implements a digital frequency shift to enable synchronizing to an external clock during normal start-up and fault conditions. Figure 44, Figure 45, and Figure 46 show the device synchronized to an external system clock in continuous-conduction mode (CCM), discontinuous-conduction (DCM), and pulse-skip mode (PSM).

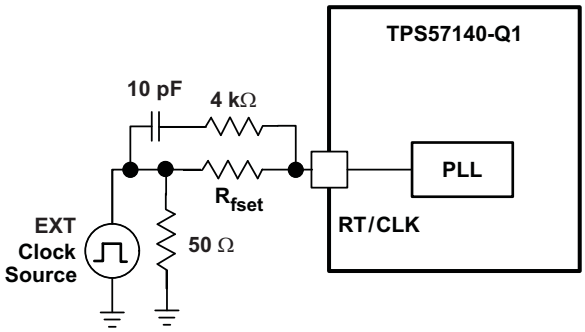



**Figure 43. Synchronizing to a System Clock**

## DETAILED DESCRIPTION (continued)

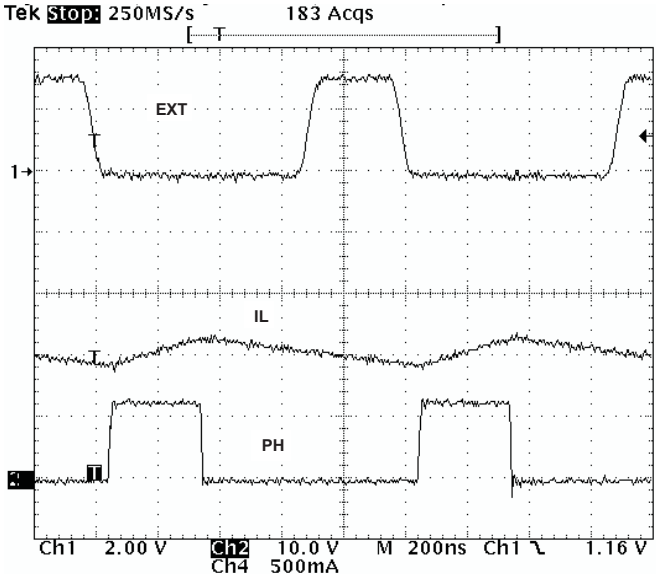



Figure 44. Plot of Synchronizing in CCM

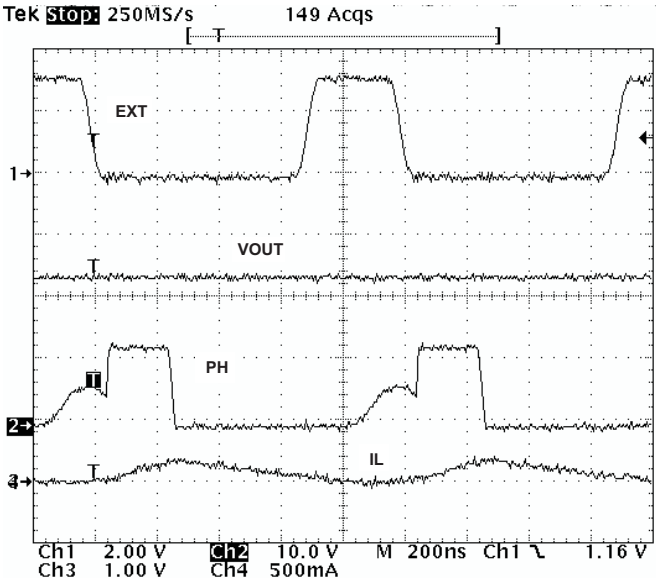



Figure 45. Plot of Synchronizing in DCM

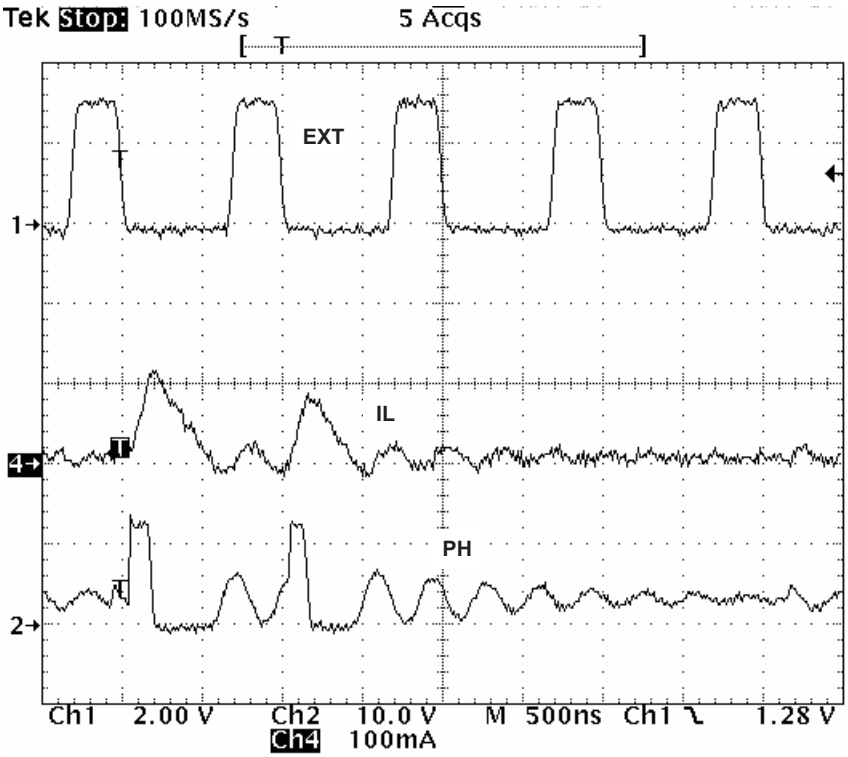



Figure 46. Plot of Synchronizing in PSM

### Power Good (PWRGD Pin)

The PWRGD pin is an open-drain output. Once the VSENSE pin is between 94% and 107% of the internal voltage reference, the PWRGD pin de-asserts and the pin floats. TI recommends using a pullup resistor between the values of 1 kΩ and 100 kΩ to a voltage source that is 5.5 V or less. PWRGD is in a defined state once the VIN input voltage is greater than 1.5 V, but with reduced current-sinking capability. PWRGD achieves full current-sinking capability as the VIN input voltage approaches 3 V.

## DETAILED DESCRIPTION (continued)

The PWRGD pin goes low when VSENSE is lower than 92% or greater than 109% of the nominal internal reference voltage. Also, PWRGD goes low if UVLO or thermal shutdown asserts or the EN pin goes low.

### Overvoltage Transient Protection

The TPS57140-Q1 incorporates an overvoltage transient protection (OVTP) circuit to minimize voltage overshoot when recovering from output fault conditions or strong unload transients on power-supply designs with low-value output capacitance. For example, with the power-supply output overloaded, the error amplifier compares the actual output voltage to the internal reference voltage. If the VSENSE pin voltage is lower than the internal reference voltage for a considerable time, the output of the error amplifier responds by clamping the error-amplifier output to a high voltage, thus requesting the maximum output current. On removal of the condition, the regulator output rises and the error-amplifier output transitions to the steady-state duty cycle. In some applications, the power-supply output voltage can respond faster than the error-amplifier output can respond; this actuality leads to the possibility of an output overshoot. The OVTP feature minimizes the output overshoot, when using a low-value output capacitor, by implementing a circuit to compare the VSENSE pin voltage to OVTP threshold, which is 109% of the internal voltage reference. A VSENSE pin voltage greater than the OVTP threshold disables the high-side MOSFET, preventing current from flowing to the output and minimizing output overshoot. The VSENSE voltage dropping lower than the OVTP threshold allows the high-side MOSFET to turn on at the next clock cycle.

### Thermal Shutdown

The device implements an internal thermal shutdown to protect itself if the junction temperature exceeds 182°C. The thermal shutdown forces the device to stop switching when the junction temperature exceeds the thermal trip threshold. Once the die temperature decreases below 182°C, the device reinitiates the power-up sequence by discharging the SS/TR pin.

### Small-Signal Model for Loop Response

Figure 47 shows an equivalent model for the TPS57140-Q1 control loop which one can model in a circuit-simulation program to check frequency response and dynamic load response. The error amplifier is a transconductance amplifier with a $gm_{EA}$ of 97 µS. One can model the error amplifier using an ideal voltage-controlled current source. Resistor $R_o$ and capacitor $C_o$ model the open-loop gain and frequency response of the amplifier. The 1-mV ac voltage source between nodes a and b effectively breaks the control loop for the frequency-response measurements. Plotting c / a shows the small-signal response of the frequency compensation. Plotting a / b shows the small-signal response of the overall loop. One can check the dynamic loop response in a time-domain analysis by replacing $R_L$ with a current source having the appropriate load-step amplitude and step rate. This equivalent model is only valid for continuous-conduction-mode designs.

## DETAILED DESCRIPTION (continued)

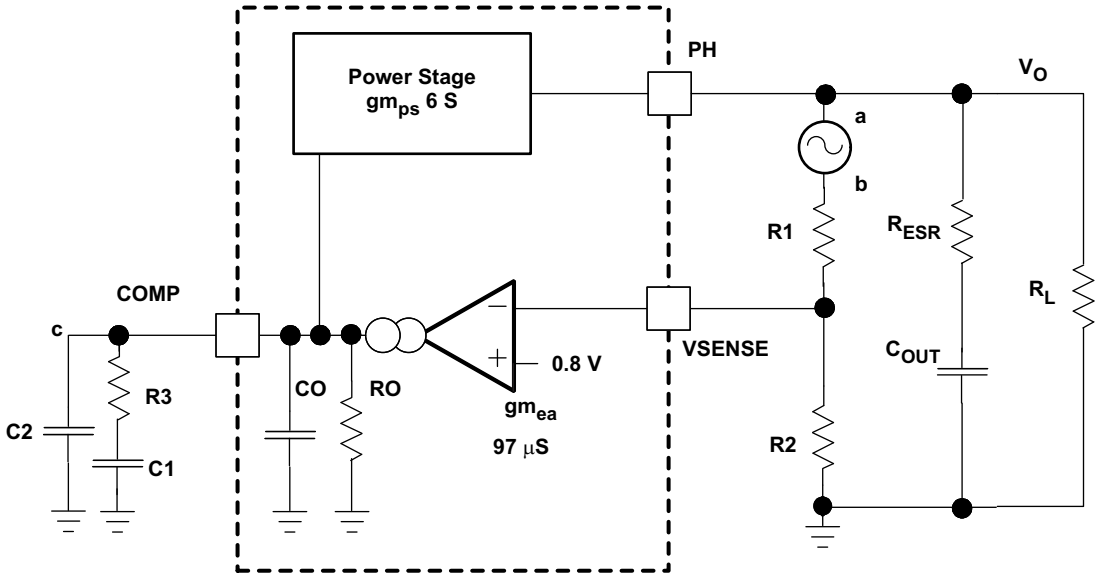



**Figure 47. Small-Signal Model for Loop Response**

### Simple Small-Signal Model for Peak-Current-Mode Control

Figure 48 describes a simple small-signal model that one can use to understand how to design the frequency compensation. One can approximate the TPS57140-Q1 power stage by a voltage-controlled current source (duty-cycle modulator) supplying current to the output capacitor and load resistor. Equation 14 shows the control-to-output transfer function, which consists of a dc gain, one dominant pole, and one ESR zero. The quotient of the change in switch current and the change in COMP pin voltage (node c in Figure 47) is the power-stage transconductance. The $gm_{PS}$ for the TPS57140-Q1 is 6 S. The low-frequency gain of the power-stage frequency response is the product of the transconductance and the load resistance as shown in Equation 15.

As the load current increases and decreases, the low-frequency gain decreases and increases, respectively. This variation with the load may seem problematic at first glance, but fortunately the dominant pole moves with the load current (see Equation 16). The combined effect is highlighted by the dashed line in the right half of Figure 48. As the load current decreases, the gain increases and the pole frequency lowers, keeping the 0-dB crossover frequency the same for the varying load conditions, which makes it easier to design the frequency compensation. The type of output capacitor chosen determines whether the ESR zero has a profound effect on the frequency-compensation design. Using high-ESR aluminum electrolytic capacitors may reduce the number of frequency-compensation components needed to stabilize the overall loop because the phase margin increases from the ESR zero at the lower frequencies (see Equation 17).

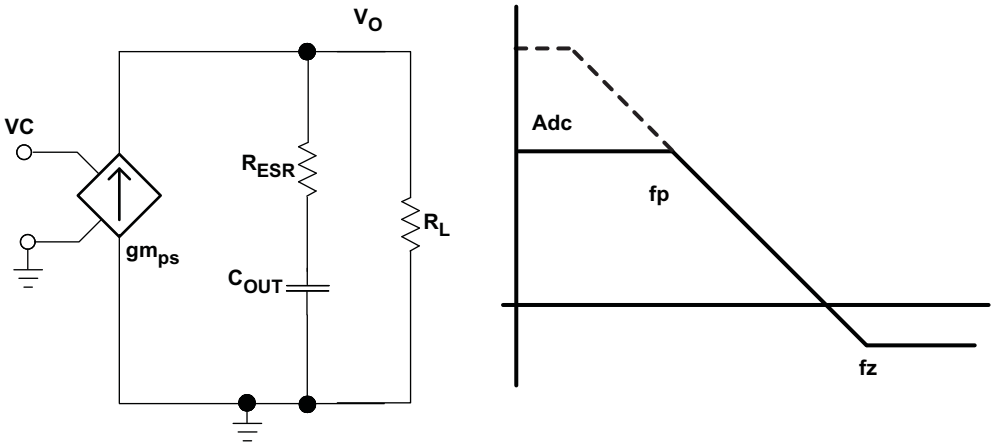



**Figure 48. Simple Small-Signal Model and Frequency Response for Peak-Current-Mode Control**

## DETAILED DESCRIPTION (continued)

$$\frac{V_{OUT}}{V_C} = Adc \times \frac{\left(1 + \frac{s}{2\pi \times f_Z}\right)}{\left(1 + \frac{s}{2\pi \times f_P}\right)} \quad (14)$$

$$Adc = gm_{ps} \times R_L \quad (15)$$

$$f_P = \frac{1}{C_{OUT} \times R_L \times 2\pi} \quad (16)$$

$$f_Z = \frac{1}{C_{OUT} \times R_{ESR} \times 2\pi} \quad (17)$$

### Small-Signal Model for Frequency Compensation

The TPS57140-Q1 uses a transconductance amplifier for the error amplifier and readily supports three of the commonly-used frequency compensation circuits. Figure 49 shows compensation circuits Type 2A, Type 2B, and Type 1. Implementation of Type 2 circuits most likely is in high-bandwidth power-supply designs using low-ESR output capacitors. Use of the Type 1 circuit is with power-supply designs having high-ESR aluminum electrolytic or tantalum capacitors. Equation 18 and Equation 19 show how to relate the frequency response of the amplifier to the small-signal model in Figure 49. Modeling of the open-loop gain and bandwidth uses the $R_O$ and $C_O$ shown in Figure 49. See the *Application Information* section for a design example using a Type 2A network with a low-ESR output capacitor.

Equation 18 through Equation 27 are a reference for those who prefer to compensate using the preferred methods. Those who prefer to use a prescribed method must use the method outlined in the *Application Information* section or use switched information.

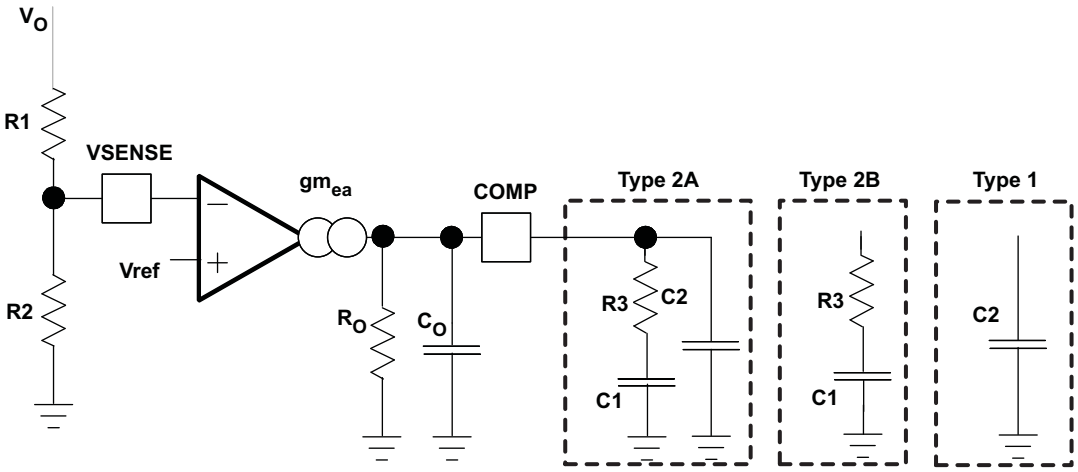



**Figure 49. Types of Frequency Compensation**

## DETAILED DESCRIPTION (continued)

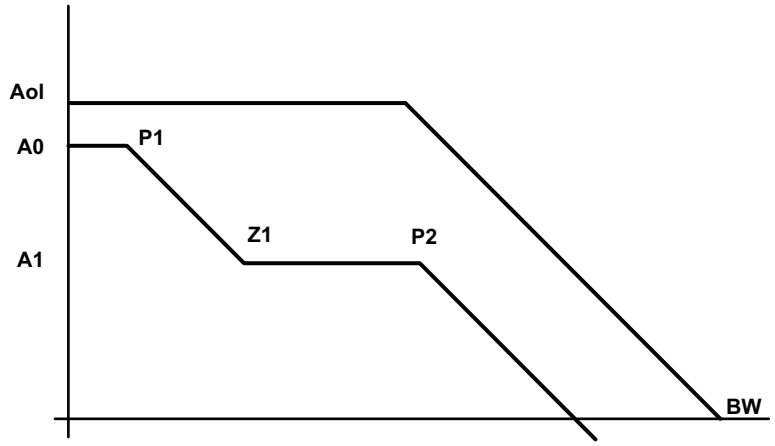



**Figure 50. Frequency Response of the Type 2A and Type 2B Frequency Compensation**

$$Ro = \frac{Aol(V/V)}{gm_{ea}} \quad (18)$$

$$C_{OUT} = \frac{gm_{ea}}{2\pi \times BW\ (Hz)} \quad (19)$$

$$EA = A0 \times \frac{\left(1 + \frac{s}{2\pi \times f_{Z1}}\right)}{\left(1 + \frac{s}{2\pi \times f_{P1}}\right) \times \left(1 + \frac{s}{2\pi \times f_{P2}}\right)} \quad (20)$$

$$A0 = gm_{ea} \times Ro \times \frac{R2}{R1 + R2} \quad (21)$$

$$A1 = gm_{ea} \times Ro \,||\, R3 \times \frac{R2}{R1 + R2} \quad (22)$$

$$P1 = \frac{1}{2\pi \times Ro \times C1} \quad (23)$$

$$Z1 = \frac{1}{2\pi \times R3 \times C1} \quad (24)$$

$$P2 = \frac{1}{2\pi \times R3 \,||\, R \times (C2 + C_{OUT})} \text{ type 2a} \quad (25)$$

$$P2 = \frac{1}{2\pi \times R3 \,||\, R \times C_{OUT}} \text{ type 2b} \quad (26)$$

$$P2 = \frac{1}{2\pi \times R \times (C2 + C_{OUT})} \text{ type 1} \quad (27)$$

## APPLICATION INFORMATION

### Design Guide — Step-By-Step Design Procedure

This example details the design of a high-frequency switching regulator design using ceramic output capacitors. One must know a few parameters in order to start the design process. The determination of these parameters is typically at the system level. For this example, we start with the following known parameters:

| | |
|---|---|
| Output Voltage | 3.3 V |
| Transient response, 0 to 1.5-A load step | ΔVout = 4% |
| Maximum output current | 1.5 A |
| Input voltage | 12 V nom., 8 V to 18 V |
| Output voltage ripple | < 33 $mV_{pp}$ |
| Start input voltage (rising VIN) | 7.25 V |
| Stop input voltage (falling VIN) | 6.25 V |

### Selecting the Switching Frequency

The first step is to decide on a switching frequency for the regulator. Typically, the user wants to choose the highest switching frequency possible, because this produces the smallest solution size. The high switching frequency allows for lower-valued inductors and smaller output capacitors compared to a power supply that switches at a lower frequency. The switching frequency that one can select has limits imposed by the minimum on-time of the internal power switch, the input voltage, the output voltage, and the frequency-shift limitation.

Use Equation 12 and Equation 13 to find the maximum switching frequency for the regulator; choose the lower value of the two equations. Switching frequencies higher than this value result in pulse skipping or the lack of overcurrent protection during a short circuit.

The typical minimum on-time, $t_{onmin}$, is 130 ns for the TPS57140-Q1. For this example, the output voltage is 3.3 V and the maximum input voltage is 18 V, which allows for a maximum switch frequency up to 1600 kHz when including the inductor resistance, on-resistance, and diode voltage in Equation 12. To ensure overcurrent runaway is not a concern during short circuits in the design, use Equation 13 or the solid curve in Figure 42 to determine the maximum switching frequency. With a maximum input voltage of 20 V, assuming a diode voltage of 0.5 V, inductor resistance of 100 mΩ, switch resistance of 200 mΩ, an output current of 2.8 A, the maximum switching frequency is approximately 1600 kHz.

Choosing the lower of the two values and adding some margin, a switching frequency of 1200 kHz is used. To determine the timing resistance for a given switching frequency, use Equation 11 or the curve in Figure 40.

Resistor $R_t$ sets the switching frequency as shown in Figure 51.

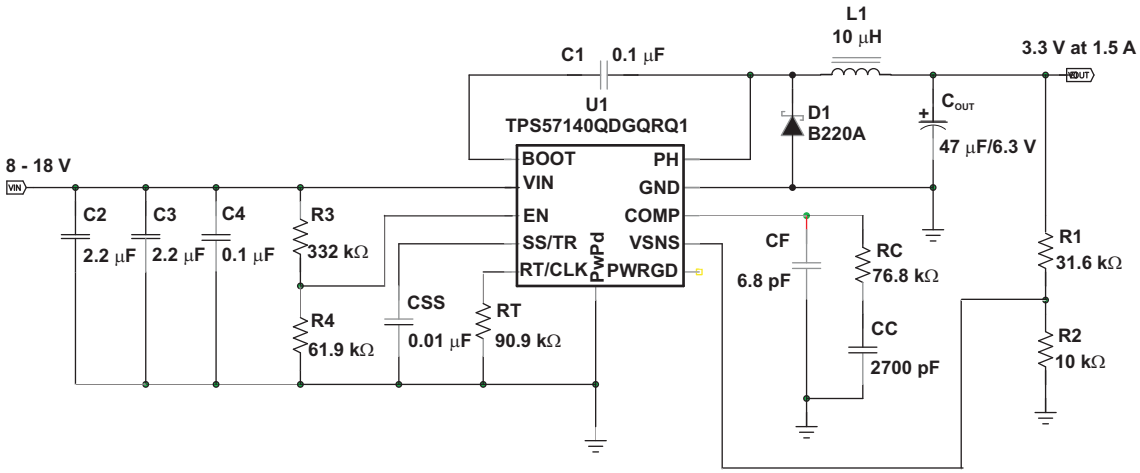



**Figure 51. High-Frequency, 3.3-V Output Power-Supply Design With Adjusted UVLO**

## Output Inductor Selection ($L_O$)

To calculate the minimum value of the output inductor, use Equation 28.

$K_{IND}$ is a coefficient that represents the amount of inductor ripple current relative to the maximum output current.

The output capacitor filters the inductor ripple current. Therefore, choosing high inductor ripple currents impacts the selection of the output capacitor, because the output capacitor must have a ripple-current rating equal to or greater than the inductor ripple current. In general, the inductor ripple value is at the discretion of the designer; however, one can use the following guidelines.

For designs using low-ESR output capacitors such as ceramics, use a value as high as $K_{IND}$ = 0.3. When using higher-ESR output capacitors, $K_{IND}$ = 0.2 yields better results. Because the inductor ripple current is part of the PWM control system, the inductor ripple current should always be greater than 100 mA for dependable operation. In a wide-input voltage regulator, it is best to choose an inductor ripple current on the larger side. This allows the inductor to still have a measurable ripple current with the input voltage at its minimum.

For this design example, use $K_{IND}$ = 0.2 and the calculated minimum inductor value is 7.6 µH. For this design, the choice was a nearest standard value of 10 µH. For the output filter inductor, it is important not to exceed the rms-current and saturation-current ratings. Find the rms and peak inductor current from Equation 30 and Equation 31.

For this design, the rms inductor current is 1.506 A and the peak inductor current is 1.62 A. The chosen inductor is a MSS6132-103. It has a saturation current rating of 1.64 A and an rms current rating of 1.9 A.

As the equation set demonstrates, lower ripple currents reduce the output voltage ripple of the regulator but require a larger value of inductance. Selecting higher ripple currents increases the output-voltage ripple of the regulator but allows for a lower inductance value.

The current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults, or transient load conditions, the inductor current can increase above the calculated peak inductor current level calculated previously. In transient conditions, the inductor current can increase up to the switch-current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the switch-current limit rather than the peak inductor current.

$$\text{Lo min} = \frac{\text{Vinmax} - \text{Vout}}{\text{Io} \times K_{IND}} \times \frac{\text{Vout}}{\text{Vinmax} \times fsw} \tag{28}$$

$$I_{RIPPLE} \le I_O \times K_{IND} \tag{29}$$

$$I_{L(rms)} = \sqrt{(I_O)^2 + \frac{1}{12} \times \left( \frac{V_{OUT} \times (\text{Vinmax} - V_{OUT})}{\text{Vinmax} \times L_O \times f_{SW}} \right)^2} \tag{30}$$

$$ILpeak = Iout + \frac{Iripple}{2} \tag{31}$$

## Output Capacitor

There are three primary considerations for selecting the value of the output capacitor. The output capacitor determines the modulator pole, the output-voltage ripple, and how the regulator responds to a large change in load current. Setect the output capacitance based on the most stringent of these three criteria.

The desired response to a large change in the load current is the first criterion. The output capacitor must supply the load with current when the regulator cannot. This situation would occur if there are desired hold-up times for the regulator where the output capacitor must hold the output voltage above a certain level for a specified amount of time after the input power is removed. The regulator also temporarily is not able to supply sufficient output current if there is a large, fast increase in the current needs of the load, such as transitioning from no load to a full load. The regulator usually needs two or more clock cycles for the control loop to see the change in load current and output voltage and adjust the duty cycle to react to the change. The output-capacitor size must be adequate to supply the extra current to the load until the control loop responds to the load change. The output capacitance must be large enough to supply the difference in current for two clock cycles while only allowing a tolerable amount of droop in the output voltage. Calculate the minimum output capacitance necessary to accomplish this using Equation 32.

Where ΔIout is the change in output current, ƒsw is the switching frequency of the regulator and ΔVout is the allowable change in the output voltage. For this example, the transient load response is specified as a 4% change in Vout for a load step from 0 A (no load) to 1.5 A (full load). For this example, ΔIout = 1.5 – 0 = 1.5 A and ΔVout = 0.04 × 3.3 V = 0.132 V. Using these numbers gives a minimum capacitance of 18.9 µF. This value does not take the ESR of the output capacitor into account in the output-voltage change. For ceramic capacitors, the ESR is usually small enough to ignore in this calculation. Aluminum electrolytic and tantalum capacitors have higher ESR that one should take into account.

The catch diode of the regulator cannot sink current, so any stored energy in the inductor produces an output voltage overshoot when the load current rapidly decreases, see Figure 52. The output capacitor must also be sized to absorb energy stored in the inductor when transitioning from a high load current to a lower load current. The excess energy that is stored in the output capacitor increases the voltage on the capacitor. The capacitor must be sized to maintain the desired output voltage during these transient periods. UseEquation 33 to calculate the minimum capacitance to keep the output voltage overshoot to a desired value, where L is the value of the inductor, $I_{OH}$ is the output current under heavy load, $I_{OL}$ is the output under light load, VF is the final peak output voltage, and Vi is the initial capacitor voltage. For this example, the worst-case load step is from 1.5 A to 0 A. The output voltage increases during this load transition, and the stated maximum in our specification is 4% of the output voltage. This makes Vf = 1.04 × 3.3 = 3.432. Vi is the initial capacitor voltage, which is the nominal output voltage of 3.3 V. Using these numbers in Equation 33 yields a minimum capacitance of 25.3 µF.

Use Equation 34 to calculate the minimum output capacitance needed to meet the ripple specification for output voltage. Where fsw is the switching frequency, $V_{oripple}$ is the maximum allowable output-voltage ripple, and $I_{ripple}$ is the ripple current of the inductor. Equation 34 yields 0.7 µF.

Use Equation 35 to calculate the maximum ESR an output capacitor can have to meet the ripple specification for the output voltage. Equation 35 indicates the ESR should be less than 147 mΩ.

The most stringent criterion for the output capacitor is 25.3 µF of capacitance to keep the output voltage in regulation during an unload transient.

Factor in additional capacitance de-ratings for aging, temperature and dc bias, increasing this minimum value. For this example, select a 47-µF 6.3-V X7R ceramic capacitor with 5 mΩ of ESR.

Capacitors generally have limits to the amount of ripple current they can handle without failing or producing excess heat. Specify an output capacitor that can support the inductor ripple current. Some capacitor data sheets specify the root-mean-square (rms) value of the maximum ripple current. Use Equation 36 to calculate the rms ripple current that the output capacitor must support. For this application, Equation 36 yields 64.8 mA.

$$C_{OUT} > \frac{2 \times \Delta I_{OUT}}{f_{SW} \times \Delta V_{OUT}} \tag{32}$$

$$C_{OUT} > L_O \times \frac{\left( (I_{OH})^2 - (I_{OL})^2 \right)}{\left( (V_f)^2 - (V_i)^2 \right)} \tag{33}$$

$$C_{OUT} > \frac{1}{8 \times f_{SW}} \times \frac{1}{\left( \frac{V_{OUT(ripple)}}{I_{RIPPLE}} \right)} \tag{34}$$

$$R_{ESR} = \frac{V_{OUT(ripple)}}{I_{RIPPLE}} \quad (35)$$

$$I_{COUT(rms)} = \frac{V_{OUT} \times \left(V_{IN(max)} - V_{OUT}\right)}{\sqrt{12} \times V_{IN(max)} \times L_O \times f_{SW}} \quad (36)$$

## Catch Diode

The TPS57140-Q1 requires an external catch diode between the PH pin and GND. The selected diode must have a reverse voltage rating equal to or greater than Vinmax. The peak current rating of the diode must be greater than the maximum inductor current. The diode should also have a low forward voltage. Schottky diodes are typically a good choice for the catch diode due to their low forward voltage. The lower the forward voltage of the diode, the higher the efficiency of the regulator is.

Typically, the higher the voltage and current ratings the diode has, the higher the forward voltage is. Because the design example has an input voltage up to 18 V, select a diode with a minimum of 20-V reverse voltage.

For the example design, Schottky diode selection is the B220A for its lower forward voltage, and it comes in a larger package size, which has good thermal characteristics over small devices. The typical forward voltage of the B220A is 0.5 volts.

The diode selection must also hAVE an appropriate power rating. The diode conducts the output current during the off-time of the internal power switch. The off-time of the internal switch is a function of the maximum input voltage, the output voltage, and the switching frequency. The output current during the off-time multiplied by the forward voltage of the diode equals the conduction losses of the diode. At higher switch frequencies, take the ac losses of the diode into account. The ac losses of the diode are due to the charging and discharging of the junction capacitance and reverse recovery. Use Equation 37 to calculate the total power dissipation, conduction losses plus ac losses, of the diode.

The B220A has a junction capacitance of 120 pF. Using Equation 37, the selected diode dissipates 0.632 W. This power dissipation, depending on mounting techniques, should produce a 16°C temperature rise in the diode when the input voltage is 18 V and the load current is 1.5 A.

If the power supply spends a significant amount of time at light load currents or in sleep mode, consider using a diode which has a low leakage current and slightly higher forward voltage drop.

$$P_D = \frac{\left(V_{IN(max)} - V_{OUT}\right) \times I_{OUT} \times Vfd}{V_{IN(max)}} + \frac{C_j \times f_{SW} \times \left(V_{IN} + Vfd\right)^2}{2} \quad (37)$$

## Input Capacitor

The TPS57140-Q1 requires a high-quality ceramic, type X5R or X7R, input decoupling capacitor of at least 3 µF of effective capacitance, and in some applications a bulk capacitance. The effective capacitance includes any dc-bias effects. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple-current rating greater than the maximum input-current ripple of the TPS57140-Q1. Calculate the input-ripple current using Equation 38.

The value of a ceramic capacitor varies significantly over temperature and the amount of dc bias applied to the capacitor. One can minimize the capacitance variations due to temperature by selecting a dielectric material that is stable over temperature. Designers usually select X5R and X7R ceramic dielectrics for power regulator capacitors because they have a high capacitance-to-volume ratio and are fairly stable over temperature. The output capacitor selection must also take the dc bias into account. The capacitance value of a capacitor decreases as the dc bias across a capacitor increases.

This example design requires a ceramic capacitor with at least a 20-V voltage rating to support the maximum input voltage. Common standard ceramic capacitor voltage ratings include 4 V, 6.3 V, 10 V, 16 V, 25 V, 50 V, and 100 V, so select a 25-V capacitor. For this example, the selection is two 2.2-µF, 25-V capacitors in parallel. Table 1 shows a selection of high-voltage capacitors. The input capacitance value determines the input-voltage ripple of the regulator. Calculate the input-voltage ripple using Equation 39. Using the design example values, Ioutmax = 1.5 A, Cin = 4.4 µF, $f$sw = 1200 kHz, yields an input-voltage ripple of 71 mV and an rms input-ripple current of 0.701 A.

$$\text{Icirms} = \text{Iout} \times \sqrt{\frac{\text{Vout}}{\text{Vin min}} \times \frac{(\text{Vin min} - \text{Vout})}{\text{Vin min}}} \tag{38}$$

$$\Delta\text{Vin} = \frac{\text{Iout max} \times 0.25}{\text{Cin} \times f\text{sw}} \tag{39}$$

**Table 1. Capacitor Types**

| VENDOR | VALUE (µF) | EIA Size | VOLTAGE | DIALECTRIC | COMMENTS |
|---|---|---|---|---|---|
| Murata | 1 to 2.2 | 1210 | 100 V | X7R | GRM32 series |
| | 1 to 4.7 | | 50 V | | |
| | 1 | 1206 | 100 V | | GRM31 series |
| | 1 to 2.2 | | 50 V | | |
| Vishay | 1 10 1.8 | 2220 | 50 V | | VJ X7R series |
| | 1 to 1.2 | | 100 V | | |
| | 1 to 3.9 | 2225 | 50 V | | |
| | 1 to 1.8 | | 100 V | | |
| TDK | 1 to 2.2 | 1812 | 100 V | | C series C4532 |
| | 1.5 to 6.8 | | 50 V | | |
| | 1 to 2.2 | 1210 | 100 V | | C series C3225 |
| | 1 to 3.3 | | 50 V | | |
| AVX | 1 to 4.7 | 1210 | 50 V | | X7R dielectric series |
| | 1 | | 100 V | | |
| | 1 to 4.7 | 1812 | 50 V | | |
| | 1 to 2.2 | | 100 V | | |

## Slow-Start Capacitor

The slow-start capacitor determines the minimum amount of time it takes for the output voltage to reach its nominal programmed value during power up. This is useful if a load requires a controlled voltage-slew rate. This is also used if the output capacitance is very large and would require large amounts of current to charge the capacitor quickly to the output-voltage level. The large currents necessary to charge the capacitor may make the TPS57140-Q1 reach the current limit, or excessive current draw from the input power supply may cause the input voltage rail to sag. Limiting the output-voltage slew rate solves both of these problems.

The slow-start time must be long enough to allow the regulator to charge the output capacitor up to the output voltage without drawing excessive current. Use Equation 40 to find the minimum slow start time, tss, necessary to charge the output capacitor, Cout, from 10% to 90% of the output voltage, Vout, with an average slow-start current of Issavg. In the example, to charge the 47-µF output capacitor up to 3.3 V while only allowing the average input current to be 0.125A would require a 1-ms slow-start time.

Once the slow-start time is known, calculate the slow-start capacitor value using Equation 6. For the example circuit, the slow-start time is not too critical, because the output capacitor value is 47 µF, which does not require much current to charge to 3.3 V. The example circuit has the slow-start time set to an arbitrary value of 1 ms, which requires a 3.3-nF capacitor.

$$\text{Tss} > \frac{\text{Cout} \times \text{Vout} \times 0.8}{\text{Issavg}} \tag{40}$$

### Bootstrap Capacitor Selection

Connect a 0.1-µF ceramic capacitor between the BOOT and PH pins for proper operation. TI recommends using a ceramic capacitor with X5R or better grade dielectric. The capacitor should have a 10-V or higher voltage rating.

### Undervoltage Lockout Set Point

One can adjust the undervoltage lockout (UVLO) using an external voltage divider on the EN pin of the TPS57140-Q1. The UVLO has two thresholds, one for power up when the input voltage is rising and one for power down or brownouts when the input voltage is falling. For the example design, the supply should turn on and start switching once the input voltage increases above 7.25 V (enabled). After the regulator starts switching, it should continue to do so until the input voltage falls below 6.25 V (UVLO stop).

Set the programmable UVLO and enable voltages by using a resistor divider between Vin and ground to the EN pin. Use Equation 2 through Equation 3 to calculate the resistance values necessary. For the example application, 332 kΩ between Vin and EN and 61.9 kΩ between EN and ground are required to produce the 7.25- and 6.25-volt start and stop voltages.

### Output Voltage and Feedback Resistors Selection

For the example design, the selected resistance for R2 is 10 kΩ. Using Equation 1, the calculated value of R1 is 31.25 kΩ. The nearest standard 1% resistor is 31.6 kΩ. Due to current leakage of the VSENSE pin, the current flowing through the feedback network should be greater than 1 µA in order to maintain the output voltage accuracy. This requirement makes the maximum value of R2 equal to 800 kΩ. Choosing higher resistor values decreases quiescent current and improves efficiency at low output currents, but may introduce noise-immunity problems.

### Compensation

There are several industry techniques used to compensate dc-dc regulators. The method presented here yields high phase margins. For most conditions, the regulator has a phase margin between 60° and 90°. The method presented here ignores the effects of the slope compensation that is internal to the TPS57140-Q1. Ignoring the slope compensation usually causes the actual crossover frequency to be lower than the crossover frequency used in the calculations.

Use SwitcherPro software for a more accurate design.

The uncompensated regulator has a dominant pole, typically located between 300 Hz and 3 kHz, due to the output capacitor and load resistance, and a pole due to the error amplifier. One zero exists due to the output capacitor and the ESR. The zero frequency is higher than either of the two poles.

If left uncompensated, the double pole created by the error amplifier and the modulator would lead to an unstable regulator. Stabilizing the regulator requires one pole to be canceled out. One design approach is to locate a compensating zero at the modulator pole. Then select a crossover frequency that is higher than the modulator pole. Calculate the gain of the error amplifier to achieve the desired crossover frequency. The capacitor used to create the compensation zero, along with the output impedance of the error amplifier, forms a low-frequency pole to provide a minus-one slope through the crossover frequency. Then adding a compensating pole cancels the zero due to the output-capacitor ESR. If the ESR zero resides at a frequency higher than the switching frequency, then it can be ignored.

To compensate the TPS57140-Q1 using this method, first calculate the modulator pole and zero using the following equations:

$$fp\ mod = \frac{Ioutmax}{2 \times \pi \times Vout \times Cout} \quad (41)$$

where Ioutmax is the maximum output current, Cout is the output capacitance and Vout is the nominal output voltage.

$$fz\ mod = \frac{1}{2 \times \pi \times Resr \times Cout} \quad (42)$$

For the example design, the location of the modulator pole is at 1.5 kHz and the ESR zero is at 338 kHz.

Next, the designer must select a crossover frequency which determines the bandwidth of the control loop. The crossover-frequency location must be at a frequency at least five times higher than the modulator pole. The crossover-frequency selection must also be such that the available gain of the error amplifier at the crossover frequency is high enough to allow for proper compensation.

Use Equation 47 to calculate the maximum crossover frequency when the ESR-zero location is at a frequency that is higher than the desired crossover frequency. This is usually the case for ceramic or low-ESR tantalum capacitors. Aluminum electrolytic and tantalum capacitors typically produce a modulator zero at a low frequency due to their high ESR.

The example application uses a low-ESR ceramic capacitor with 10 mΩ of ESR, making the zero at 338 kHz.

This value is much higher than typical crossover frequencies, so calculate the maximum crossover frequency using both Equation 43 and Equation 46.

Using Equation 46 gives a minimum crossover frequency of 7.6 kHz and Equation 43 gives a maximum crossover frequency of 45.3 kHz.

Arbitrarily select a crossover frequency of 45 kHz from this range.

$$F_{c\,max} \le 2100 \sqrt{\frac{F_{pmod}}{V_{out}}} \text{ for ceramic capacitors.} \quad (43)$$

$$F_{c\,max} \le \frac{51442}{\sqrt{V_{out}}} \text{ for Tantalum or Aluminum capacitors.} \quad (44)$$

$$F_{c\,max} \le \frac{F_{sw}}{5} \text{ for all cases.} \quad (45)$$

$$F_{c\,min} \ge 5 \times F_{pmod} \text{ for all cases.} \quad (46)$$

After selection of a crossover frequency, $F_c$, calculate the gain of the modulator at the crossover frequency using Equation 47.

$$G_{MOD(fc)} = \frac{gm_{(PS)} \times R_{LOAD} \times (2\pi \times f_C \times C_{OUT} \times R_{ESR} + 1)}{2\pi \times f_C \times C_{OUT} \times (R_{LOAD} + R_{ESR}) + 1} \quad (47)$$

For the example problem, the gain of the modulator at the crossover frequency is 0.542. Next, calculate the compensation components. Use a resistor in series with a capacitor to create a compensating zero. A capacitor in parallel to these two components forms the compensating pole. However, calculating the values of these components varies, depending on whether the ESR-zero location is above or below the crossover frequency. For ceramic or low-ESR tantalum output capacitors, the zero location is usually above the crossover frequency. For aluminum electrolytic and tantalum capacitors, the modulator-zero location is usually lower in frequency than the crossover frequency. For cases where the modulator zero is higher than the crossover frequency (ceramic capacitors):

$$R_C = \frac{V_{OUT}}{G_{MOD(fc)} \times gm_{(EA)} \times V_{REF}} \quad (48)$$

$$Cc = \frac{1}{\pi \times Rc \times fp\ mod} \quad (49)$$

$$Cf = \frac{Co \times Resr}{Rc} \quad (50)$$

For cases where the modulator zero is less than the crossover frequency (aluminum or tantalum capacitors), the equations are:

$$R_C = \frac{V_{OUT}}{G_{MOD(fc)} \times f_{Z(mod)} \times gm_{(EA)} \times V_{REF}} \quad (51)$$

$$Cc = \frac{1}{\pi \times Rc \times fp\,mod} \quad (52)$$

$$Cf = \frac{1}{2 \times \pi \times Rc \times fz\,mod} \quad (53)$$

For the example problem, the ESR-zero location is at a higher frequency compared to the crossover frequency, so use Equation 50 through Equation 53 to calculate the compensation components. For the example problem, the calculated components are: Rc = 76.2 kΩ, Cc = 2710 pF, and Cf = 6.17 pF.

The calculated value of the Cf capacitor is not a standard value, so use a value of 2700 pF. Use 6.8 pF for Cc. The Rc resistor sets the gain of the error amplifier, which determines the crossover frequency. The calculated Rc resistor is not a standard value, so use 76.8 kΩ.

## APPLICATION CURVES

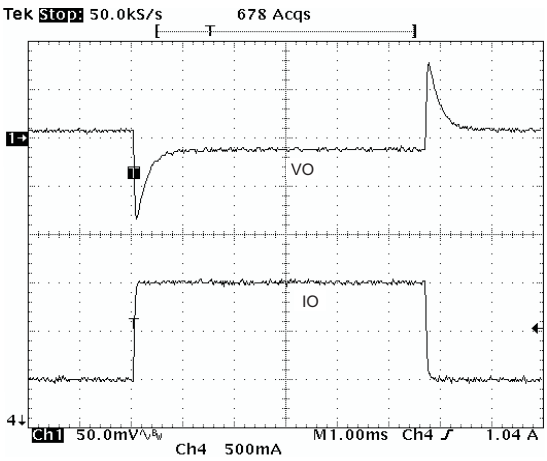



**Figure 52. Load Transmit**

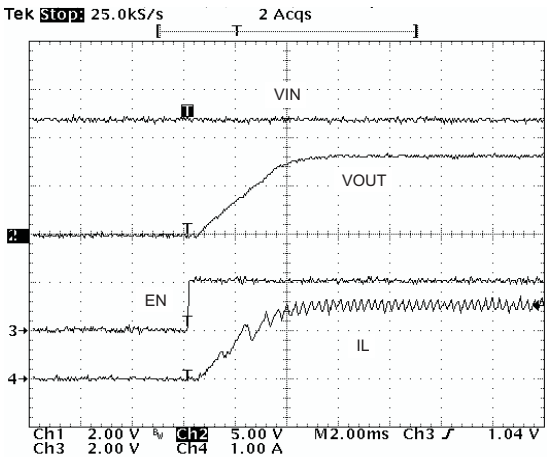



**Figure 53. Startup With EN**

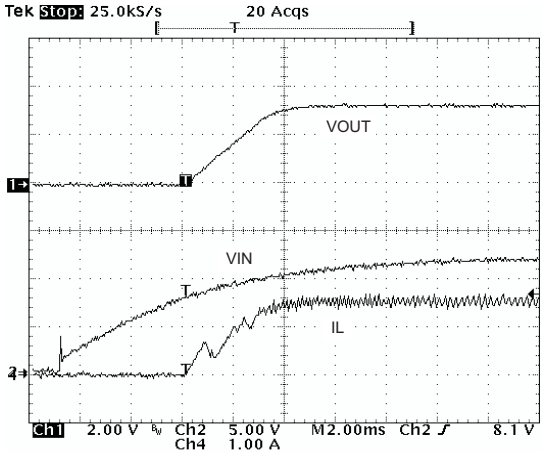



**Figure 54. VIN Power Up**

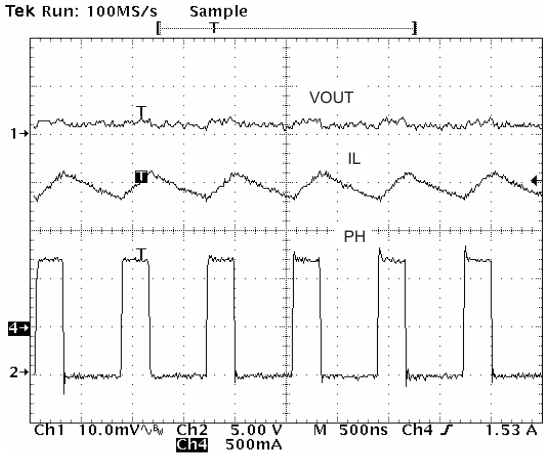



**Figure 55. Output Ripple, CCM**

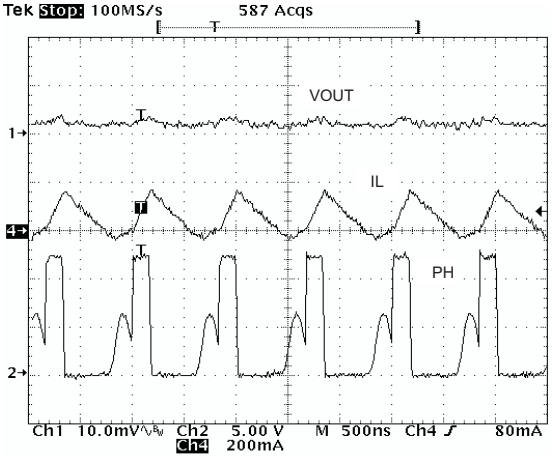



**Figure 56. Output Ripple, DCM**

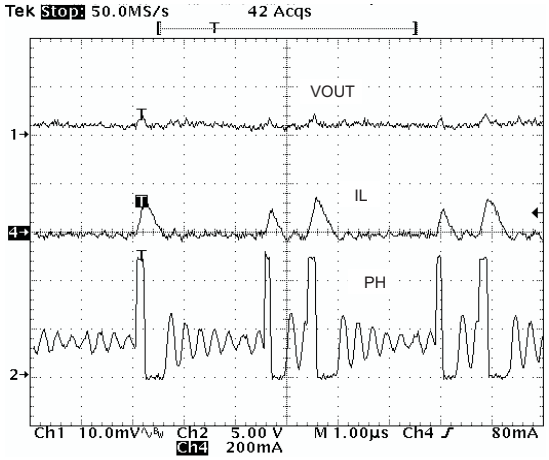



**Figure 57. Output Ripple, PSM**

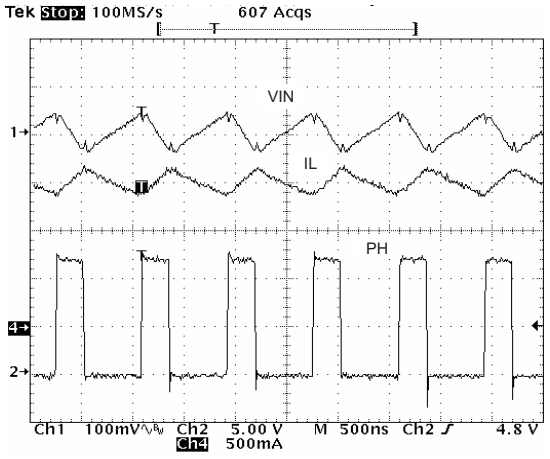



**Figure 58. Input Ripple, CCM**

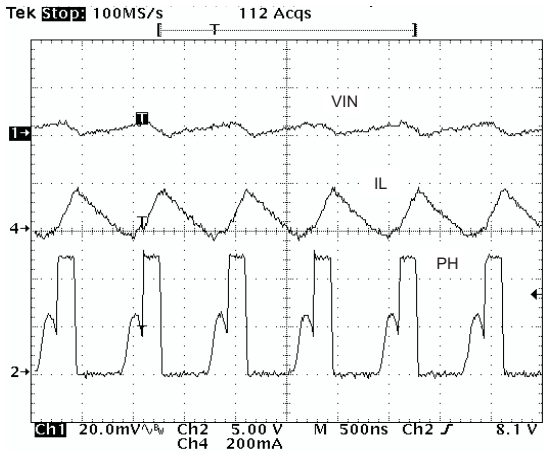



**Figure 59. Input Ripple, DCM**

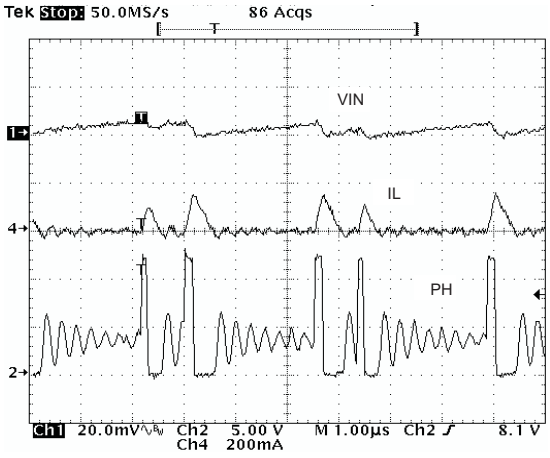



**Figure 60. Input Ripple, PSM**

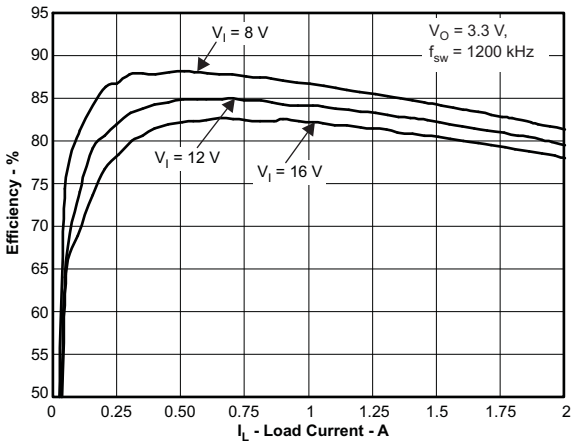



**Figure 61. Efficiency versus Load Current**

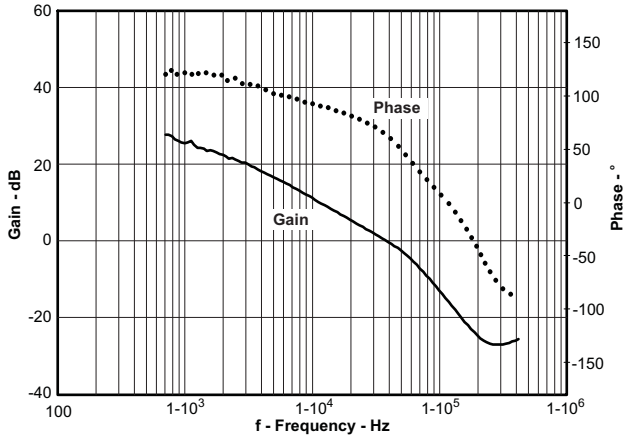



**Figure 62. Overall Loop Frequency Response**

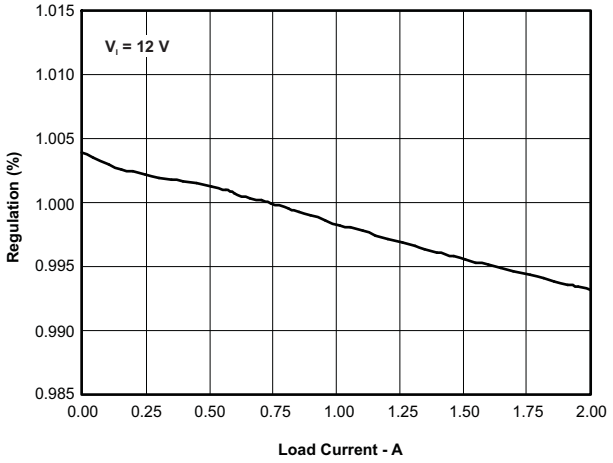



**Figure 63. Regulation versus Load Current**

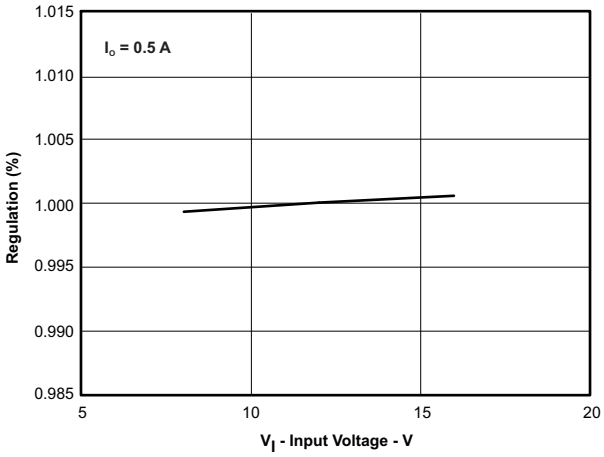



**Figure 64. Regulation versus Input Voltage**

## Power-Dissipation Estimate

The following formulas show how to estimate the IC power dissipation under continuous-conduction-mode (CCM) operation. Do not use these equations used if the device is working in discontinuous-conduction mode (DCM).

The power dissipation of the IC includes conduction loss (Pcon), switching loss (Psw), gate-drive loss (Pgd), and supply current (Pq).

$$Pcon = Io^2 \times R_{DS(on)} \times \frac{Vout}{Vin} \quad (54)$$

$$P_{SW} = V_{IN}^2 \times f_{SW} \times I_O \times 0.25\times10^{-9}\text{sec/V} \quad (55)$$

$$P_{gd} = V_{IN} \times 3\times10^{-9}\text{Asec} \times f_{SW} \quad (56)$$

$$P_q = 116\mu A \times V_{IN} \quad (57)$$

where:

IOUT is the output current (A).
Rdson is the on-resistance of the high-side MOSFET (Ω).
VOUT is the output voltage (V).
VIN is the input voltage (V).
fsw is the switching frequency (Hz).

So

$$Ptot = Pcon + Psw + Pgd + Pq \quad (58)$$

For a given $T_A$,

$$TJ = TA + Rth \times Ptot \quad (59)$$

For a given $T_{JMAX}$ = 150°C

$$TAmax = TJmax - Rth \times Ptot \quad (60)$$

where:

Ptot is the total device power dissipation (W).
$T_A$ is the ambient temperature (°C).
$T_J$ is the junction temperature (°C).
Rth is the thermal resistance of the package (°C/W).
$T_{JMAX}$ is maximum junction temperature (°C).
$T_{AMAX}$ is maximum ambient temperature (°C).

There are additional power losses in the regulator circuit, due to the inductor ac and dc losses, the catch diode, and trace resistance, that impact the overall efficiency of the regulator.

## Layout

Layout is a critical portion of good power-supply design. There are several signals paths that conduct quickly changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power-supply performance. To reduce these problems, bypass the VIN pin to ground with a low-ESR ceramic bypass capacitor with X5R or X7R dielectric. Take care to minimize the loop area formed by the bypass capacitor connections, the VIN pin, and the anode of the catch diode. See Figure 65 for a PCB layout example. Tie the GND pin directly to the thermal pad under the IC and the exposed thermal pad.

Connect the thermal pad to any internal PCB ground planes using multiple vias directly under the IC. Route the PH pin to the cathode of the catch diode and to the output inductor. Because the PH connection is the switching node, locate the catch diode and output inductor very close to the PH pins, and minimize the area of the PCB conductor to prevent excessive capacitive coupling. For operation at full-rated load, the top-side ground area must provide adequate heat dissipating area. The RT/CLK pin is sensitive to noise, so locate the RT resistor as close as possible to the IC and route the traces to minimize their lengths. Place the additional external components approximately as shown. It may be possible to obtain acceptable performance with alternate PCB layouts; however, this layout produces good results and can serve as a guideline.

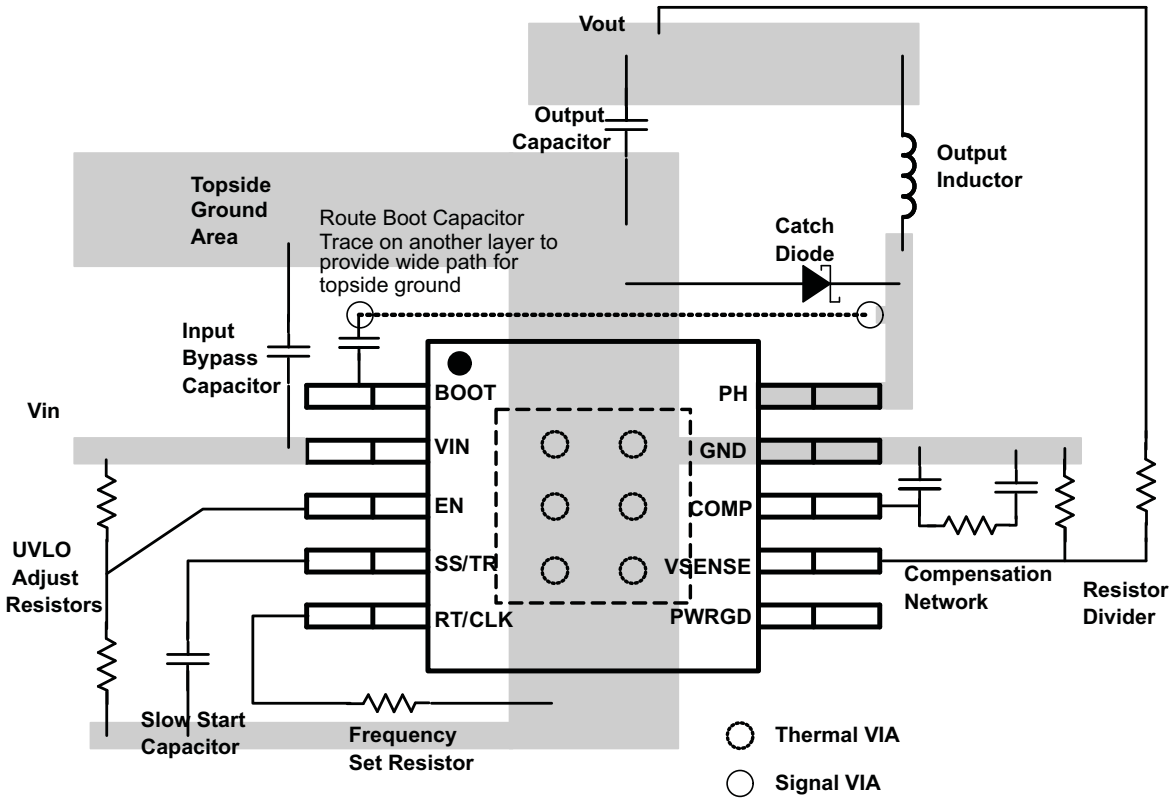



**Figure 65. PCB Layout Example**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS57140QDGQRQ1 | ACTIVE | MSOP-PowerPAD | DGQ | 10 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | 5714Q | Samples |
| TPS57140QDRCRQ1 | ACTIVE | SON | DRC | 10 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 125 | 5714Q | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

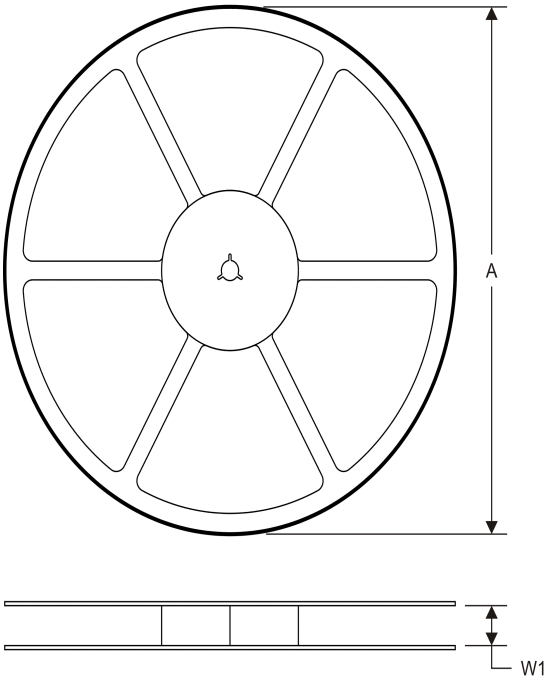
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

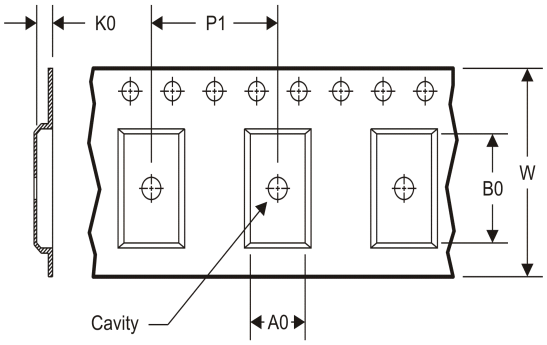
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**




**TAPE DIMENSIONS**



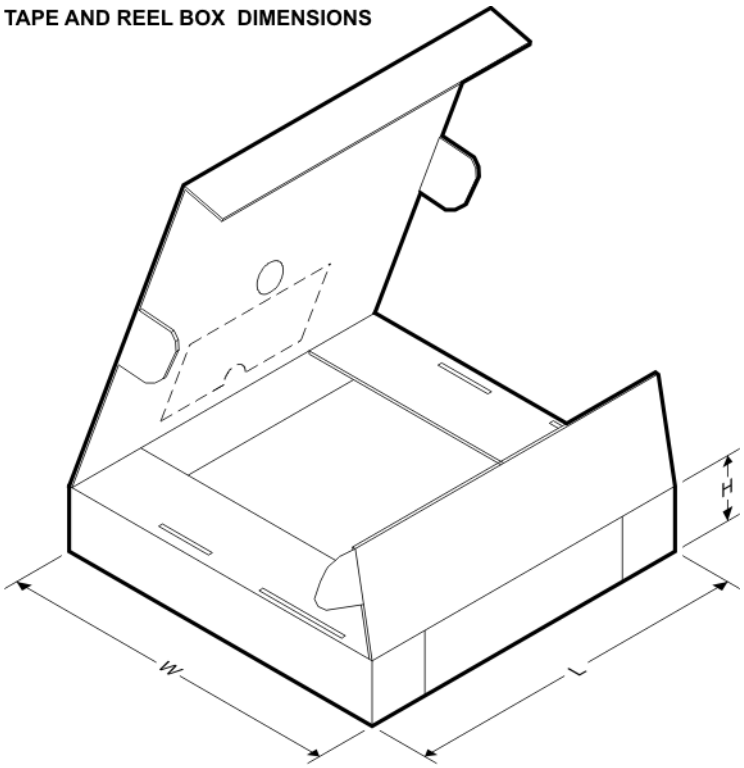

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**TAPE AND REEL INFORMATION**

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS57140QDGQRQ1 | MSOP-Power PAD | DGQ | 10 | 2500 | 330.0 | 12.4 | 5.3 | 3.3 | 1.3 | 8.0 | 12.0 | Q1 |
| TPS57140QDRCRQ1 | SON | DRC | 10 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.0 | 8.0 | 12.0 | Q2 |

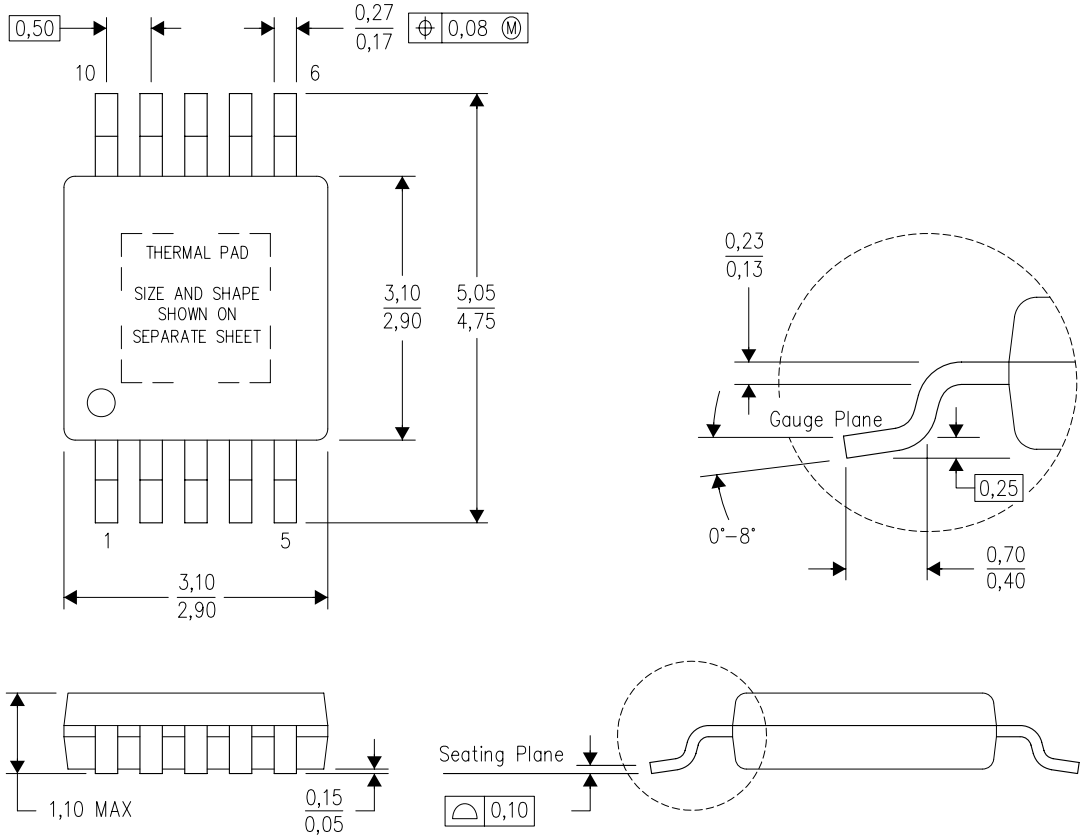
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS57140QDGQRQ1 | MSOP-PowerPAD | DGQ | 10 | 2500 | 370.0 | 355.0 | 55.0 |
| TPS57140QDRCRQ1 | SON | DRC | 10 | 3000 | 370.0 | 355.0 | 55.0 |

DGQ (S–PDSO–G10) PowerPAD™ PLASTIC SMALL OUTLINE




4073273/F 11/11

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–187 variation BA–T.

**PowerPAD is a trademark of Texas Instruments.**

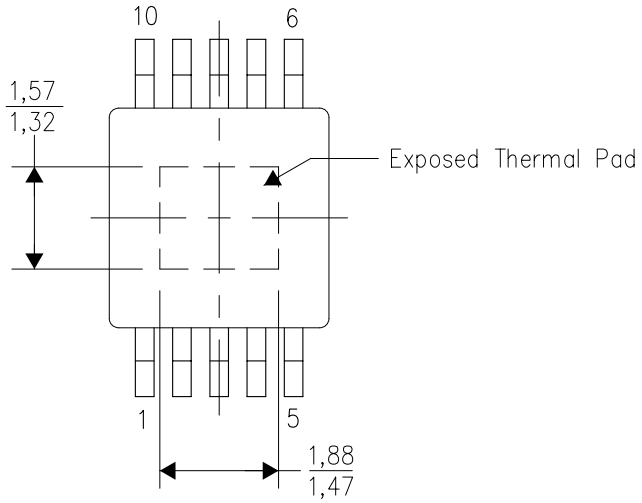
DGQ (S–PDSO–G10) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.




Top View

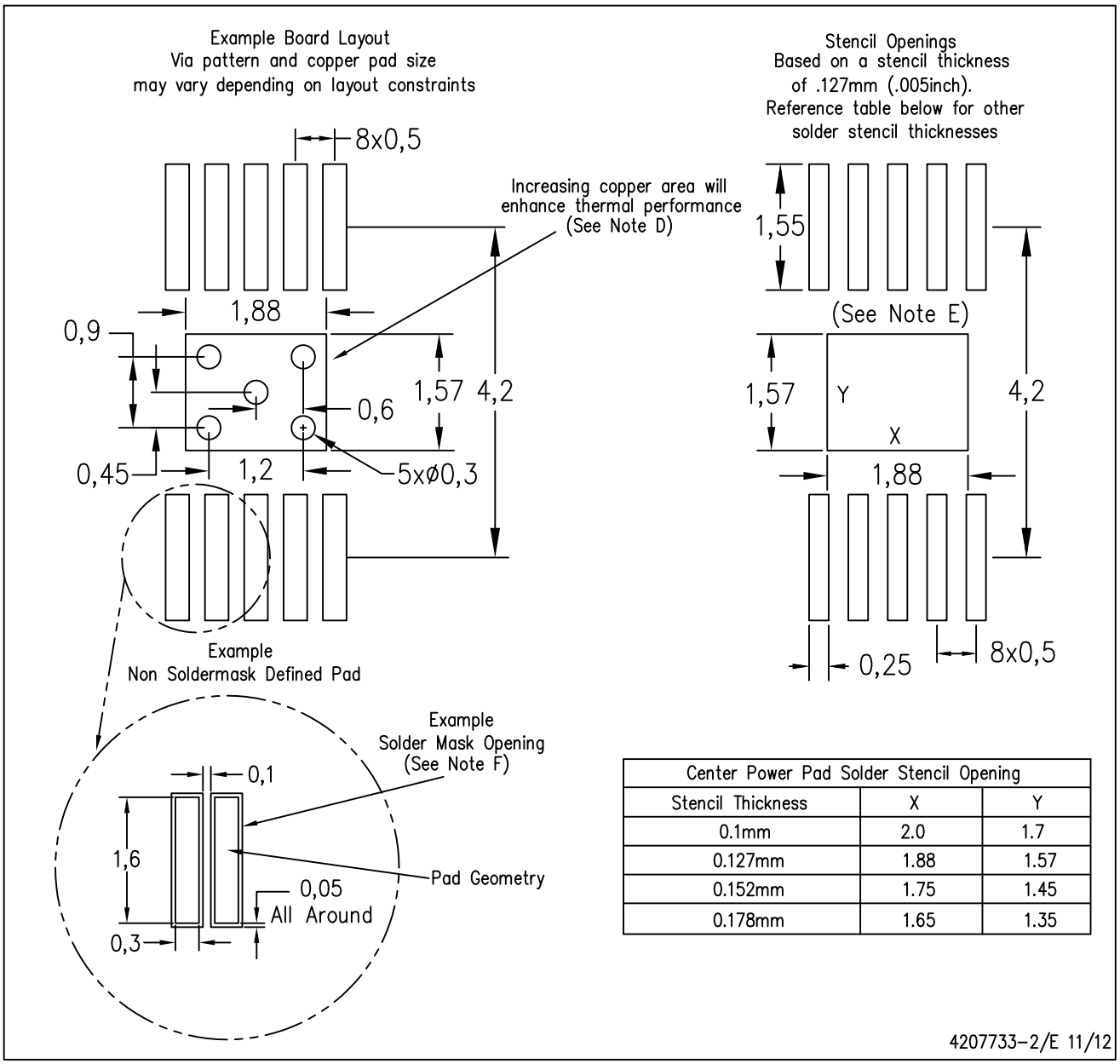
Exposed Thermal Pad Dimensions

4206324–2/F 01/11

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

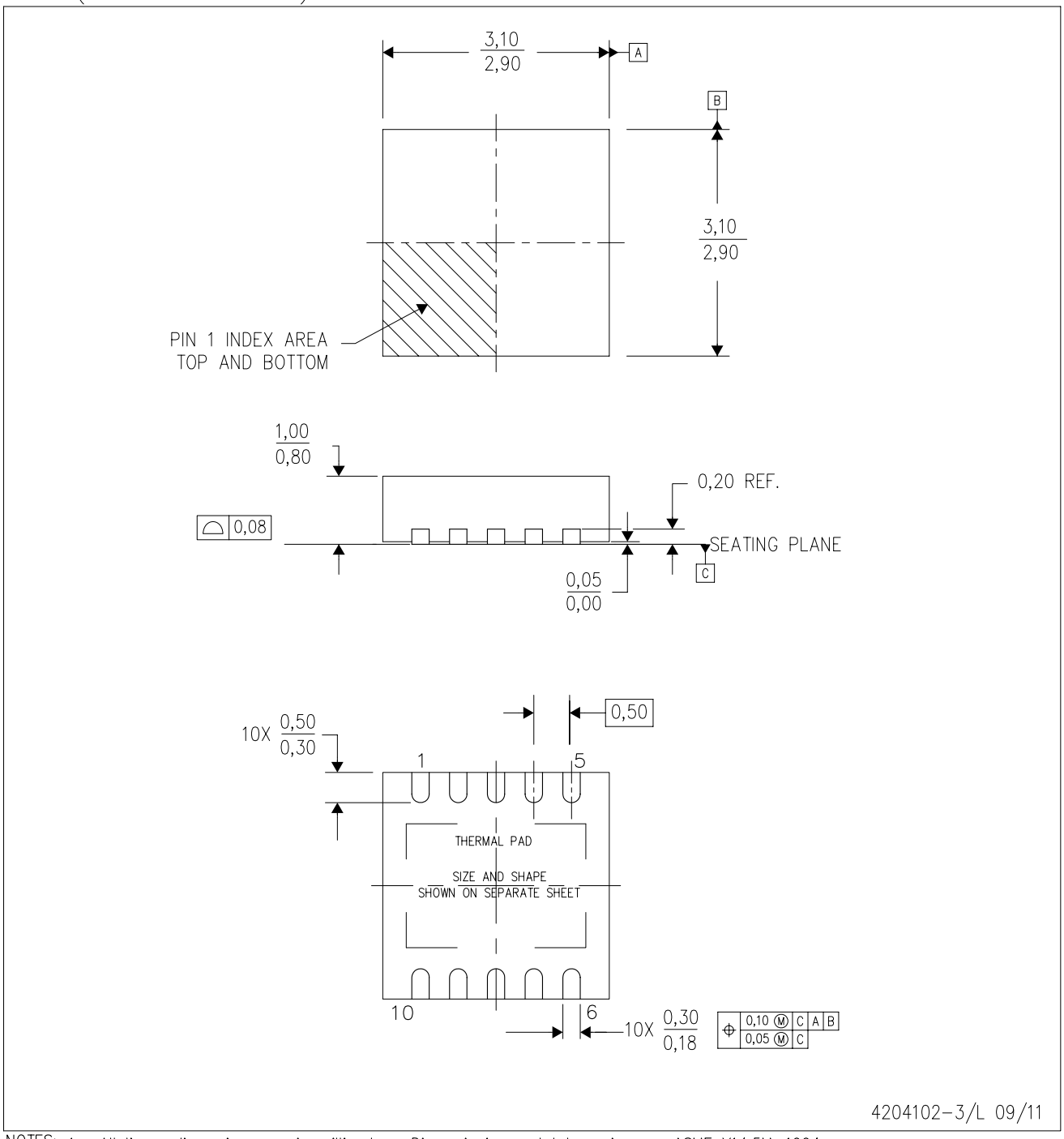
DGQ (S–PDSO–G10) PowerPAD™ PLASTIC SMALL OUTLINE




| Center Power Pad Solder Stencil Opening | | |
|---|---|---|
| Stencil Thickness | X | Y |
| 0.1mm | 2.0 | 1.7 |
| 0.127mm | 1.88 | 1.57 |
| 0.152mm | 1.75 | 1.45 |
| 0.178mm | 1.65 | 1.35 |

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance, if present.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions, if present

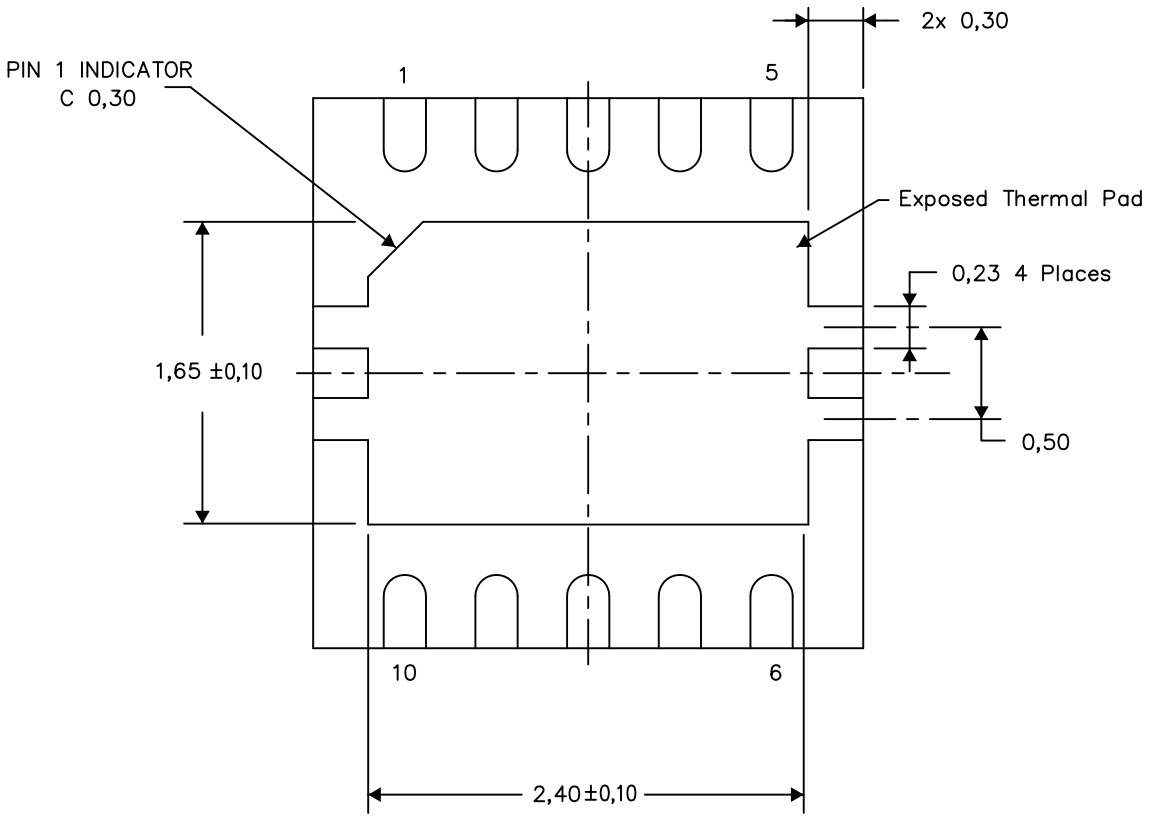
DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



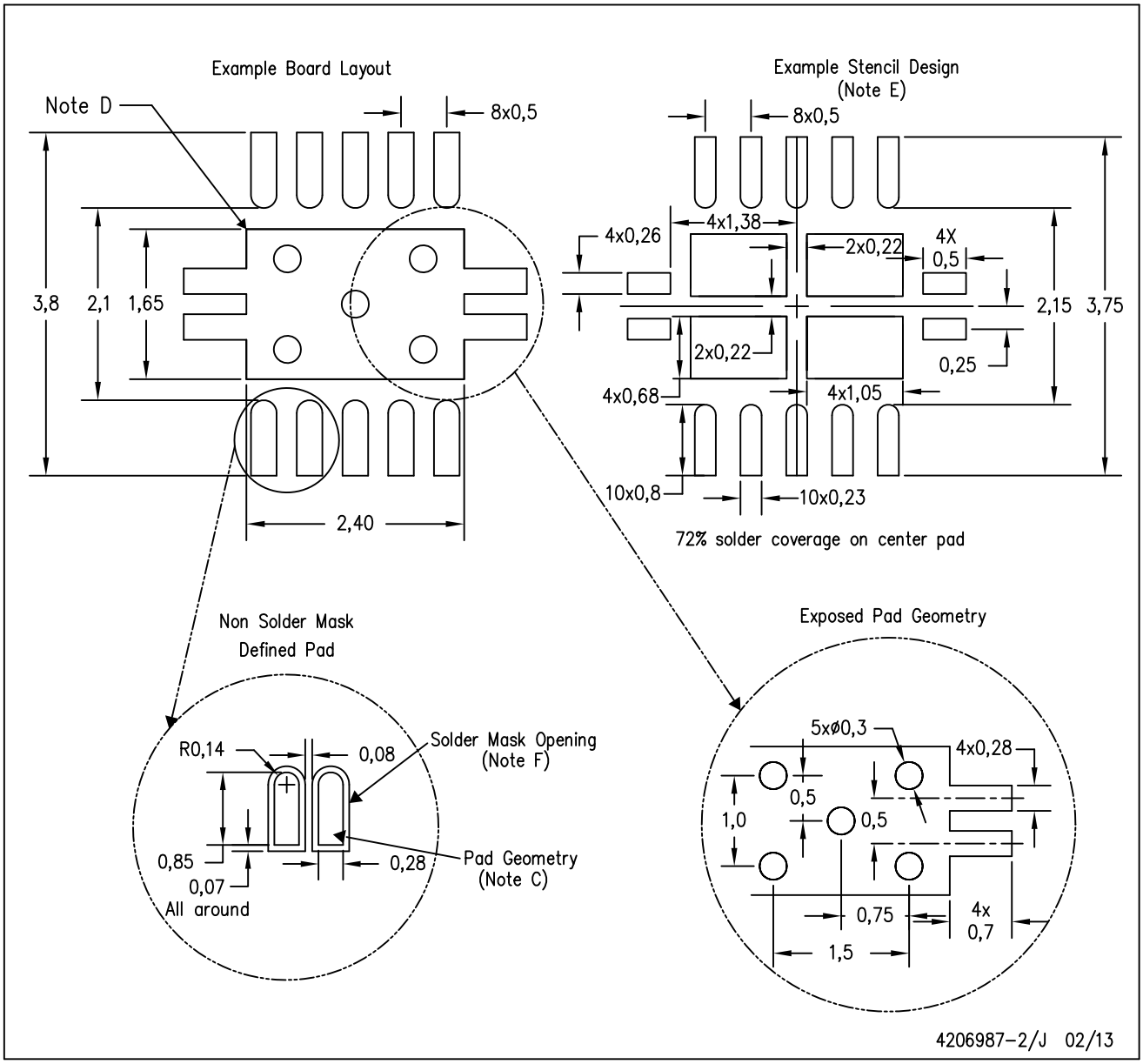

Bottom View

Exposed Thermal Pad Dimensions

4206565–3/R 03/13

NOTE: A. All linear dimensions are in millimeters

DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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