



## 2.95-V to 14.5-V Input, 6-A Synchronous Buck, Integrated Power Solution

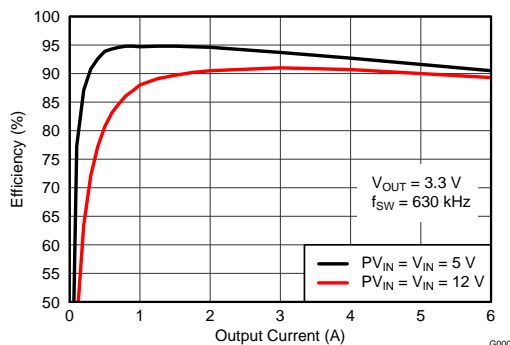
 Check for Samples: [TPS84621](#)

### FEATURES

- Complete Integrated Power Solution Allows Small Footprint, Low-Profile Design
- Efficiencies Up To 96%
- Wide-Output Voltage Adjust 0.6 V to 5.5 V, with 1% Reference Accuracy
- Supports Parallel Operation for Higher Current
- Optional Split Power Rail allows input voltage down to 1.6 V
- Adjustable Switching Frequency (250 kHz to 780 kHz)
- Synchronizes to an External Clock
- Adjustable Slow-Start
- Output Voltage Sequencing / Tracking
- Power Good Output
- Programmable Undervoltage Lockout (UVLO)
- Output Overcurrent Protection (Hiccup Mode)
- Over-Temperature Protection
- Pre-bias Output Start-up
- Operating Temperature Range:  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$
- Enhanced Thermal Performance:  $13^{\circ}\text{C/W}$
- Meets EN55022 Class B Emissions
- Design Help visit <http://www.ti.com/TPS84621>

### APPLICATIONS

- Broadband & Communications Infrastructure
- Automated Test and Medical Equipment
- Compact PCI / PCI Express / PXI Express
- DSP and FPGA Point of Load Applications
- High Density Distributed Power Systems



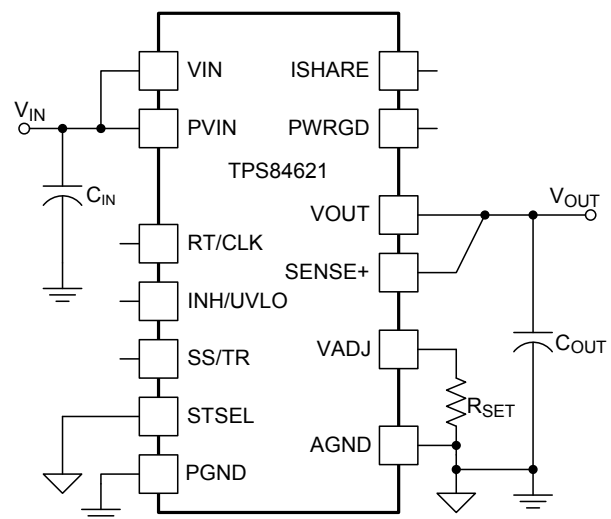
### DESCRIPTION

The TPS84621 is an easy-to-use integrated power solution that combines a 6-A DC/DC converter with power MOSFETs, an inductor, and passives into a low profile, BQFN package. This total power solution allows as few as 3 external components and eliminates the loop compensation and magnetics part selection process.

The  $9 \times 15 \times 2.8\text{ mm}$  BQFN package is easy to solder onto a printed circuit board and allows a compact point-of-load design with greater than 90% efficiency and excellent power dissipation with a thermal impedance of  $13^{\circ}\text{C/W}$  junction to ambient. The device delivers the full 6-A rated output current at  $85^{\circ}\text{C}$  ambient temperature without airflow.

The TPS84621 offers the flexibility and the feature-set of a discrete point-of-load design and is ideal for powering performance DSPs and FPGAs. Advanced packaging technology afford a robust and reliable power solution compatible with standard QFN mounting and testing techniques.

### SIMPLIFIED APPLICATION



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this datasheet, or see the TI website at [www.ti.com](http://www.ti.com).

### ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

over operating temperature range (unless otherwise noted)		VALUE		UNIT
		MIN	MAX	
Input Voltage	VIN, PVIN, INH/UVLO	-0.3	16	V
	PWRGD, RT/CLK	-0.3	6	V
	VADJ, SS/TR, STSEL, ISHARE	-0.3	3	V
Output Voltage	PH	-1	20	V
	PH 10ns Transient	-3	20	V
V <sub>DIF</sub> (GND to exposed thermal pad)		-0.2	0.2	V
Source Current	RT/CLK	-100	+100	μA
	PH		Current Limit	A
Sink Current	PH		Current Limit	A
	PVIN		Current Limit	A
	PWRGD	-0.1	5	mA
Operating Junction Temperature		-40	125 <sup>(2)</sup>	°C
Storage Temperature		-65	150	°C
Mechanical Shock	Mil-STD-883D, Method 2002.3, 1 msec, 1/2 sine, mounted		1500	G
Mechanical Vibration	Mil-STD-883D, Method 2007.2, 20-2000Hz		20	

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) See the temperature derating curves in the Typical Characteristics section for thermal information.

## THERMAL INFORMATION

THERMAL METRIC <sup>(1)</sup>		TPS84621	UNIT
		RUQ47	
		47 PINS	
$\theta_{JA}$	Junction-to-ambient thermal resistance <sup>(2)</sup>	13	°C/W
$\theta_{JCTop}$	Junction-to-case (top) thermal resistance <sup>(3)</sup>	9	
$\theta_{JCbot}$	Junction-to-case (bottom) thermal resistance <sup>(4)</sup>	3.8	
$\theta_{JB}$	Junction-to-board thermal resistance <sup>(5)</sup>	6	
$\psi_{JT}$	Junction-to-top characterization parameter <sup>(6)</sup>	2.5	
$\psi_{JB}$	Junction-to-board characterization parameter <sup>(7)</sup>	5	

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, [SPRA953](#).

(2) The junction-to-ambient thermal resistance,  $\theta_{JA}$ , applies to devices soldered directly to a 100 mm x 100 mm double-sided PCB with 1 oz. copper and natural convection cooling. Additional airflow reduces  $\theta_{JA}$ .

(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

(4) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

(5) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.

(6) The junction-to-top characterization parameter,  $\psi_{JT}$ , estimates the junction temperature,  $T_J$ , of a device in a real system, using a procedure described in JESD51-2A (sections 6 and 7).  $T_J = \psi_{JT} * P_{dis} + T_T$ ; where  $P_{dis}$  is the power dissipated in the device and  $T_T$  is the temperature of the top of the device.

(7) The junction-to-board characterization parameter,  $\psi_{JB}$ , estimates the junction temperature,  $T_J$ , of a device in a real system, using a procedure described in JESD51-2A (sections 6 and 7).  $T_J = \psi_{JB} * P_{dis} + T_B$ ; where  $P_{dis}$  is the power dissipated in the device and  $T_B$  is the temperature of the board 1mm from the device.

## PACKAGE SPECIFICATIONS

TPS84621		UNIT
Weight		1.26 grams
Flammability	Meets UL 94 V-O	
MTBF Calculated reliability	Per Bellcore TR-332, 50% stress, $T_A = 40^\circ\text{C}$ , ground benign	33.9 Mhrs

### ELECTRICAL CHARACTERISTICS

Over  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  free-air temperature,  $\text{PVIN} = \text{VIN} = 12\text{ V}$ ,  $\text{V}_{\text{OUT}} = 1.8\text{ V}$ ,  $\text{I}_{\text{OUT}} = 6\text{ A}$ ,  
 $\text{C}_{\text{IN}1} = 2 \times 22\ \mu\text{F}$  ceramic,  $\text{C}_{\text{IN}2} = 68\ \mu\text{F}$  poly-tantalum,  $\text{C}_{\text{OUT}1} = 4 \times 47\ \mu\text{F}$  ceramic (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	
$\text{I}_{\text{OUT}}$	Output current	$\text{T}_A = 85^{\circ}\text{C}$ , natural convection		0		6	A	
VIN	Input bias voltage range	Over $\text{I}_{\text{OUT}}$ range		4.5		14.5	V	
PVIN	Input switching voltage range	Over $\text{I}_{\text{OUT}}$ range		1.6 <sup>(1)</sup>		14.5 <sup>(2)</sup>	V	
UVLO	VIN Undervoltage lockout	VIN = increasing			4.0	4.5	V	
		VIN = decreasing		3.5	3.85			
$\text{V}_{\text{OUT(adj)}}$	Output voltage adjust range	Over $\text{I}_{\text{OUT}}$ range		0.6 <sup>(2)</sup>		5.5	V	
$\text{V}_{\text{OUT}}$	Set-point voltage tolerance	$\text{T}_A = 25^{\circ}\text{C}$ , $\text{I}_{\text{OUT}} = 0\text{ A}$				$\pm 1.0\%$ <sup>(3)</sup>		
	Temperature variation	$-40^{\circ}\text{C} \leq \text{T}_A \leq +85^{\circ}\text{C}$ , $\text{I}_{\text{OUT}} = 0\text{ A}$			$\pm 0.3\%$			
	Line regulation	Over PVIN range, $\text{T}_A = 25^{\circ}\text{C}$ , $\text{I}_{\text{OUT}} = 0\text{ A}$			$\pm 0.1\%$			
	Load regulation	Over $\text{I}_{\text{OUT}}$ range, $\text{T}_A = 25^{\circ}\text{C}$			$\pm 0.1\%$			
	Total output voltage variation	Includes set-point, line, load, and temperature variation				$\pm 1.5\%$ <sup>(3)</sup>		
$\eta$	Efficiency	PVIN = VIN = 12 V $\text{I}_O = 2\text{ A}$	$\text{V}_{\text{OUT}} = 5\text{ V}$ , $\text{f}_{\text{SW}} = 780\text{ kHz}$		92 %			
			$\text{V}_{\text{OUT}} = 3.3\text{ V}$ , $\text{f}_{\text{SW}} = 630\text{ kHz}$		91 %			
			$\text{V}_{\text{OUT}} = 2.5\text{ V}$ , $\text{f}_{\text{SW}} = 530\text{ kHz}$		89 %			
			$\text{V}_{\text{OUT}} = 1.8\text{ V}$ , $\text{f}_{\text{SW}} = 480\text{ kHz}$		88 %			
			$\text{V}_{\text{OUT}} = 1.2\text{ V}$ , $\text{f}_{\text{SW}} = 480\text{ kHz}$		85 %			
		PVIN = VIN = 5 V $\text{I}_O = 2\text{ A}$	$\text{V}_{\text{OUT}} = 3.3\text{ V}$ , $\text{f}_{\text{SW}} = 630\text{ kHz}$		95 %			
			$\text{V}_{\text{OUT}} = 2.5\text{ V}$ , $\text{f}_{\text{SW}} = 530\text{ kHz}$		93 %			
			$\text{V}_{\text{OUT}} = 1.8\text{ V}$ , $\text{f}_{\text{SW}} = 480\text{ kHz}$		91 %			
			$\text{V}_{\text{OUT}} = 1.2\text{ V}$ , $\text{f}_{\text{SW}} = 480\text{ kHz}$		89 %			
			$\text{V}_{\text{OUT}} = 0.8\text{ V}$ , $\text{f}_{\text{SW}} = 480\text{ kHz}$		85 %			
		$\text{V}_{\text{OUT}} = 0.6\text{ V}$ , $\text{f}_{\text{SW}} = 250\text{ kHz}$		83 %				
	Output voltage ripple	20 MHz bandwidth			30		mV <sub>PP</sub>	
$\text{I}_{\text{LIM}}$	Overcurrent threshold				11		A	
	Transient response	1.0 A/ $\mu\text{s}$ load step from 50 to 100% $\text{I}_{\text{OUT(max)}}$	Recovery time		80		$\mu\text{s}$	
			$\text{V}_{\text{OUT}}$ over/undershoot		60		mV	
$\text{V}_{\text{INH-H}}$	Inhibit Control	Inhibit High Voltage		1.30		Open <sup>(4)</sup>	V	
$\text{V}_{\text{INH-L}}$		Inhibit Low Voltage		-0.3		1.05		
	INH Input current	$\text{INH} < 1.1\text{ V}$			-1.15		$\mu\text{A}$	
	INH Hysteresis current	$\text{INH} > 1.26\text{ V}$			-3.4		$\mu\text{A}$	
$\text{I}_{\text{I(stby)}}$	Input standby current	INH pin to AGND			2	4	$\mu\text{A}$	
Power Good	PWRGD Thresholds	$\text{V}_{\text{OUT}}$ rising	Good		94%			
			Fault		109%			
		$\text{V}_{\text{OUT}}$ falling	Fault		91%			
			Good		106%			
	PWRGD Low Voltage	$\text{I(PWRGD)} = 2\text{ mA}$			0.3		V	
$\text{f}_{\text{SW}}$	Switching frequency	Over VIN and $\text{I}_{\text{OUT}}$ ranges, RT/CLK pin OPEN		200	250	300	kHz	
$\text{f}_{\text{CLK}}$	Synchronization frequency	CLK Control			250	780	kHz	
$\text{V}_{\text{CLK-H}}$	CLK High-Level				2.0	5.5	V	
$\text{V}_{\text{CLK-L}}$	CLK Low-Level					0.8	V	
$\text{D}_{\text{CLK}}$	CLK Duty cycle				20%	80%		
	Thermal Shutdown			Thermal shutdown		160	175	
		Thermal shutdown hysteresis			10		$^{\circ}\text{C}$	

- (1) The minimum PVIN voltage is 1.6V or ( $\text{V}_{\text{OUT}} + 0.9\text{ V}$ ), whichever is greater. VIN must be greater than 4.5V.
- (2) The maximum PVIN voltage is 14.5V or ( $15 \times \text{V}_{\text{OUT}}$ ), whichever is less.
- (3) The stated limit of the set-point voltage tolerance includes the tolerance of both the internal voltage reference and the internal adjustment resistor. The overall output voltage tolerance will be affected by the tolerance of the external  $\text{R}_{\text{SET}}$  resistor.
- (4) This control pin has an internal pullup. If this pin is left open circuit, the device operates when input power is applied. A small low-leakage MOSFET is recommended for control. See the application section for further guidance.

**ELECTRICAL CHARACTERISTICS (continued)**

Over  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  free-air temperature,  $\text{PVIN} = \text{VIN} = 12\text{ V}$ ,  $\text{V}_{\text{OUT}} = 1.8\text{ V}$ ,  $\text{I}_{\text{OUT}} = 6\text{ A}$ ,

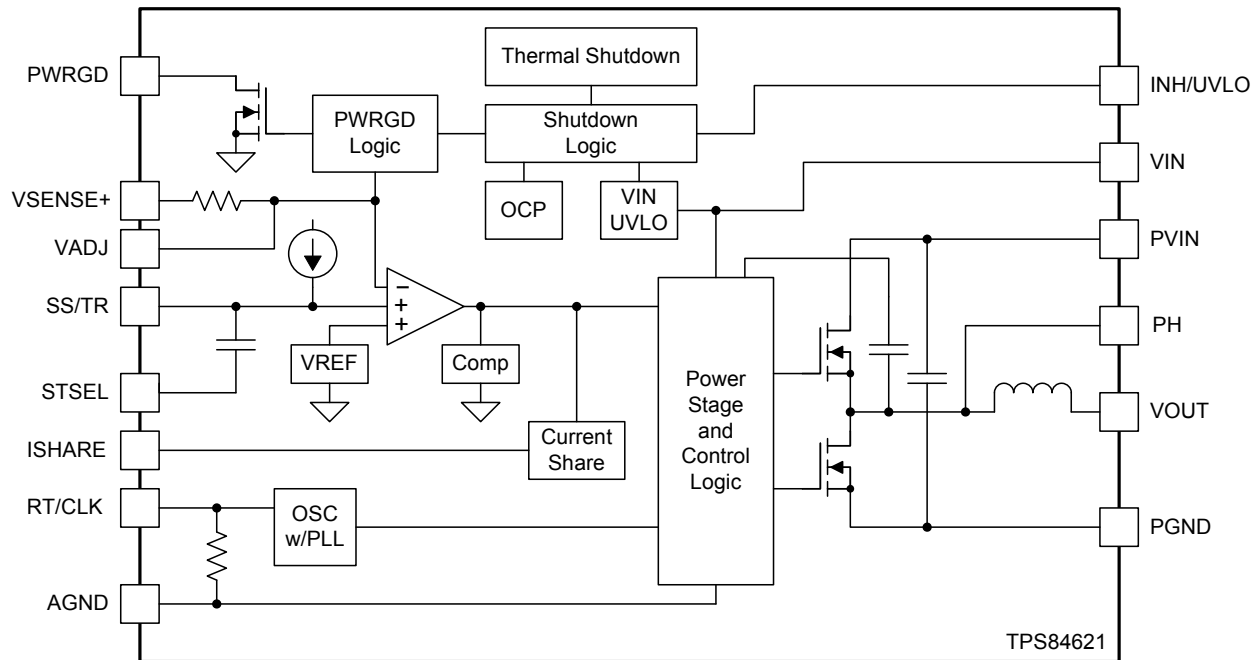
$\text{C}_{\text{IN}1} = 2 \times 22\text{ }\mu\text{F}$  ceramic,  $\text{C}_{\text{IN}2} = 68\text{ }\mu\text{F}$  poly-tantalum,  $\text{C}_{\text{OUT}1} = 4 \times 47\text{ }\mu\text{F}$  ceramic (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\text{C}_{\text{IN}}$ External input capacitance	Ceramic	44 <sup>(5)</sup>			$\mu\text{F}$
	Non-ceramic	68 <sup>(5)</sup>			
$\text{C}_{\text{OUT}}$ External output capacitance	Ceramic	47 <sup>(6)</sup>	200	1500	$\mu\text{F}$
	Non-ceramic		220 <sup>(6)</sup>	5000	
	Equivalent series resistance (ESR)				35

- (5) A minimum of  $100\mu\text{F}$  of polymer tantalum and/or ceramic external capacitance is required across the input ( $\text{VIN}$  and  $\text{PVIN}$  connected) for proper operation. Locate the capacitor close to the device. See Table 4 for more details. When operating with split  $\text{VIN}$  and  $\text{PVIN}$  rails, place  $4.7\mu\text{F}$  of ceramic capacitance directly at the  $\text{VIN}$  pin.
- (6) The amount of required output capacitance varies depending on the output voltage (see Table 3). The amount of required capacitance must include at least  $1 \times 47\mu\text{F}$  ceramic capacitor. Locate the capacitance close to the device. Adding additional capacitance close to the load improves the response of the regulator to load transients. See Table 3 and Table 4 more details.

**DEVICE INFORMATION**

**FUNCTIONAL BLOCK DIAGRAM**



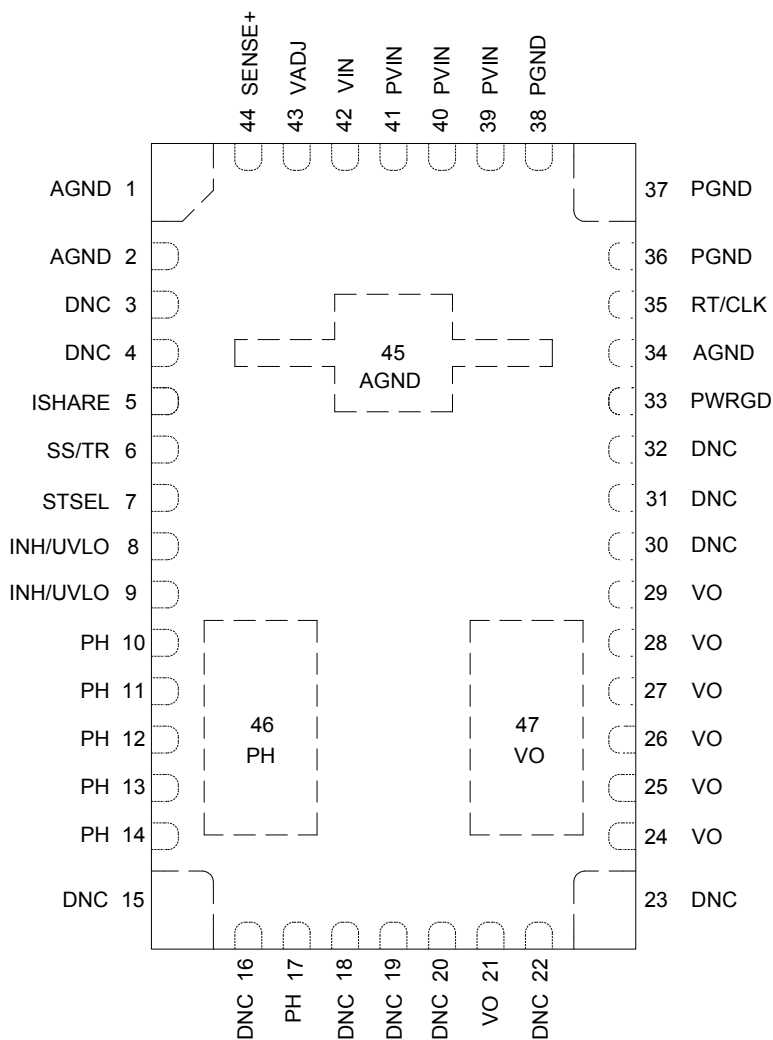
### PIN DESCRIPTIONS

TERMINAL		DESCRIPTION
NAME	NO.	
AGND	1	Zero VDC reference for the analog control circuitry. Connect AGND to PGND at a single point. Connect near the output capacitors. See <a href="#">Figure 43</a> for a recommended layout.
	2	
	34	
	45	
INH/UVLO	8	Inhibit and UVLO adjust pin. Use an open drain or open collector output logic to control the INH function. A resistor divider between this pin, AGND and VIN adjusts the UVLO voltage. Tie both pins together when using this control.
	9	
ISHARE	5	Current share pin. Connect this pin to other TPS84621 device's ISHARE pin when paralleling multiple TPS84621 devices. When unused, treat this pin as a Do Not Connect (DNC) and leave it isolated from all other signals or ground.
DNC	3	Do Not Connect. Do not connect these pins to AGND, to another DNC pin, or to any other voltage. These pins are connected to internal circuitry. Each pin must be soldered to an isolated pad.
	4	
	15	
	16	
	18	
	19	
	20	
	22	
	23	
	30	
	31	
	32	
PGND	36	Common ground connection for the PVIN, VIN, and VOUT power connections. See <a href="#">Figure 43</a> for a recommended layout.
	37	
	38	
PH	10	Phase switch node. These pins should be connected to a small copper island under the device for thermal relief. Do not connect any external component to this pin or tie it to a pin of another function.
	11	
	12	
	13	
	14	
	17	
46		
PWRGD	33	Power good fault pin. Asserts low if the output voltage is out of range. A pull-up resistor is required.
PVIN	39	Input switching voltage. This pin supplies voltage to the power switches of the converter. See <a href="#">Figure 43</a> for a recommended layout.
	40	
	41	
RT/CLK	35	This pin automatically selects between RT mode and CLK mode. A timing resistor adjusts the switching frequency of the device. In CLK mode, the device synchronizes to an external clock.
SENSE+	44	Remote sense connection. Connect this pin to VOUT at the load for improved regulation. This pin must be connected to VOUT at the load, or at the module pins.
SS/TR	6	Slow-start and tracking pin. Connecting an external capacitor to this pin adjusts the output voltage rise time. A voltage applied to this pin allows for tracking and sequencing control.
STSEL	7	Slow-start or track feature select. Connect this pin to AGND to enable the internal SS capacitor with a SS interval of approximately 1.1 ms. Leave this pin open to enable the TR feature.
VADJ	43	Connecting a resistor between this pin and AGND sets the output voltage.
VIN	42	Input bias voltage pin. Supplies the control circuitry of the power converter. See <a href="#">Figure 43</a> for a recommended layout.

**PIN DESCRIPTIONS (continued)**

TERMINAL		DESCRIPTION
NAME	NO.	
VOUT	21	Output voltage. Connect output capacitors between these pins and PGND.
	24	
	25	
	26	
	27	
	28	
	29	
	47	

**RUQ PACKAGE  
47 PIN  
TOP VIEW**



TYPICAL CHARACTERISTICS (P<sub>VIN</sub> = V<sub>IN</sub> = 12 V) (1) (2)

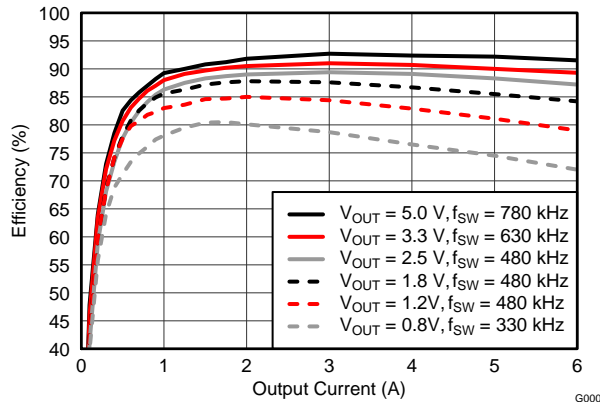


Figure 1. Efficiency vs. Output Current

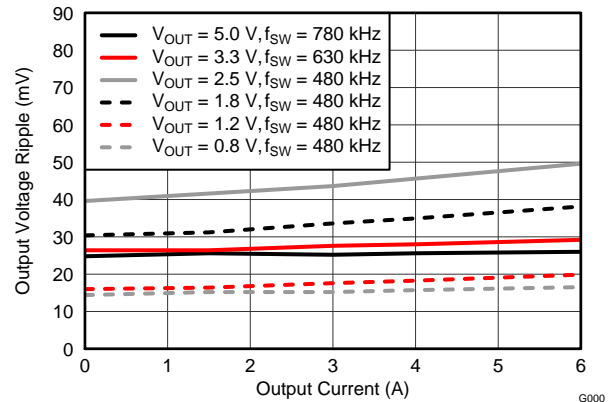


Figure 2. Voltage Ripple vs. Output Current

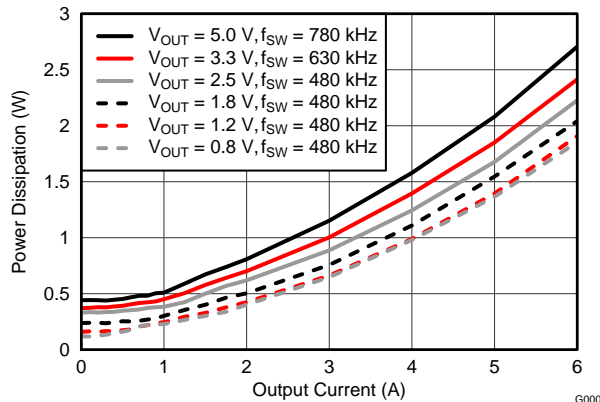


Figure 3. Power Dissipation vs. Output Current

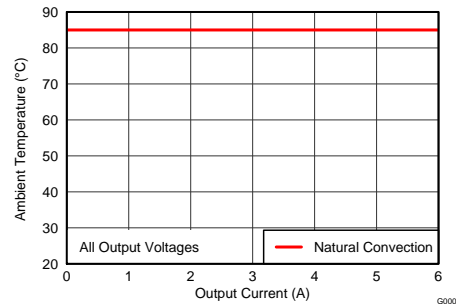


Figure 4. Safe Operating Area

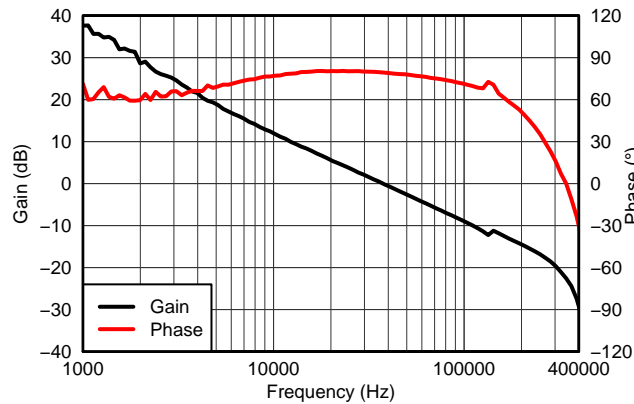


Figure 5. V<sub>OUT</sub> = 1.8 V, I<sub>OUT</sub> = 6 A, C<sub>OUT1</sub> = 200 μF ceramic, f<sub>SW</sub> = 480 kHz

- (1) The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to [Figure 1](#), [Figure 2](#), and [Figure 3](#).
- (2) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to devices soldered directly to a 100 mm × 100 mm double-sided PCB with 1 oz. copper. Applies to [Figure 4](#).



TYPICAL CHARACTERISTICS (P<sub>VIN</sub> = V<sub>IN</sub> = 5 V) <sup>(1)</sup> <sup>(2)</sup>

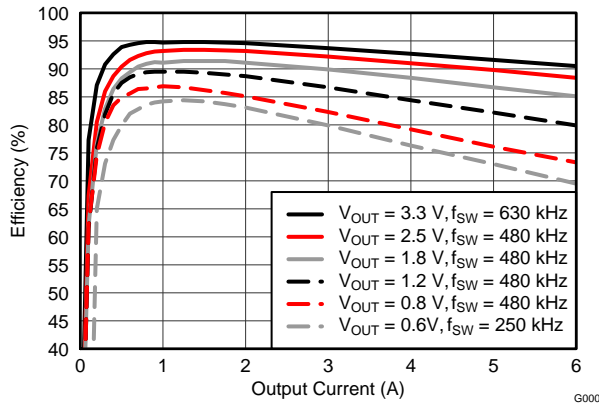


Figure 6. Efficiency vs. Output Current

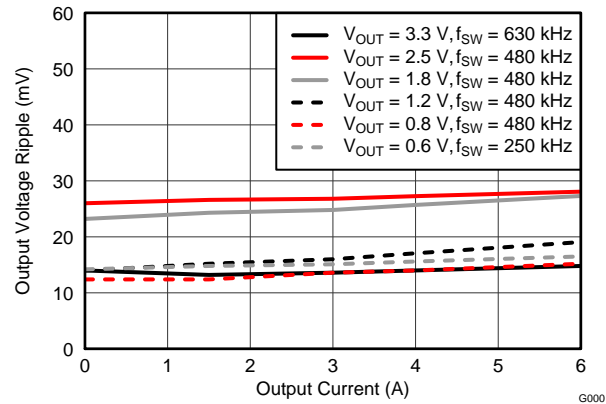


Figure 7. Voltage Ripple vs. Output Current

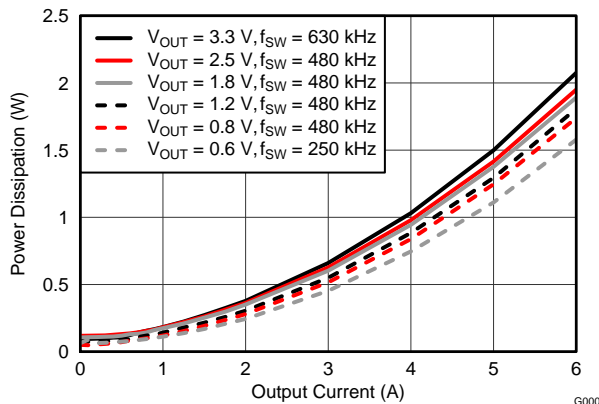


Figure 8. Power Dissipation vs. Output Current

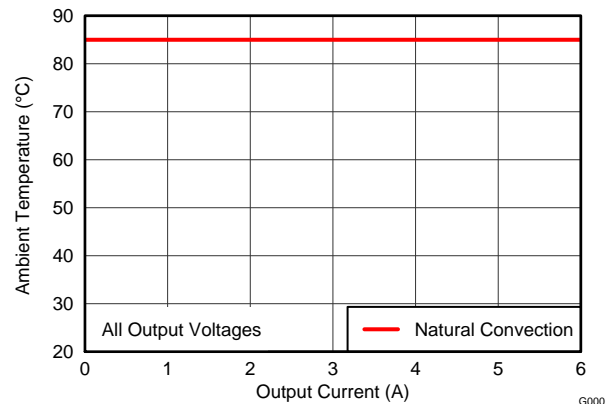


Figure 9. Safe Operating Area

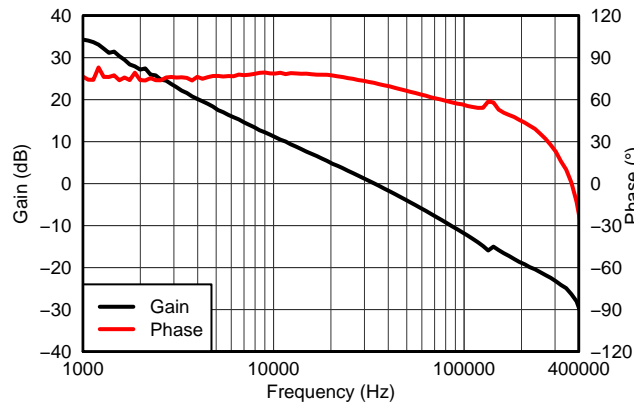


Figure 10. V<sub>OUT</sub> = 1.8 V, I<sub>OUT</sub> = 6 A, C<sub>OUT1</sub> = 200 μF ceramic, f<sub>SW</sub> = 480 kHz

- (1) The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to Figure 6, Figure 7, and Figure 8.
- (2) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to devices soldered directly to a 100 mm × 100 mm double-sided PCB with 1 oz. copper. Applies to Figure 9.

TYPICAL CHARACTERISTICS (P<sub>VIN</sub> = 12 V, V<sub>IN</sub> = 5 V) <sup>(1)</sup> <sup>(2)</sup>

- (1) The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to Figure 11, Figure 12, and Figure 13.
- (2) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to devices soldered directly to a 100 mm × 100 mm double-sided PCB with 1 oz. copper. Applies to Figure 14 and Figure 15.

TYPICAL CHARACTERISTICS (PVIN = 12 V, VIN = 5 V) (3) (4) (continued)

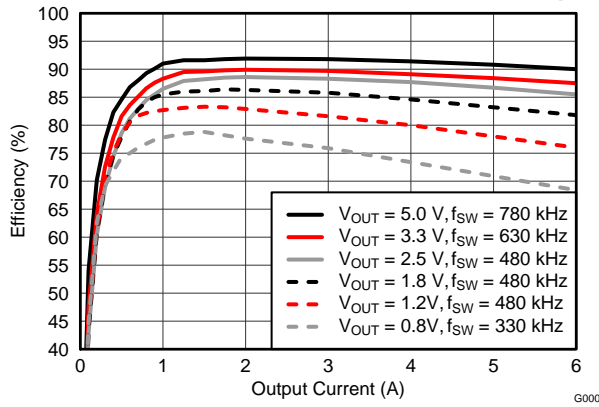


Figure 11. Efficiency vs. Output Current

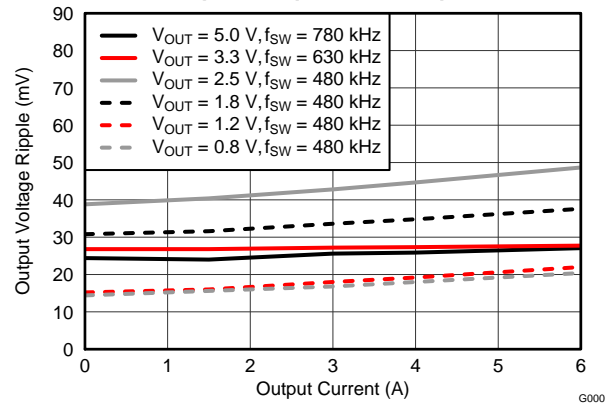


Figure 12. Voltage Ripple vs. Output Current

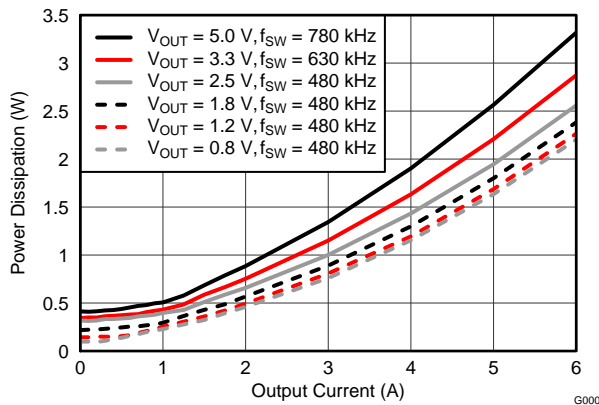


Figure 13. Power Dissipation vs. Output Current

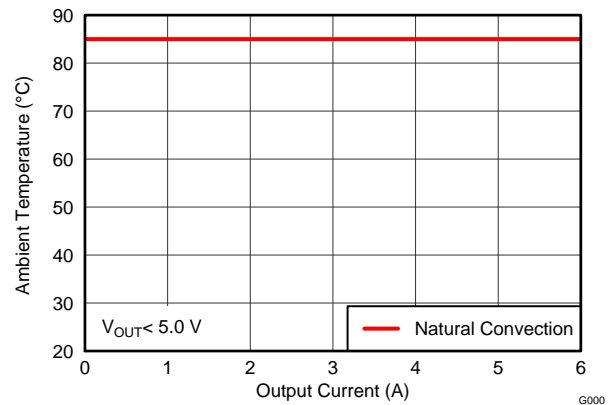


Figure 14. Safe Operating Area

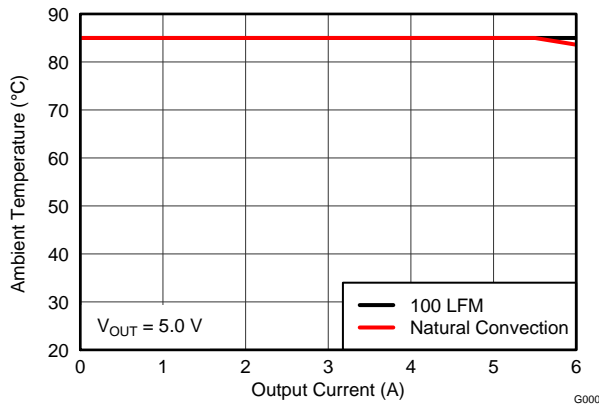


Figure 15. Safe Operating Area

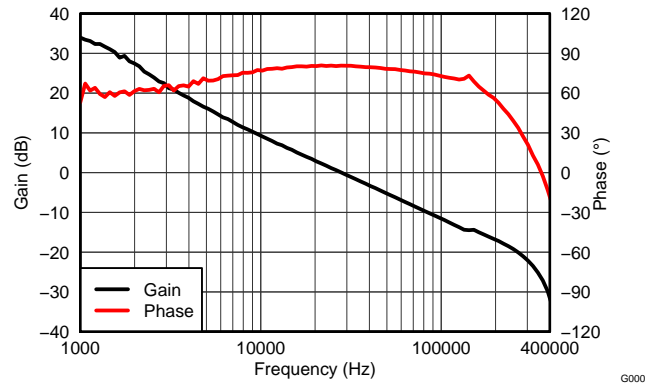


Figure 16.  $V_{OUT} = 2.5 V$ ,  $I_{OUT} = 6 A$ ,  $C_{OUT1} = 200 \mu F$  ceramic,  $f_{SW} = 480 kHz$

## APPLICATION INFORMATION

### ADJUSTING THE OUTPUT VOLTAGE

The V<sub>ADJ</sub> control sets the output voltage of the TPS84621. The output voltage adjustment range is from 0.6V to 5.5V. The adjustment method requires the addition of R<sub>SET</sub>, which sets the output voltage, the connection of SENSE+ to V<sub>OUT</sub>, and in some cases R<sub>RT</sub> which sets the switching frequency. The R<sub>SET</sub> resistor must be connected directly between the V<sub>ADJ</sub> (pin 43) and AGND (pin 45). The SENSE+ pin (pin 44) must be connected to V<sub>OUT</sub> either at the load for improved regulation or at V<sub>OUT</sub> of the device. The R<sub>RT</sub> resistor must be connected directly between the RT/CLK (pin 35) and AGND (pin 34). [Table 1](#) gives the standard external R<sub>SET</sub> resistor for a number of common bus voltages, along with the required R<sub>RT</sub> resistor for that output voltage.

**Table 1. Standard R<sub>SET</sub> Resistor Values for Common Output Voltages**

RESISTORS	OUTPUT VOLTAGE V <sub>OUT</sub> (V)						
	0.9	1.0	1.2	1.8	2.5	3.3	5.0
R <sub>SET</sub> (kΩ)	2.87	2.15	1.43	0.715	0.453	0.316	0.196
R <sub>RT</sub> (kΩ)	261	261	200	200	165	121	86.6

For other output voltages, the value of the required resistor can either be calculated using the following formula, or simply selected from the range of values given in [Table 2](#).

$$R_{SET} = \frac{1.43}{\left(\left(\frac{V_{OUT}}{0.6}\right) - 1\right)} \text{ (k}\Omega\text{)} \quad (1)$$

**Table 2. Standard R<sub>SET</sub> Resistor Values**

V <sub>OUT</sub> (V)	R <sub>SET</sub> (kΩ)	R <sub>RT</sub> (kΩ)	f <sub>sw</sub> (kHz)	V <sub>OUT</sub> (V)	R <sub>SET</sub> (kΩ)	R <sub>RT</sub> (kΩ)	f <sub>sw</sub> (kHz)
0.6	open	open	250	3.1	0.348	140	580
0.7	8.66	590	330	3.2	0.332	140	580
0.8	4.32	590	330	3.3	0.316	121	630
0.9	2.87	261	430	3.4	0.309	121	630
1.0	2.15	261	430	3.5	0.294	121	630
1.1	1.74	261	430	3.6	0.287	121	630
1.2	1.43	200	480	3.7	0.280	121	630
1.3	1.24	200	480	3.8	0.267	107	680
1.4	1.07	200	480	3.9	0.261	107	680
1.5	0.953	200	480	4.0	0.255	107	680
1.6	0.866	200	480	4.1	0.243	107	680
1.7	0.787	200	480	4.2	0.237	95.3	730
1.8	0.715	200	480	4.3	0.232	95.3	730
1.9	0.665	200	480	4.4	0.226	95.3	730
2.0	0.619	200	480	4.5	0.221	95.3	730
2.1	0.576	200	480	4.6	0.215	95.3	730
2.2	0.536	200	480	4.7	0.210	95.3	730
2.3	0.511	200	480	4.8	0.205	86.6	780
2.4	0.475	200	480	4.9	0.200	86.6	780
2.5	0.453	200	480	5.0	0.196	86.6	780
2.6	0.432	165	530	5.1	0.191	86.6	780
2.7	0.412	165	530	5.2	0.187	86.6	780
2.8	0.392	165	530	5.3	0.182	86.6	780
2.9	0.374	165	530	5.4	0.178	86.6	780
3.0	0.357	140	580	5.5	0.174	86.6	780

## CAPACITOR RECOMMENDATIONS FOR THE TPS84621 POWER SUPPLY

### Capacitor Technologies

#### *Electrolytic, Polymer-Electrolytic Capacitors*

When using electrolytic capacitors, high-quality, computer-grade electrolytic capacitors are recommended. Polymer-electrolytic type capacitors are recommended for applications where the ambient operating temperature is less than 0°C. The Sanyo OS-CON capacitor series is suggested due to the lower ESR, higher rated surge, power dissipation, ripple current capability, and small package size. Aluminum electrolytic capacitors provide adequate decoupling over the frequency range of 2 kHz to 150 kHz, and are suitable when ambient temperatures are above 0°C.

#### *Ceramic Capacitors*

The performance of aluminum electrolytic capacitors is less effective than ceramic capacitors above 150 kHz. Multilayer ceramic capacitors have a low ESR and a resonant frequency higher than the bandwidth of the regulator. They can be used to reduce the reflected ripple current at the input as well as improve the transient response of the output.

#### *Tantalum, Polymer-Tantalum Capacitors*

Polymer-tantalum type capacitors are recommended for applications where the ambient operating temperature is less than 0°C. The Sanyo POSCAP series and Kemet T530 capacitor series are recommended rather than many other tantalum types due to their lower ESR, higher rated surge, power dissipation, ripple current capability, and small package size. Tantalum capacitors that have no stated ESR or surge current rating are not recommended for power applications.

### Input Capacitor

The TPS84621 requires a minimum input capacitance of 100  $\mu\text{F}$  of ceramic and/or polymer-tantalum capacitors. The ripple current rating of the capacitor must be at least 450 mArms. [Table 4](#) includes a preferred list of capacitors by vendor.

### Output Capacitor

The required output capacitance is determined by the output voltage of the TPS84621. See [Table 3](#) for the amount of required capacitance. The required output capacitance must be comprised of all ceramic capacitors. When adding additional non-ceramic bulk capacitors, low-ESR devices like the ones recommended in [Table 4](#) are required. The required capacitance above the minimum is determined by actual transient deviation requirements. See [Table 5](#) for typical transient response values for several output voltage, input voltage and capacitance combinations. [Table 4](#) includes a preferred list of capacitors by vendor.

**Table 3. Required Output Capacitance**

V <sub>OUT</sub> RANGE (V)		MINIMUM REQUIRED C <sub>OUT</sub> ( $\mu\text{F}$ )
MIN	MAX	
0.6	< 0.8	400 $\mu\text{F}$ ceramic
0.8	< 1.2	300 $\mu\text{F}$ ceramic
1.2	< 3.0	200 $\mu\text{F}$ ceramic
3.0	< 4.0	100 $\mu\text{F}$ ceramic
4.0	5.5	47 $\mu\text{F}$ ceramic

**Table 4. Recommended Input/Output Capacitors<sup>(1)</sup>**

VENDOR	SERIES	PART NUMBER	CAPACITOR CHARACTERISTICS		
			WORKING VOLTAGE (V)	CAPACITANCE (µF)	ESR <sup>(2)</sup> (mΩ)
Murata	X5R	GRM32ER61E226K	16	22	2
TDK	X5R	C3225X5R0J476K	6.3	47	2
Murata	X5R	GRM32ER60J476M	6.3	47	2
Sanyo	POSCAP	16TQC68M	16	68	50
Kemet	T520	T520V107M010ASE025	10	100	25
Sanyo	POSCAP	6TPE100MI	6.3	100	25
Sanyo	POSCAP	2R5TPE220M7	2.5	220	7
Kemet	T530	T530D227M006ATE006	6.3	220	6
Kemet	T530	T530D337M006ATE010	6.3	330	10
Sanyo	POSCAP	2TPF330M6	2.0	330	6
Sanyo	POSCAP	6TPE330MFL	6.3	330	15

**(1) Capacitor Supplier Verification**

Please verify availability of capacitors identified in this table.

**RoHS, Lead-free and Material Details**

Please consult capacitor suppliers regarding material composition, RoHS status, lead-free status, and manufacturing process requirements.

**(2) Maximum ESR @ 100kHz, 25°C.**
**Transient Response**
**Table 5. Output Voltage Transient Response**

C <sub>IN1</sub> = 47 µF CERAMIC, C <sub>IN2</sub> = 220 µF POLYMER-TANTALUM						
V <sub>OUT</sub> (V)	V <sub>IN</sub> (V)	C <sub>OUT1</sub> Ceramic	C <sub>OUT2</sub> BULK	VOLTAGE DEVIATION (mV)		RECOVERY TIME (µs)
				2 A LOAD STEP, (1 A/µs)	3 A LOAD STEP, (1 A/µs)	
0.6	5	400 µF	330 µF	20	30	120
0.8	5	300 µF	220 µF	25	35	140
		300 µF	330 µF	20	30	140
	12	300 µF	220 µF	30	35	140
		300 µF	330 µF	25	30	140
1.2	5	200 µF	100 µF	40	50	150
		200 µF	220 µF	35	45	150
	12	200 µF	100 µF	35	45	150
		200 µF	220 µF	30	40	150
1.8	5	200 µF	-	65	85	160
		200 µF	100 µF	55	96	160
	12	200 µF	-	55	80	160
		200 µF	100 µF	50	75	160
3.3	5	100 µF	100 µF	90	140	180
	12	100 µF	100 µF	85	125	180

Transient Waveforms

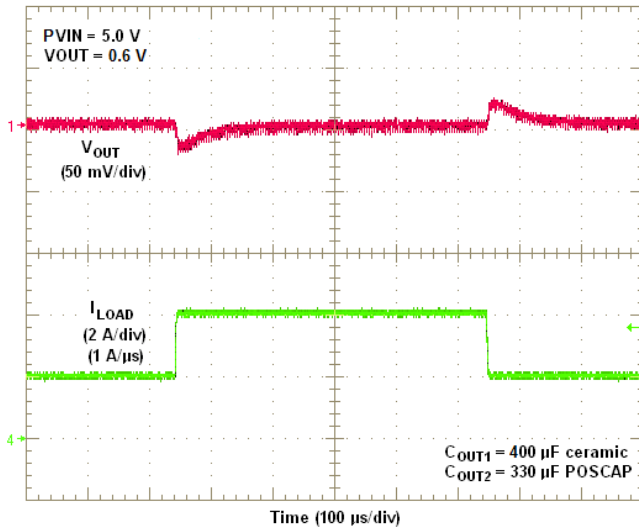


Figure 17. PVIN = 5V, VOUT = 0.6V, 2A Load Step

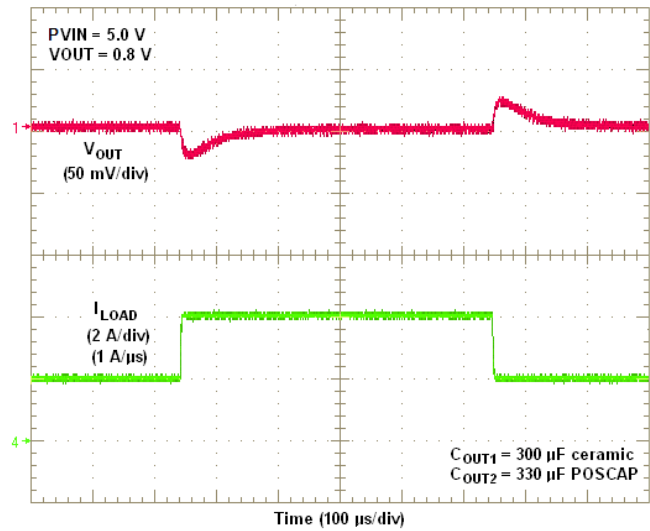


Figure 18. PVIN = 5V, VOUT = 0.8V, 2A Load Step

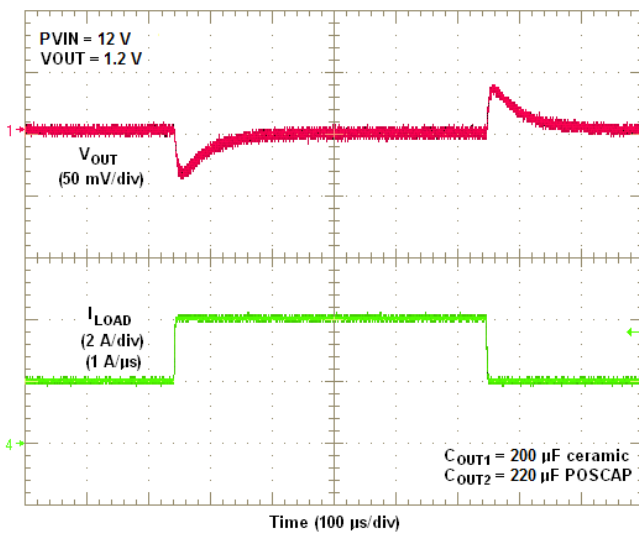


Figure 19. PVIN = 12V, VOUT = 1.2V, 2A Load Step

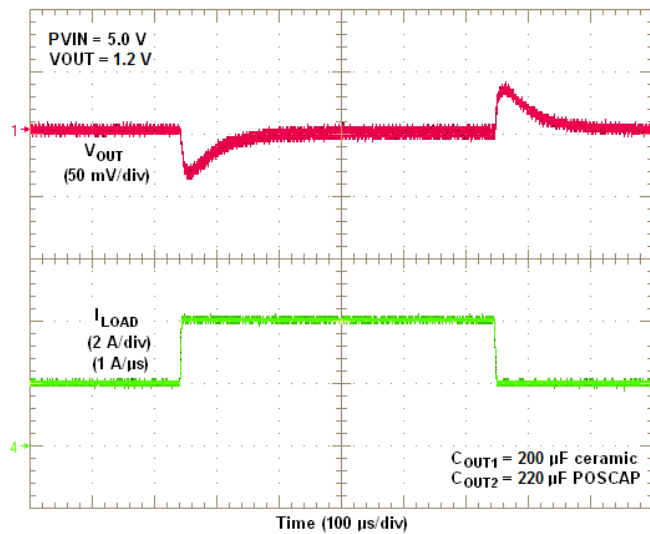


Figure 20. PVIN = 5V, VOUT = 1.2V, 2A Load Step

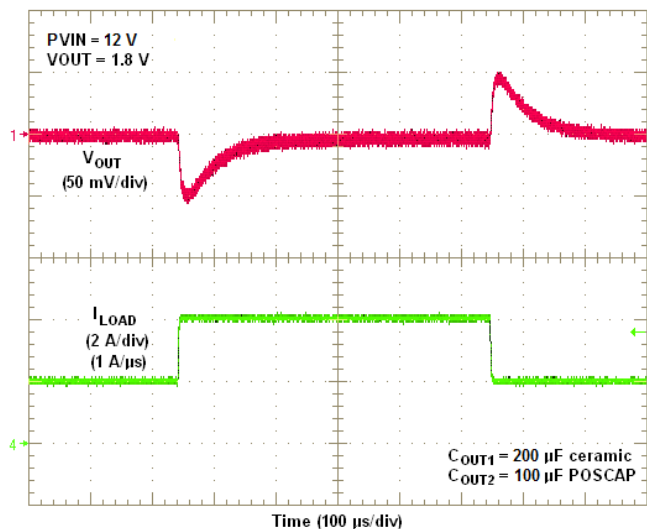


Figure 21. PVIN = 12V, VOUT = 1.8V, 2A Load Step

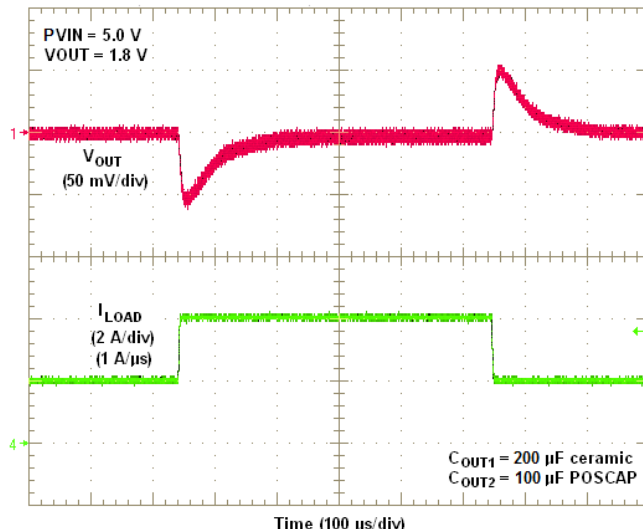


Figure 22. PVIN = 5V, VOUT = 1.8V, 2A Load Step

Application Schematics

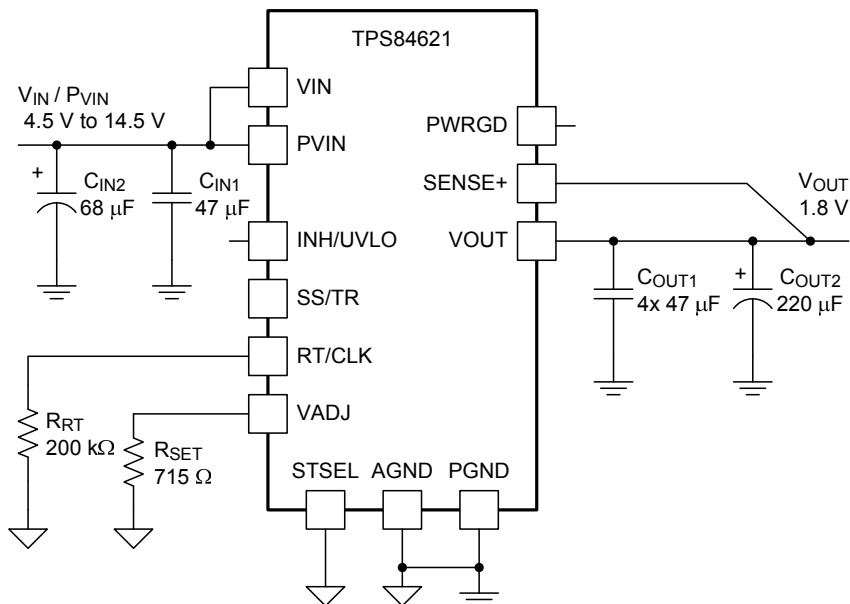
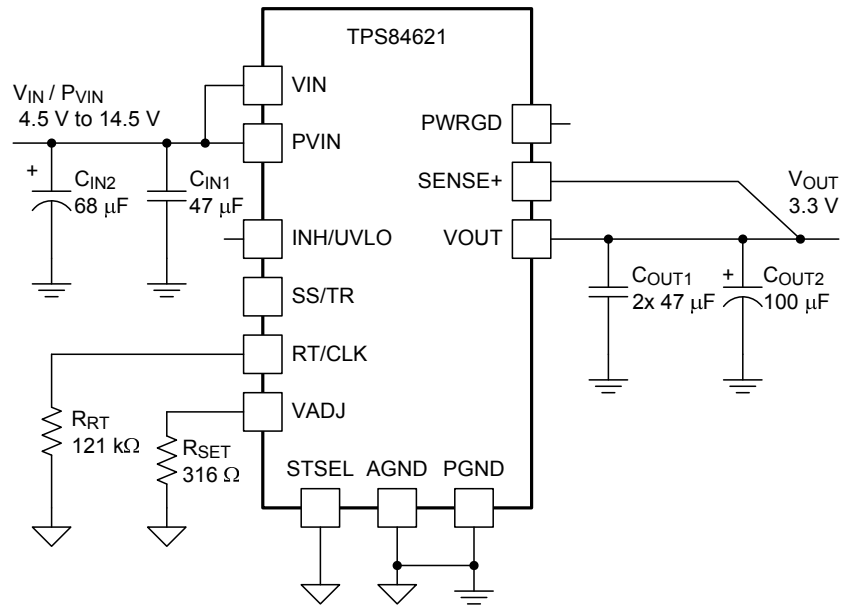
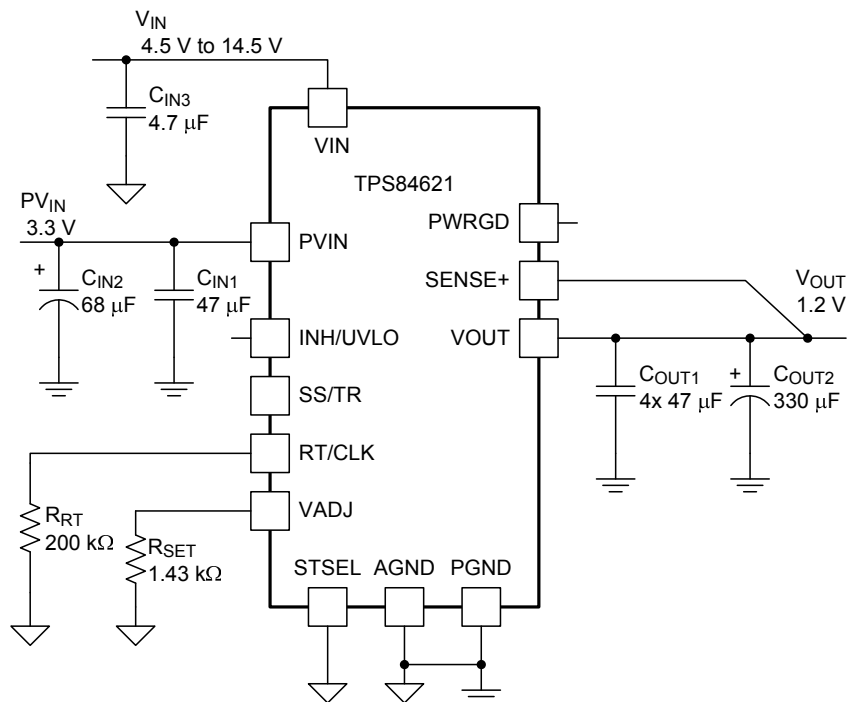


Figure 23. Typical Schematic  
 PVIN = VIN = 4.5 V to 14.5 V, VOUT = 1.8 V



**Figure 24. Typical Schematic**  
**PVIN = VIN = 4.5 V to 14.5 V, VOUT = 3.3 V**



**Figure 25. Typical Schematic**  
**PVIN = 3.3 V, VIN = 4.5 V to 14.5 V, VOUT = 1.2 V**



## VIN and PVIN Input Voltage

The TPS84621 allows for a variety of applications by using the VIN and PVIN pins together or separately. The VIN voltage supplies the internal control circuits of the device. The PVIN voltage provides the input voltage to the power converter system.

If tied together, the input voltage for the VIN pin and the PVIN pin can range from 4.5 V to 14.5 V. If using the VIN pin separately from the PVIN pin, the VIN pin must be between 4.5 V and 14.5 V, and the PVIN pin can range from as low as 1.6 V to 14.5 V. A voltage divider connected to the INH/UVLO pin can adjust the either input voltage UVLO appropriately. See the [Programmable Undervoltage Lockout \(UVLO\)](#) section of this datasheet for more information.

### 3.3-V Input Operation

Applications operating from 3.3 V must provide at least 4.5 V for VIN. See application note, [SLVA561](#) for help creating 5 V from 3.3 V using a small, simple charge pump device.

### Power Good (PWRGD)

The PWRGD pin is an open drain output. Once the voltage on the SENSE+ pin is between 94% and 106% of the set voltage, the PWRGD pin pull-down is released and the pin floats. The recommended pull-up resistor value is between 10 k $\Omega$  and 100 k $\Omega$  to a voltage source that is 5.5 V or less. The PWRGD pin is in a defined state once VIN is greater than 1.0 V, but with reduced current sinking capability. The PWRGD pin achieves full current sinking capability once the VIN pin is above 4.5V. The PWRGD pin is pulled low when the voltage on SENSE+ is lower than 91% or greater than 109% of the nominal set voltage. Also, the PWRGD pin is pulled low if the input UVLO or thermal shutdown is asserted, the INH pin is pulled low, or the SS/TR pin is below 1.4 V.

### Parallel Operation

Up to six TPS84621 devices can be paralleled for increased output current. Multiple connections must be made between the paralleled devices and the component selection is slightly different than for a stand-alone TPS84621 device. A typical TPS84621 parallel schematic is shown in Figure 26. Refer to application note, [SLVA574](#) for information and design help when paralleling multiple TPS84621 devices.

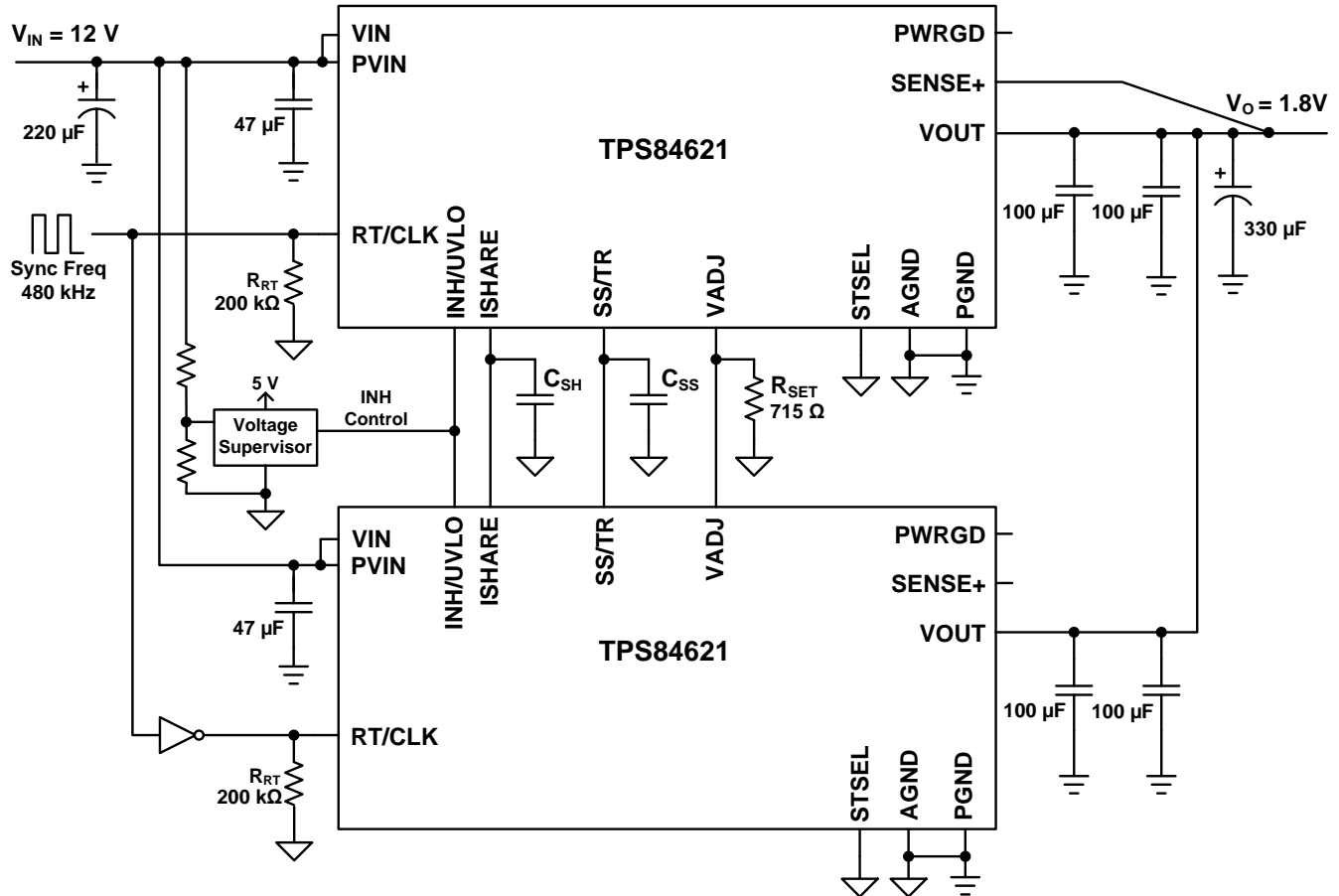


Figure 26. Typical TPS84621 Parallel Schematic

## Power-Up Characteristics

When configured as shown in the front page schematic, the TPS84621 produces a regulated output voltage following the application of a valid input voltage. During the power-up, internal soft-start circuitry slows the rate that the output voltage rises, thereby limiting the amount of in-rush current that can be drawn from the input source. The soft-start circuitry introduces a short time delay from the point that a valid input voltage is recognized. Figure 27 shows the start-up waveforms for a TPS84621, operating from a 5-V input ( $PV_{IN}=V_{IN}$ ) and with the output voltage adjusted to 1.8 V. Figure 28 shows the start-up waveforms for a TPS84621 starting up into a pre-biased output voltage. The waveforms were measured with a 3-A constant current load.

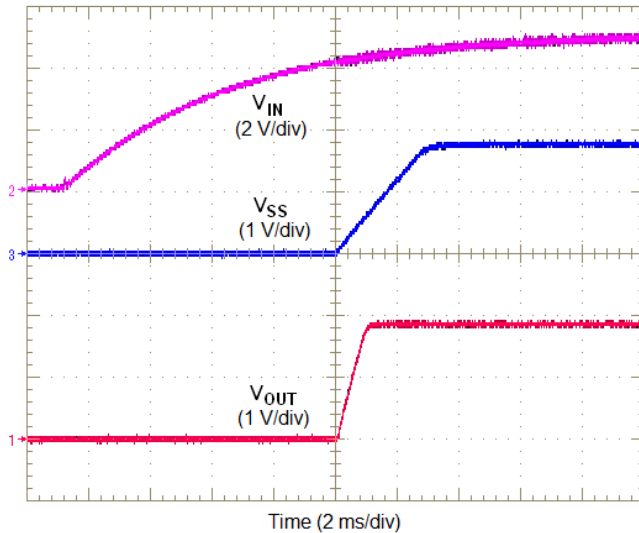


Figure 27. Start-Up Waveforms

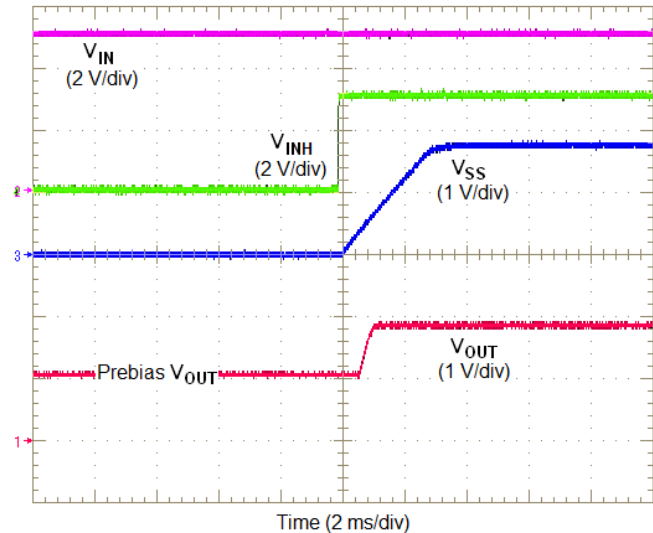


Figure 28. Start-up into Pre-bias

## Pre-Biased Start-Up

The TPS84621 has been designed to prevent discharging a pre-biased output. During monotonic pre-biased startup, the TPS84621 does not allow current to sink until the SS/TR pin voltage is higher than 1.4 V.

## Remote Sense

The SENSE+ pin must be connected to  $V_{OUT}$  at the load, or at the device pins.

Connecting the SENSE+ pin to  $V_{OUT}$  at the load improves the load regulation performance of the device by allowing it to compensate for any I-R voltage drop between its output pins and the load. An I-R drop is caused by the high output current flowing through the small amount of pin and trace resistance. This should be limited to a maximum of 300 mV.

### NOTE

The remote sense feature is not designed to compensate for the forward drop of nonlinear or frequency dependent components that may be placed in series with the converter output. Examples include OR-ing diodes, filter inductors, ferrite beads, and fuses. When these components are enclosed by the SENSE+ connection, they are effectively placed inside the regulation control loop, which can adversely affect the stability of the regulator.

## Thermal Shutdown

The internal thermal shutdown circuitry forces the device to stop switching if the junction temperature exceeds 175°C typically. The device reinitiates the power up sequence when the junction temperature drops below 165°C typically.

### Output On/Off Inhibit (INH)

The INH pin provides electrical on/off control of the device. Once the INH pin voltage exceeds the threshold voltage, the device starts operation. If the INH pin voltage is pulled below the threshold voltage, the regulator stops switching and enters low quiescent current state.

The INH pin has an internal pull-up current source, allowing the user to float the INH pin for enabling the device. If an application requires controlling the INH pin, use an open drain/collector device, or a suitable logic gate to interface with the pin.

Figure 29 shows the typical application of the inhibit function. The Inhibit control has its own internal pull-up to VIN potential. An open-collector or open-drain device is recommended to control this input.

Turning Q1 on applies a low voltage to the inhibit control (INH) pin and disables the output of the supply, shown in Figure 30. If Q1 is turned off, the supply executes a soft-start power-up sequence, as shown in Figure 31. A regulated output voltage is produced within 3 ms. The waveforms were measured with a 3-A constant current load.

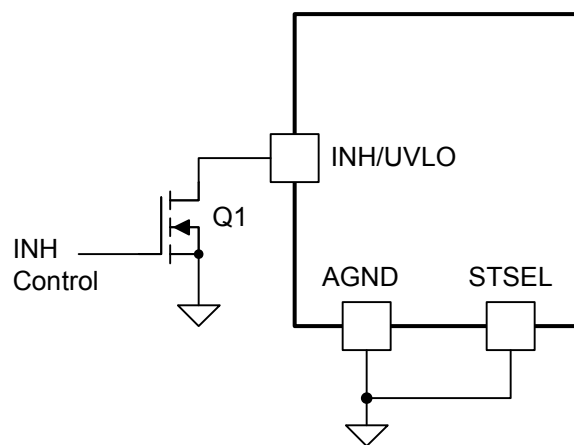


Figure 29. Typical Inhibit Control

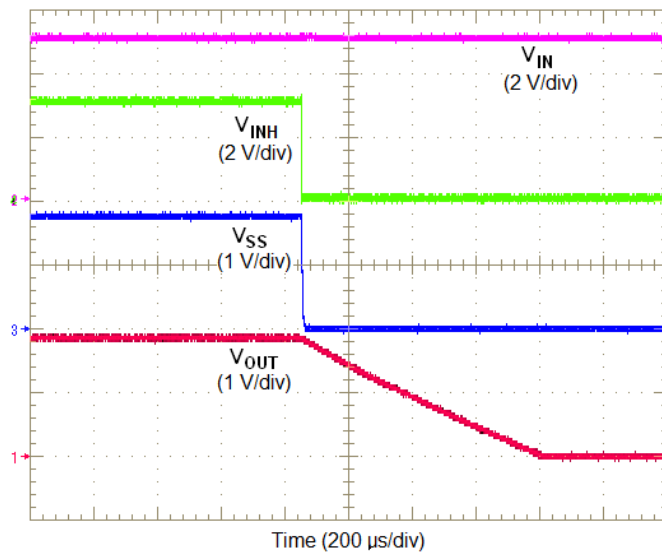


Figure 30. Inhibit Turn-Off

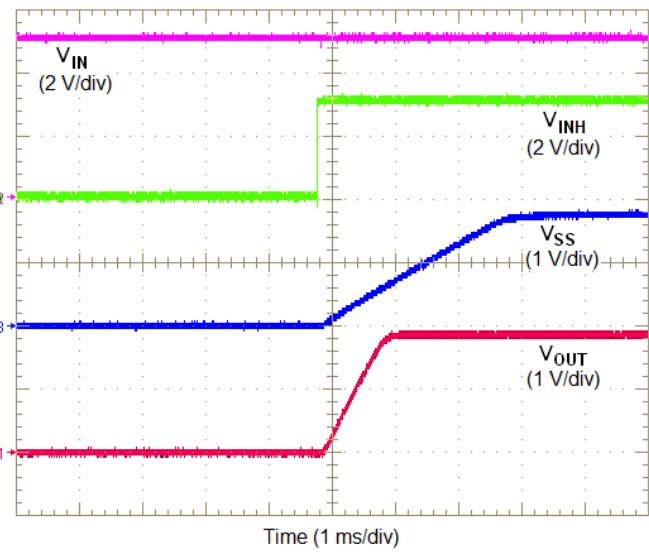


Figure 31. Inhibit Turn-On

### Slow Start (SS/TR)

Connecting the STSEL pin to AGND and leaving SS/TR pin open enables the internal SS capacitor with a slow start interval of approximately 1.1 ms. Adding additional capacitance between the SS pin and AGND increases the slow start time. Table 6 shows an additional SS capacitor connected to the SS/TR pin and the STSEL pin connected to AGND. See Table 6 below for SS capacitor values and timing interval.

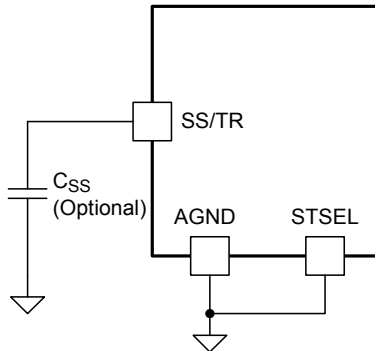


Figure 32. Slow-Start Capacitor (C<sub>SS</sub>) and STSEL Connection

Table 6. Slow-Start Capacitor Values and Slow-Start Time

C <sub>SS</sub> (pF)	open	2200	4700	10000	15000	22000	25000
SS Time (msec)	1.1	1.9	2.8	4.6	6.4	8.8	9.8

### Overcurrent Protection

For protection against load faults, the TPS84621 incorporates output overcurrent protection. Applying a load that exceeds the regulator's overcurrent threshold causes the regulated output to shut down. Following shutdown, the module periodically attempts to recover by initiating a soft-start power-up as shown in Figure 33. This is described as a hiccup mode of operation, whereby the module continues in a cycle of successive shutdown and power up until the load fault is removed. During this period, the average current flowing into the fault is significantly reduced. Once the fault is removed, the module automatically recovers and returns to normal operation as shown in Figure 34.

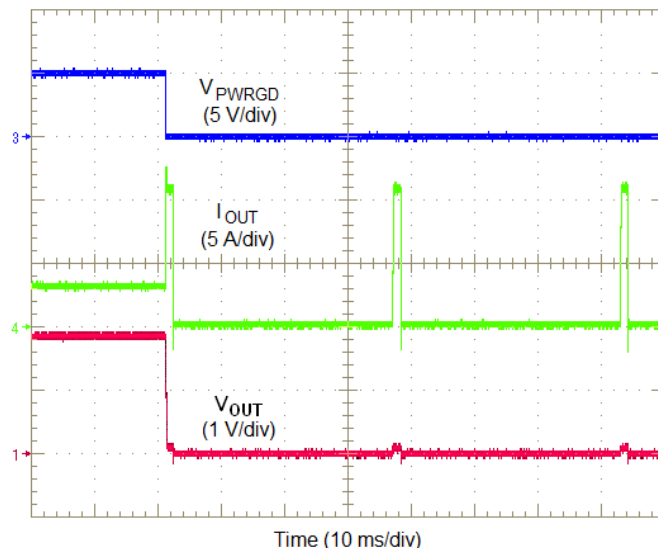


Figure 33. Overcurrent Limiting

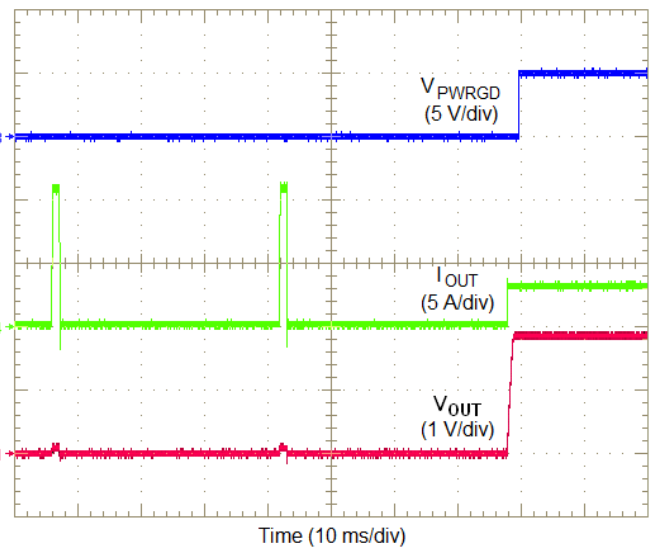
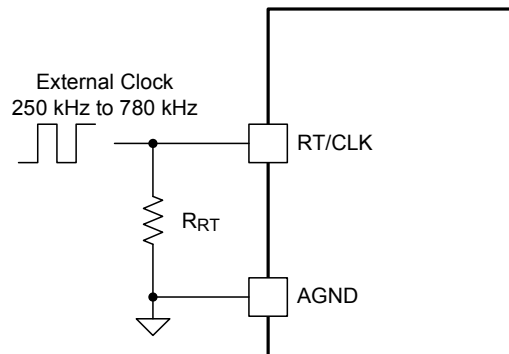


Figure 34. Removal of Overcurrent Condition

## Synchronization (CLK)

An internal phase locked loop (PLL) has been implemented to allow synchronization between 250 kHz and 780 kHz, and to easily switch from RT mode to CLK mode. To implement the synchronization feature, connect a square wave clock signal to the RT/CLK pin with a duty cycle between 20% to 80%. The clock signal amplitude must transition lower than 0.8 V and higher than 2.0 V. The start of the switching cycle is synchronized to the falling edge of RT/CLK pin. In applications where both RT mode and CLK mode are needed, the device can be configured as shown in .

Before the external clock is present, the device works in RT mode and the switching frequency is set by RT resistor. When the external clock is present, the CLK mode overrides the RT mode. The first time the CLK pin is pulled above the RT/CLK high threshold (2.0 V), the device switches from RT mode to the CLK mode and the RT/CLK pin becomes high impedance as the PLL starts to lock onto the frequency of the external clock. It is not recommended to switch from CLK mode back to RT mode because the internal switching frequency drops to 100 kHz first before returning to the switching frequency set by the RT resistor ( $R_{RT}$ ).



**Figure 35. CLK/RT Configuration**

The synchronization frequency must be selected based on the output voltages of the devices being synchronized. [Table 7](#) shows the allowable frequencies for a given range of output voltages. For the most efficient solution, always synchronize to the lowest allowable frequency. For example, an application requires synchronizing three TPS84621 devices with output voltages of 1.2 V, 1.8 V and 3.3 V, all powered from  $PV_{IN} = 12$  V. [Table 7](#) shows that all three output voltages should be synchronized to 630 kHz.

**Table 7. Synchronization Frequency vs Output Voltage**

SYNCHRONIZATION FREQUENCY (kHz)	$R_{RT}$ (k $\Omega$ )	$PV_{IN} = 12$ V		$PV_{IN} = 5$ V	
		$V_{OUT}$ RANGE (V)		$V_{OUT}$ RANGE (V)	
		MIN	MAX	MIN	MAX
250	open	0.6	1.0	0.6	1.3
280	1100	0.6	1.2	0.6	1.6
330	590	0.6	1.5	0.6	4.5
380	357	0.7	1.7	0.6	4.5
430	261	0.8	2.1	0.6	4.5
480	200	0.9	2.5	0.6	4.5
530	165	1.0	2.9	0.6	4.5
580	140	1.1	3.2	0.6	4.5
630	121	1.2	3.7	0.6	4.5
680	107	1.3	4.1	0.6	4.5
730	95.3	1.4	4.7	0.6	4.5
780	86.6	1.5	5.5	0.6	4.5

### Sequencing (SS/TR)

Many of the common power supply sequencing methods can be implemented using the SS/TR, INH and PWRGD pins. The sequential method is illustrated in Figure 36 using two TPS84621 devices. The PWRGD pin of the first device is coupled to the INH pin of the second device which enables the second power supply once the primary supply reaches regulation. Figure 37 shows sequential turn-on waveforms of two TPS84621 devices.

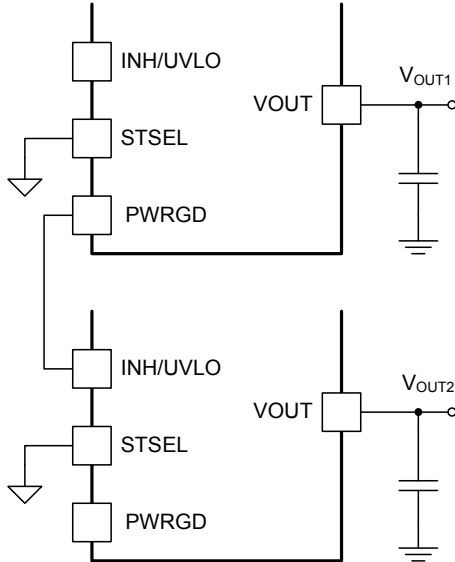


Figure 36. Sequencing Schematic

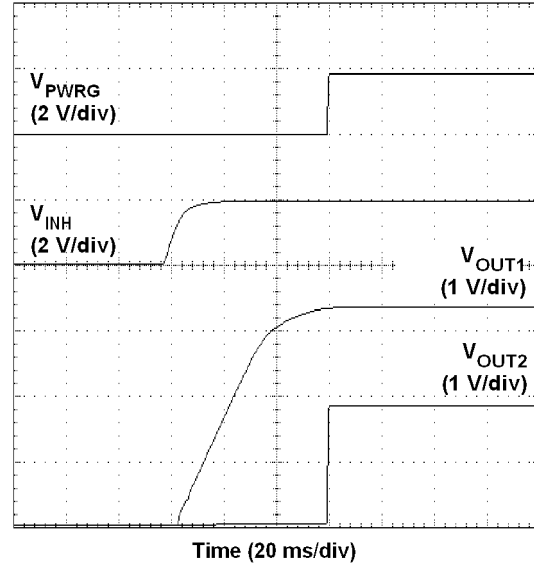


Figure 37. Sequencing Waveforms

Simultaneous power supply sequencing can be implemented by connecting the resistor network of R1 and R2 shown in Figure 38 to the output of the power supply that needs to be tracked or to another voltage reference source. Figure 39 shows simultaneous turn-on waveforms of two TPS84621 devices. Use Equation 2 and Equation 3 to calculate the values of R1 and R2.

$$R1 = \frac{(V_{OUT2} \times 12.6)}{0.6} \text{ (k}\Omega\text{)}$$

$$(2) \quad R2 = \frac{0.6 \times R1}{(V_{OUT2} - 0.6)} \text{ (k}\Omega\text{)} \quad (3)$$

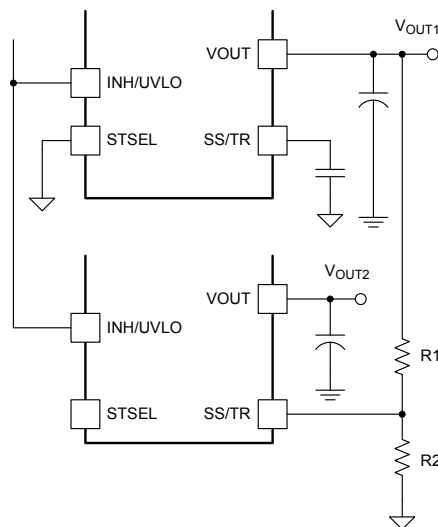


Figure 38. Simultaneous Tracking Schematic

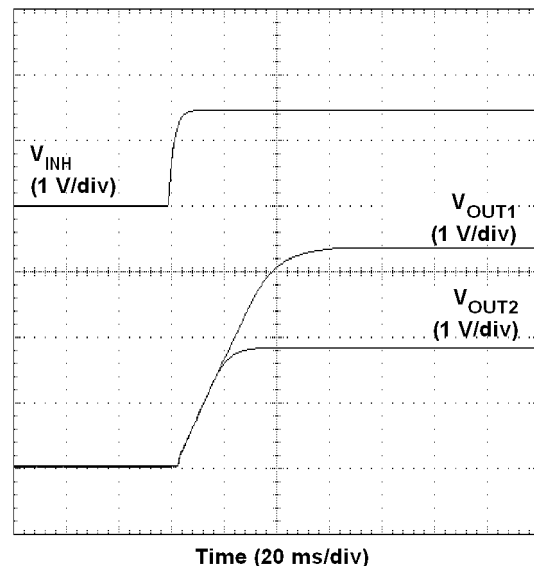


Figure 39. Simultaneous Tracking Waveforms

### Programmable Undervoltage Lockout (UVLO)

The TPS84621 implements internal UVLO circuitry on the VIN pin. The device is disabled when the VIN pin voltage falls below the internal VIN UVLO threshold. The internal VIN UVLO rising threshold is 4.5 V(max) with a typical hysteresis of 150 mV.

If an application requires either a higher UVLO threshold on the VIN pin or a higher UVLO threshold for a combined VIN and PVIN, then the UVLO pin can be configured as shown in Figure 40 or Figure 41. Table 8 lists standard values for  $R_{UVLO1}$  and  $R_{UVLO2}$  to adjust the VIN UVLO voltage up.

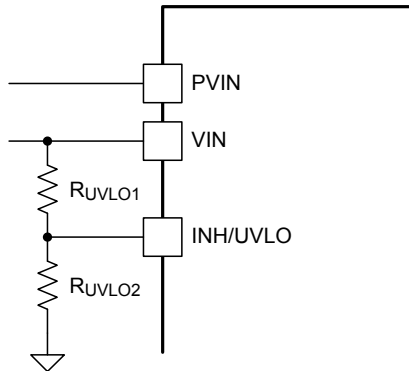


Figure 40. Adjustable VIN UVLO

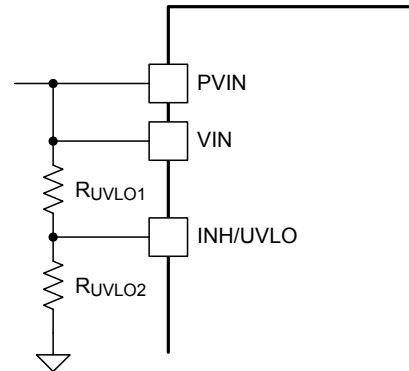


Figure 41. Adjustable VIN and PVIN Undervoltage Lockout

Table 8. Standard Resistor values for Adjusting VIN UVLO

VIN UVLO (V)	5.0	5.5	6.0	6.5	7.0	7.5	8.0	8.5	9.0	9.5	10.0
$R_{UVLO1}$ (k $\Omega$ )	68.1	68.1	68.1	68.1	68.1	68.1	68.1	68.1	68.1	68.1	68.1
$R_{UVLO2}$ (k $\Omega$ )	21.5	18.7	16.9	15.4	14.0	13.0	12.1	11.3	10.5	9.76	9.31
Hysteresis (mV)	400	415	430	450	465	480	500	515	530	550	565

For a split rail application, if a secondary UVLO on PVIN is required, VIN must be  $\geq 4.5V$ . Figure 42 shows the PVIN UVLO configuration. Use Table 9 to select  $R_{UVLO1}$  and  $R_{UVLO2}$  for PVIN. If PVIN UVLO is set for less than 3.0 V, a 5.1-V zener diode should be added to clamp the voltage on the UVLO pin below 6 V.

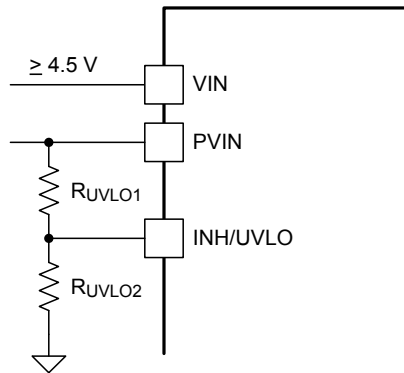


Figure 42. Adjustable PVIN Undervoltage Lockout, (VIN  $\geq 4.5$  V)

Table 9. Standard Resistor Values for Adjusting PVIN UVLO, (VIN  $\geq 4.5$  V)

PVIN UVLO (V)	2.0	2.5	3.0	3.5	4.0	4.5	
$R_{UVLO1}$ (k $\Omega$ )	68.1	68.1	68.1	68.1	68.1	68.1	For higher PVIN UVLO voltages see Table UV for resistor values
$R_{UVLO2}$ (k $\Omega$ )	95.3	60.4	44.2	34.8	28.7	24.3	
Hysteresis (mV)	300	315	335	350	365	385	



## Layout Considerations

To achieve optimal electrical and thermal performance, an optimized PCB layout is required. Figure 43, shows a typical PCB layout. Some considerations for an optimized layout are:

- Use large copper areas for power planes (PVIN, VOUT, and PGND) to minimize conduction loss and thermal stress.
- Place ceramic input and output capacitors close to the device pins to minimize high frequency noise.
- Locate additional output capacitors between the ceramic capacitor and the load.
- Place a dedicated AGND copper area beneath the TPS84621.
- Isolate the PH copper area from the VOUT copper area using the AGND copper area.
- Connect the AGND and PGND copper area at one point; see AGND to PGND connection point in Figure 43.
- Place  $R_{SET}$ ,  $R_{RT}$ , and  $C_{SS}$  as close as possible to their respective pins.
- Use multiple vias to connect the power planes to internal layers.

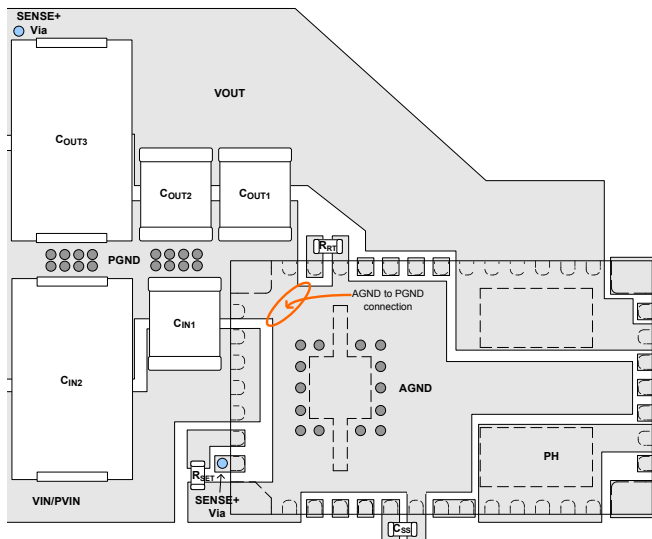


Figure 43. Typical Top-Layer Recommended Layout

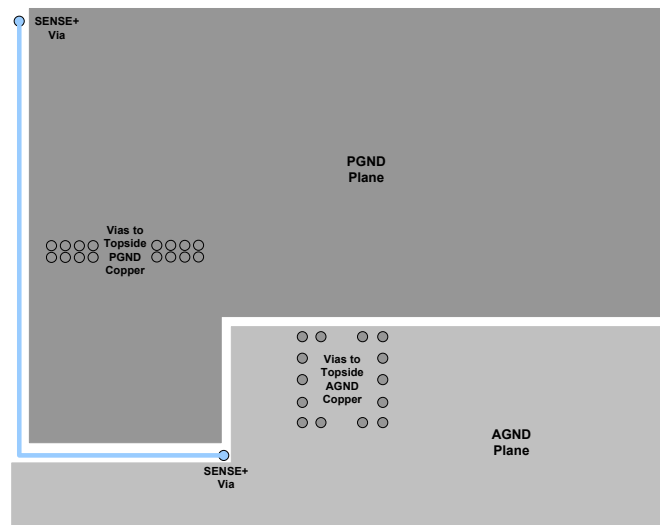
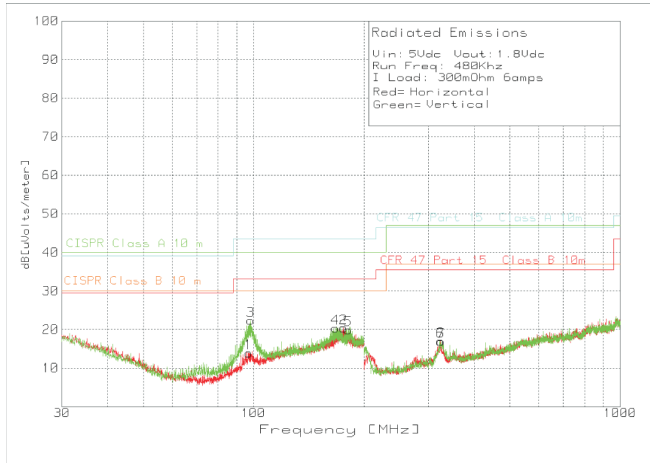


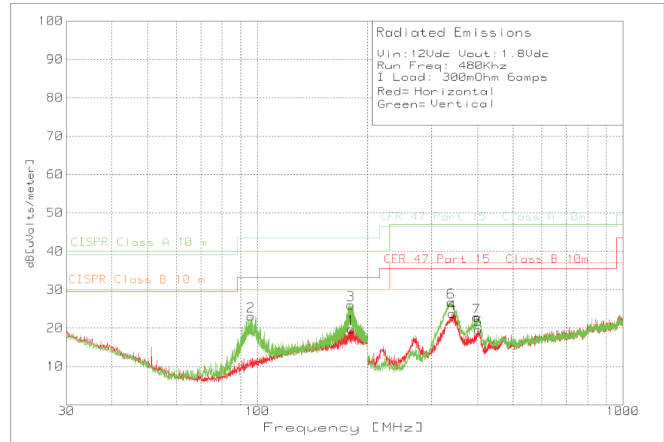
Figure 44. Typical GND-Layer Recommended Layout

**EMI**

The TPS84621 is compliant with EN55022 Class B radiated emissions. [Figure 46](#) and [Figure 45](#) show typical examples of radiated emissions plots for the TPS84621 operating from 5V and 12V respectively. Both graphs include the plots of the antenna in the horizontal and vertical positions.



**Figure 45. Radiated Emissions 5-V Input, 1.8-V Output, 6-A Load (EN55022 Class B)**



**Figure 46. Radiated Emissions 12-V Input, 1.8-V Output, 6-A Load (EN55022 Class B)**

**Changes from Original (DECEMBER 2011) to Revision A Page**


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- Changed – updated pin names in package drawing. .... 7
- 

**Changes from Revision A (MAY 2012) to Revision B Page**


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- Added Thermal Information table ..... 3
- 

**Changes from Revision B (OCTOBER 2012) to Revision C Page**


---

- Changed the minimum input voltage to 2.95V from 4.5V ..... 1
  - Added ISHARE parameter to Absolute Maximum Ratings table. .... 2
  - Added ISHARE to the Pin Description table. .... 6
  - Added Parallel Operation section. .... 18
-

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
TPS84621RUQR	ACTIVE	B1QFN	RUQ	47	500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
TPS84621RUQT	ACTIVE	B1QFN	RUQ	47	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

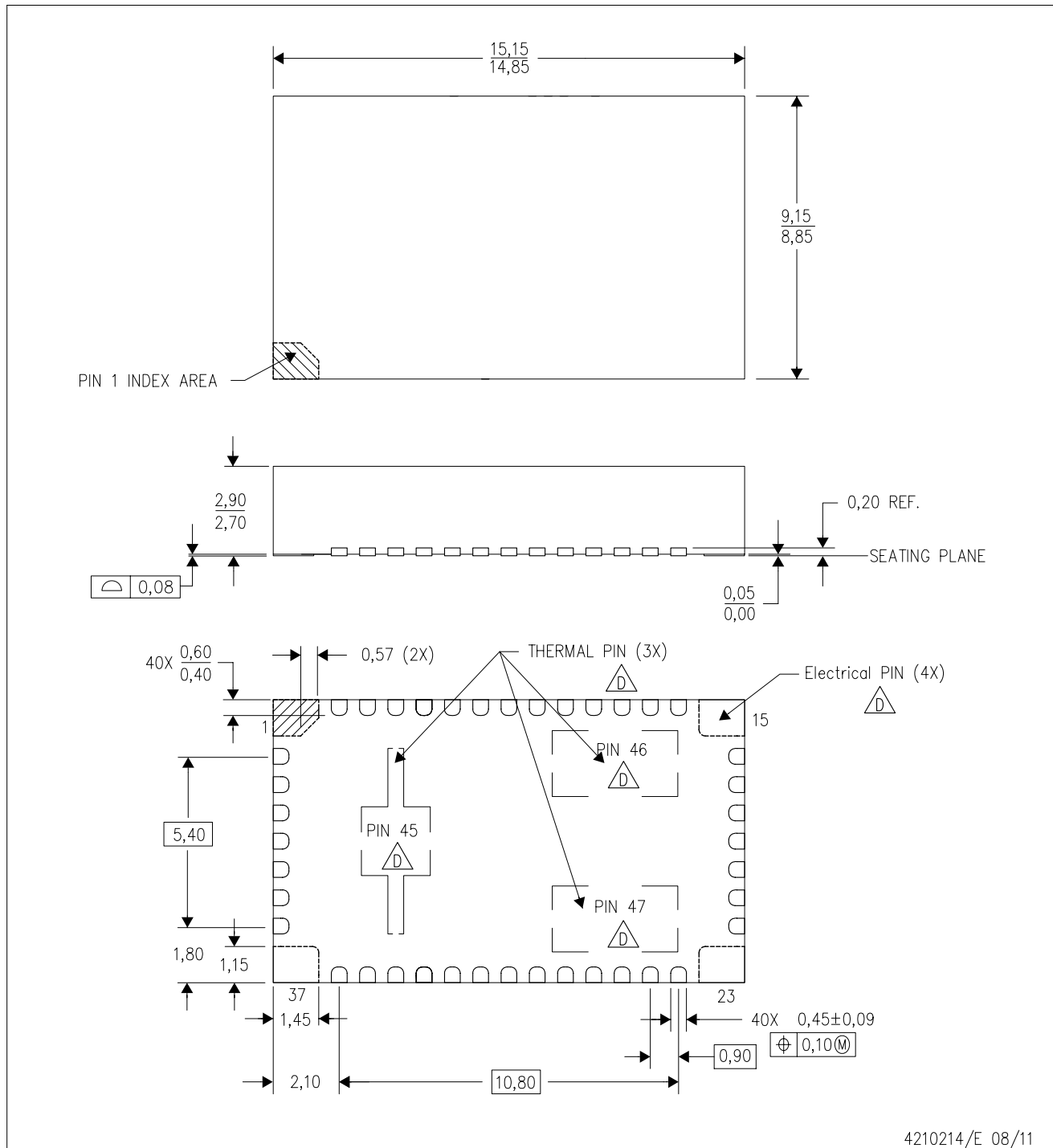
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# MECHANICAL DATA

RUQ (R-PB1QFN-N47)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Quad Flatpack, No-leads (QFN) package configuration.
  -  The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  -  The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane.

# THERMAL PAD MECHANICAL DATA

RUQ (R-PB1QFN-N47)

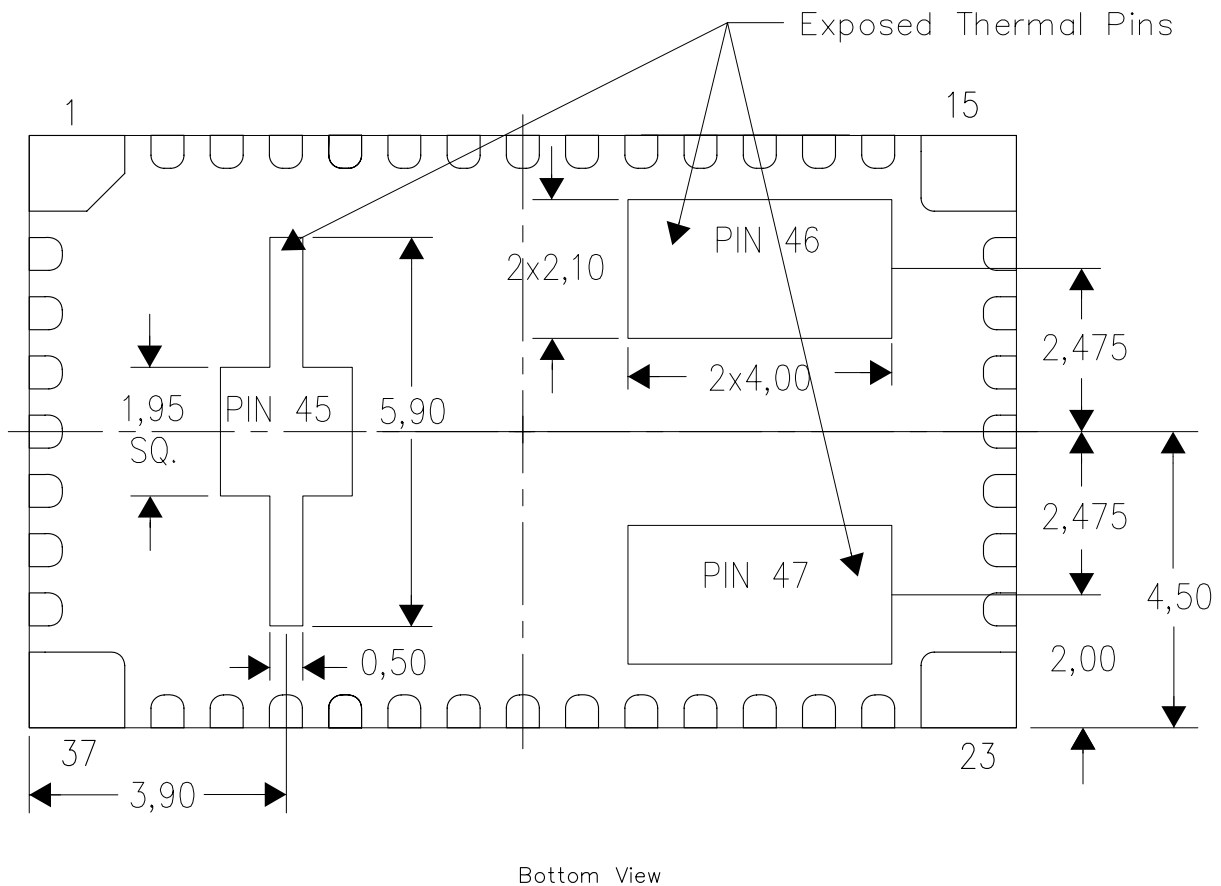
PLASTIC QUAD FLATPACK NO-LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



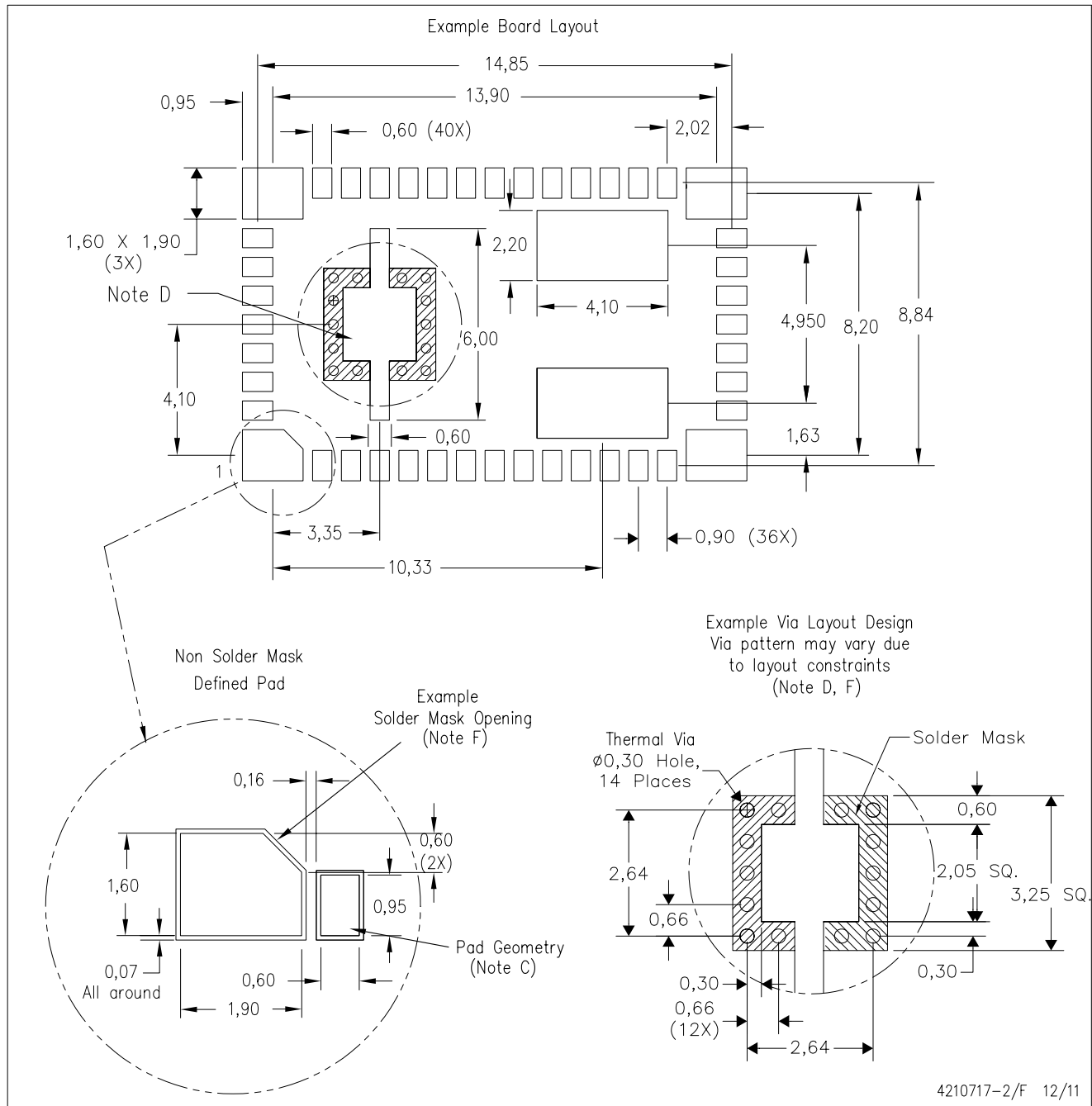
Exposed Thermal Pad Dimensions

4210496/C 09/10

NOTE: A. All linear dimensions are in millimeters

RUQ (R-PB1QFN-N47)

PLASTIC QUAD FLATPACK NO-LEAD



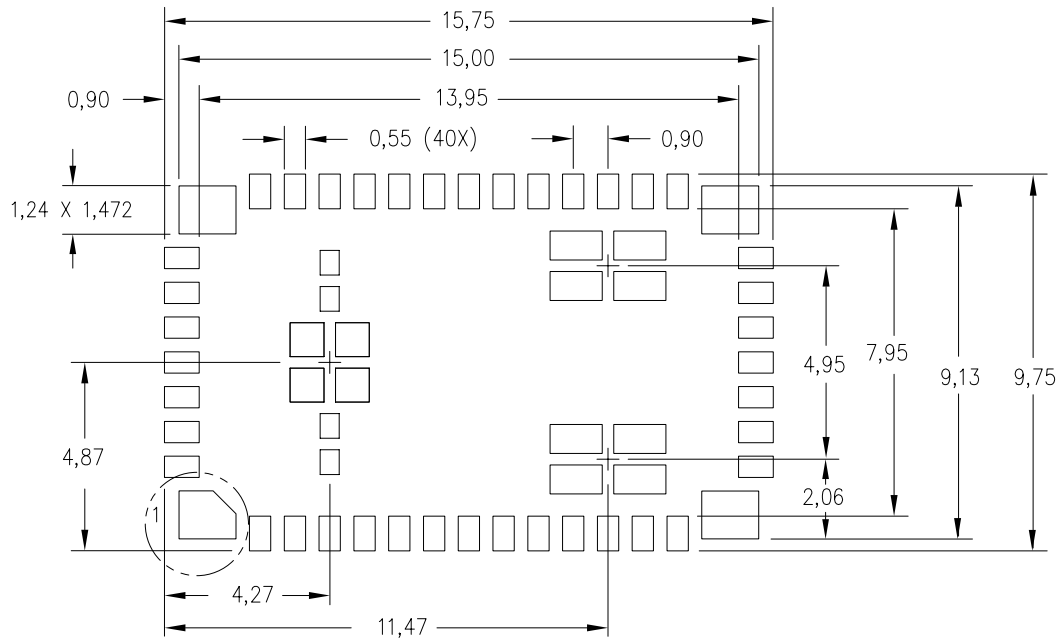
- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
  - G. See sheet 3 for stencil design recommendation..

RUQ (R-PB1QFN-N47)

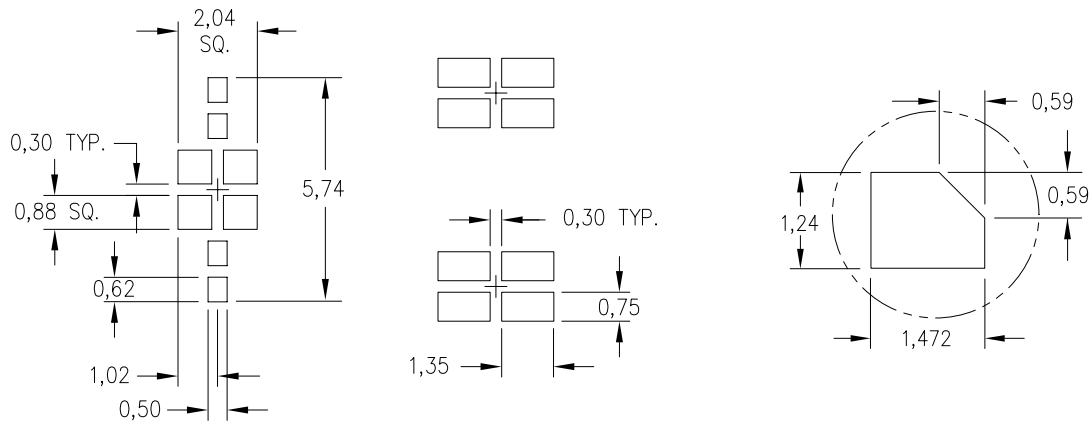
PLASTIC QUAD FLATPACK NO-LEAD

DETAIL OF SHEET 2

Example Stencil Design (Note E)  
Stencil Thickness = 0,125mm



60% solder coverage on center pads



4210717-3/F 12/11

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.



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