# 40-V Step-Down Converter With Eco-mode™ Codec and LDO Regulator

**Check for Samples: TPS65320-Q1**

## FEATURES

- **Qualified for Automotive Applications**
- **AEC-Q100 Qualified with the Following Results:**
  - **Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature**
  - **Device HBM ESD Classification Level H2**
  - **Device CDM ESD Classification Level C3B**
- **One High-VIN Buck Converter**
  - **Input Range of 3.6 V to 40 V**
  - **Asynchronous Buck Converter (Internal FET)**
    - **Max Load Current 3.2 A, Output Adjustable 1.1 V to 20 V**
  - **High-Duty-Cycle Operation Supported**
  - **Adjustable Switch-Mode Frequency 100 kHz to 2.5 MHz**
  - **Less Than 140-μA Standby Current in Low-Power Mode**
- **One Low-Dropout Voltage (LDO) Regulator**
  - **280-mA Current Capability with 40-μA Standby Current in Low-Load Condition**
  - **Input Supply Auto-Source to Balance Efficiency and Low Standby Current**
  - **Power-Good Output (Push-Pull)**
  - **Low-Dropout Voltage of 300 mV at $I_{OUT}$ = 200 mA (Typical)**
- **Overcurrent Protection for All Regulators**
- **Overtemperature Protection**
- **14-Pin HTSSOP Package With PowerPAD™ Package**

## APPLICATIONS

- **Qualified for Automotive Applications**
- **Infotainment, Telematics**
- **TFT Cluster**
- **Advanced Driver Assistant System**

## DESCRIPTION

The TPS65320-Q1 power supply is a combination of a single high-voltage switch-mode asynchronous buck power supply and an LDO regulator. This is a monolithic high-voltage switching regulator with an integrated switch of 40 V, a power MOSFET, and a low-standby-current LDO. The device has a voltage supervisor which monitors the outputs of the switch-mode power supply. To reduce heat, the input supply of the LDO can auto-source from the input voltage to the output of the buck. The low-voltage tracking feature can possibly eliminate the need to use a boost converter during cold-crank conditions.

The TPS65320-Q1 has a switching frequency range from 100 kHz to 2.5 MHz, providing customers with a flexible design to fit their system needs. The external loop compensations allow the user to optimize the converter response for the appropriate operating conditions. The standby current of the buck regulator is 140 μA for low-power mode.

The device has built-in protection features such as soft start, pulse-by-pulse current limit, thermal sensing, and shutdown due to excessive power dissipation.

## APPLICATION SCHEMATIC

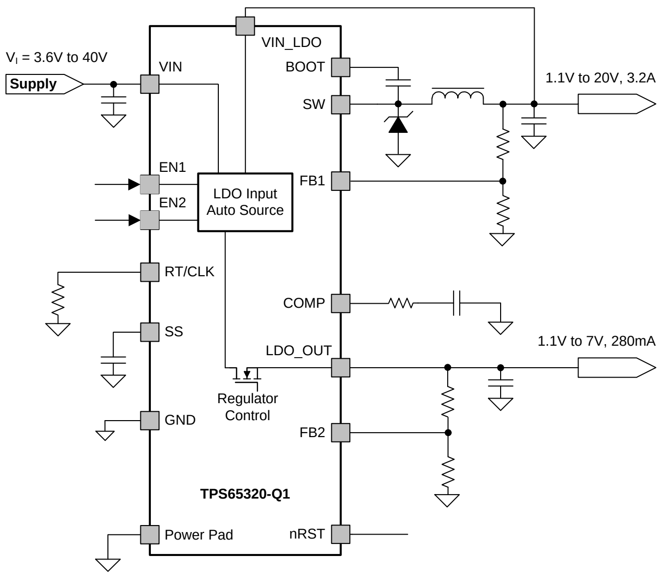



Figure 1. Typical Application Schematic

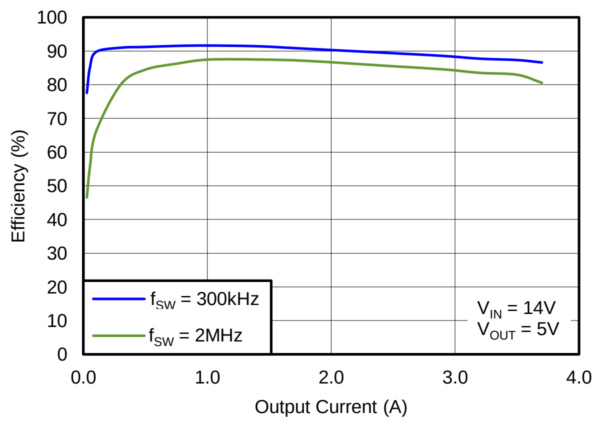



Figure 2. Buck Efficiency versus Output Current

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE AND ORDERING INFORMATION

For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

## ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

| | | | VALUE | UNIT |
|---|---|---|---|---|
| Supply inputs | VIN | | –0.3 to 45 | V |
| | VIN_LDO | | –0.3 to 20 | |
| Control | EN1, EN2 | | –0.3 to 45 | V |
| Buck converter | FB1 | | –0.3 to 3.6 | V |
| | SW | | –0.3 to 40<br>–2 V for 30 ns | |
| | BOOT | | –0.3 to 46 | |
| | BOOT-SW | | 8 | |
| | COMP | | –0.3 to 3.6 | |
| | SS | | –0.3 to 3.6 | |
| | RT/CLK, SS | | –0.3 to 3.6 | |
| LDO regulator | LDO_OUT | | –0.3 to 7 | V |
| | FB2 | | –0.3 to 7 | |
| | nRST | | –0.3 to 7 | |
| Electrostatic discharge (ESD) ratings | Human-body model (HBM) AEC-Q100 classification level H2 | | 2 | kV |
| | Charged-device model (CBM) AEC-Q100 classification level C3B | Corner pins | 750 | V |
| | | All other pins | 500 | |
| $T_A$ | Operating ambient temperature | | 125 | °C |
| $T_{stg}$ | Storage temperature range | | –55 to 165 | °C |
| $T_J$ | Operating junction temperature range | | –40 to 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## THERMAL INFORMATION

| THERMAL METRIC(1) | | TPS65320-Q1 | UNIT |
|---|---|---|---|
| | | PWP (14 PINS) | |
| $\theta_{JA}$ | Junction-to-ambient thermal resistance | 49.9 | °C/W |
| $\theta_{JCtop}$ | Junction-to-case (top) thermal resistance | 31 | |
| $\theta_{JB}$ | Junction-to-board thermal resistance | 26.6 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 1 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 26.4 | |
| $\theta_{JCbot}$ | Junction-to-case (bottom) thermal resistance | 3.7 | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

## RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Supply inputs | VIN | 3.6 | | 40 | V |
| | VIN_LDO | 3.6 | | 20 | |
| Buck regulator | BOOT1 | 3.6 | | 46 | V |
| | SW1 | –1 | | 40 | |
| | VFB1 | 0 | | 3 | |
| | SS | 0 | | 3 | |
| | COMP | 0 | | 3 | |
| | RT/CLK | 0 | | 3 | |
| LDO regulator | LDO_OUT | 1.1 | | 5.5 | V |
| | VFB2 | 0 | | 5.25 | |
| | nRST | 0 | | 5.25 | |
| Control | EN1 | 0 | | 40 | V |
| | EN2 | 0 | | 40 | |
| Temperature | Operating junction temperature range, $T_J$ | –40 | | 150 | °C |

## ELECTRICAL CHARACTERISTICS

$V_{IN}$ = 6 V to 27 V, EN1 = EN2 = $V_{IN}$, $T_J$ = –40°C to 150°C, unless otherwise noted

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **VIN (INPUT POWER SUPPLY)** | | | | | | |
| | Operating input voltage | Normal mode, after initial start-up | 3.6 | 14 | 40 | V |
| | Shutdown supply current | EN1 = EN2 = 0 V, 25°C | | 2 | 5 | µA |
| **ENABLE AND UVLO (EN1 AND EN2 PINS)** | | | | | | |
| | Enable low level | | | | 0.7 | V |
| | Enable high level | | 2.5 | | | V |
| $V_{IN}$ falling | Internal UVLO threshold | Ramp $V_{IN}$ down until output turns OFF | 2 | 2.6 | 3 | V |
| $V_{IN}$ rising | Internal UVLO threshold | Ramp $V_{IN}$ up until output turns ON | 2.5 | 2.8 | 3.2 | V |
| **BUCK CONVERTER** | | | | | | |
| | Operating: non-switching supply | VFB1 = 0.83 V, VIN = 12 V, 25°C | | 110 | 140 | µA |
| | Output capacitor | ESR = 0.001 Ω to 0.1 Ω, large output capacitance may be required for load transient | 10 | | | µF |
| **HIGH-SIDE MOSFET** | | | | | | |
| | On-resistance | $V_{IN}$ = 12 V, SW = 6 V | | 127 | 250 | mΩ |
| $t_{ON\text{-}min}$ | Minimum on-time | $f_{SW}$ = 2.5 MHz | | 100 | | ns |
| **ERROR AMPLIFIER** | | | | | | |
| | Input current | | | 50 | | nA |
| | Error-amplifier transconductance (gm) | –2 µA < $I_{COMP}$ < 2 µA, $V_{COMP}$ = 1 V | | 310 | | µS |
| | Error-amplifier transconductance (gm) during soft start | –2 µA < $I_{COMP}$ < 2 µA, $V_{COMP}$ = 1 V<br>$V_{FB1}$ = 0.4 V | | 70 | | µS |
| | Error-amplifier dc gain | $V_{FB1}$ = 0.8 V | | 100 | | dB |
| | Error-amplifier bandwidth | | | 6000 | | kHz |
| | Error-amplifier source or sink | $V_{COMP}$ = 1 V, 100-mV overdrive | | ±27 | | µA |
| | COMP to switch-current transconductance | | | 10.5 | | S |
| $V_{FB1}$ | Voltage reference | $V_{VIN\_LDO}$ = 3.6 V to 10 V | 0.788 | 0.8 | 0.812 | V |
| **CURRENT LIMIT** | | | | | | |
| | Current-limit threshold | $V_{IN}$ = 12 V, $T_J$ = 25°C | 4 | 6 | | A |

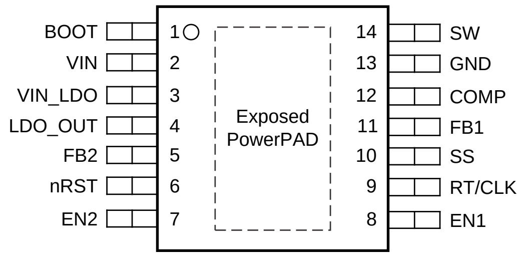
## ELECTRICAL CHARACTERISTICS (continued)

$V_{IN}$ = 6 V to 27 V, EN1 = EN2 = $V_{IN}$, $T_J$ = –40°C to 150°C, unless otherwise noted

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **TIMING RESISTOR AND EXTERNAL CLOCK (RT/CLK PIN)** | | | | | | |
| $f_{SW}$ | Switching-frequency range using RT mode | | 100 | | 2500 | kHz |
| | Switching frequency | RT = 200 kΩ | 450 | 581 | 720 | kHz |
| | Switching-frequency range using CLK mode | | 300 | | 2200 | kHz |
| | Minimum CLK input pulse width | | | 40 | | ns |
| RT/CLK | High threshold | | | 1.9 | 2.2 | V |
| | Low threshold | | 0.5 | 0.7 | | V |
| | Falling edge to SW rising edge delay | Measured at 500 kHz with RT resistor in series | | 60 | | ns |
| PLL | Lock-in time | Measured at 500 kHz | | 100 | | μs |
| **LDO** | | | | | | |
| $\Delta V_{LINE\text{-}REG}$ | Line regulation | $V_{IN}$ = 6 V to 30 V, $I_{OUT}$ = 10 mA, $V_{OUT}$ = 3.3 V | | | 20 | mV |
| $\Delta V_{LOAD\text{-}REG}$ | Load regulation | $I_{OUT}$ = 10 mA to 200 mA, $V_{IN}$ = 14 V, $V_{OUT}$ = 3.3 V | | | 35 | mV |
| $V_{DROPOUT}$ ($V_{IN} – V_{OUT}$) | Dropout voltage | $I_{OUT}$ = 200 mA | | 300 | 450 | mV |
| $I_{OUT}$ | Output current | $V_{OUT}$ in regulation | 0 | | 280 | mA |
| | Error-amplifier dc gain | | | 800 | | V/V |
| VIN_LDO | Operating input voltage on VIN_LDO pin | Buck regulator is in regulation and supplying at least LDO output voltage plus dropout voltage $V_{DROPOUT}$. | 4 | | 20 | V |
| $V_{FB2}$ | Voltage reference | $V_{LDO\_OUT}$ = 1 V to 5 V | 0.788 | 0.8 | 0.812 | V |
| $I_{CL}$ | Output current limit | $V_{OUT}$ = 0 V ($V_{OUT}$ pin is shorted to ground.) | 280 | | 1000 | mA |
| $I_{q\_LPM\_}$ | Quiescent current | EN1 = 0 V, EN2 = 5 V, $I_{OUT}$ = 0.01 mA to 0.75 mA | | 28 | 40 | μA |
| PSRR | Power supply ripple rejection | $V_{IN\text{-}RIPPLE}$ = 0.5 $V_{PP}$, $I_{OUT}$ = 200 mA, frequency = 100 Hz, $V_{OUT}$ = 5 V and $V_{OUT}$ = 3.3 V | | 60 | | dB |
| | | $V_{IN\text{-}RIPPLE}$ = 0.5 $V_{PP}$, $I_{OUT}$ = 200 mA, frequency = 150 kHz, $V_{OUT}$ = 5 V and $V_{OUT}$ = 3.3 V | | 30 | | dB |
| | Output capacitor | ESR = 0.001 Ω to 100 mΩ, large output capacitance may be required for load transient | 1 | | 40 | μF |
| **RESET (nRST PIN)** | | | | | | |
| | RESET threshold | LDO_OUT decreasing | 88% | 92% | 95% | |
| $V_{OH}$ | Output high | | –5% × $V_{ldo\_out}$ | | | V |
| $V_{OL}$ | Output low | Reset asserted due to falling LDO_OUT, $I_{OL}$ = 1 mA | 0 | 0.045 | 0.4 | V |
| | Filter time | Delay before asserting nRST low | 6 | 10 | 15 | μs |
| **SS (INTERNAL SOFT START TIMER FOR SWITCH MODE CONVERTER)** | | | | | | |
| $I_{SS}$ | Soft-start source current | SS = 0 V | | 2 | 4 | μA |
| $T_{SHUTDOWN}$ | Thermal-shutdown trip point | | | 170 | | ºC |
| $T_{hys}$ | Hysteresis | | | 10 | | ºC |

# PIN CONFIGURATION

**TPS65320-Q1**
**PWP-14 HTSSOP Package**
**(Top View)**




# PIN FUNCTIONS

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| BOOT | 1 | O | Boot node for LX |
| COMP | 12 | O | Buck error amplifier output to connect external compensation components |
| EN1 | 8 | I | Enable and disable input for buck converter (high-voltage tolerant) internally pulls to ground. Pull up externally to enable. |
| EN2 | 7 | I | Enable and disable input for LDO (high-voltage tolerant) internally pulls to ground. Pull up externally to enable. |
| FB1 | 11 | I | Remote sense input for buck converter, a resistor network connection between this pin and ground and this pin and buck converter output |
| FB2 | 5 | I | Remote sense input for LDO regulator, a resistor network connection between this pin and ground and this pin and LDO_OUT |
| GND | 13 | – | Ground |
| LDO_OUT | 4 | O | Linear regulator output |
| nRST | 6 | O | Active-low, push-pull reset output, asserted high (at the actual LDO output voltage) after the LDO of the device starts regulating |
| RT/CLK | 9 | I | External resistor connected to ground to program the internal oscillator. An alternative option is to feed an external clock to provide a reference for the switching frequency. |
| SS | 10 | I | External capacitor to ground to set the soft-start time |
| SW | 14 | I | Source node of internal switching FET |
| VIN | 2 | – | Input for internal supply and drain-node input for internal high-side MOSFET |
| VIN_LDO | 3 | – | Supply for LDO if Buck regulator is in regulation and supplying at least LDO output voltage plus dropout voltage $V_{DROPOUT}$. Otherwise, VIN is an internal LDO-supply. Do not connect VIN_LDO to VIN. |
| Exposed thermal pad | – | – | Electrically connect to ground and solder to the ground plane of the PCB for thermal efficiency. |

## TYPICAL CHARACTERISTICS

**BUCK CONVERTER LOAD TRANSIENT TEST (5 V / 2 MHz)**

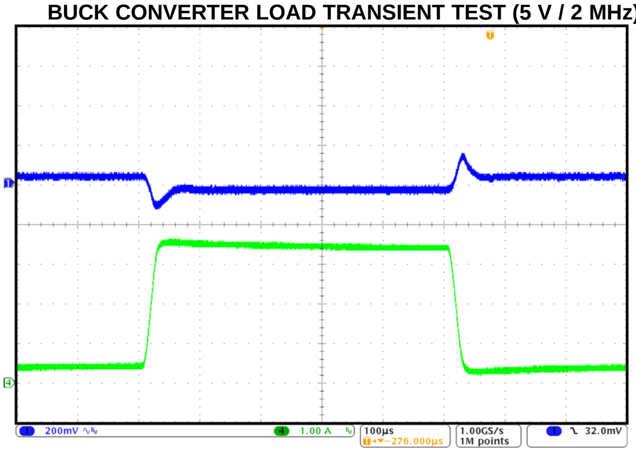



Figure 3.

**BUCK CONVERTER START-UP OPERATION**

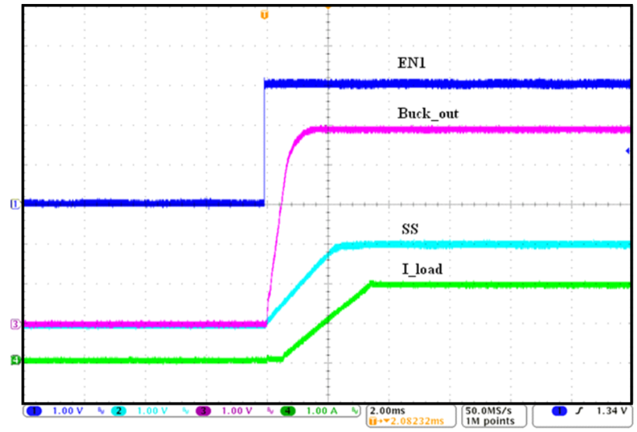



Figure 4.

**BUCK $V_{OUT}$ OUTPUT VOLTAGE**

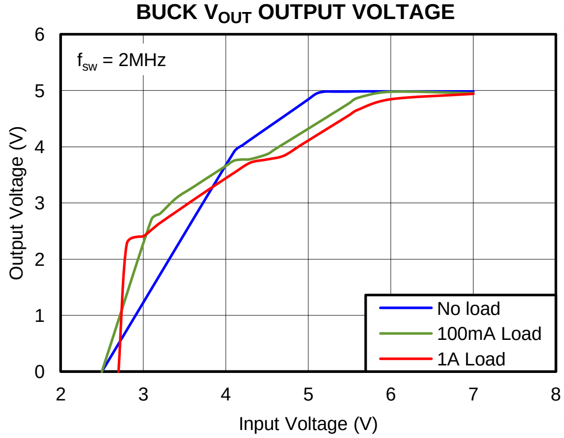



Figure 5.

**SWITCHING FREQUENCY versus $V_{FB1}$**

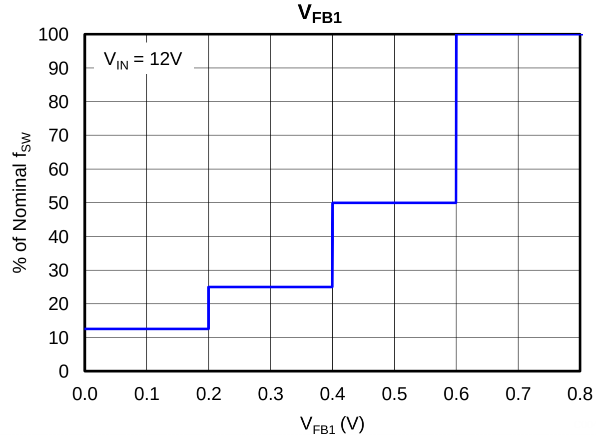



Figure 6.

**SWITCHING FREQUENCY versus RT/CLK RESISTANCE**

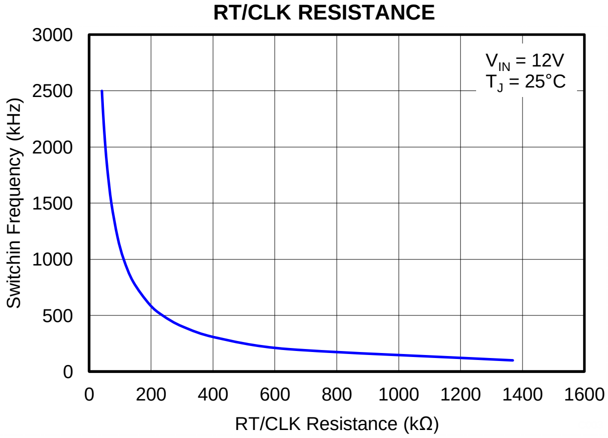



Figure 7.

**BUCK VOLTAGE REFERENCE versus JUNCTION TEMPERATURE**

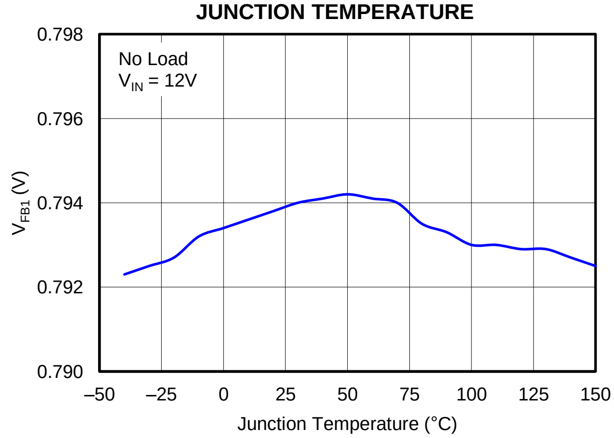



Figure 8.

## TYPICAL CHARACTERISTICS (continued)

LDO LOAD REGULATION

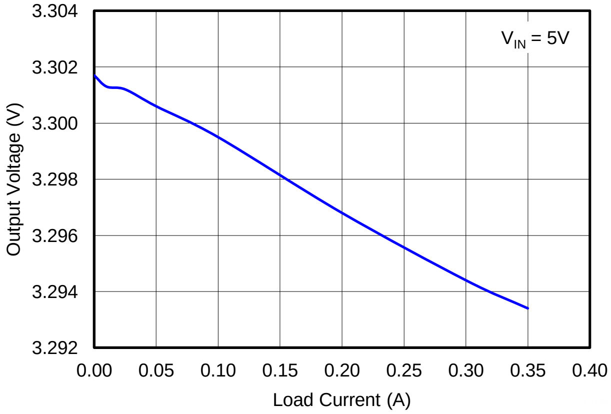



**Figure 9.**

LDO DROPOUT VOLTAGE

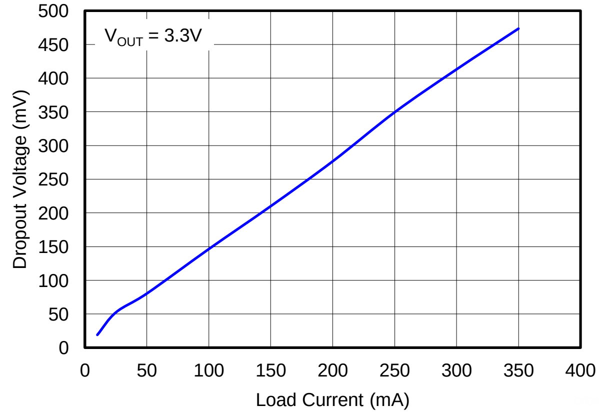



**Figure 10.**

LDO START-UP OPERATION

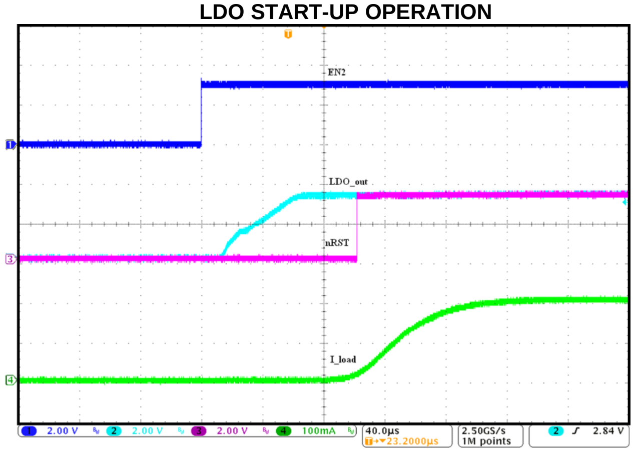



**Figure 11.**

LDO LOAD TRANSIENT (50 mA to 300 mA)

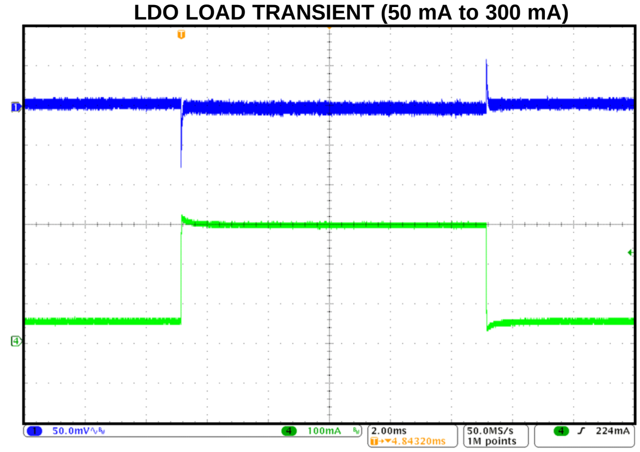



**Figure 12.**

LDO VOLTAGE REFERENCE
vs
JUNCTION TEMPERATURE

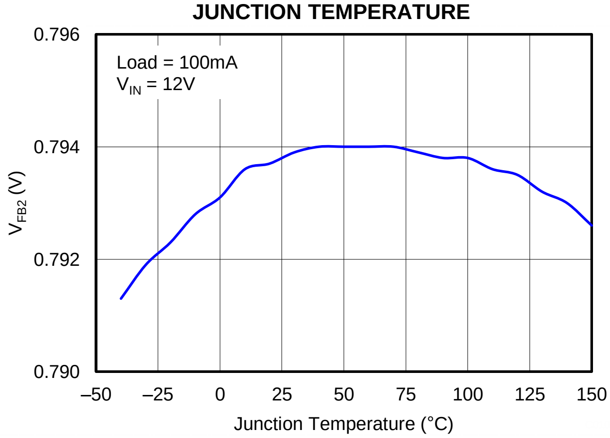



**Figure 13.**

## INTERNAL FUNCTIONAL BLOCKS

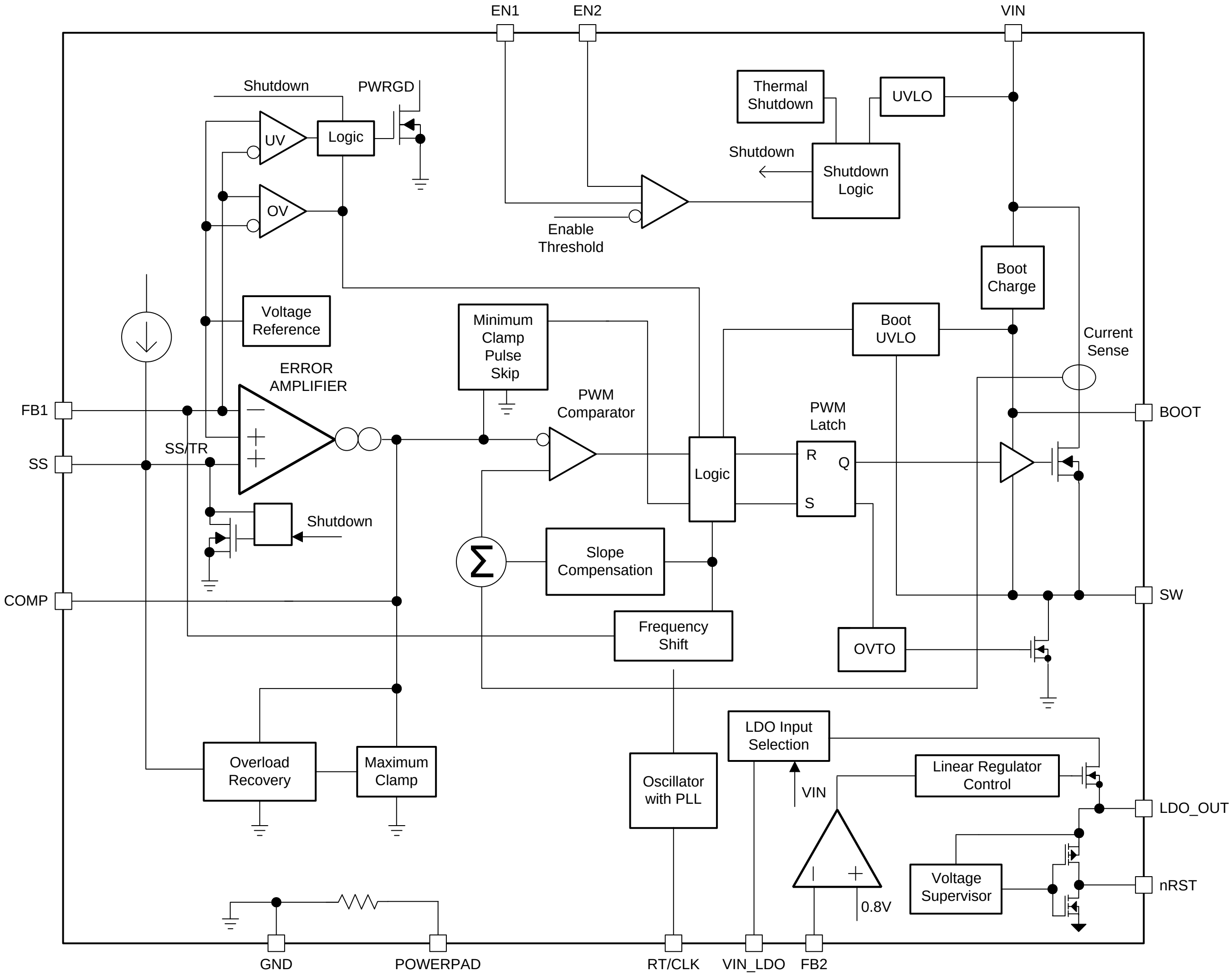



**Figure 14. Functional Block Diagram**

## DETAILED DESCRIPTION

The TPS65320-Q1 device is a 40-V, 3.2-A, step-down (buck) converter with a 280-mA LDO linear regulator. These two regulators both have low quiescent consumption during a light load to prolong the battery life.

The buck converter improves performance during line and load transients by implementing a constant-frequency and current-mode control which reduces output capacitance, simplifying external frequency-compensation design. The wide switching frequency of 100 kHz to 2500 kHz allows for efficiency and size optimization when selecting the output-filter components. One can adjust the switching frequency by using a resistor to ground on the RT/CLK pin. The buck converter has an internal phase-locked loop (PLL) on the RT/CLK pin that synchronizes the power switch turnon to the falling edge of an external system clock.

The TPS65320-Q1 reduces the external component count by integrating the boot recharge diode. A capacitor between the BOOT and SW pins supplies the bias voltage for the integrated high-side MOSFET. An undervoltage lockout (UVLO) circuit monitors the boot capacitor voltage and turns the high-side MOSFET off when the boot voltage falls below a preset threshold. The TPS65320-Q1 can operate at high duty cycles because of the boot UVLO. One can step the output voltage down to as low as the 0.8-V reference. Soft start is featured to minimize inrush currents or to provide power-supply sequencing during power up. Connect a small-value capacitor to the pin to adjust the soft-start time. One can couple a resistor divider to the pin for critical power-supply sequencing requirements.

The LDO regulator only consumes about 40-µA current in light load. The LDO can also track the battery when battery voltage is low (in a cold-crank condition). The input of the LDO has a unique feature; it can auto source the input supply from either the buck output or the battery. If both the buck and LDO are enabled, the device switches the input of the LDO to the output of the buck to reduce heat. With the buck disabled or the buck output voltage out of regulation ($V_{FB1}$ less than 91% of $V_{REF}$), the device switches the LDO input automatically to the input voltage.

The LDO of the TPS65320-Q1 device has a power-good comparator (nRST) that asserts when the regulated output voltage is less than 91% of the nominal output voltage.

### Buck Converter

#### Fixed-Frequency PWM Control

The TPS65320-Q1 uses an adjustable, fixed-frequency peak current mode control. Use of external resistors on the VFB1 pin compares the output voltage to an internal voltage reference through an error amplifier that drives the COMP pin. An internal oscillator initiates the turnon of the high-side power switch. The device compares the error amplifier output to the high-side power-switch current. When the power switch current reaches the level set by the COMP voltage, the power switch turns off. The COMP pin voltage increases and decreases as the output current increases and decreases. The device implements a current limit by clamping the COMP pin voltage to a maximum level.

#### Slope Compensation Output

The TPS65320-Q1 adds a compensating ramp to the switch current signal. This slope compensation prevents sub-harmonic oscillations. The available peak inductor current remains constant over the full duty-cycle range.

#### Pulse-Skip Eco-mode™ Control Scheme

The TPS65320-Q1 operates in a pulse-skip mode at light load currents to improve efficiency by reducing switching and gate drive losses. Design of the TPS65320-Q1 is such that if the output voltage is within regulation and the peak switch current at the end of any switching cycle is below the pulse-skipping-current threshold, the device enters pulse-skip mode. This current threshold is the current level corresponding to a nominal COMP voltage, or 720 mV. The current at which entry to the pulse-skip mode occurs depends on switching frequency, inductor choice, output-capacitor selection, and compensation network.

When in pulse-skip mode, the device clamps the COMP pin voltage at 720 mV, inhibiting the high-side MOSFET. Further decreases in load current or in output voltage cannot drive the COMP pin below this clamp-voltage level.

Because the device is not switching, the output voltage begins to decay. As the voltage control loop compensates for the falling output voltage, the COMP pin voltage begins to rise. At this time, the high-side MOSFET turns on and a switching pulse initiates on the next switching cycle. The peak current is set by the COMP pin voltage. The output current recharges the output capacitor to the nominal voltage, then the peak switch current starts to decrease, and eventually falls below the pulse-skip-mode threshold, at which time the device enters Eco-mode again.

For pulse-skip-mode operation, the TPS65320-Q1 senses peak current, not average or load current. Therefore, the load current where the device enters pulse-skip mode is dependent on the output inductor value. When the load current is low and the output voltage is within regulation, the device enters a sleep mode and draws only 140-µA input quiescent current. The internal PLL remains operating when the device is in sleep mode.

### Low Dropout Operation and Bootstrap Voltage (BOOT)

The TPS65320-Q1 has an integrated boot regulator and requires a small ceramic capacitor between the BOOT and SW pins to provide the gate-drive voltage for the high-side MOSFET. The BOOT capacitor recharges when the high-side MOSFET is off and the low-side diode conducts. The value of this ceramic capacitor should be 0.1 µF. TI recommends a ceramic capacitor with an X7R or X5R grade dielectric and a voltage rating of 10 V or higher because of the stable characteristics over temperature and voltage.

To improve drop out, the TPS65320-Q1 operates at 100% duty cycle as long as the BOOT to SW pin voltage is greater than 2.1 V. When the voltage from BOOT to SW drops below 2.1 V, the high-side MOSFET turns off using a UVLO circuit, which allows the low-side diode to conduct and refresh the charge on the BOOT capacitor. Because the supply current sourced from the BOOT capacitor is low, the high-side MOSFET can remain on for more switching cycles than are required to refresh the capacitor, and therefore the effective duty cycle of the switching regulator is high.

Voltage drops across the power MOSFET, inductor resistance, low-side diode, and printed circuit board resistance are the main influence on the effective duty cycle during dropout of the regulator. During operating conditions in which the input voltage drops and the regulator is operating in continuous conduction mode, the high-side MOSFET can remain on for 100% of the duty cycle to maintain output regulation until the BOOT to SW voltage falls below 2.1 V.

Pay attention in maximum-duty-cycle applications which experience extended time periods with light loads or no load. When the voltage across the BOOT capacitor falls below the 2.1-V UVLO threshold, the high-side MOSFET turns off, but there may not be enough inductor current to pull the SW pin down to recharge the BOOT capacitor. The high-side MOSFET of the regulator stops switching because the voltage across the BOOT capacitor is less than 2.1 V. The output capacitor then decays until the difference in the input voltage and output voltage is greater than 2.1 V, which exceeds the BOOT UVLO threshold, and the device starts switching again until reaching the desired output voltage. This operating condition persists until the input voltage and/or the load current increases. When TPS65320-Q1 tries to turn on the high-side MOSFET continuously during the high-side off state, the internal small low-side MOSFET turns on for a short time to charge the BOOT capacitor. Then the SW node pulls low to recharge the BOOT capacitor for maximum-duty-cycle operation.

### Error Amplifier

The buck converter of the TPS65320-Q1 has a transconductance amplifier for the error amplifier. The error amplifier compares the VFB1 voltage to the lower of the internal soft-start (SS) voltage or the internal 0.8-V voltage reference. The transconductance (gm) of the error amplifier is 310 µS during normal operation. During the soft-start operation, the transconductance is a fraction of the normal operating gm. When the voltage of the VFB1 pin is below 0.8 V and the device is regulating using internal SS voltage, the gm is 70 µS. The frequency-compensation components (capacitor, series resistor, and capacitor) are added to the COMP pin to ground.

### Voltage Reference

The voltage reference system produces a precise ±2% voltage reference over temperature by scaling the output of a temperature stable band-gap circuit.

### Slow-Start/Tracking Pin (SS/TR)

The TPS65320-Q1 effectively uses the lower voltage of the internal voltage reference or the SS/TR pin voltage as the reference voltage of the power supply and regulates the output accordingly. A capacitor on the SS/TR pin to ground implements a slow-start time. The TPS65320-Q1 has an internal pullup current source of 2 µA that charges the external slow-start capacitor. Equation 1 shows the calculations for the slow start time (10% to 90%). The voltage reference ($V_{REF}$) is 0.8 V and the slow-start current ($I_{SS}$) is 2 µA. The slow-start capacitor should remain lower than 0.47 µF and greater than 0.47 nF.

$$C_{ss}(nF) = \frac{T_{ss}(ms) \times I_{ss}(\mu A)}{V_{ref}(V) \times 0.8} \tag{1}$$

At power up, the TPS65320-Q1 does not start switching until the slow-start pin discharges to less than 40 mV to ensure a proper power up.

Also, on exceeding the $V_{IN}$ UVLO, pulling the EN pin below the enable threshold, or the occurrence a thermal shutdown event during normal operation, the TPS65320-Q1 stops switching, which requires discharging the SS/TR pin to 40 mV.

### Overload Recovery Circuit

The TPS65320-Q1 has an overload recovery (OLR) circuit. The OLR circuit slow-starts the output from the overload voltage to the nominal regulation voltage on removal of the fault condition. The OLR circuit discharges the SS/TR pin to a voltage slightly greater than the VFB1 pin voltage using an internal pulldown of 382 µA when the error amplifier changes to a high voltage from a fault condition. On removal of the fault condition, the output slow-starts from the fault voltage to nominal output voltage.

### Constant Switching Frequency and Timing Resistor (RT/CLK Pin)

The switching frequency of the TPS65320-Q1 is adjustable over a wide range from approximately 100 kHz to 2500 kHz by placing a resistor on the RT/CLK pin. The RT/CLK pin voltage is typically 0.5 V and must have a resistor to ground to set the switching frequency. To determine the timing resistance for a given switching frequency, use Equation 2 or the curves in Figure 6. To reduce the solution size, the user typically sets the switching frequency as high as possible, but consider tradeoffs of the supply efficiency, maximum input voltage, and minimum controllable on-time. The minimum controllable on-time is typically 100 ns and limits the maximum operating input voltage. The frequency-shift circuit also limits the maximum switching frequency. The following sections discuss more details of the maximum switching frequency.

$$R_T(k\Omega) = \frac{206033}{f_{sw}(kHz)^{1.0888}} \tag{2}$$

### Overcurrent Protection and Frequency Shift

The TPS65320-Q1 implements current mode control, which uses the COMP pin voltage to turn off the high-side MOSFET on a cycle-by-cycle basis. During each cycle, the switch current and COMP pin voltage are compared. When the peak switch current intersects the COMP voltage, the high-side switch turns off. During overcurrent conditions that pull the output voltage low, the error amplifier responds by driving the COMP pin high, increasing the switch current. Internal clamping of the error-amplifier output functions as a switch-current limit.

The TPS65320-Q1 implements a frequency shift. The switching frequency is divided by 8, 4, 2, and 1 as the voltage ramps from 0 to 0.8 volts on the VFB1 pin. During short-circuit events (particularly with high-input-voltage applications), the control loop has a finite minimum controllable on-time, and the output has a low voltage. During the switch on-time, the inductor current ramps to the peak current limit because of the high input voltage and minimum on-time. During the switch off-time, the inductor would normally not have enough off-time and output voltage for the inductor to ramp down by the ramp-up amount. The frequency shift effectively increases the off-time, allowing the current to ramp down.

### Selecting the Switching Frequency

The switching frequency that is selected should be the lower value of the two equations, Equation 3 and Equation 4. Equation 3 is the maximum switching frequency limitation set by the minimum controllable on-time. Setting the switching frequency above this value causes the regulator to skip switching pulses. The device maintains regulation, but pulse-skipping leads to high inductor current and a significant increase in output ripple voltage.

Equation 4 is the maximum switching frequency limit set by the frequency-shift protection. To have adequate output short-circuit protection at high input voltages, set the switching frequency should be set be less than the $f_{sw}$ (maxshift) frequency. In Equation 4, to calculate the maximum switching frequency one must take into account that the output voltage decreases from the nominal voltage to 0 volts, and the $f_{div}$ integer increases from 1 to 8 corresponding to the frequency shift.

In Figure 15, the solid line illustrates a typical safe operating area regarding frequency shift and assumes the output voltage is zero volts, the resistance of the inductor is 0.130 Ω, the FET on-resistance is 0.127 Ω, and the diode voltage drop is 0.5 V. The dashed line is the maximum switching frequency to avoid pulse skipping.

$$f_{SW}(\text{max skip}) = \left(\frac{1}{t_{ON}}\right) \times \left(\frac{(I_L \times R_{dc} + V_{out} + V_d)}{(V_{in} - I_L \times R_{hs} + V_d)}\right) \tag{3}$$

$$f_{SW}(\text{shift}) = \left(\frac{f_{div}}{t_{ON}}\right) \times \left(\frac{(I_L \times R_{dc} + V_{outsc} + V_d)}{(V_{in} - I_L \times R_{hs} + V_d)}\right) \tag{4}$$

where:

- $I_L$ = inductor current
- $R_{DC}$ = inductor resistance
- $V_{IN}$ = maximum input voltage
- $V_{OUT}$ = output voltage
- $V_{OUTSC}$ = output voltage during short
- $V_d$ = diode voltage drop
- $R_{hs}$ = FET on resistance (typ. 127 mΩ)
- $t_{ON}$ = controllable on-time (typ. 100 ns)
- $f_{div}$ = frequency divide factor (equals 1, 2, 4 or 8)

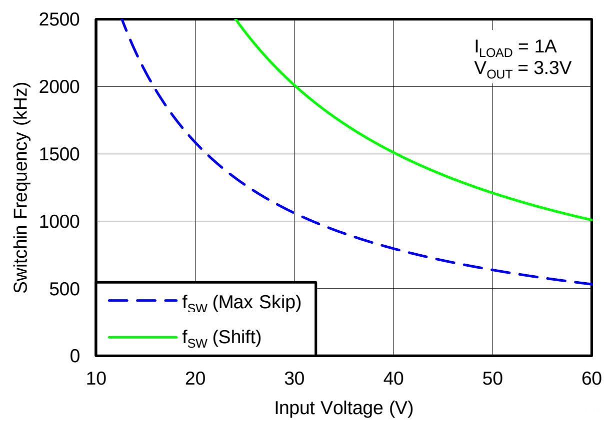



**Figure 15. Maximum Switching Frequency versus Input Voltage**

### How to Interface to RT/CLK Pin

One can use the RT/CLK pin to synchronize the regulator to an external system clock. To implement the synchronization feature, connect a square wave to the RT/CLK pin through the circuit network shown in Figure 16. The square-wave amplitude must transition lower than 0.5 V and higher than 2.2 V on the RT/CLK pin and have an on-time greater than 40 ns and an off-time greater than 40 ns. The synchronization frequency range is 300 kHz to 2200 kHz. The rising edge of SW is synchronizes with the falling edge of RT/CLK pin signal. Design the external synchronization circuit n such a way that the device has the default frequency-set resistor connected from the RT/CLK pin to ground should the synchronization signal turn off. TI recommendes using a frequency-set resistor connected as shown in Figure 16 through a 50-Ω resistor to ground. The resistor should set the switching frequency close to the external CLK frequency. TI also recommends ac-coupling the synchronization signal through a 10-pF ceramic capacitor to the RT/CLK pin and a 4-kΩ series resistor. The series resistor reduces SW jitter in heavy-load applications when synchronizing to an external clock, and in applications which transition from synchronizing to RT mode. The first time CLK is pulled above the CLK threshold, the device switches from the RT resistor frequency to PLL mode. Along with the resulting removal of the internal 0.5-V voltage source, the CLK pin becomes high-impedance as the PLL starts to lock onto the external signal. Because there is a PLL on the regulator, the switching frequency can be higher or lower than the frequency set with the external resistor. The device transitions from the resistor mode to the PLL mode and then increases or decreases the switching frequency until the PLL locks onto the CLK frequency within 100 microseconds.

When the device transitions from the PLL mode to the resistor mode, the switching frequency slows down from the CLK frequency to 150 kHz, then reapplies the 0.5-V voltage, and the resistor then sets the switching frequency. The switching-frequency divisor changes to 8, 4, 2, and 1 as the voltage ramps from 0 to 0.8 volts on the FB1 pin. The device implements a digital frequency shift to enable synchronizing to an external clock during normal start-up and fault conditions.

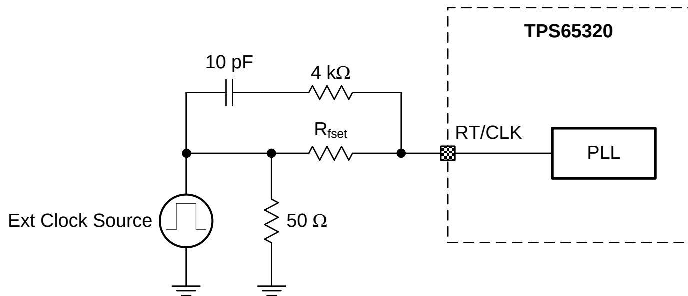



**Figure 16. Synchronizing to a System Clock**

### Enable and Undervoltage Lockout

TPS65320-Q1 enables are high-voltage-tolerant input pins with an internal pulldown circuit. A high input activates the device and turns the regulators ON.

TPS65320-Q1 has an internal UVLO circuit to shut down the output if the input voltage falls below an internally fixed UVLO threshold level. This ensures that both regulators are not latched into an unknown state during low-input-voltage conditions. The regulators power up when the input voltage exceeds the voltage level.

### Overvoltage Transient Protection

The TPS65320-Q1 incorporates an overvoltage transient protection (OVTP) circuit to minimize voltage overshoot when recovering from output fault conditions or strong unload transients on power-supply designs with low-value output capacitance. For example, with the power-supply output overloaded, the error amplifier compares the actual output voltage to the internal reference voltage. If the FB1 pin voltage is lower than the internal reference voltage for a considerable time, the output of the error amplifier responds by clamping the error amplifier output to a high voltage, thus requesting the maximum output current. On removal of the condition, the regulator output rises and the error-amplifier output transitions to the steady-state duty cycle. In some applications, the power-supply output voltage can respond faster than the error-amplifier output can respond; this actuality leads to the possibility of an output overshoot. The OVTP feature minimizes the output overshoot when using a low-value output capacitor by implementing a circuit to compare the FB1 pin voltage to the OVTP threshold (which is 109% of the internal voltage reference). The FB1 pin voltage going higher than the OVTP threshold disables the high-side MOSFET, preventing current from flowing to the output and minimizing output overshoot. The FB1 voltage dropping lower than the OVTP threshold allows the high-side MOSFET to turn on at the next clock cycle.

### Small-Signal Model for Loop Response

Figure 17 shows an equivalent model for the TPS65320-Q1 control loop which one can model in a circuit-simulation program to check frequency response and dynamic load response. The error amplifier is a transconductance amplifier with a $gm_{ea}$ of 310 µS. One can model the error amplifier using an ideal voltage-controlled current source. Resistor $R_o$ and capacitor $C_o$ model the open-loop gain and frequency response of the amplifier. The 1-mV ac voltage source between nodes a and b effectively breaks the control loop for the frequency-response measurements. Plotting c versus a shows the small signal response of the frequency compensation. Plotting a versus b shows the small signal response of the overall loop. Check the dynamic loop response by replacing $R_L$ with a current source that has the appropriate load-step amplitude and step rate in a time-domain analysis. This equivalent model is only valid for continuous-conduction-mode designs.

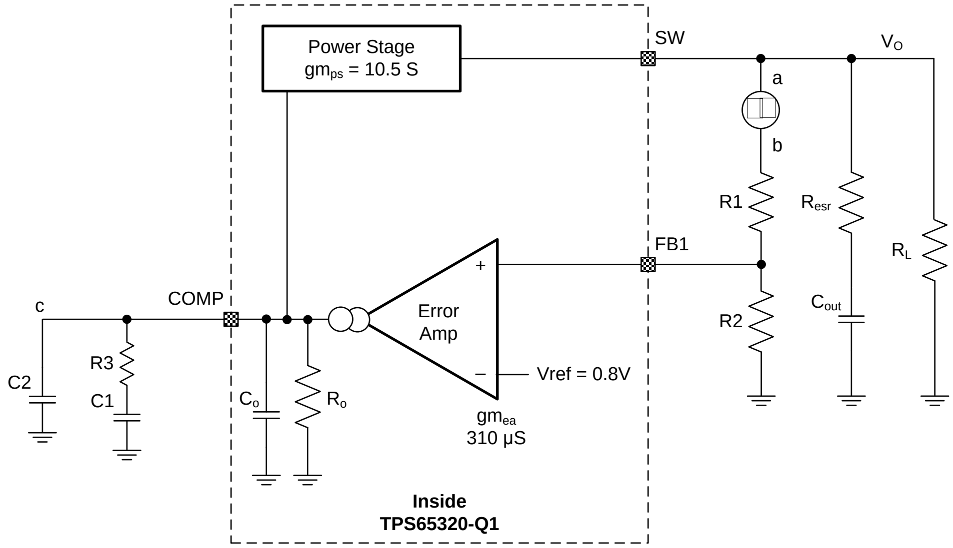



**Figure 17. Small-Signal Model for Loop Response**

## Simple Small-Signal Model for Peak-Current Mode Control

Figure 18 describes a simple small-signal model that one can use to understand how to design the frequency compensation. A voltage-controlled current source (duty cycle modulator) supplying current to the output capacitor and load resistor can approximate the TPS65320-Q1 power stage. Equation 5 shows the control-to-output transfer function, which consists of a dc gain, one dominant pole, and one ESR zero. The quotient of the change in switch current divided by the change in COMP pin voltage (node c in Figure 17) is the power-stage transconductance. The $gm_{PS}$ for the TPS65320-Q1 is 10.5 S. The low-frequency gain of the power stage is the product of the transconductance and the load resistance as shown in Equation 6.

As the load current increases and decreases, the low-frequency gain decreases and increases, respectively. This variation with the load may seem problematic at first, but the dominant pole moves with the load current (see Equation 7). The dashed line in the right half of Figure 18 highlights the combined effect. As the load current decreases, the gain increases and the pole frequency lowers, keeping the 0-dB crossover frequency the same for the varying load conditions, which makes it easier to design the frequency compensation. The type of output capacitor chosen determines whether the ESR zero has a profound effect on the frequency compensation design. Using high-ESR aluminium electrolytic capacitors may reduce the number of frequency-compensation components needed to stabilize the overall loop because the phase margin increases from the ESR zero at the lower frequencies (see Equation 8).

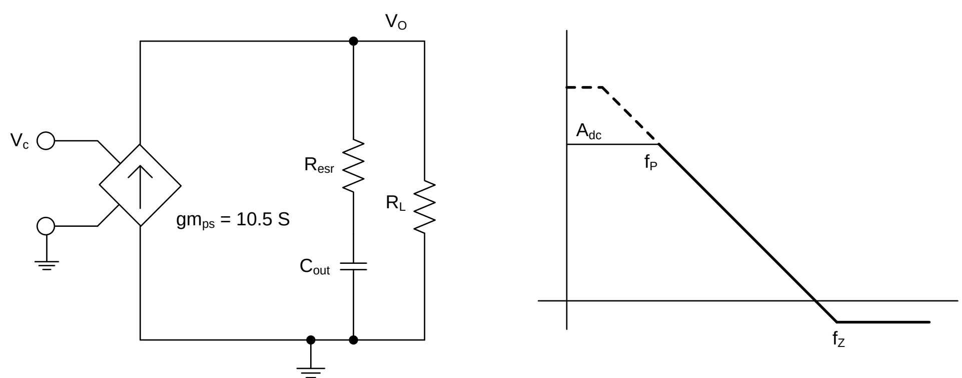



**Figure 18. Simple Small-Signal Model and Frequency Response for Peak-Current Mode**

$$\frac{V_{out}}{V_C} = A_{dc} \times \frac{\left(1 + \frac{s}{2\pi \times f_Z}\right)}{\left(1 + \frac{s}{2\pi \times f_P}\right)} \quad (5)$$

$$A_{dc} = gm_{ps} \times R_L \quad (6)$$

$$f_{P\_mod} = \frac{1}{2\pi \times R_L \times C_{out}} \quad (7)$$

$$f_{Z\_mod} = \frac{1}{2\pi \times R_{ESR} \times C_{out}} \quad (8)$$

### Small-Signal Model for Frequency Compensation

The buck converter of the TPS65320-Q1 device uses a transconductance amplifier for the error amplifier. Figure 19 shows compensation circuits. Implementation of Type 2 circuits is most likely in high-bandwidth power-supply designs. The purpose of loop compensation is to ensure stable operation while maximizing dynamic performance. Use of the Type 1 circuit is with power-supply designs that have high-ESR aluminum electrolytic or tantalum capacitors. Equation 9 and Equation 10 show how to relate the frequency response of the amplifier to the small-signal model in Figure 19. Modeling of the open-loop gain and bandwidth uses the $R_o$ and $C_o$ shown in Figure 19. See the Application Information section for a design example with a Type 2A network that has a low-ESR output capacitor. For stability purposes, the target is to have a loop-gain slope that is –20 dB/decade at the crossover frequency. Also, the crossover frequency should not exceed one-fifth of the switching frequency (120 kHz in the case of a 600-kHz switching frequency).

For dynamic purposes, the higher the bandwidth, the faster the load-transient response. A large dc gain means high dc regulation accuracy (dc voltage changes little with load or line variations). To achieve this loop gain, set the compensation components according to the shape of the control-output bode plot.

Equation 9 through Equation 19 serve as a reference to calculate the compensation components. $R_o$ and C1 form the dominant pole (P1). A resistor (R3) and a capacitor (C1) in series to ground work as zero (Z1). In addition, one can add a lower-value capacitor (C2) in parallel with R3 to work as an optional pole. This capacitor can be used to filter noise at switching frequency, and it is also needed if the output capacitor has high ESR.

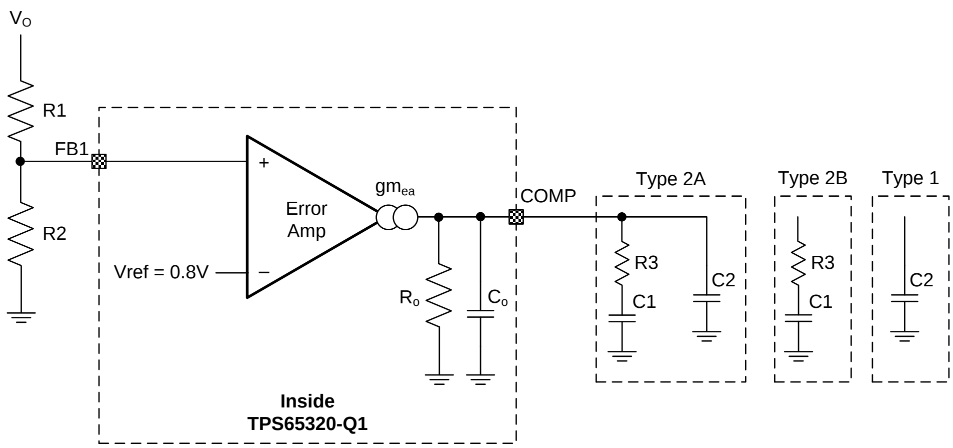



**Figure 19. Types of Frequency Compensation**

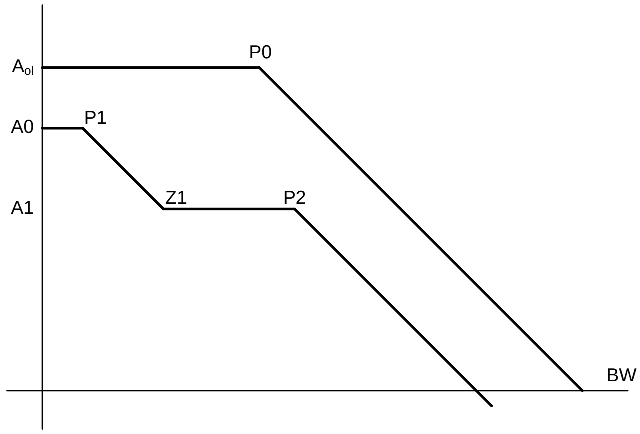



**Figure 20. Frequency Response of the Type 2 Frequency Compensation**

$$R_o = \frac{A_{ol}\ (V/V)}{gm_{ea}} \quad (9)$$

$$C_o = \frac{gm_{ea}}{2\pi \times BW(Hz)} \quad (10)$$

$$P0 = \frac{1}{2\pi \times R_o \times C0} \quad (11)$$

$$EA = A0 \times \frac{\left(1 + \frac{2}{2\pi \times f_{Z1}}\right)}{\left(1 + \frac{2}{2\pi \times f_{P1}}\right) \times \left(1 + \frac{2}{2\pi \times f_{P2}}\right)} \quad (12)$$

$$A0 = gm_{ea} \times R_o \times \frac{R2}{R1 + R2} \quad (13)$$

$$A1 = gm_{ea} \times R_o \,||\, R3 \times \frac{R2}{R1 + R2} \quad (14)$$

$$P1 = \frac{1}{2\pi \times R_o \times C1} \quad (15)$$

$$Z1 = \frac{1}{2\pi \times R3 \times C1} \quad (16)$$

$$P2 = \frac{1}{2\pi \times R3 \times C2} \quad \text{Type 2A} \quad (17)$$

$$P2 = \frac{1}{2\pi \times R3 \times C_O} \quad \text{Type 2B} \quad (18)$$

$$P2 = \frac{1}{2\pi \times R_O \times C2} \quad \text{Type 1} \quad (19)$$

## LDO Regulator

For the TPS65320-Q1 device, the design of the internal linear regulator is for low power consumption and quiescent current about 40 µA in light-load applications.

### Charge-Pump Operation

The LDO has an internal charge pump which turns on or off depending on the input voltage. The charge-pump switching circuitry does not cause conducted emissions to exceed required thresholds on the input voltage line. The charge-pump switching thresholds are hysteretic. Figure 21 shows the typical switching thresholds for the charge pump.

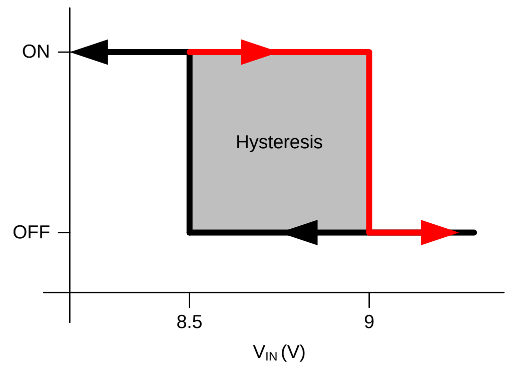



**Figure 21. Charge-Pump Switching Thresholds**

**Table 1. Typical Quiescent Current Consumption**

| | Charge Pump ON | Charge Pump OFF |
|---|---|---|
| LDO $I_q$ | 300 µA | 40 µA |

### Low-Voltage Tracking

At low input voltages, the regulator drops out of regulation, and the output voltage tracks input minus a voltage based on the load current ($I_{OUT}$) and switch resistance ($R_{SW}$). This feature allows for a smaller input capacitor and can possibly eliminate the need to use a boost convertor during cold-crank conditions.

### Power-Good Output, nRST

The nRST pin is a push-pull output. The power-on-reset output asserts low until the output voltage on LDO_OUT exceeds the setting thresholds (91%) and the deglitch timer has expired. Additionally, whenever the EN2 pin is low or open, nRST immediately asserts low regardless of the output voltage. If a thermal shutdown occurs due to excessive thermal conditions, this pin also asserts low.

### Thermal Shutdown

The device implements an internal thermal shutdown to protect itself if the junction temperature exceeds 170°C (typical). The thermal shutdown forces the device to stop switching when the junction temperature exceeds the thermal trip threshold. Once the junction temperature decreases below 160°C (typical), the device re-initiates the power-up sequence.

### Modes of Operation

The device has two hardware enable pins, and one can turn off either the buck or the LDO by pulling the enable pin low, as listed in Table 2. One unique feature of the TPS65320-Q1 device is the input auto source of the LDO. With both the buck and the LDO enabled, the LDO gets input from the output of the buck through the VIN_LDO pin. In this mode, the buck output voltage must be higher than the LDO output voltage. With the buck disabled and the LDO still enabled, the input of the LDO changes automatically from VIN_LDO to VIN. This is helpful for standby operations which need a very low standby current, such as automotive infotainment, telematics, and so on. The LDO changes its input when the buck output voltage is out of regulation ($V_{FB1}$ is less than 91% of $V_{REF1}$).

**Table 2. Device Operation Modes**

| Buck | LDO | Description |
|---|---|---|
| EN1 | EN2 | |
| 0 | 0 | Both buck and LDO disabled |
| 0 | 1 | Buck disabled. LDO enabled and LDO input source is from the battery. |
| 1 | 0 | Buck enabled and LDO disabled |
| 1 | 1 | Both buck and LDO enabled and LDO input source is from buck output. Buck output voltage must be higher than LDO output voltage. |

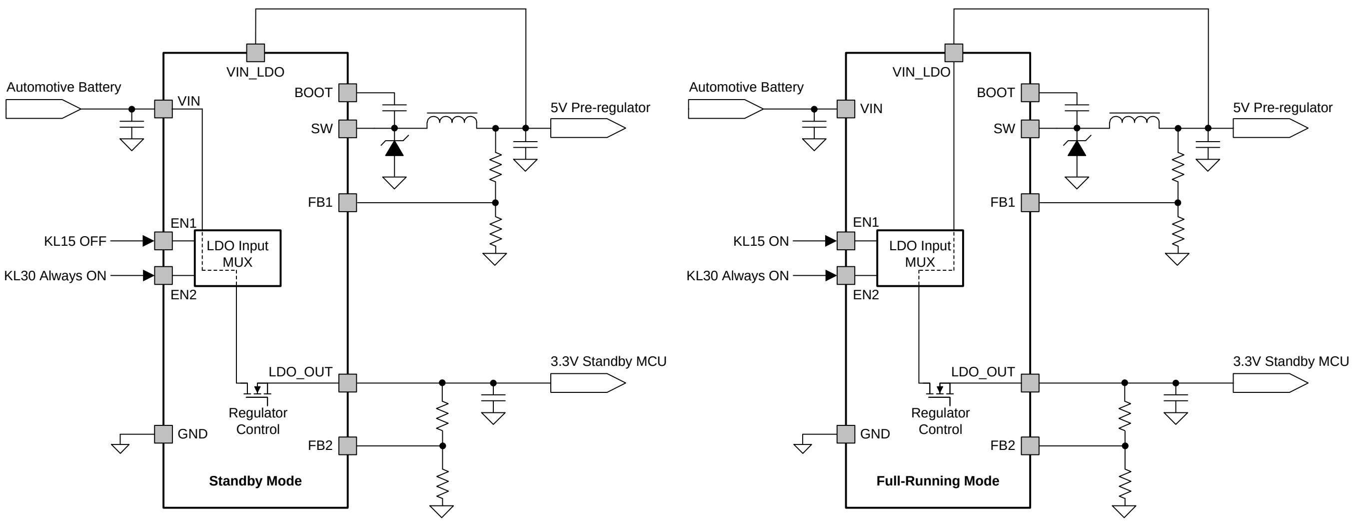



**Figure 22. Example of LDO Auto Source in Standby Condition**

# APPLICATION INFORMATION

## Design Guide – Step By Step Design Procedure

This example details the design of a high-frequency switching regulator and linear regulator using ceramic output capacitors. A few parameters must be known in order to start the design process. Determination of these parameters is typically t the system level. This example starts with the following known parameters (buck converter first):

| | |
|---|---|
| Input voltage, VIN1 | 9 V to 16 V, typical 12 V |
| Output voltage, VREG1 (buck regulator) | 5 V ± 2% |
| Maximum output current $I_{O\_max1}$ | 3 A |
| Minimum output current $I_{O\_min1}$ | 0.01 A |
| Transient response 0.01 A to 0.8 A | 3% |
| Output ripple voltage | 1% |
| Switching frequency $f_{SW}$ | 2.2 MHz |
| Output voltage, VREG2 (LDO regulator) | 3.3 V ± 2% |
| Overvoltage threshold | 106% of output voltage |
| Undervoltage threshold | 91% of output voltage |

## Selecting the Switching Frequency

The first step is to decide on a switching frequency for the regulator. Typically, the user chooses the highest switching frequency possible because this produces the smallest solution size. The high switching frequency allows for lower-valued inductors and smaller output capacitors compared to a power supply that switches at a lower frequency. The selectable switching frequency is limited by the minimum on-time of the internal power switch, the input voltage, the output voltage, and the frequency-shift limitation.

Consider minimum on-time and frequency-shift protection as described in Equation 3 and Equation 4. To find the maximum switching frequency for the regulator, choose the lower value of the two results. Switching frequencies higher than these values result in pulse skipping or the lack of overcurrent protection during a short circuit. The typical minimum on-time, $t_{onmin}$, is 100 ns for the TPS65320-Q1 device. For this example, where the output voltage is 5 V and the maximum input voltage is 16 V, use a switching frequency of 2200 kHz. To determine the timing resistance for a given switching frequency, use Equation 2. The R1 resistor in Figure 23 sets the switching frequency. A 2.2-MHz switching frequency requires a 47-kΩ resistor.

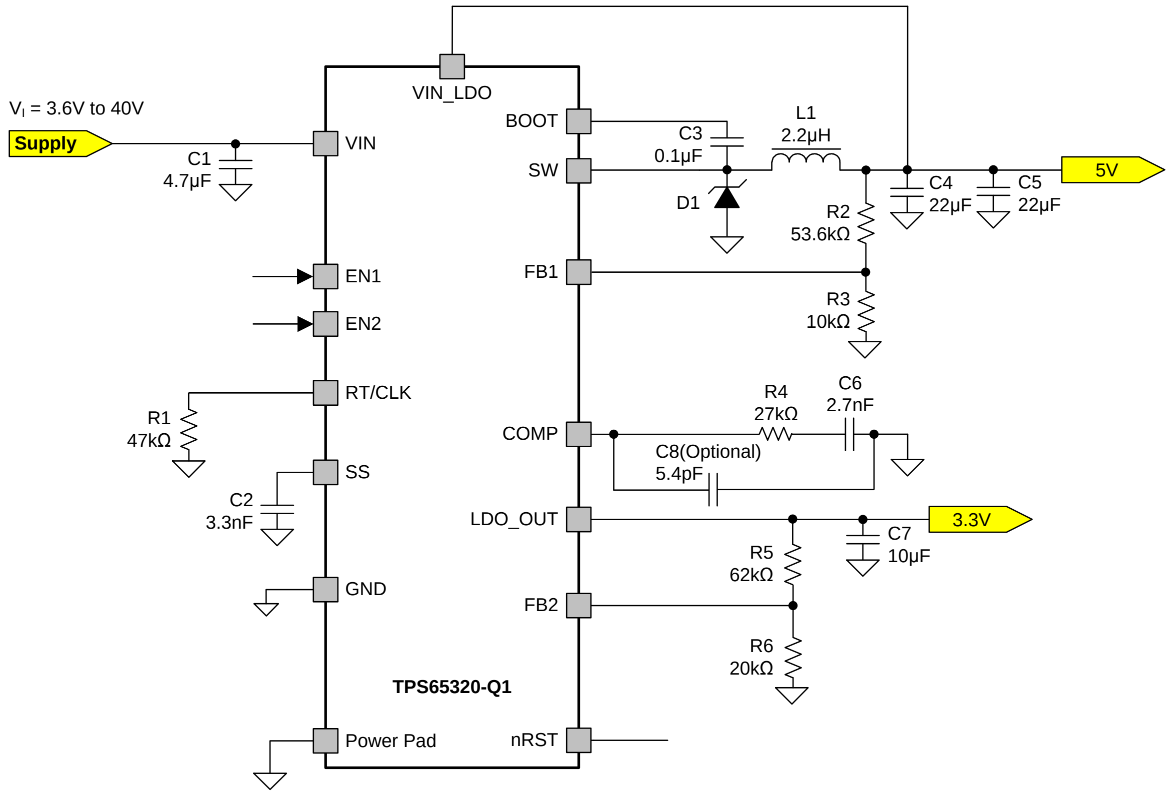



**Figure 23. TPS65320-Q1 Design Example With 2.2-MHz Switching Frequency**

## Output Inductor Selection

To calculate the minimum value of the output inductor, use Equation 20. The output capacitor filters the inductor ripple current. Therefore, choosing high inductor ripple currents impacts the selection of the output capacitor, because the output capacitor must have a ripple-current rating equal to or greater than the inductor ripple current. In general, the inductor ripple value is at the discretion of the designer; however, one can use the following guidelines. $K_{IND}$ is a coefficient that represents the amount of inductor ripple current relative to the maximum output current.

For designs using low-ESR output capacitors such as ceramics, one can use a value as high as $K_{IND}$ = 0.3. When using higher-ESR output capacitors, $K_{IND}$ = 0.2 yields better results. In a wide-input voltage regulator, it is best to choose an inductor ripple current on the larger side. This allows the inductor to still have a measurable ripple current with the input voltage at its minimum.

For this design example, use $K_{IND}$ = 0.3 and the minimum inductor value calculates to be 1.73 µH. For this design, the choice is a nearest standard value: 2.2 µH. For the output filter inductor, it is important not to exceed the rms-current and saturation-current ratings. One can find the rms and peak inductor currents from Equation 22 and Equation 23. The inductor ripple current is 0.71 A, and the rms current is 3.01 A.

For this design, the rms inductor current is 3.01 A and the peak inductor current is 3.36 A. The chosen inductor is a Coilcraft MSS1038-103NLB. It has a saturation-current rating of 4.52 A and an rms-current rating of 4.05 A. As the equation set demonstrates, lower ripple current reduces the output ripple voltage of the regulator but requires a larger value of inductance. Selecting higher ripple currents increases the output ripple voltage of the regulator but allows for a lower inductance value.

$$L_{omin} = \frac{V_{in\_max} - V_{out}}{I_O \times K_{IND}} \times \frac{V_{out}}{V_{in\_max} \times f_{SW}} \tag{20}$$

$$I_{ripple} = \frac{V_{out} \times \left(V_{in\_max} - V_{out}\right)}{V_{in\_max} \times L_o \times f_{SW}} \tag{21}$$

$$I_{L-RMS} = \sqrt{I_O{}^2 + \frac{1}{12} I_{ripple}{}^2} \tag{22}$$

$$I_{L-peak} = I_O + \frac{I_{ripple}}{2} \tag{23}$$

## Output Capacitor

There are three primary considerations for selecting the value of the output capacitor. The output capacitor determines the modulator pole, the output ripple voltage, and how the regulator responds to a large change in load current. Select the output capacitance based on the most stringent of these three criteria. The desired response to a large change in the load current is the first criterion. The output capacitor must supply the load with current when the regulator cannot. This situation occurs if there are desired hold-up times for the regulator where the output capacitor must hold the output voltage above a certain level for a specified amount of time after removal of the input power. The regulator is also temporarily not able to supply sufficient output current if there is a large and fast increase in the current needs of the load, such as transitioning from no load to a full load. The regulator usually needs two or more clock cycles for the control loop to see the change in load current and output voltage and adjust the duty cycle to react to the change. Size the output capacitor to supply the extra current to the load until the control loop responds to the load change. The output capacitance must be large enough to supply the difference in current for two clock cycles while only allowing a tolerable amount of droop in the output voltage. Equation 24 shows the minimum output capacitance necessary to accomplish this.

Where $\Delta I_{OUT}$ is the change in output current, $f_{sw}$ is the switching frequency of the regulators, and $\Delta V_{OUT}$ is the allowable change in the output voltage. For this example, the specified transient load response is a 3% change in $V_{OUT}$ for a load step from 0.01 A to 0.8 A (full load). For this example, $\Delta I_{OUT}$ = 0.8 – 0.01 = 0.79 A and $\Delta V_{OUT}$ = 0.03 × 5 = 0.15 V. Using these numbers gives a minimum capacitance of 4.7 µF. This value does not take the ESR of the output capacitor into account in the output voltage change. For ceramic capacitors, the ESR is usually small enough to ignore in this calculation. Aluminum electrolytic and tantalum capacitors have higher ESR that one should take into account.

The catch diode of the regulator cannot sink current, so any stored energy in the inductor produces an output-voltage overshoot when the load current rapidly decreases. Also, size the output capacitor to absorb the energy stored in the inductor when transitioning from a high load current to a lower load current. The excess energy that gets stored in the output capacitor increases the voltage on the capacitor. Size the capacitor to maintain the desired output voltage during these transient periods. Use Equation 25 to calculate the minimum capacitance to keep the output voltage overshoot to a desired value, where L is the value of the inductor, $I_{OH}$ is the output current under heavy load, $I_{OL}$ is the output under light load, $V_f$ is the final peak output voltage, and $V_i$ is the initial capacitor voltage. For this example, the worst-case load step is from 3 A to 0.01 A. The output voltage increases during this load transition, and the stated maximum in our specification is 3% of the output voltage. This makes $V_f$ = 1.03 × 5 = 5.15. $V_i$ is the initial capacitor voltage, which is the nominal output voltage of 5 V. Using these numbers in Equation 25 yields a minimum capacitance of 13 µF.

Equation 26 calculates the minimum output capacitance needed to meet the output ripple-voltage specification, where $f_{sw}$ is the switching frequency, $V_{o\_ripple}$ is the maximum allowable output ripple voltage, and $I_{L\_ripple}$ is the inductor ripple current. Equation 26 yields 0.8 µF.

Equation 27 calculates the maximum ESR an output capacitor can have to meet the output ripple-voltage specification. Equation 27 indicates the ESR should be less than 70 mΩ.

The most stringent criterion for the output capacitor is 13 µF of capacitance to keep the output voltage in regulation during a load transient.

Factor in additional capacitance deratings for aging, temperature, and dc bias, increasing this minimum value. For this example, two 22-µF, 10-V ceramic capacitors with 3 mΩ of ESR are used. Capacitors generally have limits to the amount of ripple current they can handle without failing or producing excess heat. Specify an output capacitor that can support the inductor ripple current. Some capacitor data sheets specify the root mean square (rms) value of the maximum ripple current. One can useEquation 28 to calculate the rms ripple current that the output capacitor must support. For this application, Equation 28 yields 205 mA.

$$C_{out} > \frac{2 \times \Delta I_{out}}{f_{SW} \times \Delta V_{out}} \tag{24}$$

$$C_{out} > L_o \times \frac{(I_{oh}^2 - I_{ol}^2)}{(V_f^2 - V_i^2)} \tag{25}$$

$$C_{out} > \frac{1}{8 \times f_{SW}} \times \frac{1}{\frac{V_{o\_ripple}}{I_{L\_ripple}}} \tag{26}$$

$$R_{ESR} < \frac{V_{o\_ripple}}{I_{L\_ripple}} \tag{27}$$

$$I_{corms} < \frac{V_{out} \times (V_{in\_max} - V_{out})}{\sqrt{12} \times V_{in\_max} \times L_o \times f_{SW}} \tag{28}$$

### Catch Diode

The TPS65320-Q1 requires an external catch diode between the SW pin and GND. The selected diode must have a reverse voltage rating equal to or greater than $V_{inmax}$. The peak current rating of the diode must be greater than the maximum inductor current. The diode should also have a low forward voltage. Schottky diodes are typically a good choice for the catch diode due to their low forward voltage. The lower the forward voltage of the diode, the higher the efficiency of the regulator.

Typically, the higher the voltage and current ratings the diode has, the higher the forward voltage is. Although the design example has an input voltage up to 16 V, select a diode with a minimum of 40-V reverse voltage to allow input voltage transients up to the rated voltage of the TPS65320-Q1 device.

For the example design, the selection of a Schottky diode is B540C-13-F for its lower forward voltage. Also, it comes in a larger package size, which has good thermal characteristics over small devices. The typical forward voltage of the B540C-13-F is 0.55 volts.

Also, select a diode with an appropriate power rating. The diode conducts the output current during the off-time of the internal power switch. The off-time of the internal switch is a function of the maximum input voltage, the output voltage, and the switching frequency. The output current during the off-time, multiplied by the forward voltage of the diode, equals the conduction losses of the diode. At higher switching frequencies, take the ac losses of the diode into account. The ac losses of the diode are due to the charging and discharging of the junction capacitance and reverse recovery.

### Input Capacitor

The TPS65320-Q1 device requires a high-quality ceramic input decoupling capacitor (type X5R or X7R) of at least 3 µF of effective capacitance, and in some applications a bulk capacitance. The effective capacitance includes any dc bias effects. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple-current rating greater than the maximum input-current ripple of the TPS65320-Q1. One can calculate the input ripple current using Equation 29.

The value of a ceramic capacitor varies significantly over temperature and the amount of dc bias applied to the capacitor. One can minimize the capacitance variations due to temperature by selecting a dielectric material that is stable over temperature. Designers usually select X5R and X7R ceramic dielectrics for power regulator capacitors because they have a high capacitance-to-volume ratio and are fairly stable over temperature. Also, select the output capacitor with the dc bias taken into account. The capacitance value of a capacitor decreases as the dc bias across a capacitor increases.

This example design requires a ceramic capacitor with at least a 40-V voltage rating to support the maximum input voltage. Common standard ceramic capacitor voltage ratings include 4 V, 6.3 V, 10 V, 16 V, 25 V, 50 V or 100 V, so select a 50-V capacitor. The selection for this example is 4.7-µF, 50-V capacitors in parallel. Table 3 shows a selection of high-voltage capacitors. The input-capacitance value determines the input ripple voltage of the regulator. One can calculate the input ripple voltage using Equation 30. Using the design example values, $I_{OUTmax}$ = 3 A, $C_{IN}$ = 4.7 µF, $f_{sw}$ = 2200 kHz, yields an input ripple voltage of 72.5 mV and an rms input ripple current of 1.49 A.

$$I_{cirms} = I_{out} \times \sqrt{\frac{V_{out}}{V_{in\,min}} \times \frac{(V_{in\,min} - V_{out})}{V_{in\,min}}} \tag{29}$$

$$\Delta V_{in} = \frac{I_{out\ max} \times 0.25}{C_{in} \times f_{SW}} \quad (30)$$

**Table 3. Capacitor Types**

| VENDOR | VALUE (µF) | EIA Size | VOLTAGE | DIALECTRIC | COMMENTS |
|---|---|---|---|---|---|
| Murata | 1 to 2.2 | 1210 | 100 V | X7R | GRM32 series |
| | 1 to 4.7 | | 50 V | | |
| | 1 | 1206 | 100 V | | GRM31 series |
| | 1 to 2.2 | | 50 V | | |
| AVX | 1 to 4.7 | 1210 | 50 V | | X7R dielectric series |
| | 1 | | 100 V | | |
| | 1 to 4.7 | 1812 | 50 V | | |
| | 1 to 2.2 | | 100 V | | |

## Slow-Start Capacitor

The slow-start capacitor determines the minimum amount of time it takes for the output voltage to reach its nominal programmed value during power up. This is useful if a load requires a controlled voltage-slew rate. This is also useful if the output capacitance is large and requires large amounts of current to charge the capacitor quickly to the output voltage level. The large currents necessary to charge the capacitor may make the TPS65320-Q1 device reach the current limit, or excessive current draw from the input power supply may cause the input voltage rail to sag. Limiting the output voltage-slew rate solves both of these problems.

The slow-start time must be long enough to allow the regulator to charge the output capacitor up to the output voltage without drawing excessive current. One can use Equation 31 to find the minimum slow-start time, $t_{ss}$, necessary to charge the output capacitor, $C_{OUT}$, from 10% to 90% of the output voltage, $V_{OUT}$, with an average slow-start current of $I_{ssavg}$. In the example, to charge the effective output capacitance of 44 µF up to 5 V while only allowing the average output current to be 3 A would require a 0.088-ms slow-start time.

After knowing the slow-start timen, one can calculate the slow start capacitor value using Equation 1. For the example circuit, the slow-start time is not too critical, because the output-capacitor value is 2 × 22 µF, which does not require much current to charge to 5 V. The example circuit has the slow-start time set to an arbitrary value of 1 ms, which requires a 3.125-nF slow start capacitor. This design uses the next-larger standard value of 3.3 nF.

$$T_{ss} > \frac{C_{out} \times V_{out} \times 0.8}{I_{ssavg}} \quad (31)$$

## Bootstrap Capacitor Selection

Connect a 0.1-µF ceramic capacitor between the BOOT and SW pins for proper operation. TI recommends using a ceramic capacitor with X5R or better-grade dielectric. The capacitor should have a 10-V or higher voltage rating.

## Output Voltage and Feedback Resistors Selection

The voltage divider of R2 and R3 sets the output voltage. For the example design, the selected value of R3 is 10 kΩ, and the calculated value of R2 is 53.6 kΩ. Due to current leakage of the VFB1 pin, the current flowing through the feedback network should be greater than 1 µA in order to maintain the output-voltage accuracy. Choosing higher resistor values decreases the quiescent current and improves efficiency at low output currents, but may introduce noise immunity problems.

## Compensation

There are several methods used to compensate dc-dc regulators. The method presented here is easy to calculate and ignores the effects of the slope compensation that is internal to the device. Ignoring the slope compensation usually causes the actual crossover frequency to be lower than the crossover frequency used in the calculations. This method assumes the crossover frequency is between the modulator pole and the ESR zero, and the ESR zero is at least 10 times greater than the modulator pole.

To get started, calculate the modulator pole, $f_{P\_mod}$, and the ESR zero, $f_{z\_mod}$ using Equation 32 and Equation 33. For $C_{OUT}$, use a derated value of 40 µF. Use Equation 34 and Equation 35 to estimate a starting point for the crossover frequency, $f_{co}$, to design the compensation. For the example design, $f_{P\_mod}$ is 2.39 kHz and $f_{Z\_mod}$ is 1.33 MHz. Equation 34 is the geometric mean of the modulator pole and the ESR zero and Equation 35 is the mean of the modulator pole and the switching frequency. Equation 34 yields 56.4 kHz and Equation 35 gives 51.3 kHz. Use the lower value of Equation 34 or Equation 35 for an initial crossover frequency.

For this example, the target $f_{co}$ is 51.3 kHz. Next, calculate the compensation components. Use a resistor in series with a capacitor to create a compensating zero. A capacitor in parallel to these two components forms the compensating pole.

$$f_{P\_mod} = \frac{1}{2\pi \times R_L \times C_{out}} = \frac{I_{max}}{2\pi \times V_{out} \times C_{out}} \tag{32}$$

$$f_{Z\_mod} = \frac{1}{2\pi \times R_{ESR} \times C_{out}} \tag{33}$$

$$f_{co} = \sqrt{f_{P\_mod} \times f_{Z\_mod}} \tag{34}$$

$$f_{co} = \sqrt{f_{P\_mod} \times \frac{f_{SW}}{2}} \tag{35}$$

The total loop gain, which consists of the product of the modulator gain, the feedback voltage-divider gain, and the error amplifier gain at $f_{co}$ should be equal to 1. One can juse Equation 36 to determine the compensation resistor, R4 (see schematics in Figure 23). Assume the power-stage transconductance, $gm_{ps}$, is 10.5 S. The output voltage, $V_{OUT}$, reference voltage, $V_{REF}$, and amplifier transconductance, $gm_{ea}$, are 5 V, 0.8 V and 310 µS, respectively. The calculated value for R4 is 24.74 kΩ; use 27 kΩ in this design. Use Equation 37 to set the compensation zero to the modulator pole frequency. Equation 35 yields 2468 pF for compensating capacitor C6 (see schematics in Figure 23); use 2700 pF for this design.

$$R4 = \left(\frac{2\pi \times f_{co} \times C_{out}}{gm_{ps}}\right) \times \left(\frac{V_{out}}{V_{ref} \times gm_{ea}}\right) \tag{36}$$

$$C6 = \frac{1}{2\pi \times R4 \times f_{P\_mod}} \tag{37}$$

One can implement a compensation pole if desired using an additional capacitor C8 in parallel with the series combination of R4 and C6. Use the larger value of Equation 38 and Equation 39 to calculate the C8, to set the compensation pole. Type 2B compensation does not use C8. This would demand a low ESR of the output capacitor.

$$C8 = \frac{C_{out} \times R_{ESR}}{R4} \tag{38}$$

$$C8 = \frac{1}{\pi \times R4 \times f_{SW}} \tag{39}$$

## LDO

Depending upon an end application, one may use different values of external components. In order to program the output voltage, select the feedback resistors (R5 and R6) carefully. Using smaller resistors results in higher current consumption, whereas using very large resistors impacts the sensitivity of the regulator. TI therefore recommends selecting feedback resistors such that the sum of R5 and R6 is between 20 kΩ and 200 kΩ.

If the desired regulated output voltage is 3.3 V on selecting R6, one can calculate R5. Knowing $V_{REF}$ = 0.8 V (typical), $V_{OUT}$ = 3.3 V, and selecting R6 = 20 kΩ, the calculated value of R5 is 62 kΩ.

There may be a requirement for a larger output capacitor during fast load steps to prevent the output from temporarily dropping down. TI recommends a low-ESR ceramic capacitor with dielectric of type X5R or X7R. Additionally, one can connect a bypass capacitor at the output to decouple high-frequency noise, per the end application.

## Power Dissipation

### Switch-Mode Power-Supply Losses:

The power dissipation losses are applicable for continuous-conduction-mode (CCM) operation

$P_{CON} = I_O^2 \times r_{DS(on)} \times (V_O / V_I)$ (Conduction losses)

$P_{SW} = ½ \times V_I \times I_O \times (t_r + t_f) \times f_{SW}$ (Switching losses)

$P_{Gate} = V_{drive} \times Q_g \times f_{sw}$ (Gate drive losses)

Where typically: $Q_g = 1 \times 10^{-9}$ (nC)

$P_{IC} = V_I \times I_{q\text{-normal}}$ (Supply losses)

$P_{Total} = P_{CON} + P_{SW} + P_{Gate} + P_{LDO} + P_{IC}$

Where:

$V_O$ = VREG = Output voltage

$V_I$ = Input voltage

$I_O$ = Output current

$t_r$ = FET switching rise time ($t_r$ maximum = 20 ns)

$t_f$ = FET switching fall time ($t_f$ maximum = 20 ns)

$V_{drive}$ = FET gate-drive voltage (typically $V_{drive}$ = 6 V)

$f_{SW}$ = Switching frequency

### Linear Regulator:

$P_{LDO} = (V_{buck} – V_{LDO}) \times I_O$

For a given operating ambient temperature $T_{Amb}$

$T_J = T_{Amb} + R_{th} \times P_{Total}$

For a given maximum junction temperature $T_{J\text{-}Max}$ = 150°C

$T_{Amb\text{-}Max} = T_{J\text{-}Max} - R_{th} \times P_{Total}$

Where:

$P_{Total}$ = Total power dissipation (W)

$T_{Amb}$ = Ambient temperature in °C

$T_J$ = Junction temperature in °C

$T_{Amb\text{-}Max}$ = Maximum ambient temperature in °C

$T_{J\text{-}Max}$ = Maximum junction temperature in °C

$R_{th}$ = Thermal resistance of package in (°C/W)

Other factors NOT included in the foregoing information which affect the overall efficiency and power losses are:

- Inductor ac and dc losses
- Trace resistance and losses associated with the copper trace routing connection
- Schottky diode

## PCB Layout

TI recommends the following guidelines for PCB layout of the TPS65320-Q1 device.

### Inductor L

Use a low-EMI inductor with a ferrite-type shielded core. One can use other types of inductors; however, they must have low-EMI characteristics and be located away from the low-power traces and components in the circuit.

### Input Filter Capacitors $C_I$

Locate input ceramic filter capacitors in close proximity to the VIN terminal. TI recommends surface-mount capacitors to minimize lead length and reduce noise coupling.

### Feedback

Route the feedback trace such that there is minimum interaction with any noise sources associated with the switching components. The recommended practice is to ensure the inductor is placed away from the feedback trace to prevent creating an EMI noise source.

### Traces and Ground Plane

All power (high-current) traces should be as thick and short as possible. The inductor and output capacitors should be as close to each other as possible. This reduces EMI radiated by the power traces due to high switching currents. In a two-sided PCB, TI recommends having ground planes on both sides of the PCB to help reduce noise and ground loop errors. The ground connection for the input and output capacitors and IC ground should connect to this ground plane. In a multi-layer PCB, the ground plane separates the power plane (where high switching currents and components are) from the signal plane (where the feedback trace and components are) for improved performance. Also, arrange the components such that the switching-current loops curl in the same direction. Place the high-current components such that during conduction the current path is in the same direction. This prevents magnetic field reversal caused by the traces between the two half-cycles, and helps reduce radiated EMI.

### Other Application Example

For a 300-kHz operation, the choices are a 10-µH inductor and a 47-µF × 2 output capacitor.

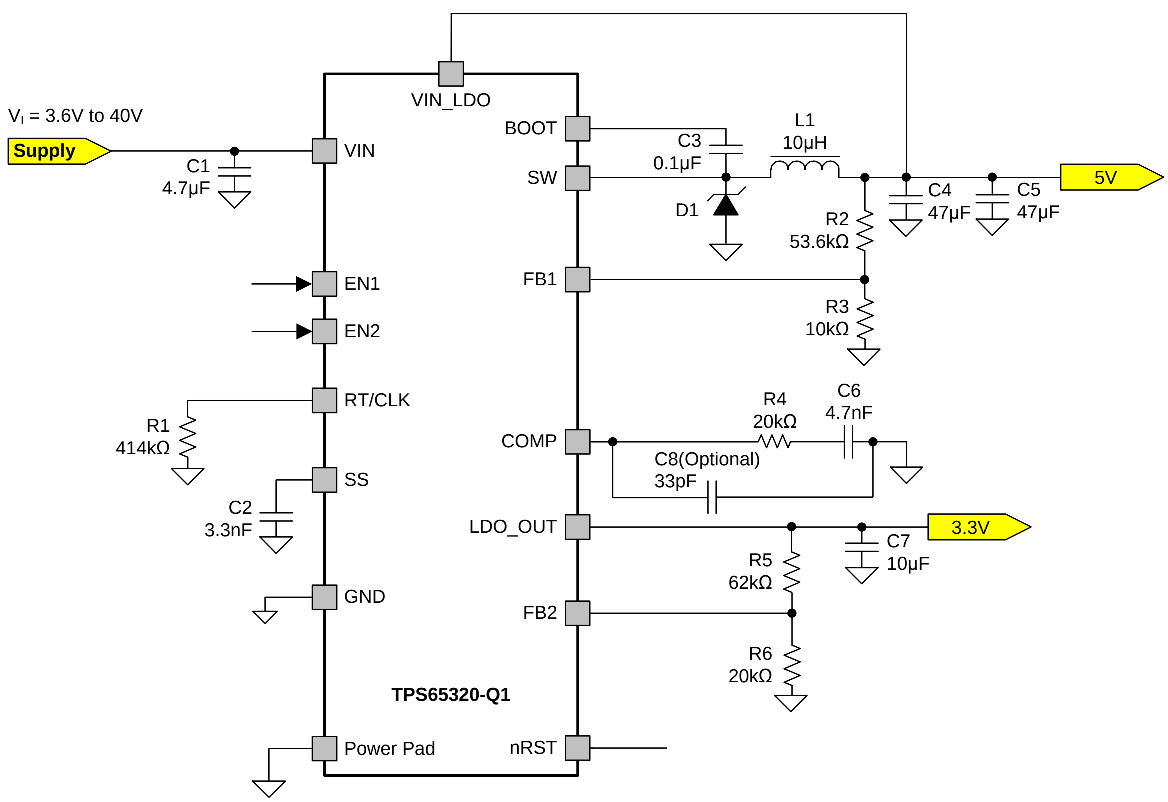



**Figure 24. TPS65320-Q1 Design Example With 300-kHz Switching Frequency**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS65320QPWPRQ1 | ACTIVE | HTSSOP | PWP | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 150 | TPS65320 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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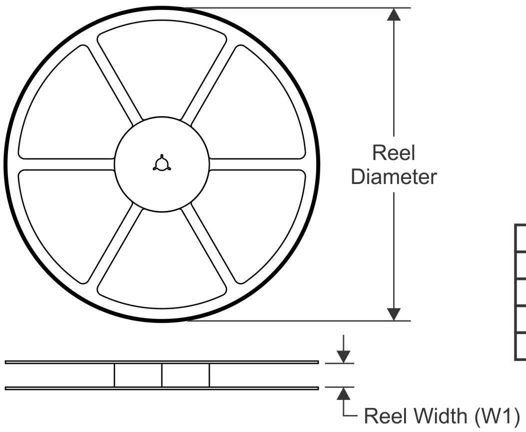
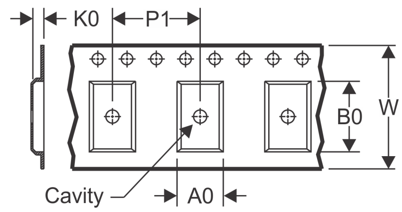
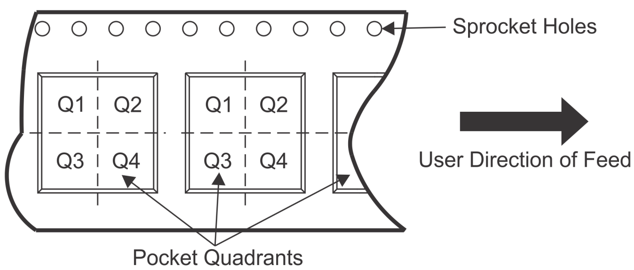


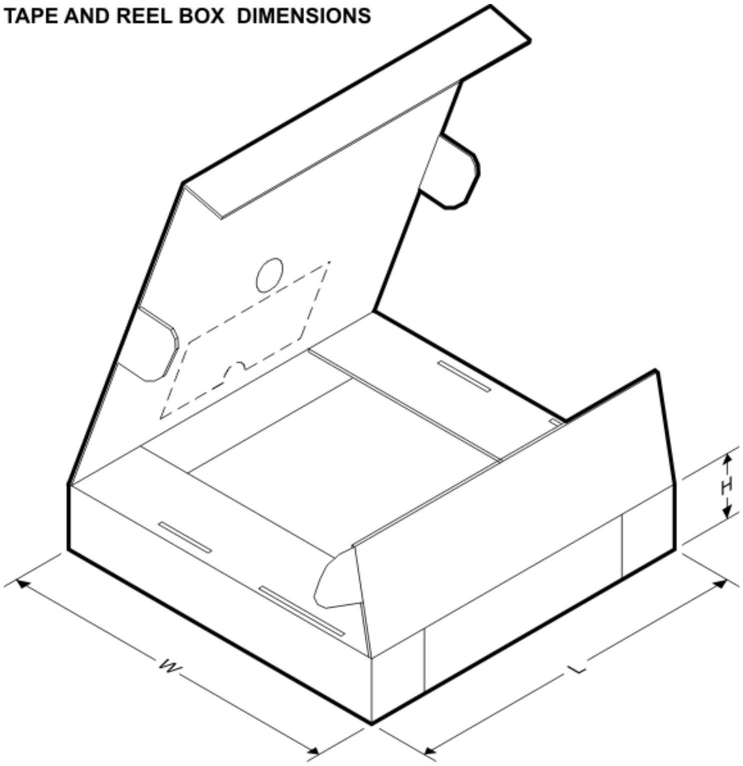

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS65320QPWPRQ1 | HTSSOP | PWP | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

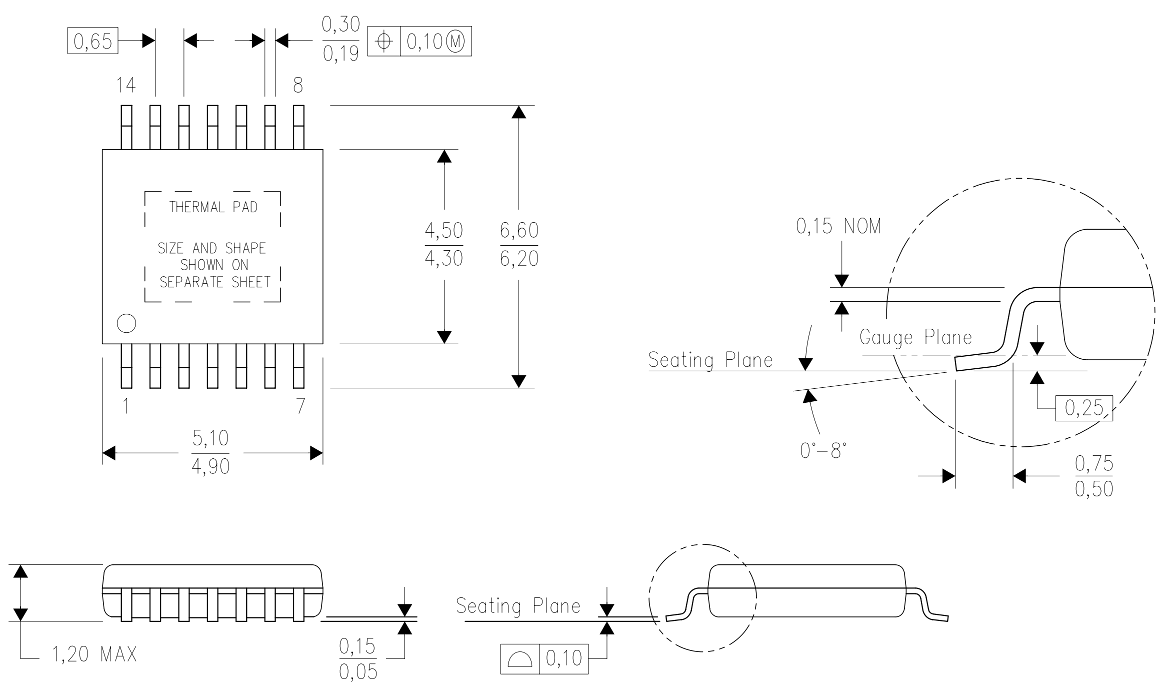
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS65320QPWPRQ1 | HTSSOP | PWP | 14 | 2000 | 367.0 | 367.0 | 35.0 |

PWP (R-PDSO-G14) PowerPAD™ PLASTIC SMALL OUTLINE




4073225-2/I 05/11

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- E. Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.

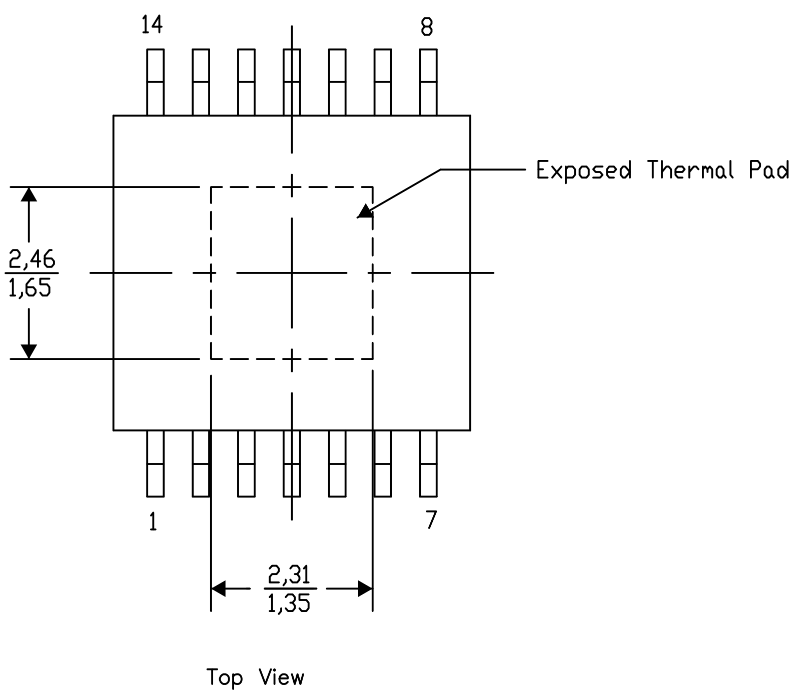
PWP (R-PDSO-G14)    PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

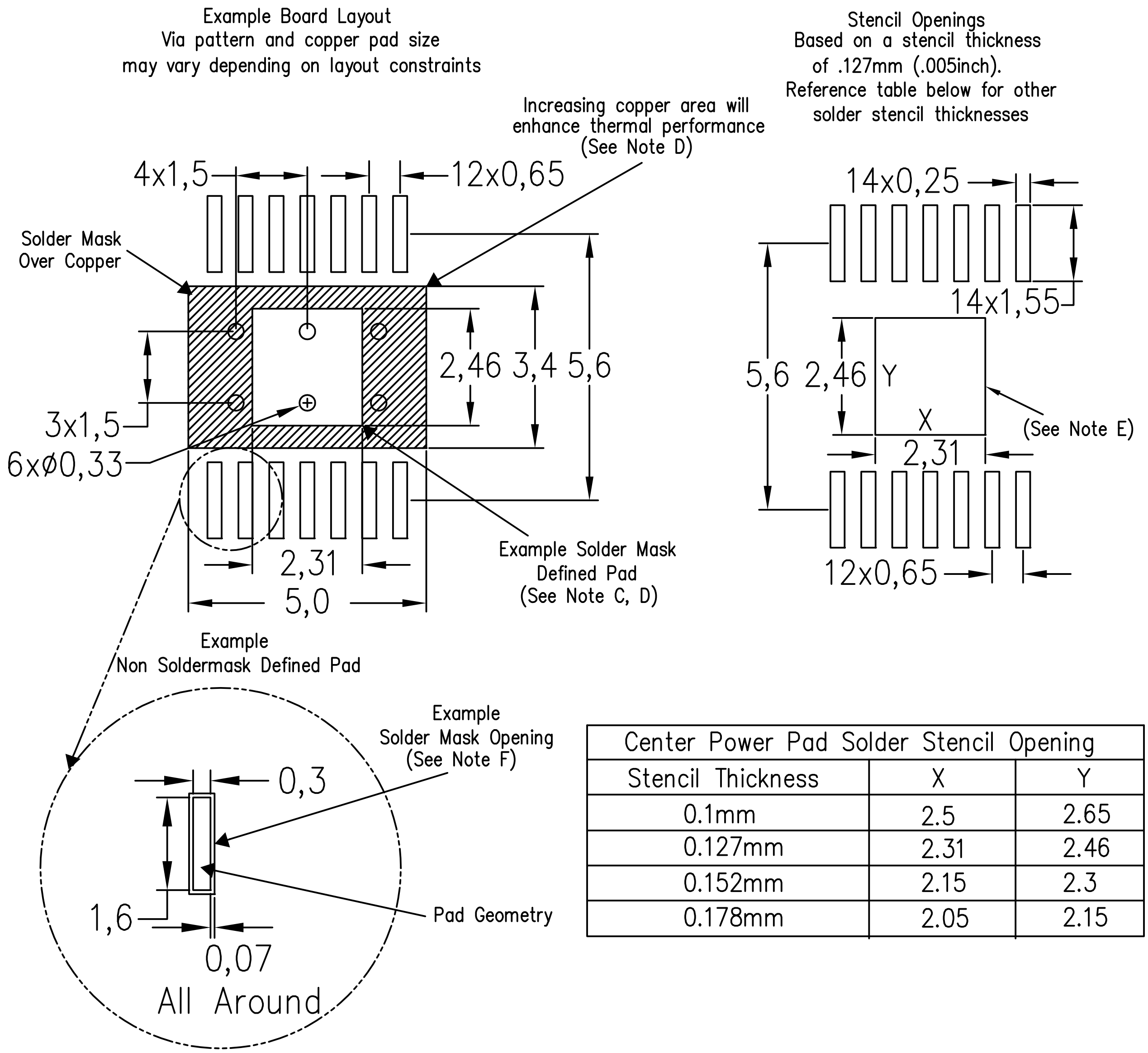



Exposed Thermal Pad Dimensions

4206332-2/AD 01/13

NOTE: A. All linear dimensions are in millimeters

PWP (R-PDSO-G14) PowerPAD™ PLASTIC SMALL OUTLINE




| Center Power Pad Solder Stencil Opening | | |
|---|---|---|
| Stencil Thickness | X | Y |
| 0.1mm | 2.5 | 2.65 |
| 0.127mm | 2.31 | 2.46 |
| 0.152mm | 2.15 | 2.3 |
| 0.178mm | 2.05 | 2.15 |

4207609-2/S 02/13

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
- F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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