ULTRA-SMALL, LOW ON RESISTANCE LOAD SWITCH WITH CONTROLLED TURN-ON

Check for Samples: TPS22910

FEATURES

- **Integrated Single Load Switch**
- **Four Terminal Wafer-Chip-Scale Package (Nominal Dimensions Shown - See Addendum for Details)**
  - **0.9 mm × 0.9 mm, 0.5 mm Pitch, 0.5 mm Height (YZV)**
- **Input Voltage Range: 1.4 V to 5.5 V**
- **Low ON-Resistance**
  - **r_{ON} = 60 mΩ at VIN = 5 V**
  - **r_{ON} = 61 mΩ at VIN = 3.3 V**
  - **r_{ON} = 74 mΩ at VIN = 1.8 V**
  - **r_{ON} = 84 mΩ at VIN = 1.5 V**
- **2-A Maximum Continuous Switch Current**
- **Low Threshold Control Input**
- **Controlled Slew-rate**
- **Under-Voltage Lock Out**
- **Full-Time Reverse Current Protection**

APPLICATIONS

- **Notebook Computer and Ultrabook™**
- **Tablets and Set-Top-Boxes**
- **Portable Industrial / Medical Equipment**
- **Portable Media Players**
- **Point Of Sale Terminals**
- **GPS Navigation Devices**
- **Digital Cameras**
- **Portable Instrumentation**
- **Smartphones / Wireless Handsets**

DESCRIPTION

The TPS22910 is a small, low r_{ON} load switch with controlled turn on. The device contains a P-channel MOSFET that can operate over an input voltage range of 1.4 V to 5.5 V. The switch is controlled by an on/off input (ON), which is capable of interfacing directly with low-voltage GPIO control signals. The TPS22910 is active low enable.

The slew rate of the device is internally controlled in order to avoid inrush current.

The TPS22910 device provides reverse current protection in ON and OFF states. An internal reverse voltage comparator disables the power-switch when the output voltage (V_{OUT}) is driven higher than the input voltage (V_{IN}), by V_{RCP}, to quickly (10µs typ) stop the flow of current towards the input side of the switch. Reverse current protection is always active, even when the power-switch is disabled. Additionally, under-voltage lockout (UVLO) protection turns the switch off if the input voltage is too low.

The TPS22910 is available in an ultra-small, space-saving 4-pin WCSP package and is characterized for operation over the free-air temperature range of –40°C to 85°C.

TYPICAL APPLICATION

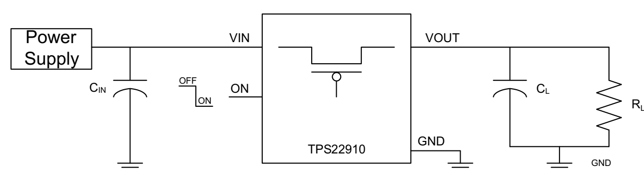


Table 1. Feature List

DEVICE	r_{ON} (typ) at 3.3 V	RISE TIME at 3.3V (typ)(1)	QUICK OUTPUT DISCHARGE(2)	MAXIMUM OUTPUT CURRENT	ENABLE
TPS22910A	61 mΩ	1 µs	No	2 A	Active Low

(1) Additional rise time options are possible. Contact factory for more information.
(2) This feature discharges the output of the switch to ground through an 150-Ω resistor, preventing the output from floating.

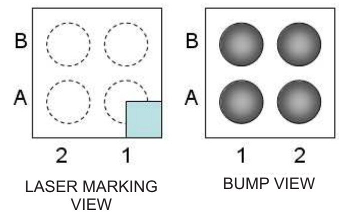
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

For package and ordering information, see the Package Option Addendum at the end of this document.

DEVICE INFORMATION

YZV PACKAGE



TERMINAL ASSIGNMENTS

B	ON	GND
A	VIN	VOUT
	2	**1**

PIN FUNCTIONS

TPS22910	PIN NAME	DESCRIPTION
YZV		
B1	GND	Ground
B2	ON	Switch control input, active low. Do not leave floating
A1	VOUT	Switch output
A2	VIN	Switch input, use a bypass capacitor (ceramic) to ground.

BLOCK DIAGRAM

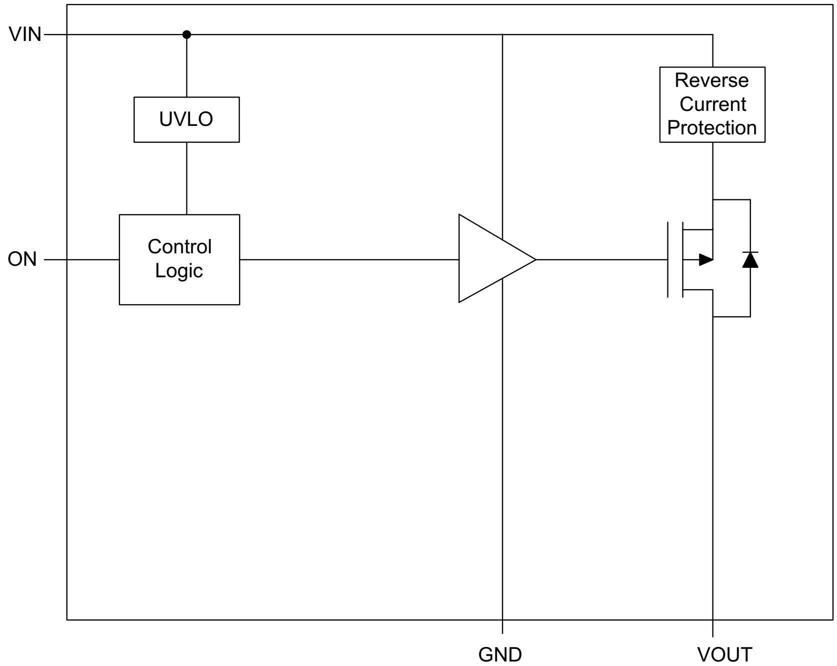


Table 2. FUNCTION TABLE

ON	VIN to VOUT
L	ON
H	OFF

ABSOLUTE MAXIMUM RATINGS

			VALUE	UNIT
V_{IN}	Input voltage range		–0.3 to 6	V
V_{OUT}	Output voltage range		–0.3 to 6	V
V_{ON}	Input voltage range		–0.3 to 6	V
I_{MAX}	Maximum continuous switch current		2	A
I_{PLS}	Maximum pulsed switch current, pulse <300 µs, 2% duty cycle		2.5	A
T_A	Operating free-air temperature range		–40 to 85	°C
T_J	Maximum junction temperature		125	°C
T_{STG}	Storage temperature range		–65 to 150	°C
T_{LEAD}	Maximum lead temperature (10-s soldering time)		300	°C
ESD	Electrostatic discharge protection	Human-Body Model (HBM)	2000	V
		Charged-Device Model (CDM)	1000	

THERMAL INFORMATION

THERMAL METRIC[1]		TPS22910 CSP 4 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	189.1	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	1.9	
θ_{JB}	Junction-to-board thermal resistance	36.8	
ψ_{JT}	Junction-to-top characterization parameter	11.3	
ψ_{JB}	Junction-to-board characterization parameter	36.8	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V_{IN}	Input voltage range		1.4	5.5	V
V_{ON}	ON voltage range		0	5.5	V
V_{OUT}	Output voltage range			V_{IN}	
V_{IH}	High-level input voltage, ON	VIN = 1.4 V to 5.5 V	1.1	5.5	V
V_{IL}	Low-level input voltage, ON	VIN = 3.61 V to 5.5 V		0.6	V
		VIN = 1.4 V to 3.6 V		0.4	V
C_{IN}	Input capacitor		1[1]		µF

(1) Refer to the application section.

ELECTRICAL CHARACTERISTICS

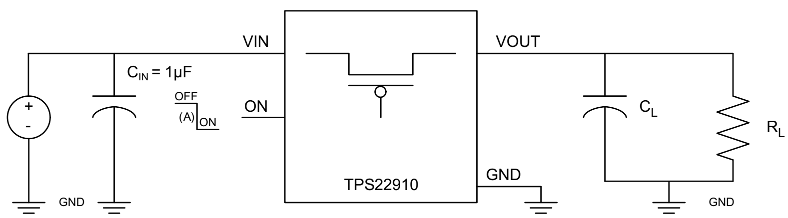
V_{IN} = 1.4 V to 5.5 V, T_A = –40ºC to 85ºC (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
I_{IN}	Quiescent current	I_{OUT} = 0 mA, V_{IN} = 5.25 V, V_{ON} = 0 V	Full		2	10	µA
		I_{OUT} = 0 mA, V_{IN} = 4.2 V, V_{ON} = 0 V			2	7.0	
		I_{OUT} = 0 mA, V_{IN} = 3.6 V, V_{ON} = 0 V			2	7.0	
		I_{OUT} = 0 mA, V_{IN} = 2.5 V, V_{ON} = 0 V			0.9	5	
		I_{OUT} = 0 mA, V_{IN} = 1.5 V, V_{ON} = 0 V			0.7	5	
$I_{IN(off)}$	Off supply current	R_L = 1 MΩ, V_{IN} = V_{ON} = 5.25 V	Full		1.2	10	µA
		R_L = 1 MΩ, V_{IN} = V_{ON} = 4.2 V			0.2	7.0	
		R_L = 1 MΩ, V_{IN} = V_{ON} = 3.6 V			0.1	7.0	
		R_L = 1 MΩ, V_{IN} = V_{ON} = 2.5 V			0.1	5	
		R_L = 1 MΩ, V_{IN} = V_{ON} = 1.5 V			0.1	5	
$I_{IN(Leakage)}$	Leakage current	V_{OUT} = 0 V, V_{IN} = V_{ON} = 5.25 V	Full		1.2	10	µA
		V_{OUT} = 0 V, V_{IN} = V_{ON} = 4.2 V			0.2	7.0	
		V_{OUT} = 0 V, V_{IN} = V_{ON} = 3.6 V			0.1	7.0	
		V_{OUT} = 0 V, V_{IN} = V_{ON} = 2.5 V			0.1	5	
		V_{OUT} = 0 V, V_{IN} = V_{ON} = 1.5 V			0.1	5	
r_{ON}	On-resistance	V_{IN} = 5.25 V, I_{OUT} = –200 mA	25°C		60	80	mΩ
			Full			110	
		V_{IN} = 5.0 V, I_{OUT} = –200 mA	25°C		60	80	
			Full			110	
		V_{IN} = 4.2 V, I_{OUT} = –200 mA	25°C		60	80	
			Full			110	
		V_{IN} = 3.3 V, I_{OUT} = –200 mA	25°C		60.7	80	
			Full			110	
		V_{IN} = 2.5 V, I_{OUT} = –200 mA	25°C		63.4	90	
			Full			120	
		V_{IN} = 1.8 V, I_{OUT} = –200 mA	25°C		74.2	100	
			Full			130	
		V_{IN} = 1.5 V, I_{OUT} = –200 mA	25°C		83.9	120	
			Full			150	
UVLO	Under voltage lockout	V_{IN} increasing, V_{ON} = 0 V, I_{OUT} = –100 mA	Full			1.2	V
		V_{IN} decreasing, V_{ON} = 0 V, R_L = 10 Ω		0.50			
I_{ON}	ON input leakage current	V_{ON} = 1.4 V to 5.25 V or GND	Full			1	µA
V_{RCP}	Reverse current voltage threshold				44		mV
t_{DELAY}	Reverse current response delay	V_{IN} = 5 V			10		µs
I_{RCP}(leak)	Reverse current protection leakage after reverse current event.	V_{OUT} – V_{IN} > V_{RCP}	25°C		0.3		µA

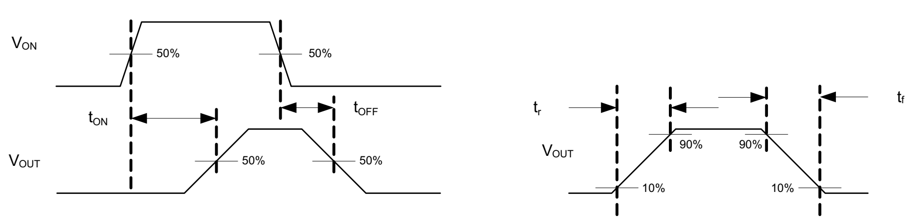
SWITCHING CHARACTERISTICS

PARAMETER		TEST CONDITION	TPS22910A TYP	UNIT
VIN = 5 V, T_A = 25ºC (unless otherwise noted)				
t_{ON}	Turn-ON time	R_L = 10 Ω, C_L = 0.1 µF	2	µs
t_{OFF}	Turn-OFF time	R_L = 10 Ω, C_L = 0.1 µF	5.5	
t_R	VOUT rise time	R_L = 10 Ω, C_L = 0.1 µF	1	
t_F	VOUT fall time	R_L = 10 Ω, C_L = 0.1 µF	3	
VIN = 3.3 V, T_A = 25ºC (unless otherwise noted)				
t_{ON}	Turn-ON time	R_L = 10 Ω, C_L = 0.1 µF	2.5	µs
t_{OFF}	Turn-OFF time	R_L = 10 Ω, C_L = 0.1 µF	7	
t_R	VOUT rise time	R_L = 10 Ω, C_L = 0.1 µF	1	
t_F	VOUT fall time	R_L = 10 Ω, C_L = 0.1 µF	3.5	
VIN = 1.5 V, T_A = 25ºC (unless otherwise noted)				
t_{ON}	Turn-ON time	R_L = 10 Ω, C_L = 0.1 µF	4.5	µs
t_{OFF}	Turn-OFF time	R_L = 10 Ω, C_L = 0.1 µF	16.5	
t_R	VOUT rise time	R_L = 10 Ω, C_L = 0.1 µF	2	
t_F	VOUT fall time	R_L = 10 Ω, C_L = 0.1 µF	7	

PARAMETRIC MEASUREMENT INFORMATION



TEST CIRCUIT



t_{ON}/t_{OFF} WAVEFORMS

(A) Rise and fall times of the control signal is 100ns.

Figure 1. Test Circuit and t_{ON}/t_{OFF} Waveforms

TYPICAL CHARACTERISTICS

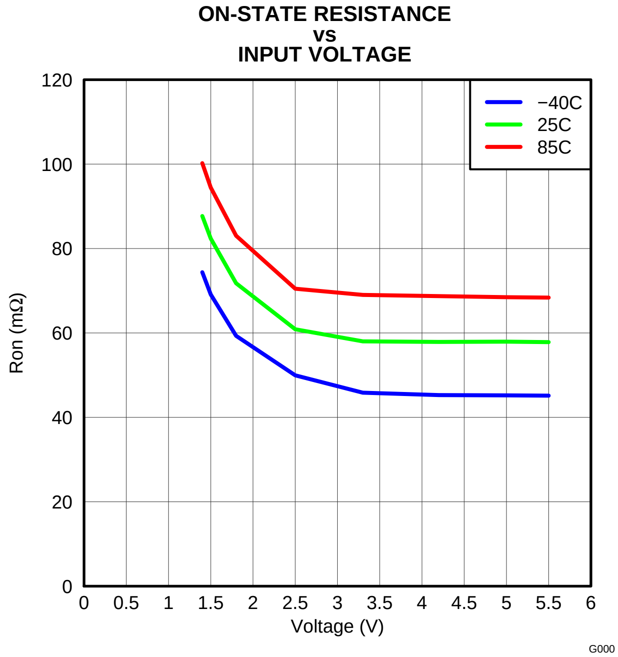


Figure 2.

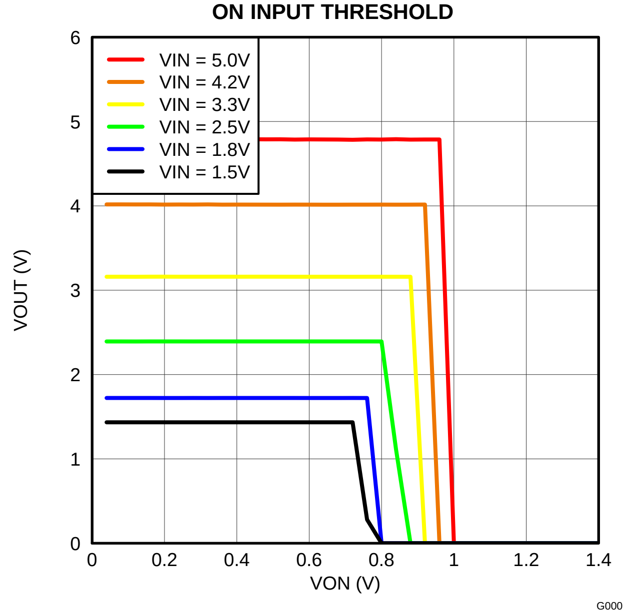


Figure 3.

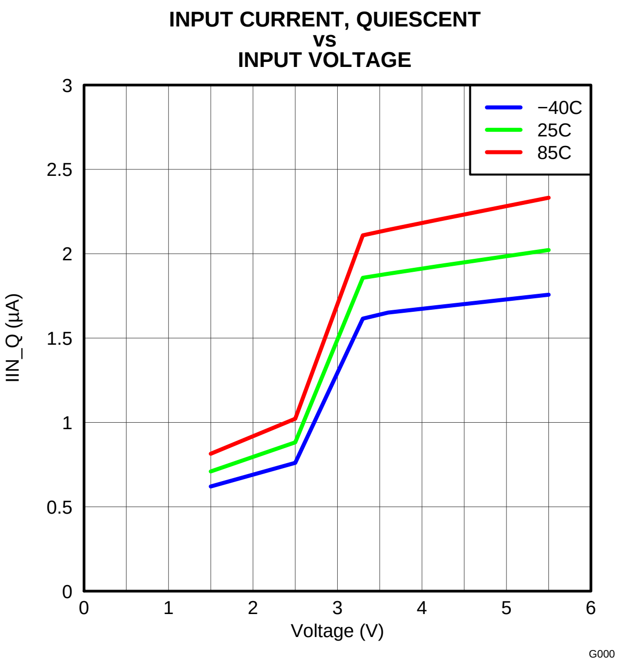


Figure 4.

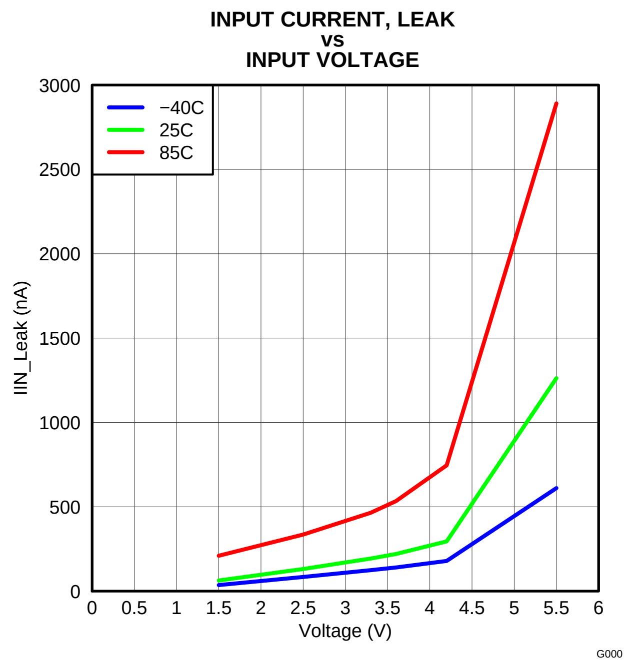


Figure 5.

TYPICAL CHARACTERISTICS (continued)

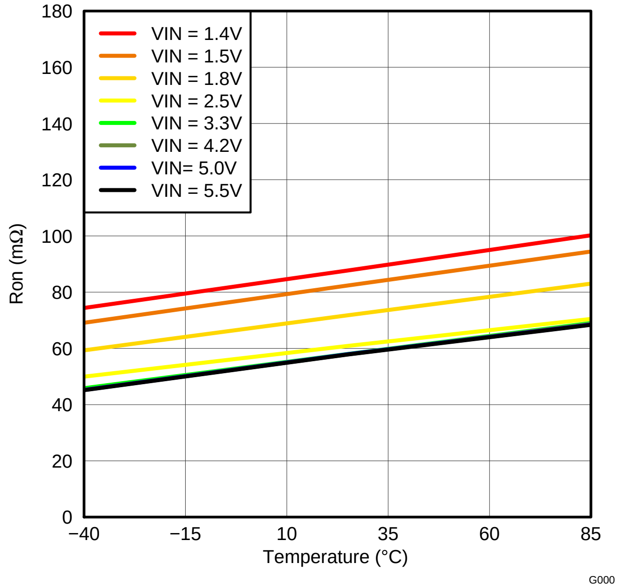


Figure 6.

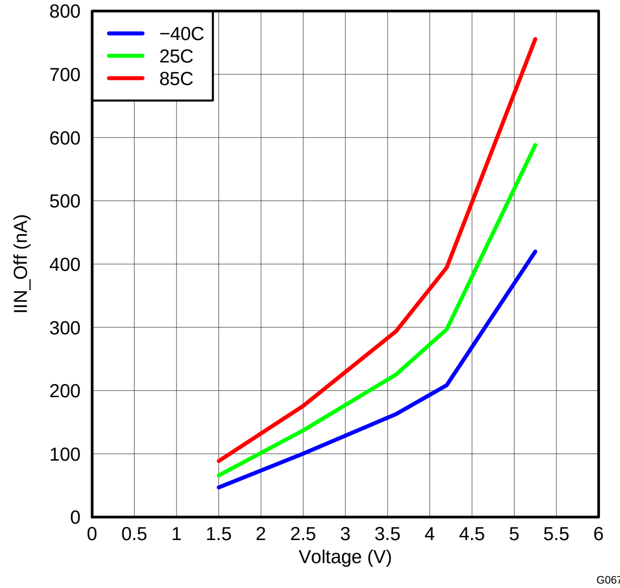


Figure 7.

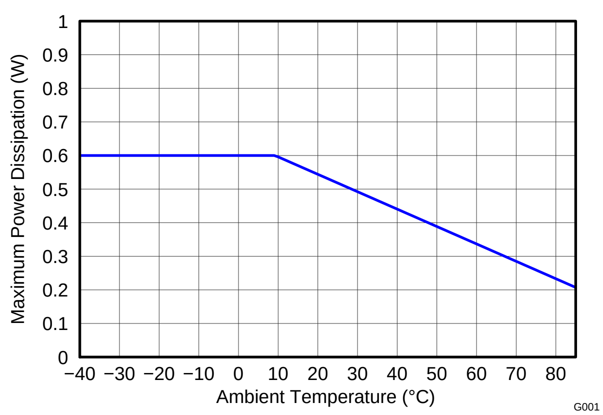


Figure 8. Allowable Power Dissipation

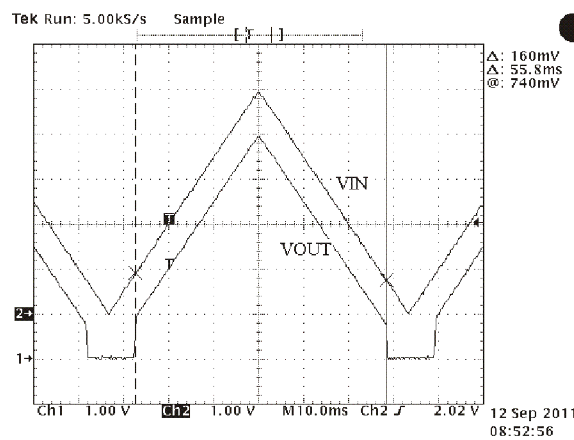


Figure 9. ULVO Response I_{OUT} = -100mA

TYPICAL CHARACTERISTICS (continued)

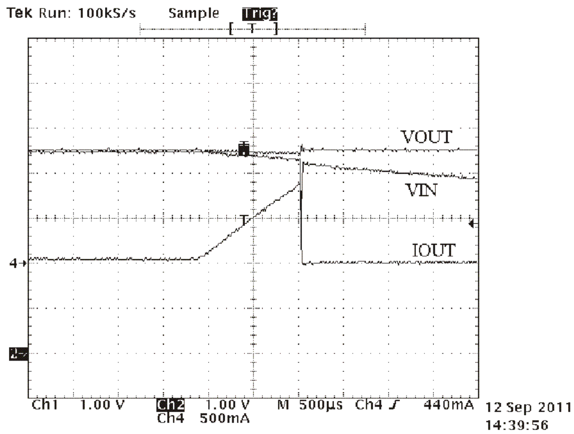


Figure 10. Reverse Current Protection V_{OUT} = 3.3V, V_{IN} = 3.3V Decreasing to 0V

TYPICAL SWITCHING CHARACTERISTICS FOR TPS22910A

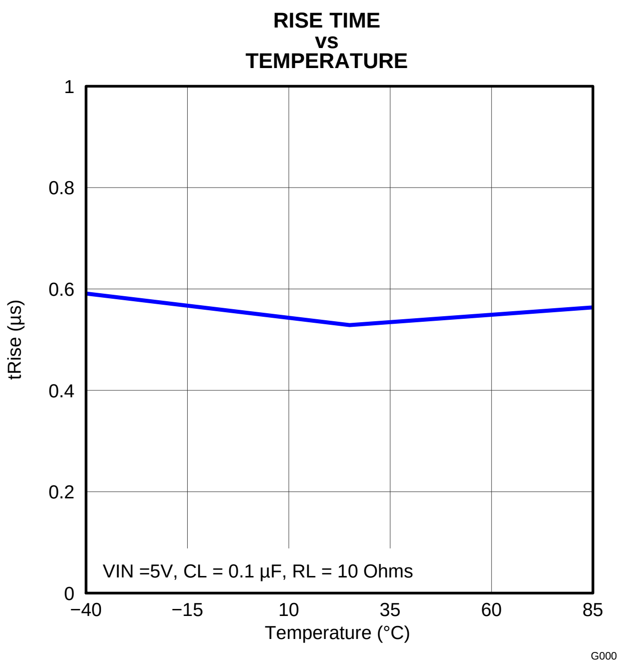


Figure 11.

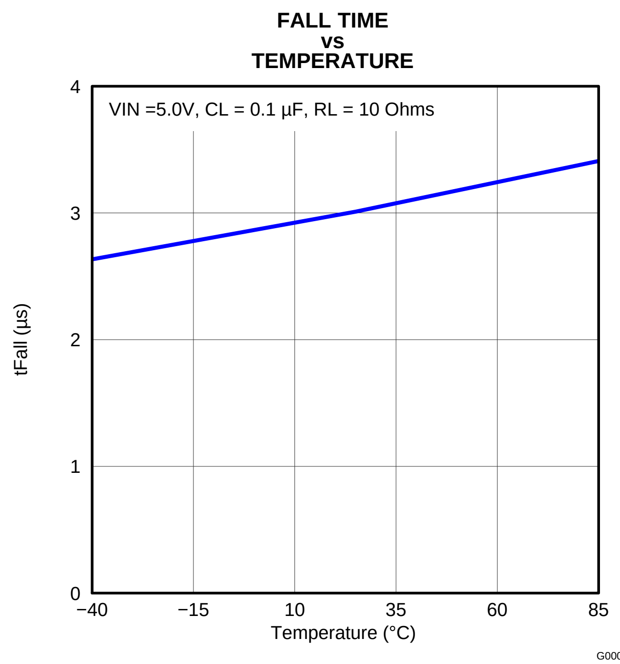


Figure 12.

TYPICAL CHARACTERISTICS (continued)

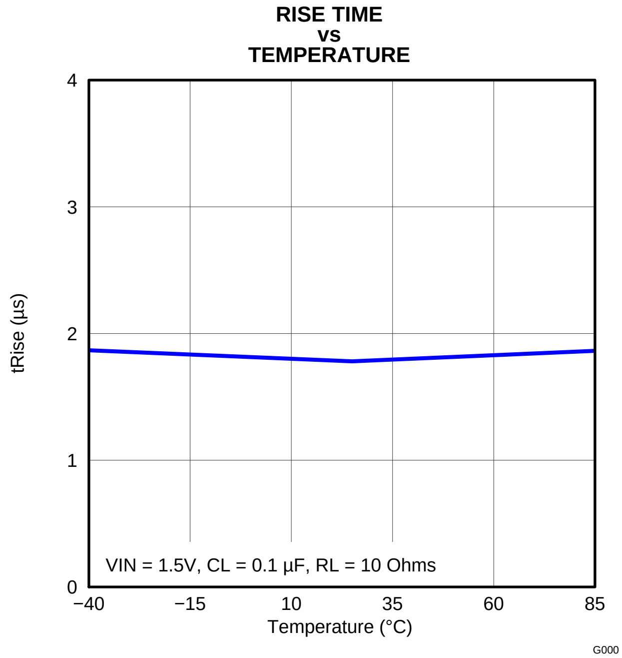


Figure 13.

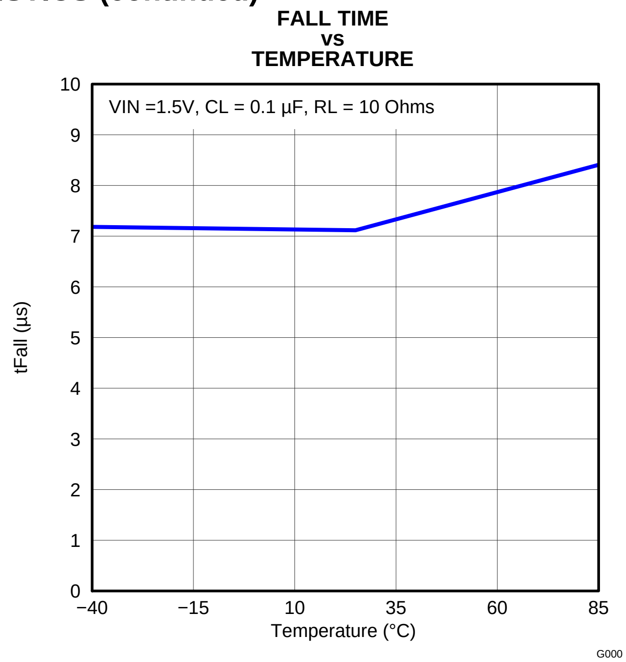


Figure 14.

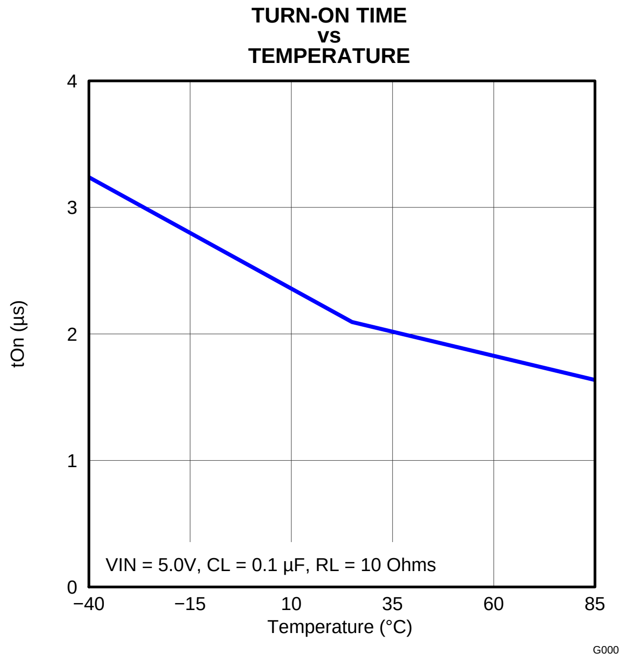


Figure 15.

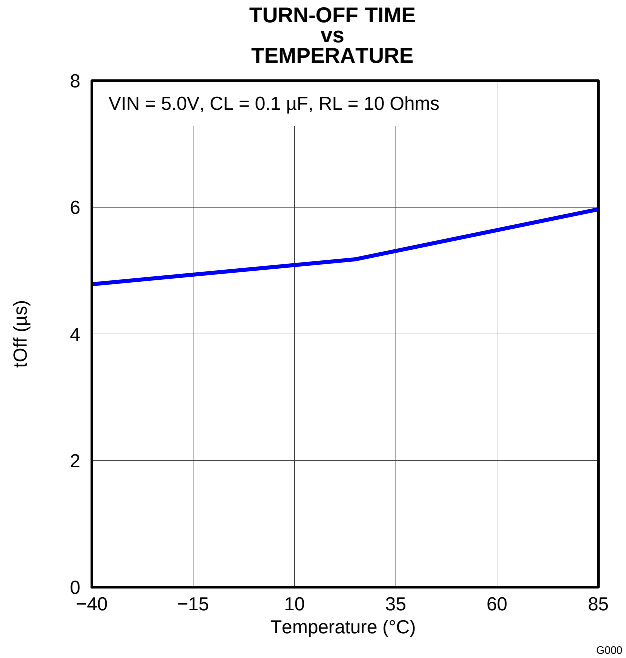


Figure 16.

TYPICAL CHARACTERISTICS (continued)

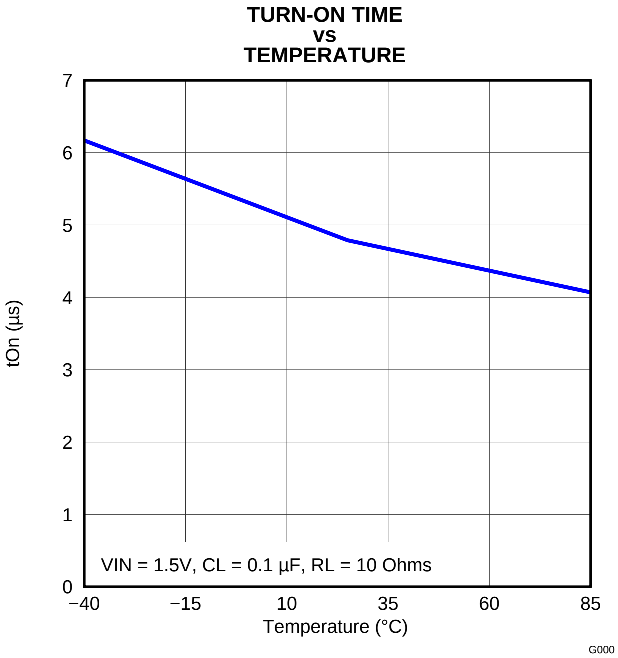


Figure 17.

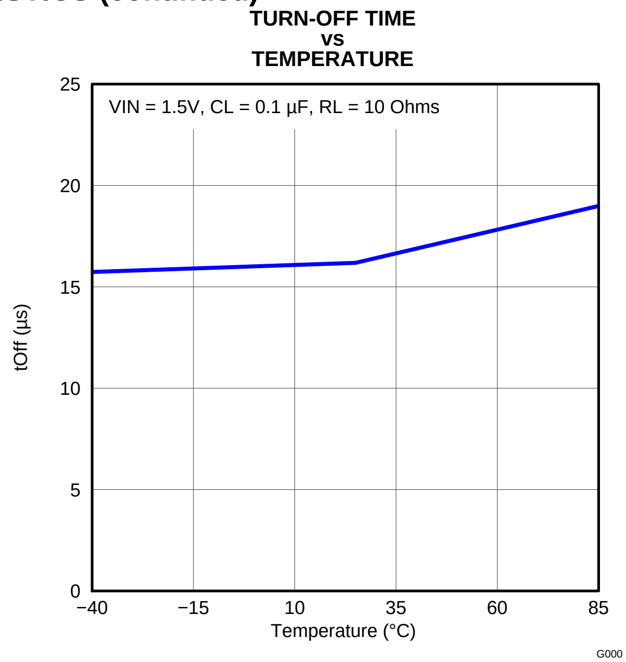


Figure 18.

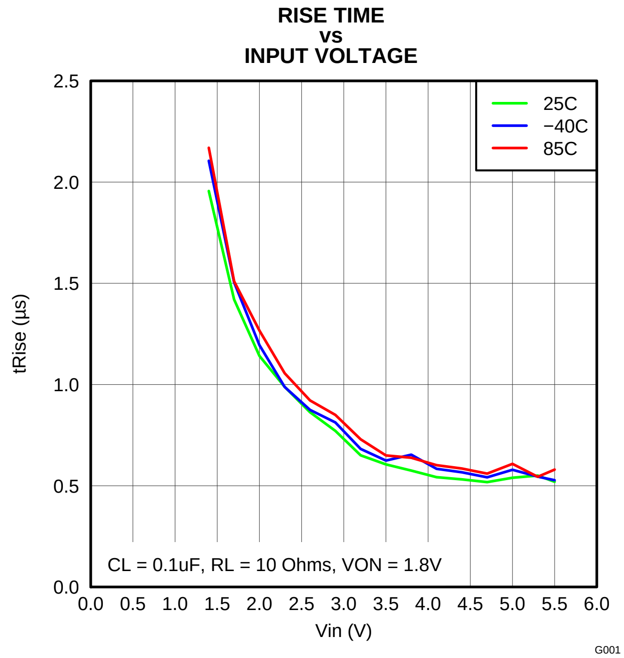


Figure 19.

TYPICAL CHARACTERISTICS (continued)

TURN-ON RESPONSE
V_{IN} = 5V, T_A = 25°C, C_{IN} = 10µF, C_L = 0.1µF, R_L = 10Ω
CH1: V_{OUT}, CH2: ON

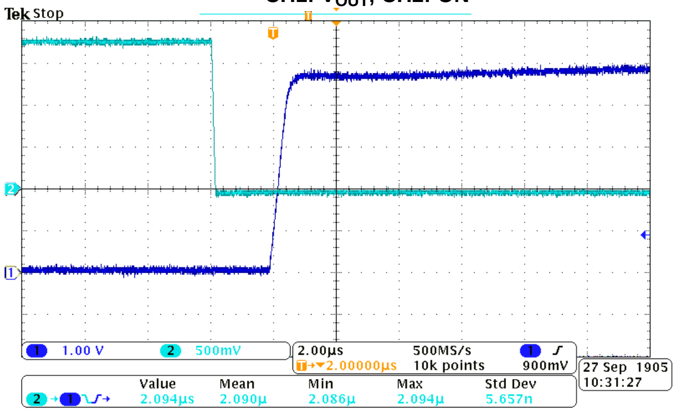


Figure 20.

TURN-OFF RESPONSE
V_{IN} = 5V, T_A = 25°C, C_{IN} = 10µF, C_L = 0.1µF, R_L = 10Ω
CH1: V_{OUT}, CH2: ON

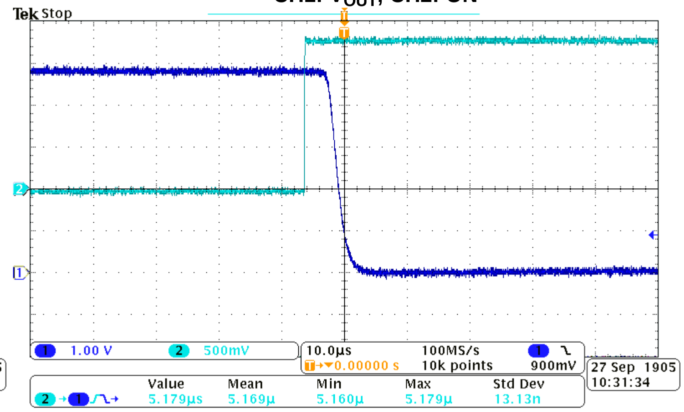


Figure 21.

TURN-ON RESPONSE TIME
V_{IN} = 5V, T_A = 25°C, C_{IN} =10µF, C_L = 1µF, R_L = 10Ω
CH1: V_{OUT}, CH2: ON

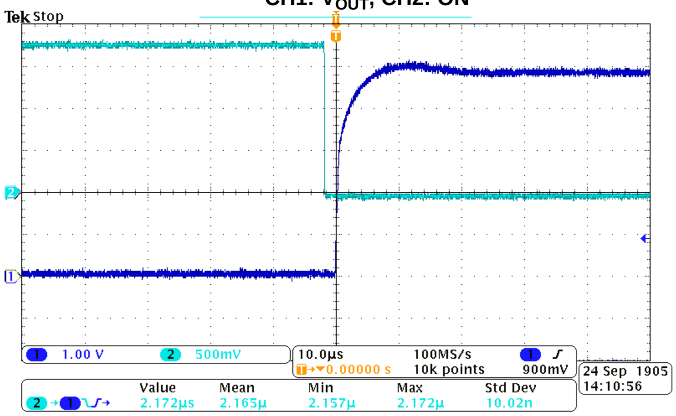


Figure 22.

TURN-OFF RESPONSE TIME
V_{IN} = 5V, T_A = 25°C, C_{IN} = 10µF, C_L = 1µF, R_L = 10Ω
CH1: V_{OUT}, CH2: ON

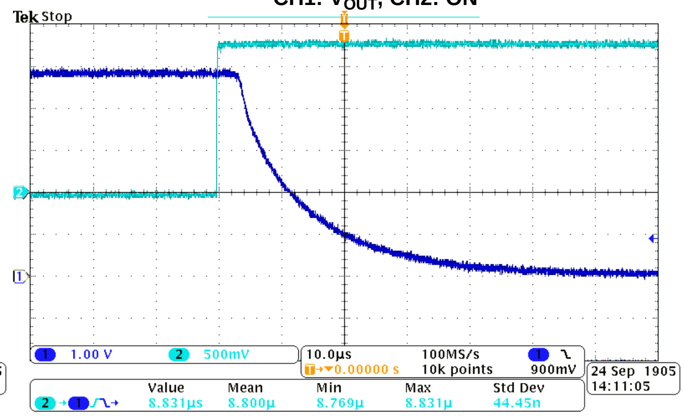


Figure 23.

TURN-ON RESPONSE TIME
V_{IN} = 1.5V, T_A = 25°C, C_{IN} = 10µF, C_L = 0.1µF, R_L = 10Ω
CH1: V_{OUT}, CH2: ON

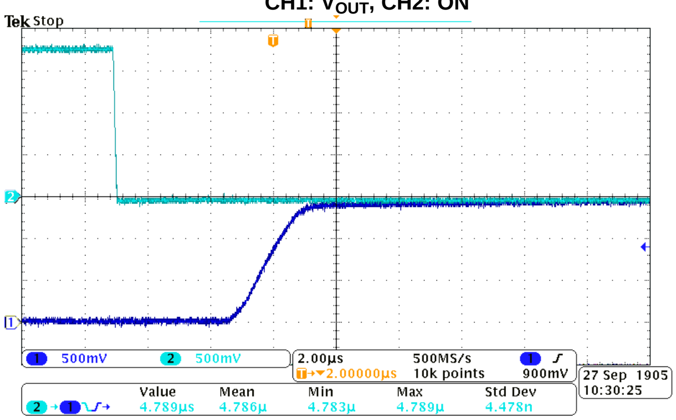


Figure 24.

TURN-OFF RESPONSE TIME
V_{IN} = 1.5V, T_A = 25°C, C_{IN} = 10µF, C_L = 0.1µF, R_L = 10Ω
CH1: V_{OUT}, CH2: ON

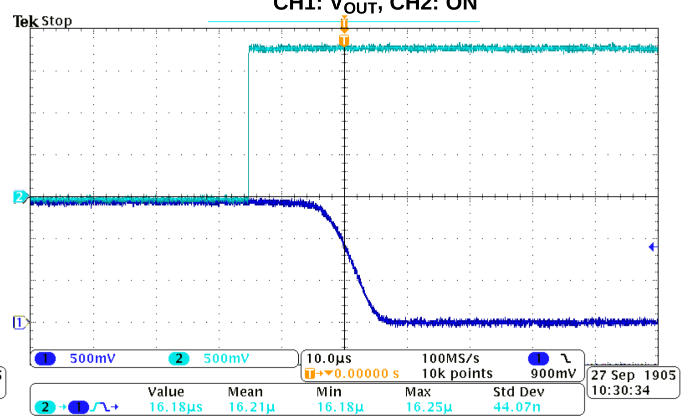


Figure 25.

TYPICAL CHARACTERISTICS (continued)

TURN-ON RESPONSE TIME
V_{IN} = 1.5V, T_A = 25°C, C_{IN} = 10µF, C_L = 1µF, R_L = 10Ω
CH1: V_{OUT}, CH2: ON

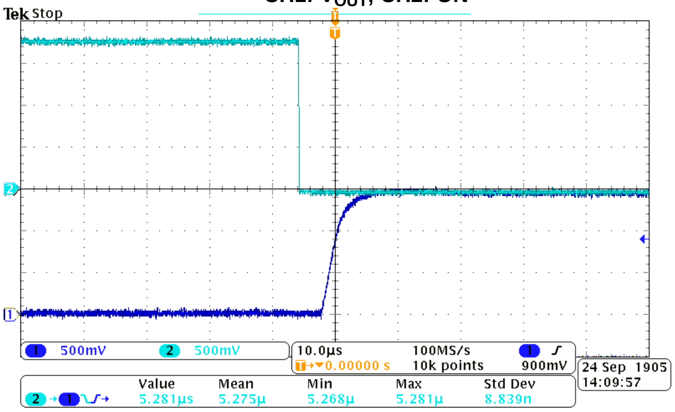


Figure 26.

TURN-OFF RESPONSE TIME
V_{IN} = 1.5V, T_A = 25°C, C_{IN} = 10µF, C_L = 1µF, R_L = 10Ω
CH1: V_{OUT}, CH2: ON

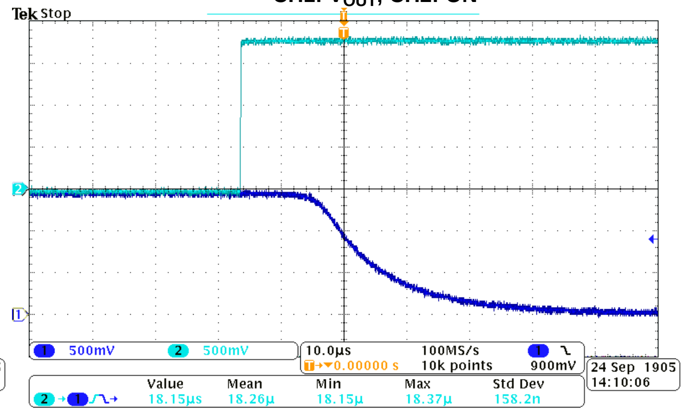


Figure 27.

APPLICATION INFORMATION

On/Off Control

The ON pin controls the state of the switch. Asserting ON low enables the switch (ON is active low). The ON pin is compatible with standard GPIO logic threshold. It can be used with any microcontroller with 1.2-V, 1.8-V, 2.5-V, 3.3-V, or 5.5-V GPIO.

Input Capacitor

To limit the voltage drop on the input supply caused by transient inrush currents, when the switch turns on into a discharged load capacitor or short-circuit, a capacitor needs to be placed between VIN and GND. A 1-μF ceramic capacitor, C_{IN}, placed close to the pins is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop.

Output Capacitor

A C_{IN} to C_L ratio of 10 to 1 is recommended for minimizing V_{IN} dip caused by inrush currents during startup. Devices with faster rise times may require a larger ratio to minimize V_{IN} dip.

Under-Voltage Lockout

Under-voltage lockout protection turns off the switch if the input voltage drops below the under-voltage lockout threshold (UVLO). With the ON pin active, the input voltage rising above the under-voltage lockout threshold will cause a controlled turn-on of the switch to limit current over-shoot.

Full-Time Reverse Current Protection

In a scenario where V_{OUT} is greater than V_{IN}, there is potential for reverse current to flow through the pass FET or the body diode. The TPS22910 monitors VIN and VOUT voltage levels. When the reverse current voltage threshold (V_{RCP}) is exceeded, the switch is disabled (within 10μs typ). Additionally, the body diode is disengaged so as to prevent any reverse current flow to VIN. The pass FET, and the output voltage (V_{OUT}), will resume normal operation when the reverse current scenario is no longer present. The peak instantaneous reverse current is the current it takes to trip the reverse current protection. After the reverse current protection has tripped due to the peak instantaneous reverse current, the DC (off-state) leakage current from VOUT and VIN is referred to as I_{RCP}(leak) (see Figure 28).

Use the following formula to calculate the amount of peak instantaneous reverse current for a particular application:

$$I_{RC} = \frac{V_{RCP}}{r_{ON(VIN)}}$$

Where,

I_{RC} is the amount of reverse current,

$r_{ON(VIN)}$ is the on-resistance at the VIN of the reverse current condition.

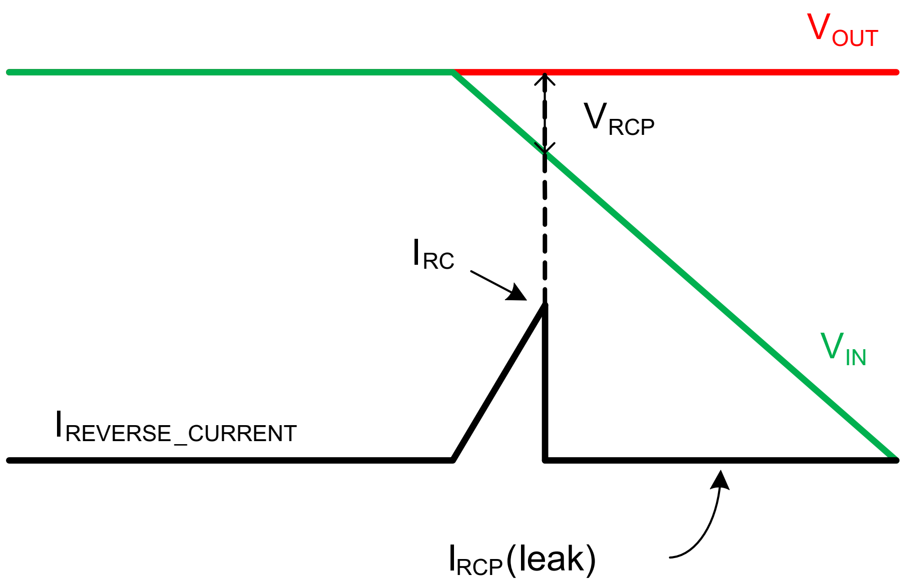


Figure 28. Reverse Current

Board Layout

For best performance, all traces should be as short as possible. To be most effective, the input and output capacitors should be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for V_{IN}, V_{OUT}, and GND helps minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance.

REVISION HISTORY

Changes from Original (November 2011) to Revision A	Page
• Deleted Quick Output Discharge Transistor from FEATURES.	1

Changes from Revision A (March 2012) to Revision B	Page
• Changed "active high" description for ON pin to "active low" in PIN FUNCTIONS table.	2

Changes from Revision B (April 2012) to Revision C	Page
• Updated FEATURES	1
• Updated FEATURES to Full-Time Reverse Current Protection.	1
• Added additional applications.	1
• Updated TYPICAL APPLICATION diagram.	1
• Updated RON (typ) a 3.3 V values in Feature List.	1
• Updated V_{IH}	4
• Updated TEST CONDITIONS for $I_{IN(off)}$ PARAMETER in ELECTRICAL CHARACTERISTICS table.	5
• Changed V_{RVP} to V_{RCP}	5
• Added $I_{RCP(leak)}$	5
• Updated INPUT CURRENT, OFF vs INPUT VOLTAGE graph	8

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS22910AYZVR	ACTIVE	DSBGA	YZV	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	75	Samples
TPS22910AYZVT	ACTIVE	DSBGA	YZV	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	75	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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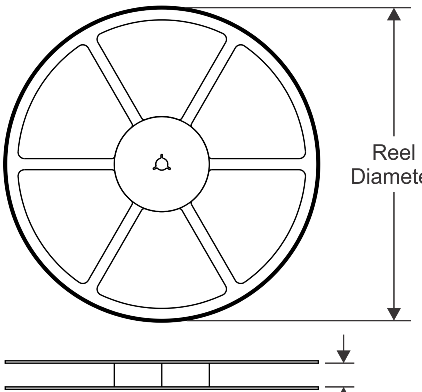
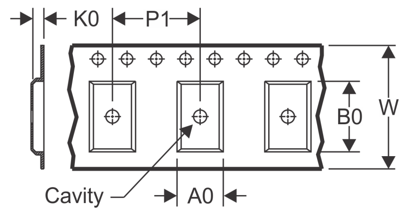
TAPE AND REEL INFORMATION

REEL DIMENSIONS

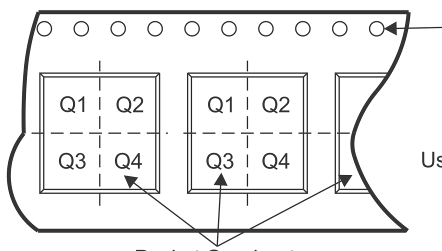


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

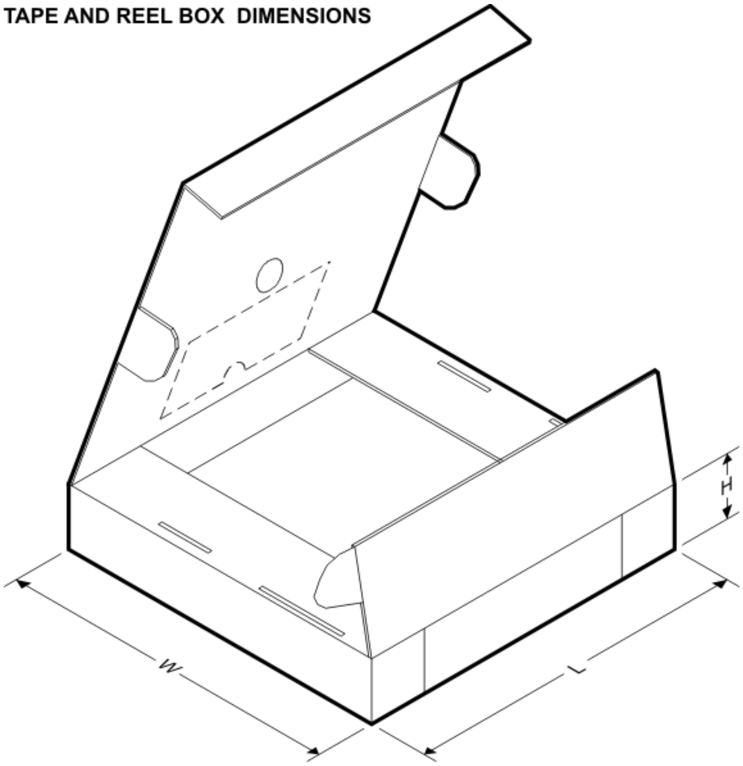
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22910AYZVR	DSBGA	YZV	4	3000	178.0	9.2	1.0	1.0	0.63	4.0	8.0	Q1
TPS22910AYZVT	DSBGA	YZV	4	250	178.0	9.2	1.0	1.0	0.63	4.0	8.0	Q1

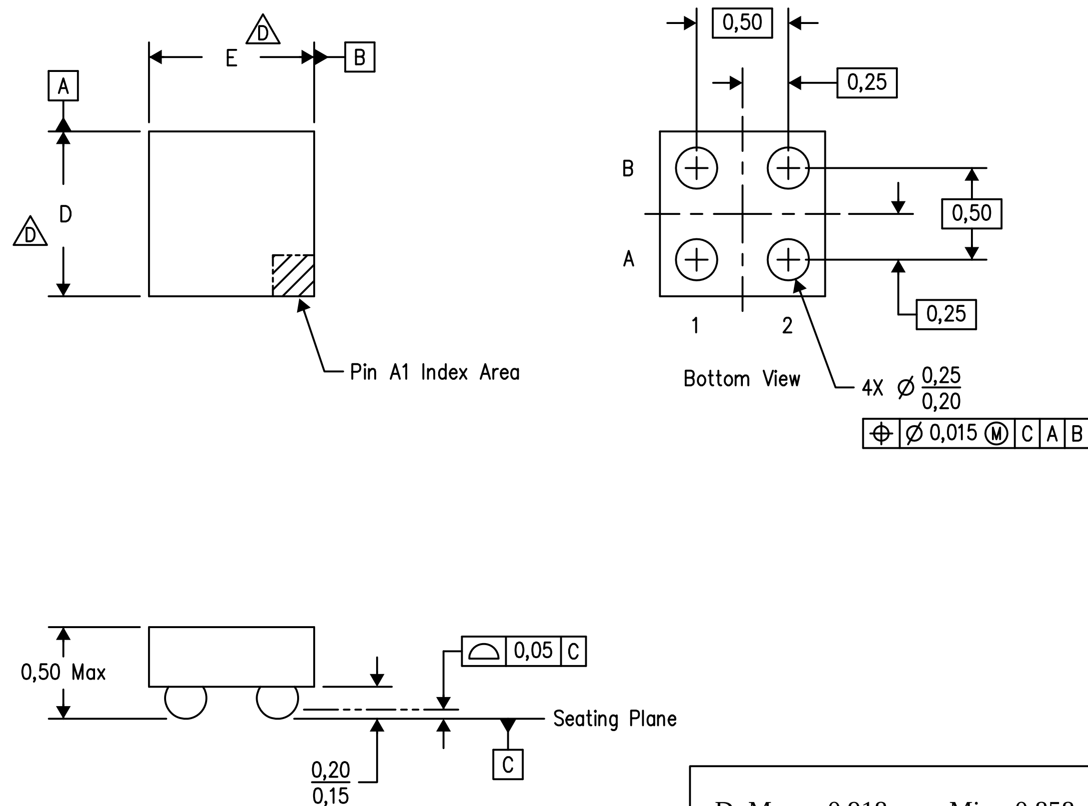
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22910AYZVR	DSBGA	YZV	4	3000	220.0	220.0	35.0
TPS22910AYZVT	DSBGA	YZV	4	250	220.0	220.0	35.0

YZV (S−XBGA−N4) DIE−SIZE BALL GRID ARRAY



D: Max = 0.918 mm, Min =0.858 mm

E: Max = 0.918 mm, Min =0.858 mm

4206083/B 04/13

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. NanoFree™ package configuration.
- D. The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative.
- E. Reference Product Data Sheet for array population. 2 x 2 matrix pattern is shown for illustration only.
- F. This package contains Pb−free balls. Refer to the 4 YEV package (drawing 4206082) for tin−lead (SnPb) balls.

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