DUAL CHANNEL PRECISION ADJUSTABLE CURRENT-LIMITED POWER SWITCH

Check for Samples: TPS2561-Q1

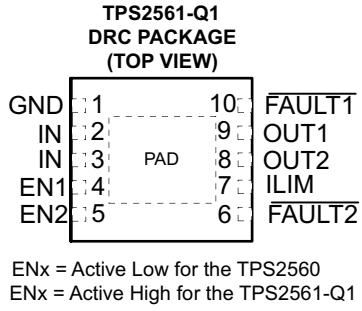
FEATURES

- **Qualified for Automotive Applications**
- **Two Separate Current Limiting Channels**
- **Meets USB Current-Limiting Requirements**
- **Adjustable Current Limit, 250 mA–2.8 A (typ)**
- **± 7.5% Current-Limit Accuracy at 2.8 A**
- **Fast Overcurrent Response - 3.5-µS (typ)**
- **Two 44-mΩ High-Side MOSFETs**
- **Operating Range: 2.5 V to 6.5 V**
- **2-µA Maximum Standby Supply Current**
- **Built-in Soft-Start**
- **15 kV or 8 kV System-Level ESD Capable**
- **UL Listed – File No. E169910**
- **CB and Nemko Certified**

DESCRIPTION

The TPS2561-Q1 is a dual-channel power-distribution switch intended for applications where precision current limiting is required or heavy capacitive loads and short circuits are encountered. These devices offer a programmable current-limit threshold between 250 mA and 2.8 A (typ) per channel through an external resistor. The power-switch rise and fall times are controlled to minimize current surges during turn on or off.

Each channel of the TPS2561-Q1 device limits the output current to a safe level by switching into a constant-current mode when the output load exceeds the current-limit threshold. The FAULTx logic output for each channel independently asserts low during overcurrent and over temperature conditions.



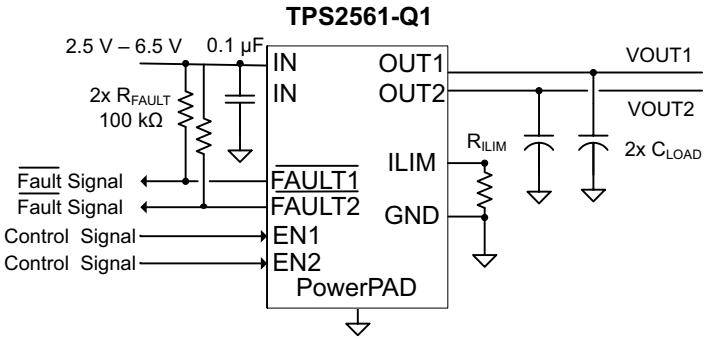


Figure 1. Typical Application as USB Power Switch

GENERAL SWITCH CATALOG

33 mΩ, single	80 mΩ, single	80 mΩ, dual	80 mΩ, dual	80 mΩ, triple	80 mΩ, quad	80 mΩ, quad
TPS201xA 0.2 A - 2 A TPS202x 0.2 A - 2 A TPS203x 0.2 A - 2 A	TPS2014 600 mA TPS2015 1 A TPS2041B 500 mA TPS2051B 500 mA TPS2045A 250 mA TPS2049 100 mA TPS2055A 250 mA TPS2061 1 A TPS2065 1 A TPS2068 1.5 A TPS2069 1.5 A	TPS2042B 500 mA TPS2052B 500 mA TPS2046B 250 mA TPS2056 250 mA TPS2062 1 A TPS2066 1 A TPS2060 1.5 A TPS2064 1.5 A	TPS2080 500 mA TPS2081 500 mA TPS2082 500 mA TPS2090 250 mA TPS2091 250 mA TPS2092 250 mA	TPS2043B 500 mA TPS2053B 500 mA TPS2047B 250 mA TPS2057A 250 mA TPS2063 1 A TPS2067 1 A	TPS2044B 500 mA TPS2054B 500 mA TPS2048A 250 mA TPS2058 250 mA	TPS2085 500 mA TPS2086 500 mA TPS2087 500 mA TPS2095 250 mA TPS2096 250 mA TPS2097 250 mA

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PowerPAD is a trademark of Texas Instruments.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

T_A (2)	PACKAGE		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	SON - DRC	Reel of 3000	TPS2561QDRCRQ1	PXPQ

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Maximum ambient temperature is a function of device junction temperature and system level considerations, such as power dissipation and board layout. See *dissipation rating table* and *recommended operating conditions* for specific information related to these devices.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1) (2)

			VALUE	UNIT
	Voltage range on IN, OUTx, ENx or $\overline{\text{ENx}}$, ILIM, $\overline{\text{FAULTx}}$		–0.3 to 7	V
	Voltage range from IN to OUTx		–7 to 7	V
	Continuous output current		Internally Limited	
	Continuous total power dissipation		See the Dissipation Rating Table	
	Continuous $\overline{\text{FAULTx}}$ sink current		25	mA
	ILIM source current		Internally Limited	mA
	ESD	HBM	2	kV
		CDM	1000	V
	ESD – system level (contact/air)(3)		8/15	kV
T_J	Maximum junction temperature		–40 to 125(4)	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Voltages are referenced to GND unless otherwise noted.
(3) Surges per EN61000-4-2, 1999 applied between USB and output ground of the TPS2561EVM (HPA424) evaluation module (documentation available on the web.) These were the test level, not the failure threshold.
(4) Ambient over temperature shutdown threshold

DISSIPATION RATING TABLE

BOARD	PACKAGE	THERMAL RESISTANCE(1) θ_{JA}	THERMAL RESISTANCE θ_{JC}	$T_A \le 25°C$ POWER RATING
High-K(2)	DRC	41.6°C/W	10.7°C/W	2403 mW

(1) Mounting per the *PowerPAD™ Thermally Enhanced Package* application report (SLMA002)
(2) The JEDEC high-K (2s2p) board used to derive this data was a 3in × 3in, multilayer board with 1-ounce internal power and ground planes and 2-ounce copper traces on top and bottom of the board.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
V_{IN}	Input voltage, IN	2.5	6.5	V
V_{ENx} / $V_{/ENx}$	Enable voltage	0	6.5	V
V_{IH}	High-level input voltage on ENx or $\overline{ENx}$	1.1		V
V_{IL}	Low-level input voltage on ENx or $\overline{ENx}$		0.66	V
I_{OUTx}	Continuous output current per channel, OUTx	0	2.5	A
	Continuous $\overline{FAULTx}$ sink current	0	10	mA
T_J	Operating virtual junction temperature	–40	125	°C
R_{ILIM}	Recommended resistor limit range	20	187	kΩ

ELECTRICAL CHARACTERISTICS

over recommended operating conditions, $V_{/ENx}$ = 0 V, or V_{ENx} = V_{IN} (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]		MIN	TYP	MAX	UNIT
POWER SWITCH							
$r_{DS(on)}$	Static drain-source on-state resistance per channel, IN to OUTx[2]	T_J = 25 °C			44	50	mΩ
		–40 °C ≤T_J ≤125 °C				79	
t_r	Rise time, output[2]	V_{IN} = 6.5 V	C_{Lx} = 1 µF, R_{Lx} = 100 Ω, (see Figure 2)	2	3	4	ms
		V_{IN} = 2.5 V		1	2	3	
t_f	Fall time, output[2]	V_{IN} = 6.5 V		0.6	0.8	1	
		V_{IN} = 2.5 V		0.4	0.6	0.8	
ENABLE INPUT EN OR $\overline{EN}$							
	Enable pin turn on/off threshold			0.66		1.1	V
	Hysteresis				55[3]		mV
I_{EN}	Input current	V_{ENx} = 0 V or 6.5 V, $V_{/ENx}$ = 0 V or 6.5 V		–0.5		0.5	µA
t_{on}	Turn-on time[2]	C_{Lx} = 1 µF, R_{Lx} = 100 Ω, (see Figure 2)				9	ms
t_{off}	Turn-off time[2]					6	ms
CURRENT LIMIT							
I_{OS}	Current-limit threshold per channel (Maximum DC output current I_{OUTx} delivered to load) and Short-circuit current, OUTx connected to GND		R_{ILIM} = 20 kΩ	2590	2800	3005	mA
			R_{ILIM} = 61.9 kΩ	800	900	1005	
			R_{ILIM} = 100 kΩ	470	560	645	
t_{IOS}	Response time to short circuit	V_{IN} = 5.0 V (see Figure 3)			3.5[3]		µs

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.
(2) Not production tested.
(3) These parameters are provided for reference only, and do not constitute part of TI's published specifications for purposes of TI's product warranty.

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating conditions, $V_{/ENx}$ = 0 V, or V_{ENx} = V_{IN} (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]		MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I_{IN_off}	Supply current, low-level output	V_{IN} = 6.5 V, No load on OUTx, V $\overline{ENx}$ = 6.5 V or V_{ENx} = 0 V			0.1	2	µA
I_{IN_on}	Supply current, high-level output	V_{IN} = 6.5 V, No load on OUT	R_{ILIM} = 20 kΩ		100	125	µA
			R_{ILIM} = 100 kΩ		85	110	µA
I_{REV}	Reverse leakage current	V_{OUTx} = 6.5 V, V_{IN} = 0 V	T_J = 25°C		0.01	1	µA
UNDERVOLTAGE LOCKOUT							
UVLO	Low-level input voltage, IN	V_{IN} rising, T_J = 25°C			2.35	2.45	V
	Hysteresis, IN	T_J = 25°C			35		mV
$\overline{FAULTx}$ FLAG							
V_{OL}	Output low voltage, $\overline{FAULTx}$	I $\overline{FAULTx}$ = 1 mA, $\overline{FAULTx}$ assertion or de-assertion due to overcurrent condition				180	mV
	Off-state leakage	V $\overline{FAULTx}$ = 6.5 V				1	µA
	$\overline{FAULTx}$ deglitch	I $\overline{FAULTx}$ = 1 mA, $\overline{FAULTx}$ assertion or de-assertion due to overcurrent condition		6	9	13	ms
THERMAL SHUTDOWN							
OTSD2	Thermal shutdown threshold[4]			155			°C
OTSD	Thermal shutdown threshold in current-limit[4]			135			°C
	Hysteresis				20[5]		°C

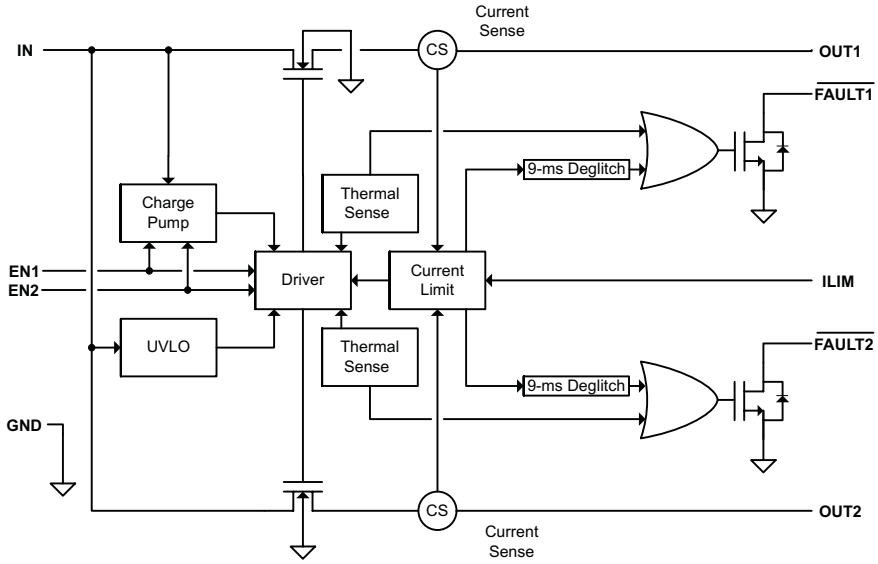
(4) Not production tested.
(5) These parameters are provided for reference only, and do not constitute part of TI's published specifications for purposes of TI's product warranty.

DEVICE INFORMATION

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
$\overline{EN1}$	-	I	Enable input, logic low turns on channel one power switch
EN1	4	I	Enable input, logic high turns on channel one power switch
$\overline{EN2}$	-	I	Enable input, logic low turns on channel two power switch
EN2	5	I	Enable input, logic high turns on channel two power switch
GND	1		Ground connection; connect externally to PowerPAD
IN	2, 3	I	Input voltage; connect a 0.1 µF or greater ceramic capacitor from IN to GND as close to the IC as possible.
$\overline{FAULT1}$	10	O	Active-low open-drain output, asserted during overcurrent or overtemperature condition on channel one.
$\overline{FAULT2}$	6	O	Active-low open-drain output, asserted during overcurrent or overtemperature condition on channel two
OUT1	9	O	Power-switch output for channel one
OUT2	8	O	Power-switch output for channel two
ILIM	7	O	External resistor used to set current-limit threshold; recommended 20 kΩ ≤ R_{ILIM} ≤ 187 kΩ.
PowerPAD™	PAD		Internally connected to GND; used to heat-sink the part to the circuit board traces. Connect PowerPAD to GND pin externally.

FUNCTIONAL BLOCK DIAGRAM



PARAMETER MEASUREMENT INFORMATION

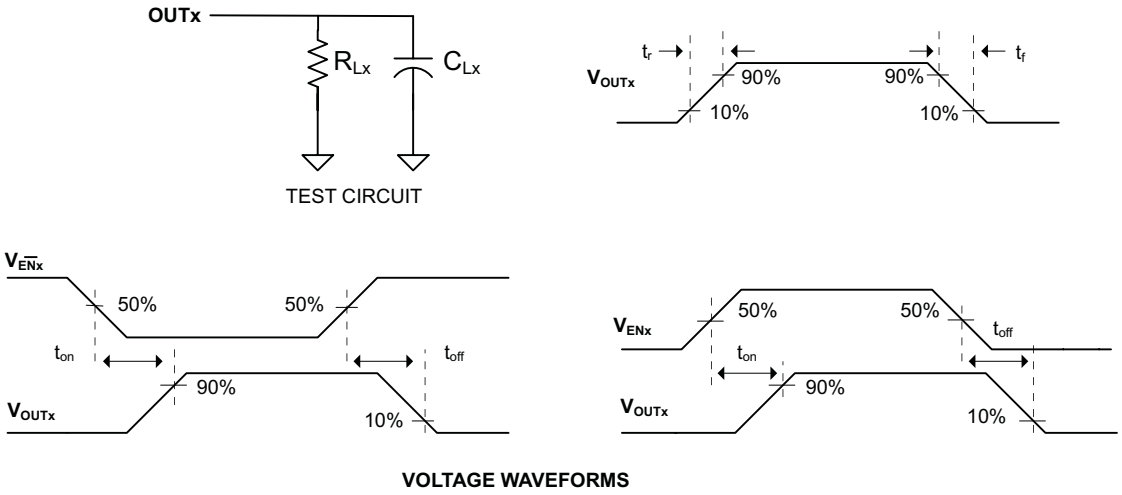


Figure 2. Test Circuit and Voltage Waveforms

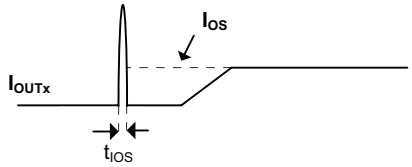


Figure 3. Response Time to Short Circuit Waveform

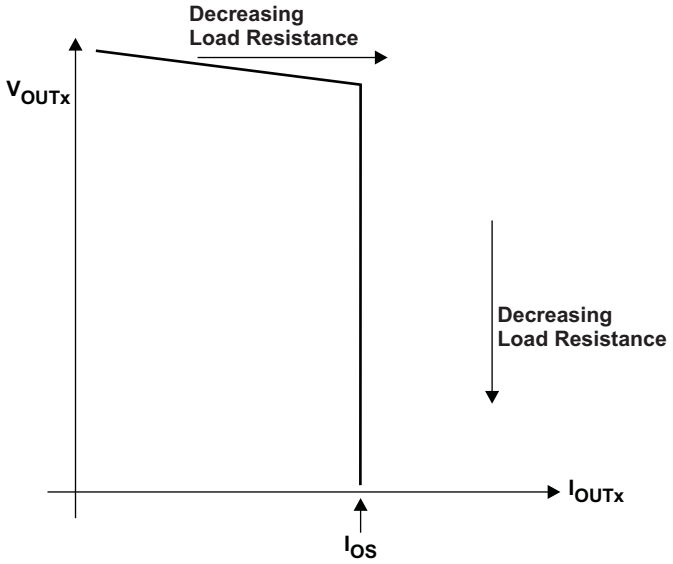


Figure 4. Output Voltage vs. Current-Limit Threshold

TYPICAL CHARACTERISTICS

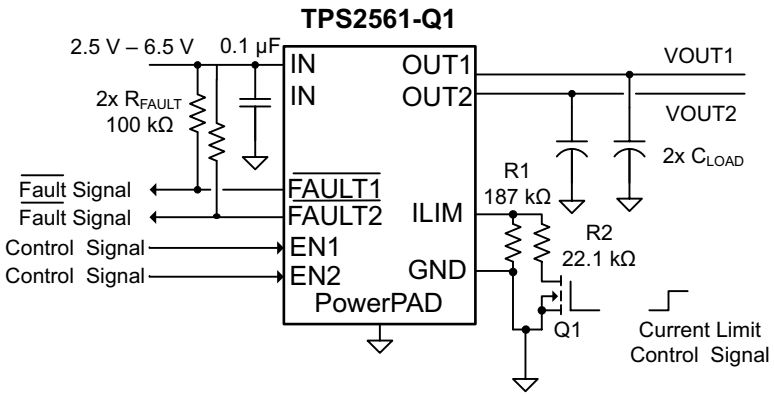


Figure 5. Typical Characteristics Reference Schematic

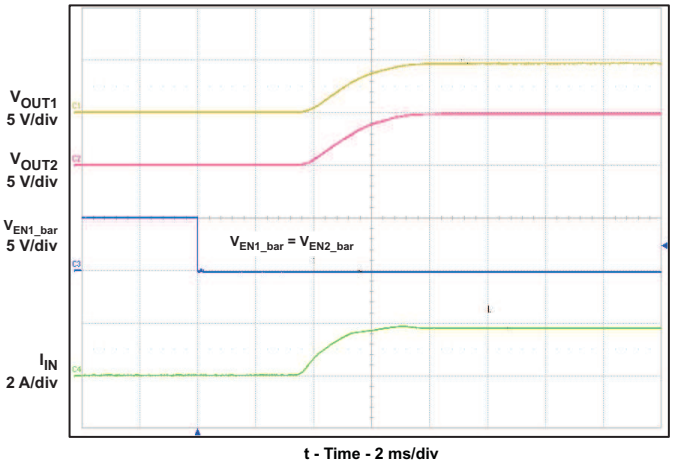


Figure 6. Turn-on Delay and Rise Time

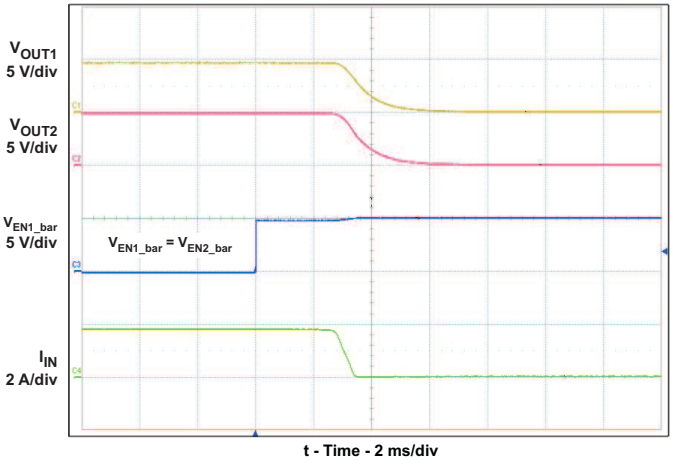


Figure 7. Turn-off Delay and Fall Time

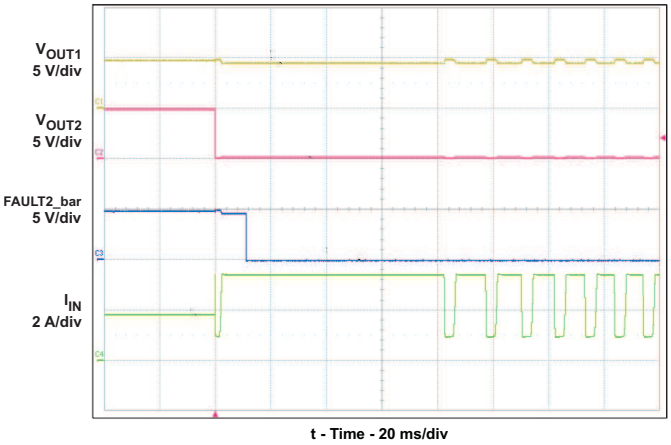


Figure 8. Full-Load to Short-Circuit Transient Response

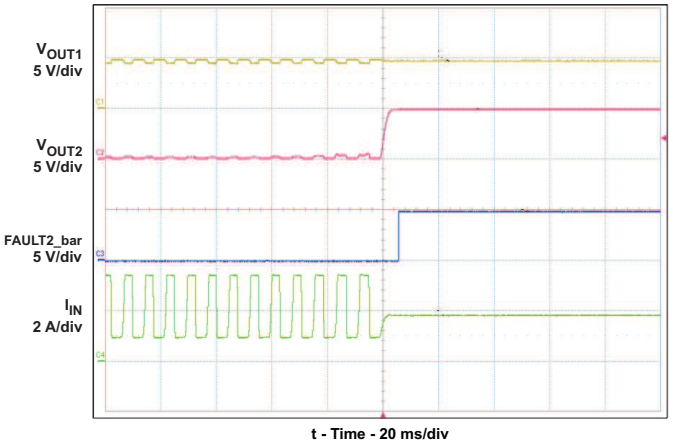


Figure 9. Short-Circuit to Full-Load Recovery Response

TYPICAL CHARACTERISTICS (continued)

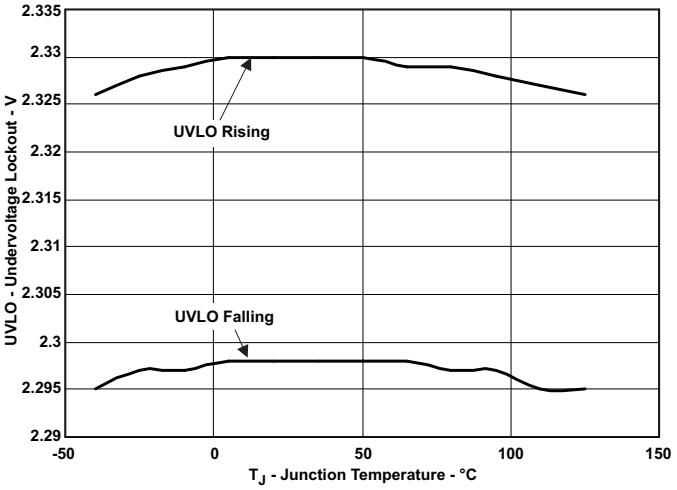


Figure 10. UVLO – Undervoltage Lockout – V

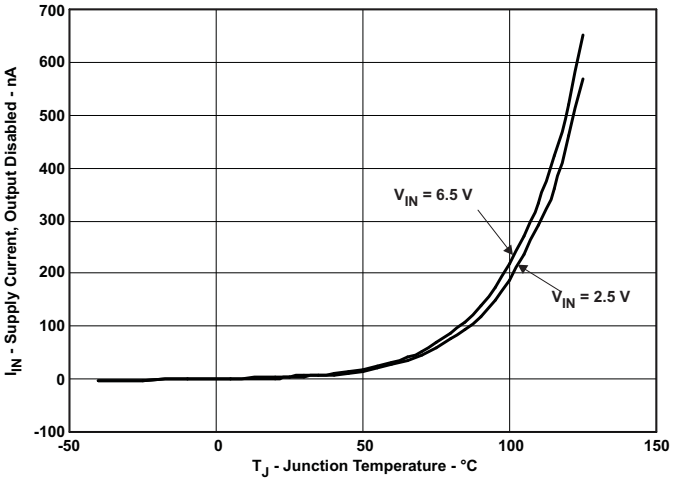


Figure 11. I_{IN} – Supply Current, Output Disabled – nA

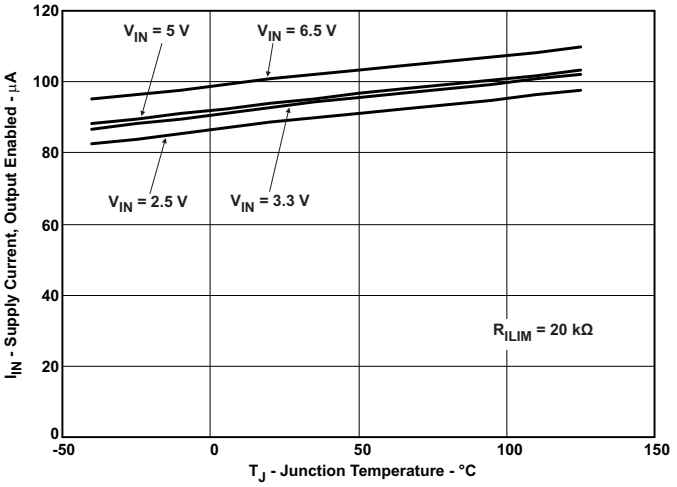


Figure 12. I_{IN} – Supply Current, Output Enabled – µA

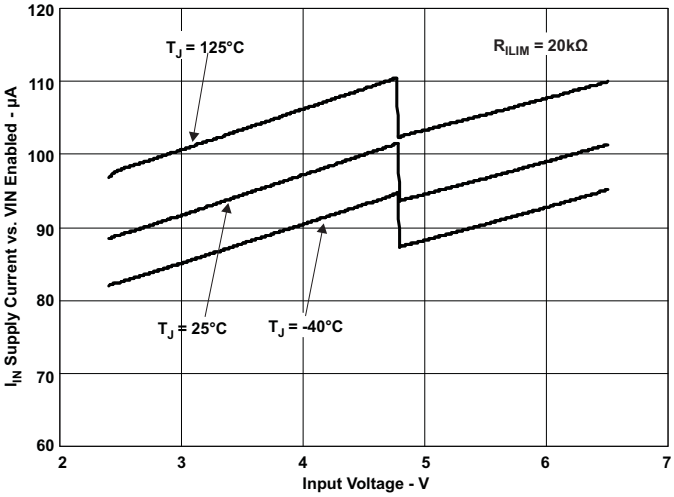


Figure 13. I_{IN} – Supply Current, Output Enabled – µA

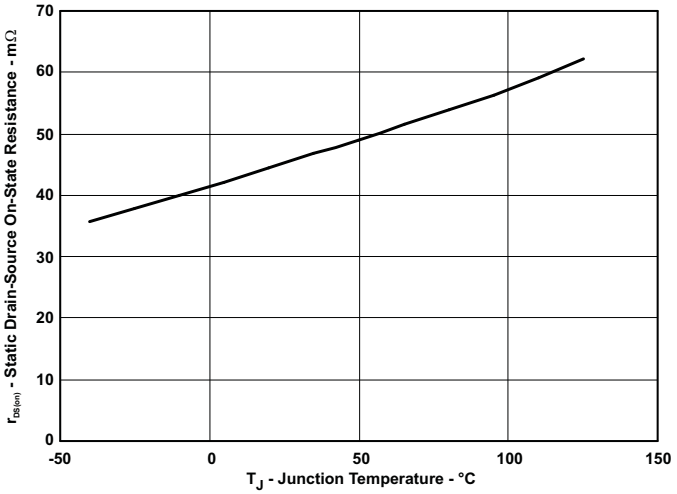


Figure 14. MOSFET $r_{DS(on)}$ vs. Junction Temperature

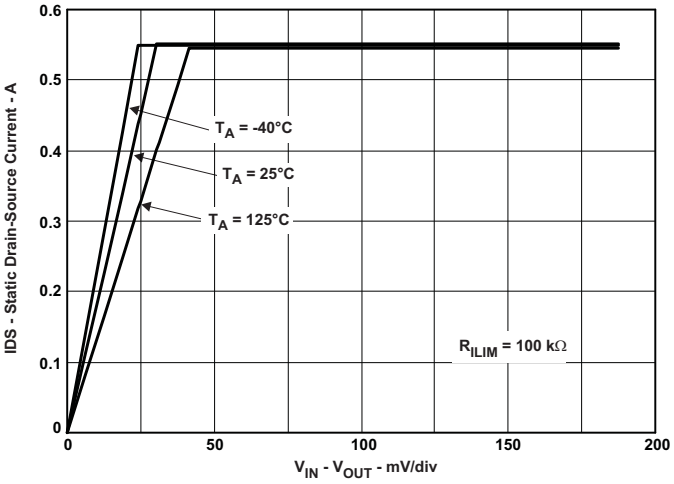


Figure 15. Switch Current vs. Drain-Source Voltage Across Switch

TYPICAL CHARACTERISTICS (continued)

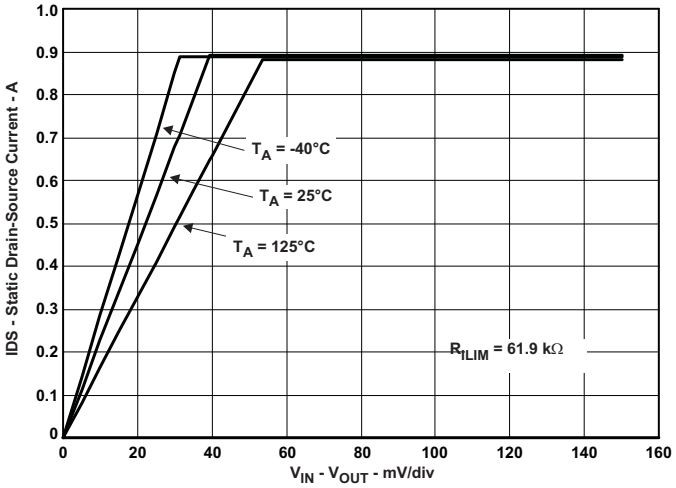


Figure 16. Switch Current vs. Drain-Source Voltage Across Switch

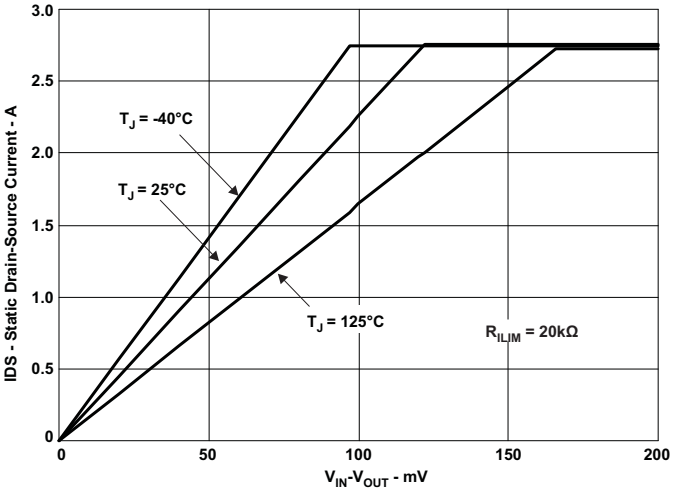


Figure 17. Switch Current vs. Drain-Source Voltage Across Switch

DETAILED DESCRIPTION

OVERVIEW

The TPS2561-Q1 is a dual-channel, current-limited power-distribution switch using N-channel MOSFETs for applications where short circuits or heavy capacitive loads are encountered. This device allows the user to program the current-limit threshold between 250 mA and 2.8 A (typ) per channel through an external resistor. This device incorporates an internal charge pump and gate drive circuitry necessary to drive the N-channel MOSFETs. The charge pump supplies power to the driver circuit for each channel and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 2.5 V and requires little supply current. The driver controls the gate voltage of the power switch. The driver incorporates circuitry that controls the rise and fall times of the output voltage to limit large current and voltage surges and provides built-in soft-start functionality. Each channel of the TPS2561-Q1 limits the output current to the programmed current-limit threshold I_{OS} during an overcurrent or short-circuit event by reducing the charge pump voltage driving the N-channel MOSFET and operating it in the linear range of operation. The result of limiting the output current to I_{OS} reduces the output voltage at OUTx because the N-channel MOSFET is no longer fully enhanced.

OVERCURRENT CONDITIONS

The TPS2561-Q1 responds to overcurrent conditions by limiting the output current per channel to I_{OS}. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Two possible overload conditions can occur.

The first condition is when a short circuit or partial short circuit is present when the device is powered-up or enabled. The output voltage is held near zero potential with respect to ground and the TPS2561-Q1 ramps the output current to I_{OS}. The TPS2561-Q1 devices will limit the current to I_{OS} until the overload condition is removed or the device begins to thermal cycle.

The second condition is when a short circuit, partial short circuit, or transient overload occurs while the device is enabled and powered on. The device responds to the overcurrent condition within time t_{IOS} (see Figure 3). The current-sense amplifier is overdriven during this time and momentarily disables the internal current-limit MOSFET. The current-sense amplifier recovers and ramps the output current to I_{OS}. Similar to the previous case, the TPS2561-Q1 device limits the current to I_{OS} until the overload condition is removed or the device begins to thermal cycle.

The TPS2561-Q1 thermal cycles if an overload condition is present long enough to activate thermal limiting in any of the above cases. The device turns off when the junction temperature exceeds 135°C (min) while in current limit. The device remains off until the junction temperature cools 20°C (typ) and then restarts. The TPS2561-Q1 cycles on and off until the overload is removed (see Figure 9) .

$\overline{\text{FAULTx}}$ RESPONSE

The $\overline{\text{FAULTx}}$ open-drain outputs are asserted (active low) on an individual channel during an overcurrent or overtemperature condition. The TPS2561-Q1 asserts the $\overline{\text{FAULTx}}$ signal until the fault condition is removed and the device resumes normal operation on that channel. The TPS2561-Q1 is designed to eliminate false $\overline{\text{FAULTx}}$ reporting by using an internal delay deglitch circuit (9-ms typ) for overcurrent conditions without the need for external circuitry. This ensures that $\overline{\text{FAULTx}}$ is not accidentally asserted due to normal operation such as starting into a heavy capacitive load. The deglitch circuitry delays entering and leaving current-limited induced fault conditions. The $\overline{\text{FAULTx}}$ signal is not deglitched when the MOSFET is disabled due to an overtemperature condition but is deglitched after the device has cooled and begins to turn on. This unidirectional deglitch prevents $\overline{\text{FAULTx}}$ oscillation during an overtemperature event.

UNDERVOLTAGE LOCKOUT (UVLO)

The undervoltage lockout (UVLO) circuit disables the power switch until the input voltage reaches the UVLO turn-on threshold. Built-in hysteresis prevents unwanted on and off cycling due to input voltage droop during turn on.

ENABLE ($\overline{\text{ENx}}$ OR ENx)

The logic enables control the power switches and device supply current. The supply current is reduced to less than 2-µA when a logic high is present on $\overline{\text{ENx}}$ or when a logic low is present on ENx. A logic low input on $\overline{\text{ENx}}$ or a logic high input on ENx enables the driver, control circuits, and power switches. The enable inputs are compatible with both TTL and CMOS logic levels.

THERMAL SENSE

The TPS2561-Q1 self protects by using two independent thermal sensing circuits that monitor the operating temperature of the power switch and disable operation if the temperature exceeds recommended operating conditions. Each channel of the TPS2561-Q1 operates in constant-current mode during an overcurrent conditions, which increases the voltage drop across the power switch. The power dissipation in the package is proportional to the voltage drop across the power switch, which increases the junction temperature during an overcurrent condition. The first thermal sensor (OTSD) turns off the individual power switch channel when the die temperature exceeds 135°C (min) and the channel is in current limit. Hysteresis is built into the thermal sensor, and the switch turns on after the device has cooled approximately 20°C.

The TPS2561-Q1 also has a second ambient thermal sensor (OTSD2). The ambient thermal sensor turns off both power switch channels when the die temperature exceeds 155°C (min) regardless of whether the power switch channels are in current limit and will turn on the power switches after the device has cooled approximately 20°C. The TPS2561-Q1 continues to cycle off and on until the fault is removed.

APPLICATION INFORMATION

INPUT AND OUTPUT CAPACITANCE

Input and output capacitance improves the performance of the device; the actual capacitance should be optimized for the particular application. For all applications, a 0.1-µF or greater ceramic bypass capacitor between IN and GND is recommended as close to the device as possible for local noise decoupling. This precaution reduces ringing on the input due to power-supply transients. Additional input capacitance may be needed on the input to reduce voltage overshoot from exceeding the absolute maximum voltage of the device during heavy transient conditions. This is especially important during bench testing when long, inductive cables are used to connect the evaluation board to the bench power supply.

Output capacitance is not required, but placing a high-value electrolytic capacitor on the output pin is recommended when large transient currents are expected on the output.

PROGRAMMING THE CURRENT-LIMIT THRESHOLD

The overcurrent threshold is user programmable through an external resistor, R_{ILIM}. R_{ILIM} sets the current-limit threshold for both channels. The TPS2561-Q1 use an internal regulation loop to provide a regulated voltage on the ILIM pin. The current-limit threshold is proportional to the current sourced out of ILIM. The recommended 1% resistor range for R_{ILIM} is 20 kΩ ≤ R_{ILIM} ≤ 187 kΩ to ensure stability of the internal regulation loop. Many applications require that the minimum current limit is above a certain current level or that the maximum current limit is below a certain current level, so it is important to consider the tolerance of the overcurrent threshold when selecting a value for R_{ILIM}. The following equations calculates the resulting overcurrent threshold for a given external resistor value (R_{ILIM}). The traces routing the R_{ILIM} resistor to the TPS2561-Q1 should be as short as possible to reduce parasitic effects on the current-limit accuracy.

$$I_{OSmax}\ (mA) = \frac{52850\ V}{R_{ILIM}^{0.957}\ k\Omega}$$

$$I_{OSnom}\ (mA) = \frac{56000\ V}{R_{ILIM}\ k\Omega}$$

$$I_{OSmin}\ (mA) = \frac{61200\ V}{R_{ILIM}^{1.056}\ k\Omega} \quad (1)$$

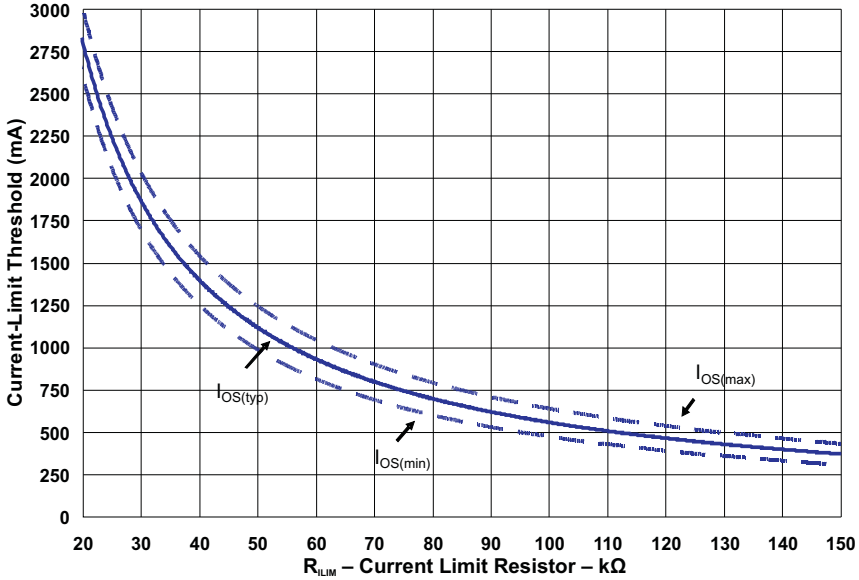


Figure 18. Current-Limit Threshold vs. R_{ILIM}

APPLICATION 1: DESIGNING ABOVE A MINIMUM CURRENT LIMIT

Some applications require that current limiting cannot occur below a certain threshold. For this example, assume that 2 A must be delivered to the load so that the minimum desired current-limit threshold is 2000 mA. Use the I_{OS} equations and Figure 18 to select R_{ILIM}.

$$I_{OSmin}\ (mA) = 2000\ mA$$

$$I_{OSmin}\ (mA) = \frac{61200\ V}{R_{ILIM}^{1.056}\ k\Omega}$$

$$R_{ILIM}\ (k\Omega) = \left(\frac{61200\ V}{I_{OSmin}\ mA}\right)^{\frac{1}{1.056}}$$

$$R_{ILIM}\ (k\Omega) = 25.52\ k\Omega \quad (2)$$

Select the closest 1% resistor less than the calculated value: R_{ILIM} = 25.5 kΩ. This sets the minimum current-limit threshold at 2 A . Use the I_{OS} equations, Figure 18, and the previously calculated value for R_{ILIM} to calculate the maximum resulting current-limit threshold.

$$R_{ILIM}\ (k\Omega) = 25.52\ k\Omega$$

$$I_{OSmax}\ (mA) = \frac{52850\ V}{R_{ILIM}^{0.957}\ k\Omega}$$

$$I_{OSmax}\ (mA) = \frac{52850\ V}{25.5^{0.957}\ k\Omega}$$

$$I_{OSmax}\ (mA) = 2382\ mA \quad (3)$$

The resulting maximum current-limit threshold is 2382 mA with a 25.5-kΩ resistor.

APPLICATION 2: DESIGNING BELOW A MAXIMUM CURRENT LIMIT

Some applications require that current limiting must occur below a certain threshold. For this example, assume that the desired upper current-limit threshold must be below 1000 mA to protect an up-stream power supply. Use the I_{OS} equations and Figure 18 to select R_{ILIM}.

$$I_{OSmax}\ (mA) = 1000\ mA$$

$$I_{OSmax}\ (mA) = \frac{52850\ V}{R_{ILIM}^{0.957}\ k\Omega}$$

$$R_{ILIM}\ (k\Omega) = \left(\frac{52850\ V}{I_{OSmax}\ mA}\right)^{\frac{1}{0.957}}$$

$$R_{ILIM}\ (k\Omega) = 63.16\ k\Omega \quad (4)$$

Select the closest 1% resistor greater than the calculated value: R_{ILIM} = 63.4 kΩ. This sets the maximum current-limit threshold at 1000 mA . Use the I_{OS} equations, Figure 18, and the previously calculated value for R_{ILIM} to calculate the minimum resulting current-limit threshold.

$$R_{ILIM}\ (k\Omega) = 63.4\ k\Omega$$

$$I_{OSmin}\ (mA) = \frac{61200\ V}{R_{ILIM}^{1.056}\ k\Omega}$$

$$I_{OSmin}\ (mA) = \frac{61200\ V}{63.4^{1.056}\ k\Omega}$$

$$I_{OSmin}\ (mA) = 765\ mA \quad (5)$$

The resulting minimum current-limit threshold is 765 mA with a 63.4-kΩ resistor.

ACCOUNTING FOR RESISTOR TOLERANCE

The previous sections described the selection of R_{ILIM} given certain application requirements and the importance of understanding the current-limit threshold tolerance. The analysis focused only on the TPS2561-Q1 performance and assumed an exact resistor value. However, resistors sold in quantity are not exact and are bounded by an upper and lower tolerance centered around a nominal resistance. The additional R_{ILIM} resistance tolerance directly affects the current-limit threshold accuracy at a system level. The following table shows a process that accounts for worst-case resistor tolerance assuming 1% resistor values. Step one follows the selection process outlined in the application examples above. Step two determines the upper and lower resistance bounds of the selected resistor. Step three uses the upper and lower resistor bounds in the I_{OS} equations to calculate the threshold limits. It is important to use tighter tolerance resistors, for example, 0.5% or 0.1%, when precision current limiting is desired.

Table 1. Common R_{ILIM} Resistor Selections

Desired Nominal Current Limit (mA)	Ideal Resistor (kΩ)	Closest 1% Resistor (kΩ)	Resistor Tolerance		Actual Limits		
			1% low (kΩ)	1% high (kΩ)	IOS MIN (mA)	IOS Nom (mA)	IOS MAX (mA)
300	186.7	187	185.1	188.9	241.6	299.5	357.3
400	140	140	138.6	141.4	328	400	471.4
600	93.3	93.1	92.2	94	504.6	601.5	696.5
800	70	69.8	69.1	70.5	684	802.3	917.6
1000	56	56.2	55.6	56.8	859.9	996.4	1129.1
1200	46.7	46.4	45.9	46.9	1052.8	1206.9	1356.3
1400	40	40.2	39.8	40.6	1225	1393	1555.9
1600	35	34.8	34.5	35.1	1426.5	1609.2	1786.2
1800	31.1	30.9	30.6	31.2	1617.3	1812.3	2001.4
2000	28	28	27.7	28.3	1794.7	2000	2199.3
2200	25.5	25.5	25.2	25.8	1981	2196.1	2405.3
2400	23.3	23.2	23	23.4	2188.9	2413.8	2633
2600	21.5	21.5	21.3	21.7	2372.1	2604.7	2831.9
2800	20	20	19.8	20.2	2560.4	2800	3034.8

POWER DISSIPATION AND JUNCTION TEMPERATURE

The low on-resistance of the N-channel MOSFET allows small surface-mount packages to pass large currents. It is good design practice to estimate power dissipation and junction temperature. The below analysis gives an approximation for calculating junction temperature based on the power dissipation in the package. However, it is important to note that thermal analysis is strongly dependent on additional system level factors. Such factors include air flow, board layout, copper thickness and surface area, and proximity to other devices dissipating power. Good thermal design practice must include all system level factors in addition to individual component analysis.

Begin by determining the $r_{DS(on)}$ of the N-channel MOSFET relative to the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read $r_{DS(on)}$ from the typical characteristics graph. Using this value, the power dissipation can be calculated by:

$$P_D = (R_{DS(on)} \times I_{OUT1}^2) + (R_{DS(on)} \times I_{OUT2}^2)$$

Where:

P_D = Total power dissipation (W)

$r_{DS(on)}$ = Power switch on-resistance of one channel (Ω)

I_{OUTx} = Maximum current-limit threshold set by R_{ILIM}(A)

This step calculates the total power dissipation of the N-channel MOSFET.

Finally, calculate the junction temperature:

$$T_J = P_D \times \theta_{JA} + T_A$$

Where:

T_A = Ambient temperature (°C)

θ_{JA} = Thermal resistance (°C/W)

P_D = Total power dissipation (W)

Compare the calculated junction temperature with the initial estimate. If they are not within a few degrees, repeat the calculation using the refined $r_{DS(on)}$ from the previous calculation as the new estimate. Two or three iterations are generally sufficient to achieve the desired result. The final junction temperature is highly dependent on thermal resistance θ_{JA}, and thermal resistance is highly dependent on the individual package and board layout. The Dissipating Rating Table provides example thermal resistances for specific packages and board layouts.

AUTO-RETRY FUNCTIONALITY

Some applications require that an overcurrent condition disables the part momentarily during a fault condition and re-enables after a pre-set time. This auto-retry functionality can be implemented with an external resistor and capacitor. During a fault condition, FAULTx pulls ENx low disabling the part. The part is disabled when ENx is pulled below the turn-off threshold, and FAULTx goes high impedance allowing C_{RETRY} to begin charging. The part re-enables when the voltage on ENx reaches the turn-on threshold, and the auto-retry time is determined by the resistor/capacitor time constant. The part will continue to cycle in this manner until the fault condition is removed.

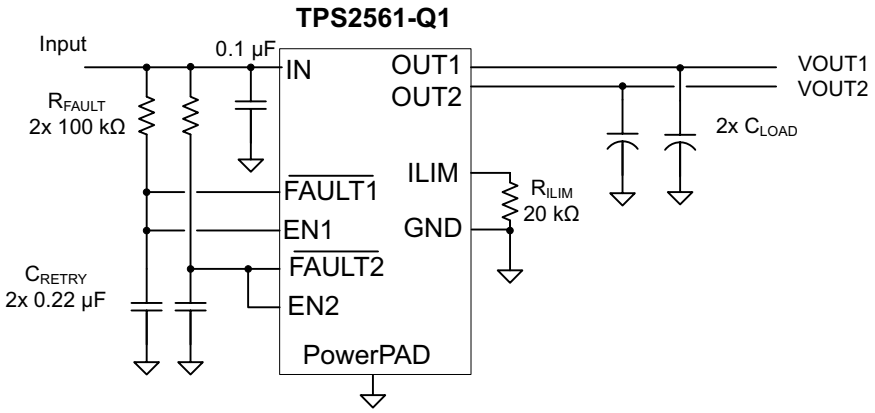


Figure 19. Auto-Retry Functionality

Some applications require auto-retry functionality and the ability to enable or disable with an external logic signal. The figure below shows how an external logic signal can drive EN through R_{FAULT} and maintain auto-retry functionality. The resistor/capacitor time constant determines the auto-retry time-out period.

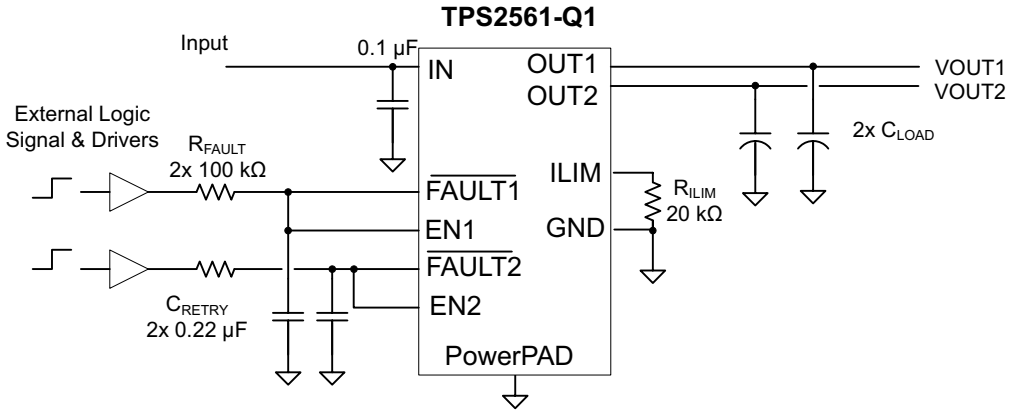


Figure 20. Auto-Retry Functionality With External EN Signal

TWO-LEVEL CURRENT-LIMIT CIRCUIT

Some applications require different current-limit thresholds depending on external system conditions. Figure 21 shows an implementation for an externally controlled, two-level current-limit circuit. The current-limit threshold is set by the total resistance from ILIM to GND (see previously discussed *Programming the Current-Limit Threshold* section). A logic-level input enables or disables MOSFET Q1 and changes the current-limit threshold by modifying the total resistance from ILIM to GND. Additional MOSFET and resistor combinations can be used in parallel to Q1 and R2 to increase the number of additional current-limit levels.

NOTE

ILIM should never be driven directly with an external signal.

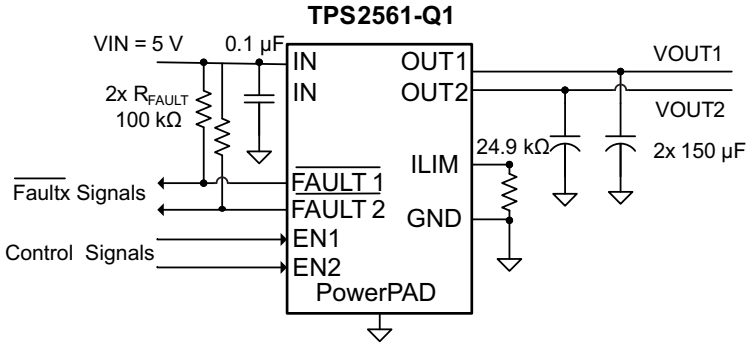


Figure 21. Two-Level Current-Limit Circuit

REVISION HISTORY

Changes from Original (December 2011) to Revision A **Page**

- Changed the revision to A, August 2012 and aligned FEATURES and DESCRIPTION to top aligned 1
- Changed part number from TPS2561 to TPS2561-Q1 in all images where part number appears. 2
- Changed the First 2 rows of TYP and MAX columns of the ELEC CHAR table from 110 / 290 to 44 / 50, second row 320 / 79 and added cross reference to second column 'Not producton tested.' 3

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TPS2561QDRCRQ1	ACTIVE	SON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

OTHER QUALIFIED VERSIONS OF TPS2561-Q1 :

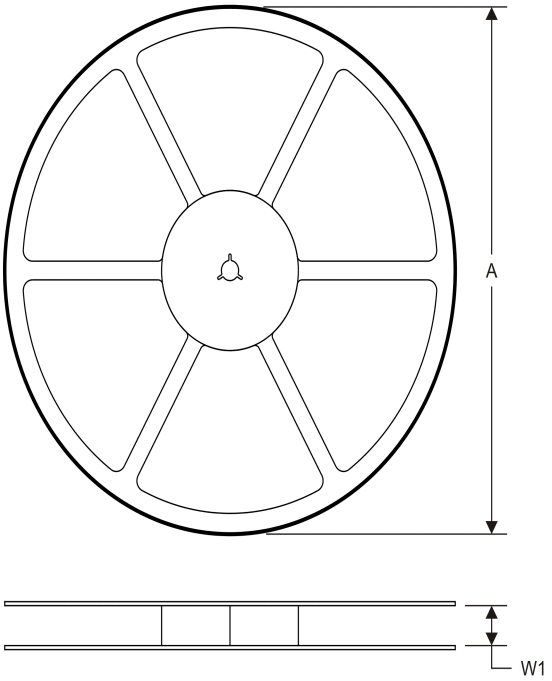
- Catalog: TPS2561

NOTE: Qualified Version Definitions:

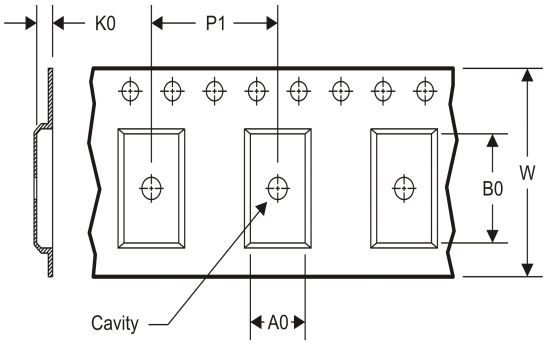
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



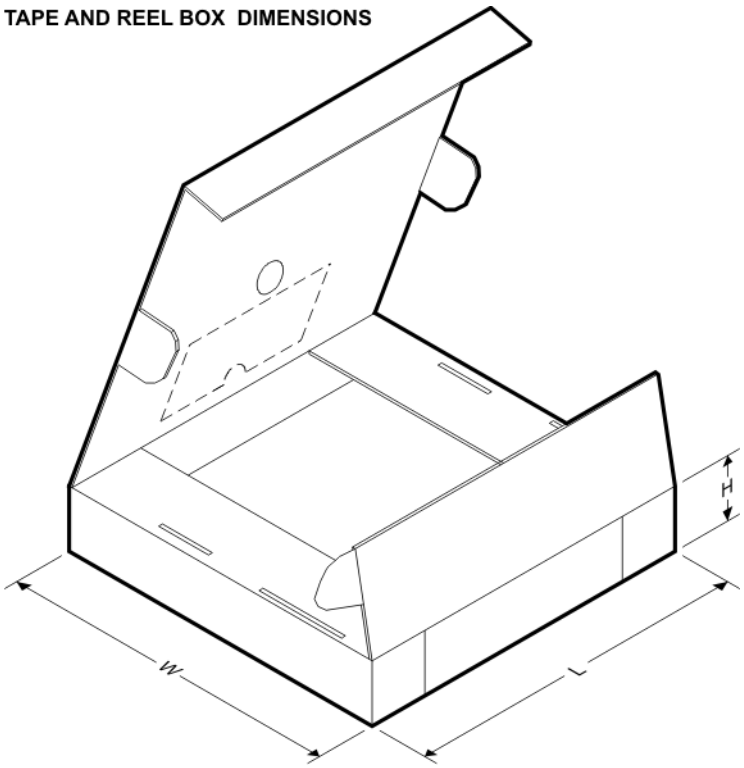
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2561QDRCRQ1	SON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

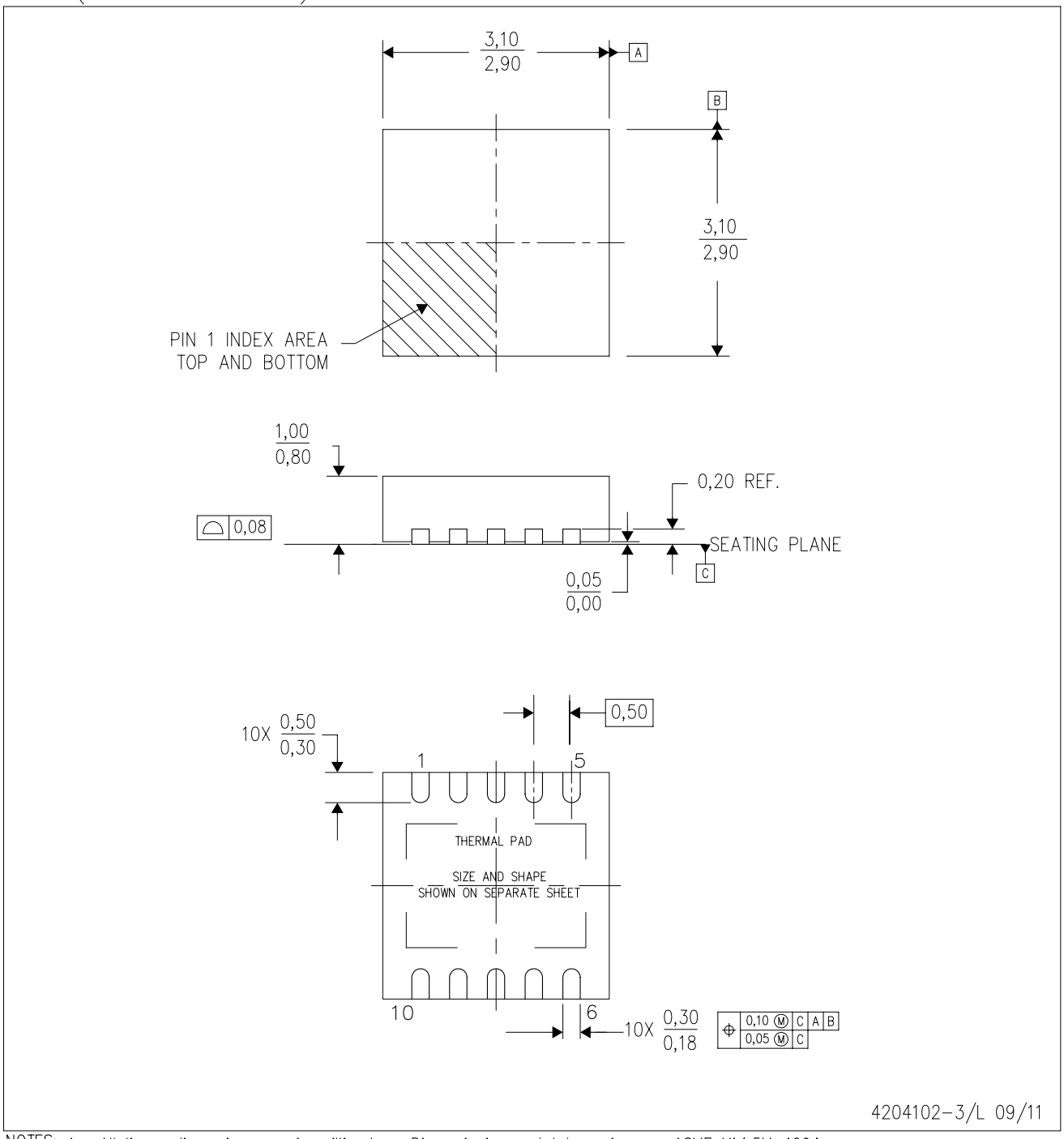
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2561QDRCRQ1	SON	DRC	10	3000	367.0	367.0	35.0

DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance, if present.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions, if present

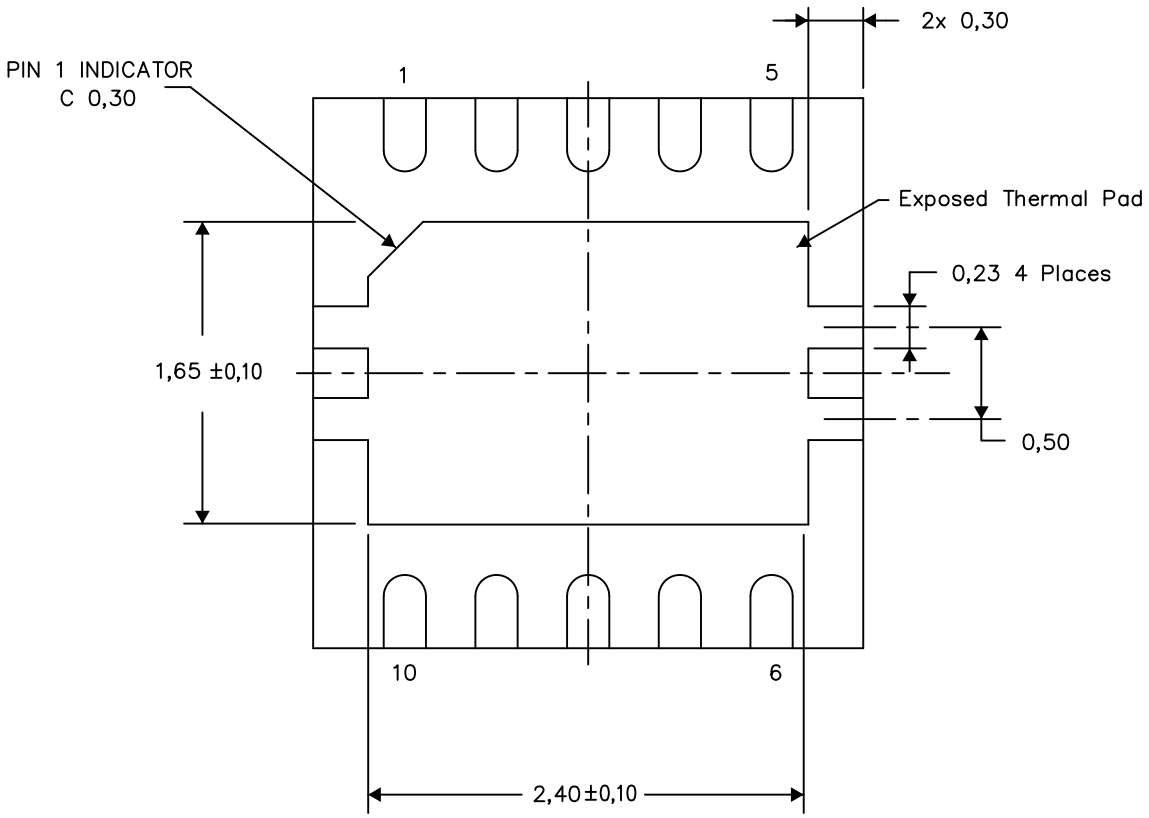
DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



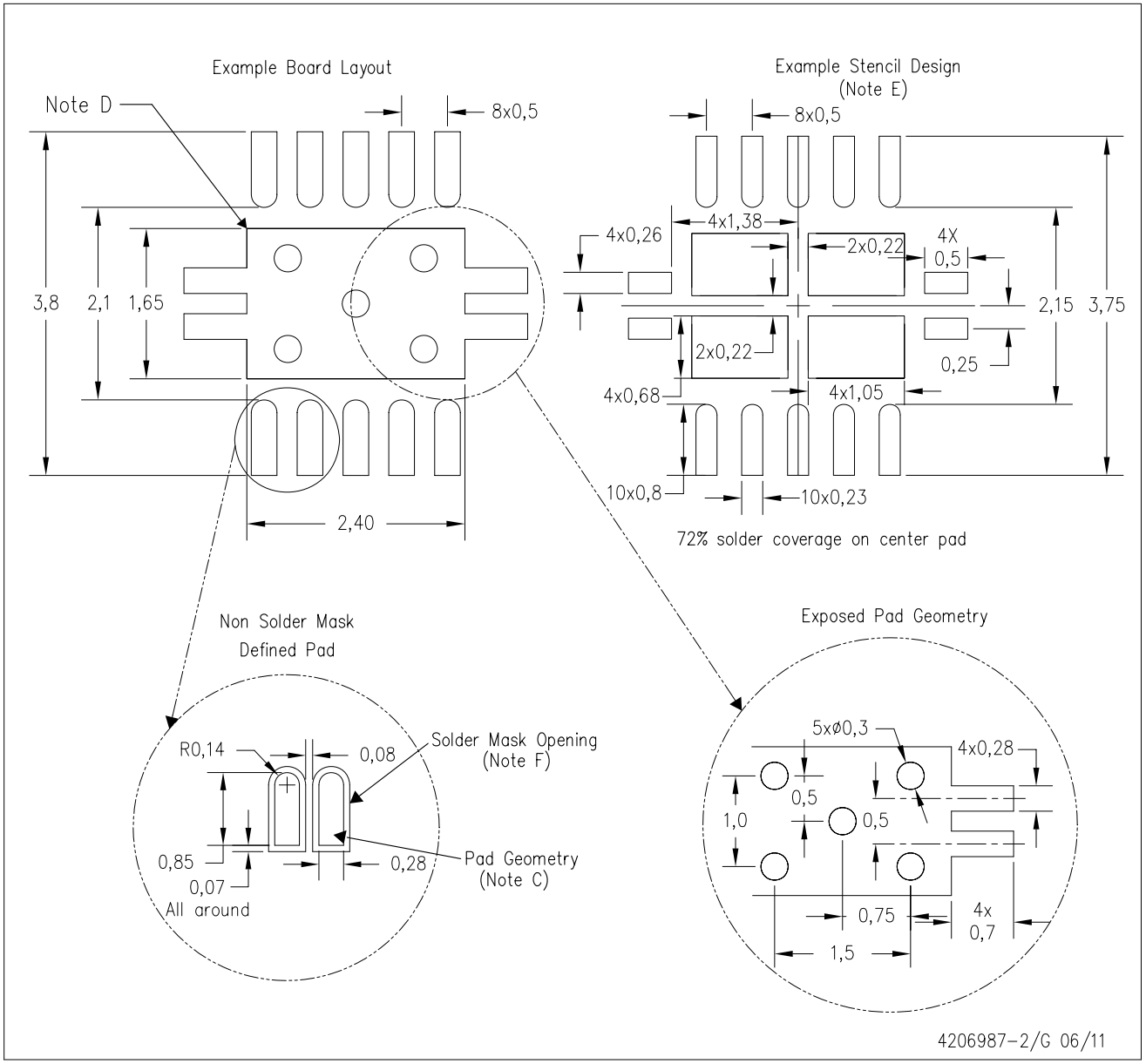
Bottom View

Exposed Thermal Pad Dimensions

4206565–3/N 07/12

NOTE: A. All linear dimensions are in millimeters

DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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