

Ultra-Small, Low on Resistance Load Switch with Controlled Turn-on

Check for Samples: [TPS22912](#)

FEATURES

- Integrated Single Load Switch
- Ultra Small CSP-4 Package 0.9mm × 0.9mm, 0.5mm Pitch
- Input Voltage Range: 1.4-V to 5.5-V
- Low ON-Resistance
 - $r_{ON} = 60\text{-m}\Omega$ at $V_{IN} = 5\text{-V}$
 - $r_{ON} = 61\text{-m}\Omega$ at $V_{IN} = 3.3\text{-V}$
 - $r_{ON} = 74\text{-m}\Omega$ at $V_{IN} = 1.8\text{-V}$
 - $r_{ON} = 84\text{-m}\Omega$ at $V_{IN} = 1.5\text{-V}$
- 2-A Maximum Continuous Switch Current
- Low Threshold Control Input
- Controlled Slew-rate Options
- Under-Voltage Lock Out
- Reverse Current Protection

APPLICATIONS

- Portable Industrial / Medical Equipment
- Portable Media Players
- Point of Sales Terminals
- GPS Navigation Devices
- Digital Cameras
- Portable Instrumentation
- Smartphones / Wireless Handsets

DESCRIPTION

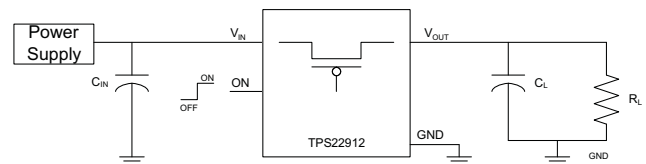
The TPS22912 is a small, low r_{ON} load switch with controlled turn-on and contains a P-channel MOSFET that can operate over an input voltage range of 1.4 V to 5.5 V. The switch is controlled by a high input (ON), which is capable of interfacing directly with low-voltage control signals.

The slew rate of the device is internally controlled in order to avoid inrush current. The TPS22912 family has various rise time options and is active high enable. (see [Table 1](#)).

The TPS22912 provides circuit breaker functionality by latching off the power switch during reverse voltage situations. An internal reverse voltage comparator disables the power switch when the output voltage (V_{OUT}) is higher than the input (V_{IN}). This process quickly (10 μ s typical) stops the flow of current towards the input side of the switch. Reverse current protection is always active, even when the device is disabled. Additionally, under-voltage lockout (UVLO) protection turns the switch off if the input voltage is too low.

The TPS22912 is available in a ultra-small, space-saving 4-pin CSP package and is characterized for operation over the free-air temperature range of -40°C to 85°C .

TYPICAL APPLICATION


Table 1. Feature List

DEVICE	r_{ON} (typ) at 3.3 V	RISE TIME at 3.3V (typ)	QUICK OUTPUT DISCHARGE ⁽¹⁾	MAXIMUM OUTPUT CURRENT	ENABLE
TPS22912A ⁽²⁾	61 m Ω	1 μ s	No	2-A	Active High
TPS22912B ⁽²⁾	61 m Ω	100 μ s	No	2-A	Active High
TPS22912C	61 m Ω	1000 μ s	No	2-A	Active High
TPS22912D ⁽²⁾	61 m Ω	4500 μ s	No	2-A	Active High

(1) This feature discharges the output of the switch to ground through a 150- Ω resistor, preventing the output from floating.

(2) Contact local sales/distributor or factory for availability.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TPS22912

SLVSB78 –APRIL 2012

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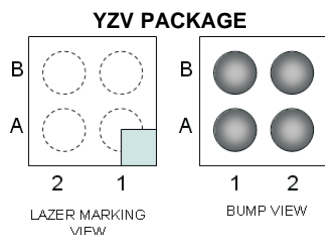
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T _A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING/ STATUS ⁽²⁾
-40°C to 85°C	YZV (0.5mm pitch)	Tape and Reel	TPS22912AYZVR	Contact factory for availability
-40°C to 85°C	YZV (0.5mm pitch)	Tape and Reel	TPS22912BYZVR	Contact factory for availability
-40°C to 85°C	YZV (0.5mm pitch)	Tape and Reel	TPS22912CYZVR	---- 78
-40°C to 85°C	YZV (0.5mm pitch)	Tape and Reel	TPS22912DYZVR	Contact factory for availability

- (1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
 (2) Contact factory for details and availability for PREVIEW devices, minimum order quantities may apply.

DEVICE INFORMATION

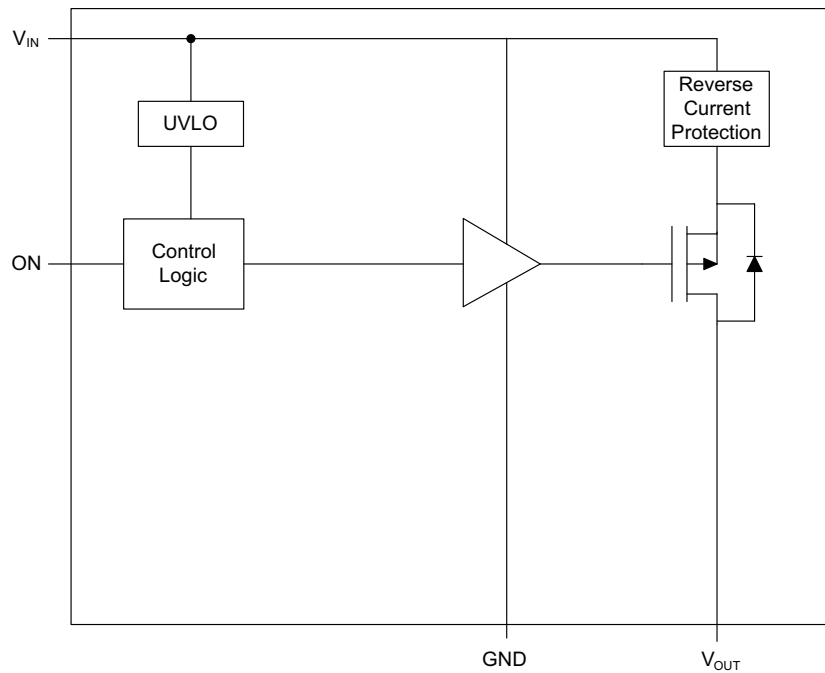


TERMINAL ASSIGNMENTS

B	ON	GND
A	V _{IN}	V _{OUT}
	2	1

PIN FUNCTIONS

TPS22912	PIN NAME	DESCRIPTION
YZV		
B1	GND	Ground
B2	ON	Switch control input, active high. Do not leave floating
A1	V _{OUT}	Switch output
A2	V _{IN}	Switch input. Use ceramic capacitor to GND for bypass.

BLOCK DIAGRAM

Table 2. FUNCTION TABLE

ON	VIN to VOUT
L	OFF
H	ON

ABSOLUTE MAXIMUM RATINGS

		VALUE	UNIT
V _{IN}	Input voltage range	-0.3 to 6	V
V _{OUT}	Output voltage range	-0.3 to 6	V
V _{ON}	Input voltage range	-0.3 to 6	V
I _{MAX}	Maximum continuous switch current	2	A
I _{PLS}	Maximum pulsed switch current, pulse ≤500 ms, 50% duty cycle	3	A
T _A	Operating free-air temperature range	-40 to 85	°C
T _J	Maximum junction temperature	125	°C
T _{STG}	Storage temperature range	-65 to 150	°C
T _{LEAD}	Maximum lead temperature (10-s soldering time)	300	°C
ESD	Electrostatic discharge protection	Human-Body Model (HBM) (VIN, VOUT, GND pins)	2000
		Charged-Device Model (CDM) (VIN, VOUT, ON, GND pins)	1000

THERMAL INFORMATION

THERMAL METRIC ⁽¹⁾		TPS22912		UNITS
		CSP		
		4 PINS		
θ_{JA}	Junction-to-ambient thermal resistance	189.1		°C/W
θ_{JcTop}	Junction-to-case (top) thermal resistance	1.9		
θ_{JB}	Junction-to-board thermal resistance	36.8		
ψ_{JT}	Junction-to-top characterization parameter	11.3		
ψ_{JB}	Junction-to-board characterization parameter	36.8		
θ_{JcBot}	Junction-to-case (bottom) thermal resistance	N/A		

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
V_{IN}	Input voltage range	1.4	5.5	V
V_{ON}	ON voltage range	0	5.5	V
V_{OUT}	Output voltage range (Note: V_{OUT} greater than V_{IN} will cause the reverse current protection of this device to trigger. See application section.)	$V_{IN}^{(1)}$		
V_{IH}	High-level input voltage, ON	$V_{IN} = 3.61\text{ V to }5.5\text{ V}$		V
		$V_{IN} = 1.4\text{ V to }3.6\text{ V}$		V
V_{IL}	Low-level input voltage, ON	$V_{IN} = 3.61\text{ V to }5.5\text{ V}$		V
		$V_{IN} = 1.4\text{ V to }3.6\text{ V}$		V
C_{IN}	Input Capacitor	1 ⁽¹⁾		μF

(1) Refer to the application section.

ELECTRICAL CHARACTERISTICS

VIN = 1.4 V to 5.5 V, TA = –40°C to 85°C (unless otherwise noted)

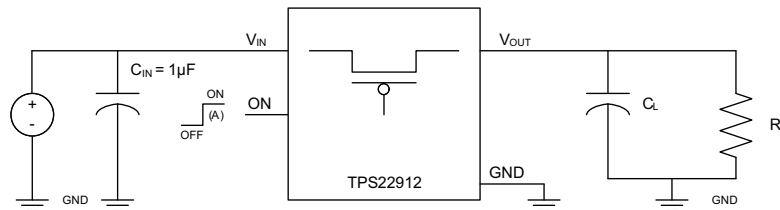
PARAMETER	TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
IIN Quiescent current	IOUT = 0, VON = VIN = 5.25 V	Full		2	10	μA
	IOUT = 0, VON = VIN = 4.2 V			2	7.0	
	IOUT = 0, VON = VIN = 3.6 V			2	7.0	
	IOUT = 0, VON = VIN = 2.5 V			0.9	5	
	IOUT = 0, VON = VIN = 1.5 V			0.7	5	
IIN(off) ⁽¹⁾ Off supply current	RL = 1 MΩ, VIN = 5.25 V, VON = GND	Full		1.2	10	μA
	RL = 1 MΩ, VIN = 4.2 V, VON = GND			0.2	7.0	
	RL = 1 MΩ, VIN = 3.6 V, VON = GND			0.1	7.0	
	RL = 1 MΩ, VIN = 2.5 V, VON = GND			0.1	5	
	RL = 1 MΩ, VIN = 1.5 V, VON = GND			0.1	5	
IIN(Leakage) Leakage current	VOUT = 0, VIN = 5.25 V, VON = GND	Full		1.2	10	μA
	VOUT = 0, VIN = 4.2 V, VON = GND			0.2	7.0	
	VOUT = 0, VIN = 3.6 V, VON = GND			0.1	7.0	
	VOUT = 0, VIN = 2.5 V, VON = GND			0.1	5	
	VOUT = 0, VIN = 1.5 V, VON = GND			0.1	5	
RON On-resistance	VIN = 5.25 V, IOUT = –200 mA	25°C		60	80	mΩ
		Full			110	
	VIN = 5.0 V, IOUT = –200 mA	25°C		60	80	
		Full			110	
	VIN = 4.2 V, IOUT = –200 mA	25°C		60	80	
		Full			110	
	VIN = 3.3 V, IOUT = –200 mA	25°C		60.7	80	
		Full			110	
	VIN = 2.5 V, IOUT = –200 mA	25°C		63.4	90	
		Full			120	
	VIN = 1.8 V, IOUT = –200 mA	25°C		74.2	100	
		Full			130	
	VIN = 1.5 V, IOUT = –200 mA	25°C		83.9	120	
		Full			150	
UVLO Under voltage lockout	VIN increasing, VON = 3.6 V, IOUT = –100 mA VIN decreasing, VON = 3.6 V, IOUT = –100 mA	Full			1.2	V
			0.50			
ION ON input leakage current	VON = 1.4 V to 5.25 V or GND	Full			1	μA
VRCPP Reverse Current Voltage Threshold	VOUT > VIN	25°C		54		mV
IRCP(leak) Reverse Current Protection Leakage after Reverse Current event	VOUT – VIN > VRCPP	25°C		0.3		μA
tDELAY Reverse Current Response Delay	VIN = 5V			10		μs

(1) Verified by characterization, not production tested.

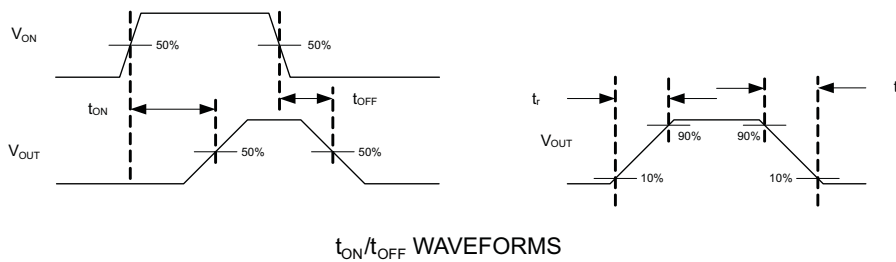
SWITCHING CHARACTERISTICS

PARAMETER		TEST CONDITION	TPS22912	UNIT
			TYP	
V_{IN} = 5 V, T_A = 25°C (unless otherwise noted)				
t _{ON}	Turn-ON time	R _L = 10 Ω, C _L = 0.1 μF	840	μs
t _{OFF}	Turn-OFF time	R _L = 10 Ω, C _L = 0.1 μF	6.6	
t _R	V _{OUT} rise time	R _L = 10 Ω, C _L = 0.1 μF	912	
t _F	V _{OUT} fall time	R _L = 10 Ω, C _L = 0.1 μF	3	
V_{IN} = 3.3 V, T_A = 25°C (unless otherwise noted)				
t _{ON}	Turn-ON time	R _L = 10 Ω, C _L = 0.1 μF	1147	μs
t _{OFF}	Turn-OFF time	R _L = 10 Ω, C _L = 0.1 μF	8.6	
t _R	V _{OUT} rise time	R _L = 10 Ω, C _L = 0.1 μF	1030	
t _F	V _{OUT} fall time	R _L = 10 Ω, C _L = 0.1 μF	3	
V_{IN} = 1.5 V, T_A = 25°C (unless otherwise noted)				
t _{ON}	Turn-ON time	R _L = 10 Ω, C _L = 0.1 μF	2513	μs
t _{OFF}	Turn-OFF time	R _L = 10 Ω, C _L = 0.1 μF	17.4	
t _R	V _{OUT} rise time	R _L = 10 Ω, C _L = 0.1 μF	1970	
t _F	V _{OUT} fall time	R _L = 10 Ω, C _L = 0.1 μF	6.5	

PARAMETRIC MEASUREMENT INFORMATION



TEST CIRCUIT



t_{ON}/t_{OFF} WAVEFORMS

(A) Rise and fall times of the control signal is 100ns.

- A. Rise and fall times of the control signal are 100 ns.

Figure 1. Test Circuit and t_{ON}/t_{OFF} Waveforms

TYPICAL CHARACTERISTICS

ON-STATE RESISTANCE
vs
INPUT VOLTAGE

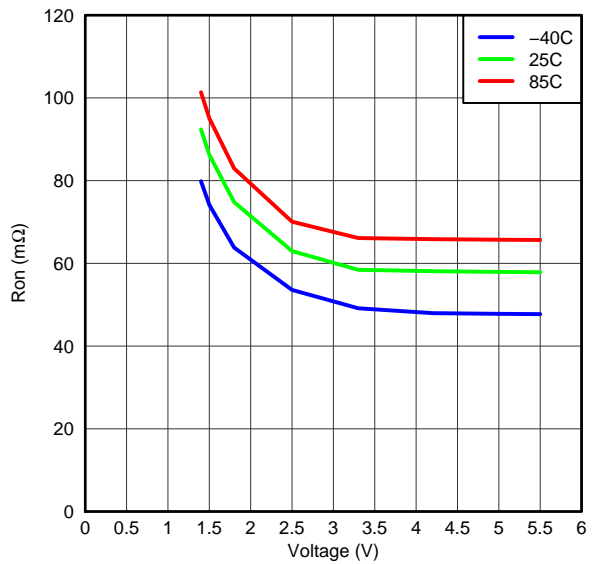


Figure 2.

ON INPUT THRESHOLD

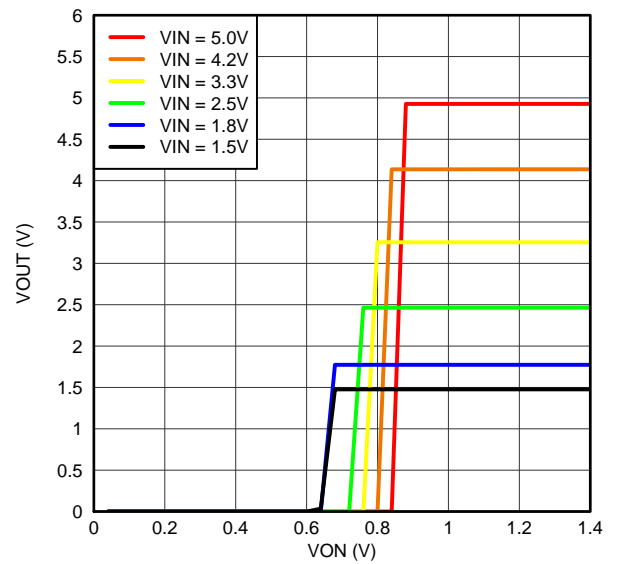


Figure 3.

INPUT CURRENT, QUIESCENT
vs
INPUT VOLTAGE

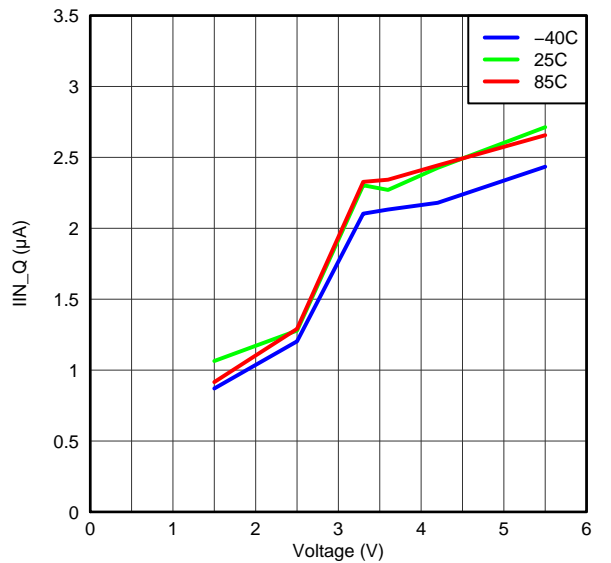


Figure 4.

INPUT CURRENT, LEAK
vs
INPUT VOLTAGE

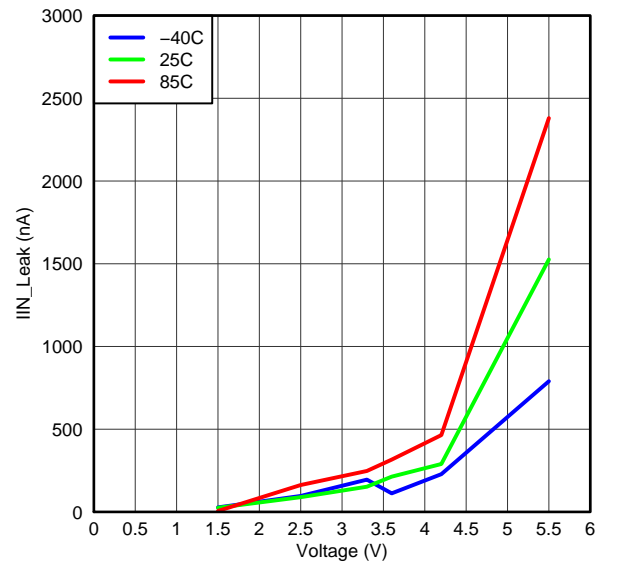


Figure 5.

TYPICAL CHARACTERISTICS (continued)

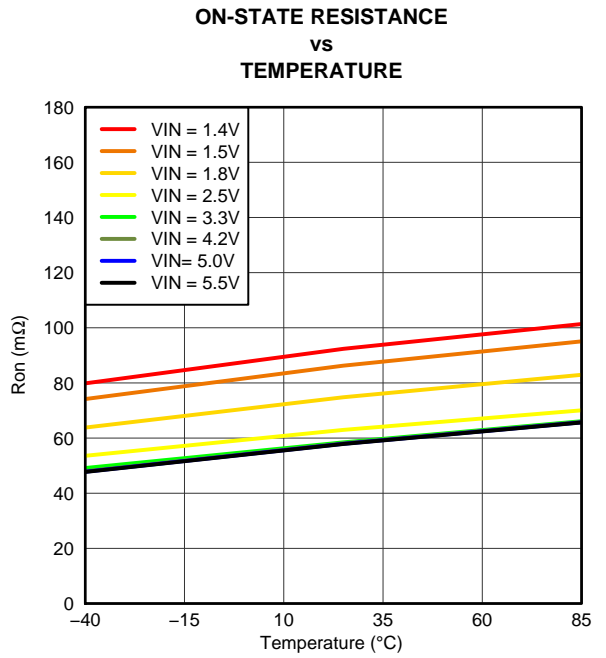


Figure 6.

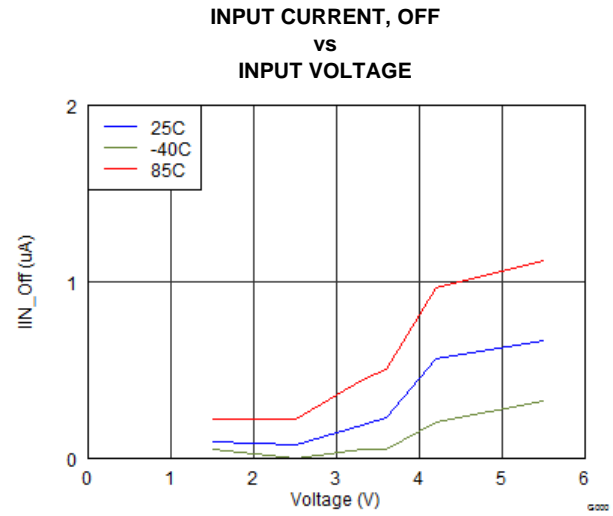


Figure 7.

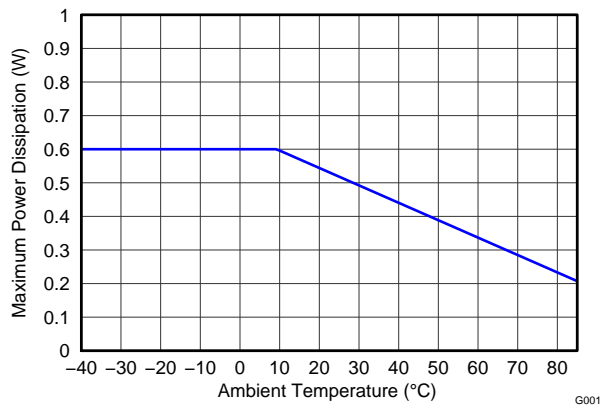


Figure 8. Allowable Power Dissipation

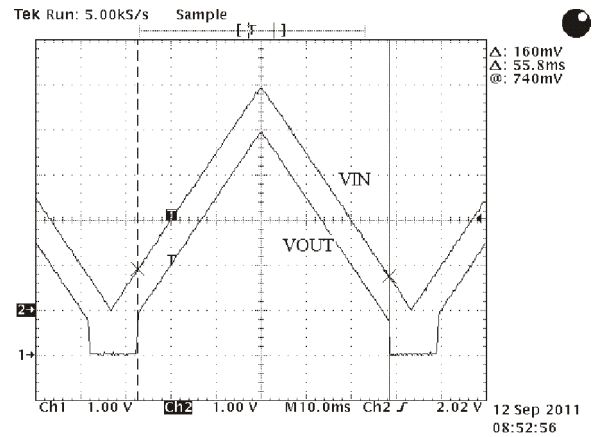


Figure 9. ULVO Response $I_{OUT} = -100\text{mA}$

TYPICAL CHARACTERISTICS (continued)

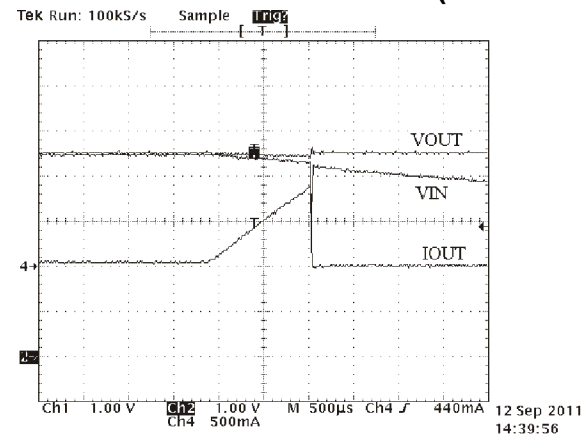


Figure 10. Reverse Current Protection $V_{OUT} = 3.3V$, $V_{IN} = 3.3V$ Decreasing to 0V

TYPICAL AC CHARACTERISTICS FOR TPS22912C

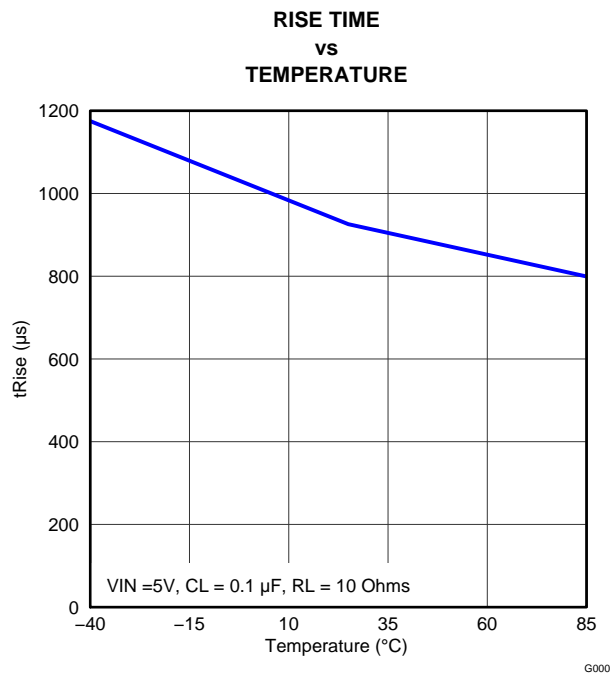


Figure 11.

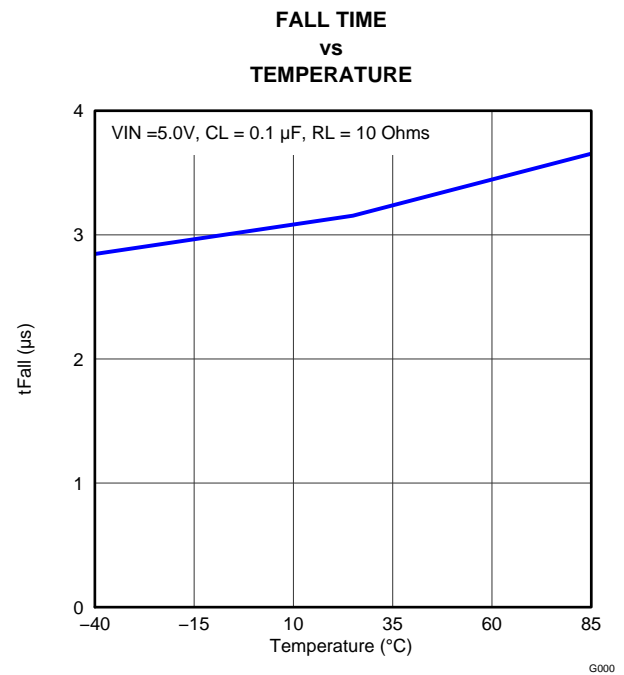


Figure 12.

TYPICAL CHARACTERISTICS (continued)

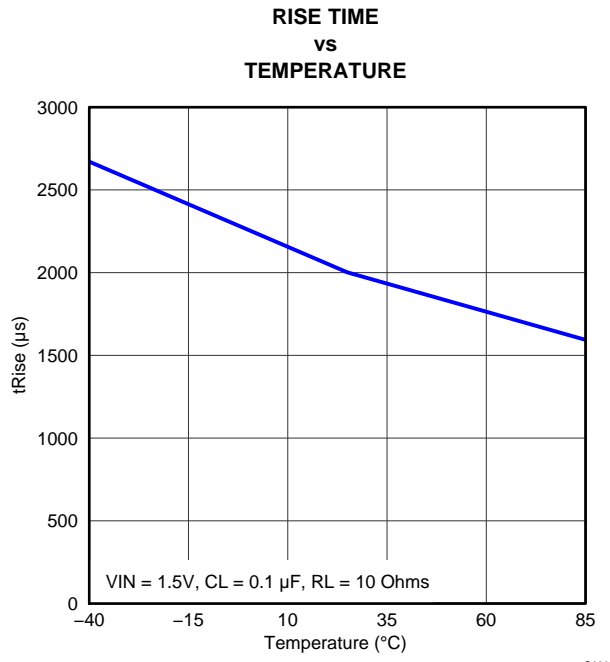


Figure 13.

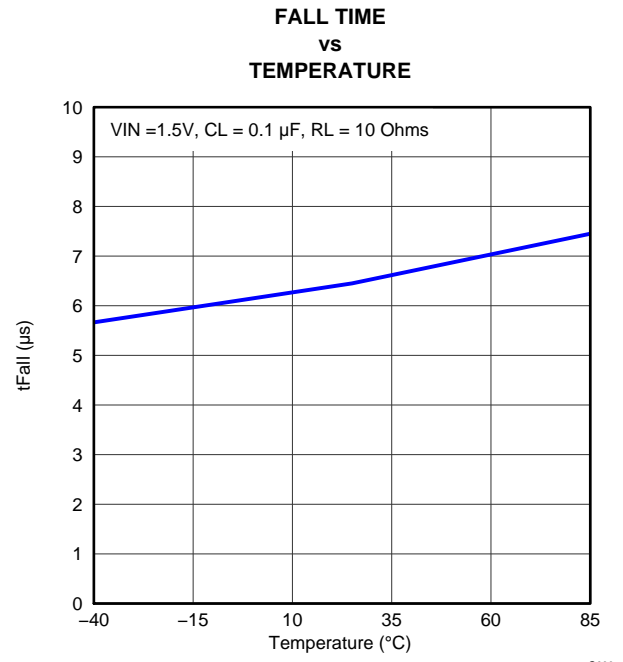


Figure 14.

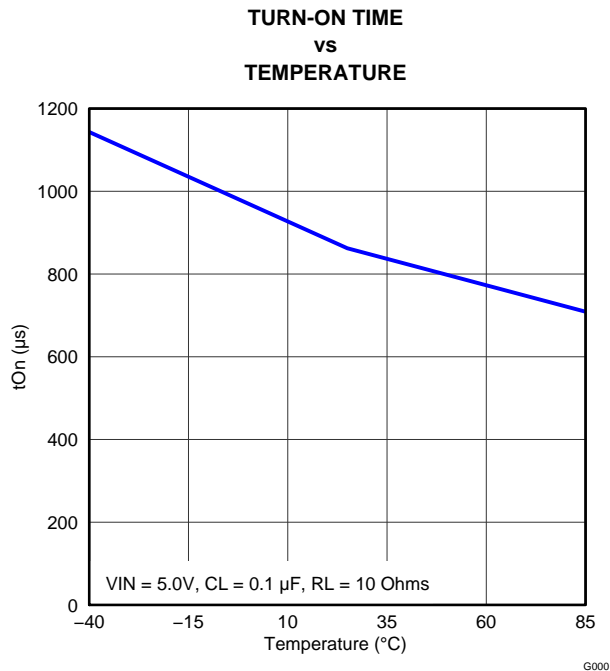


Figure 15.

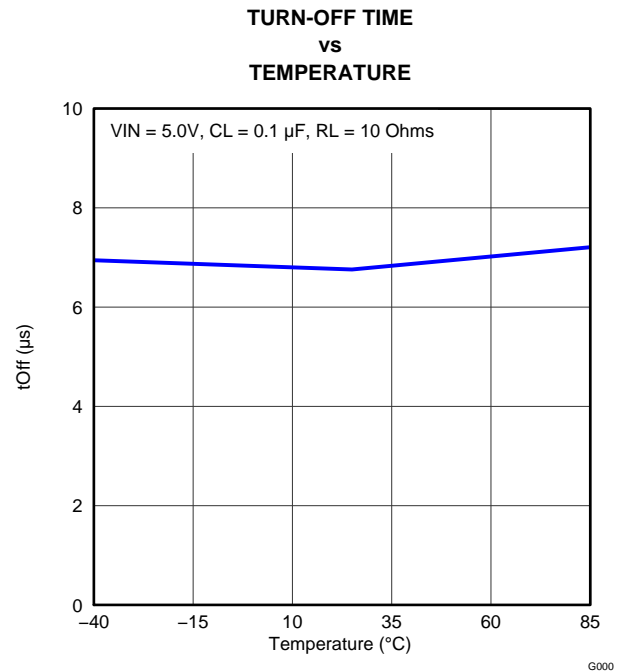


Figure 16.

TYPICAL CHARACTERISTICS (continued)

TURN-ON TIME
vs
TEMPERATURE

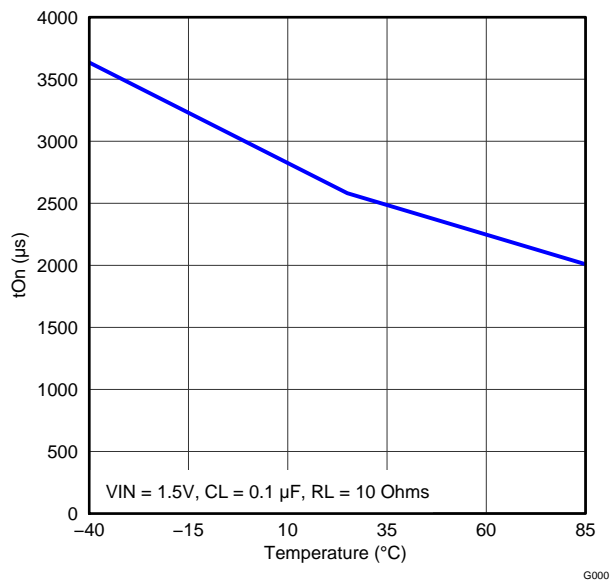


Figure 17.

TURN-OFF TIME
vs
TEMPERATURE

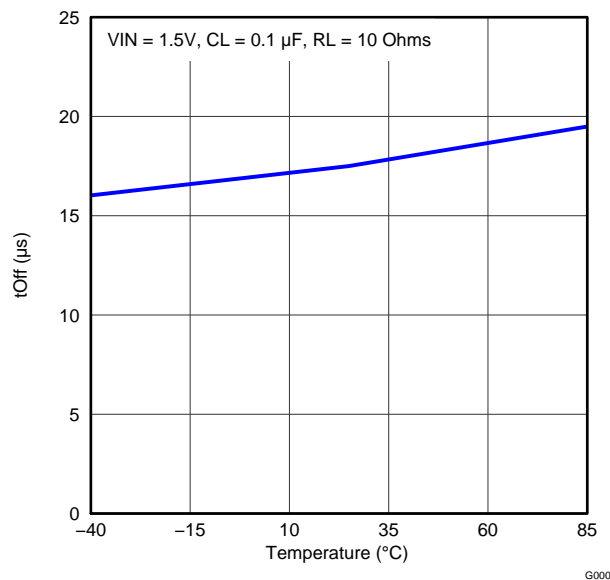


Figure 18.

RISE TIME
vs
INPUT VOLTAGE

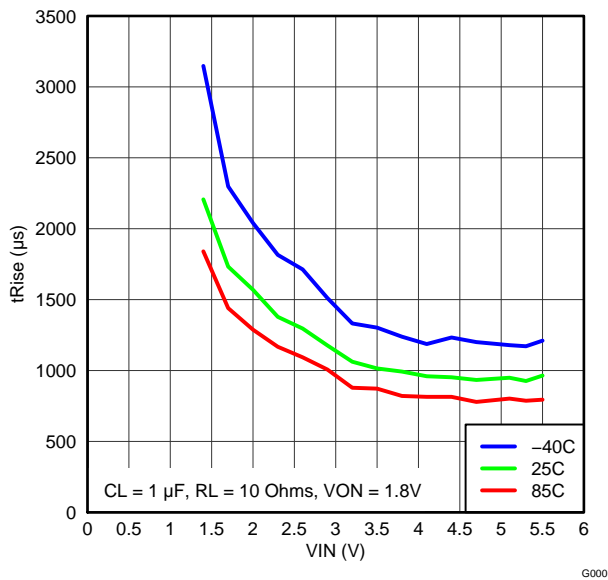


Figure 19.

TYPICAL CHARACTERISTICS (continued)

TURN-ON RESPONSE

$V_{IN} = 5V, T_A = 25^\circ C, C_{IN} = 1\mu F, C_L = 0.1\mu F, R_L = 10\Omega$

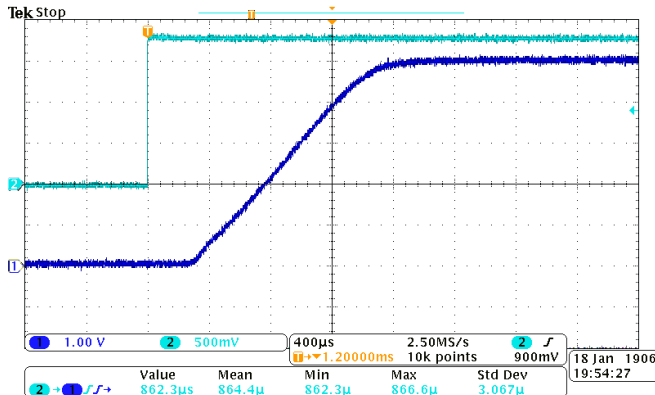


Figure 20.

TURN-OFF RESPONSE

$V_{IN} = 5V, T_A = 25^\circ C, C_{IN} = 1\mu F, C_L = 0.1\mu F, R_L = 10\Omega$

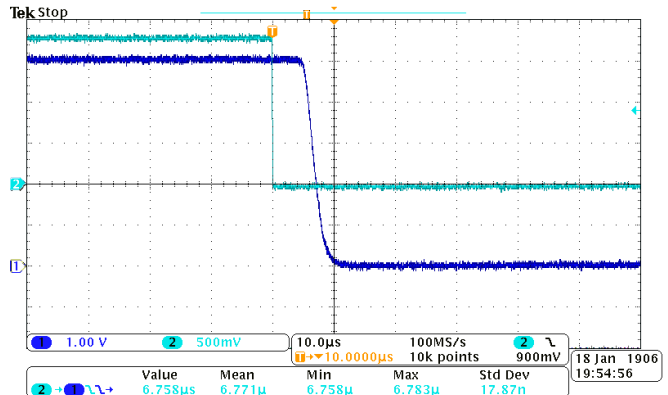


Figure 21.

TURN-ON RESPONSE TIME

$V_{IN} = 5V, T_A = 25^\circ C, C_{IN} = 10\mu F, C_L = 1\mu F, R_L = 10\Omega$

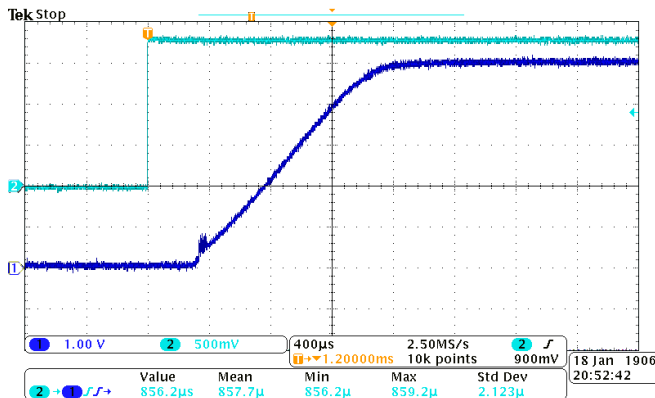


Figure 22.

TURN-OFF RESPONSE TIME

$V_{IN} = 5V, T_A = 25^\circ C, C_{IN} = 10\mu F, C_L = 1\mu F, R_L = 10\Omega$

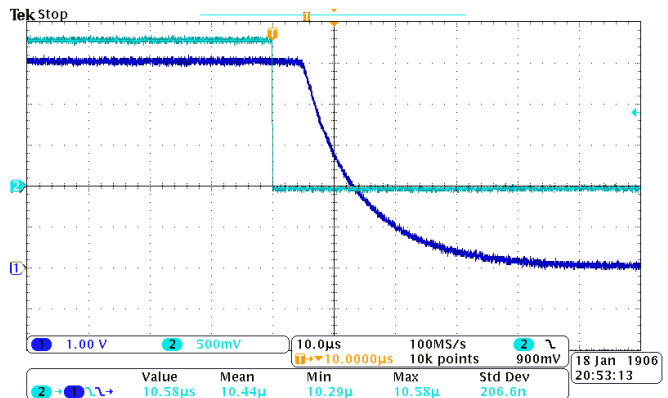


Figure 23.

TURN-ON RESPONSE TIME

$V_{IN} = 1.5V, T_A = 25^\circ C, C_{IN} = 1\mu F, C_L = 0.1\mu F, R_L = 10\Omega$

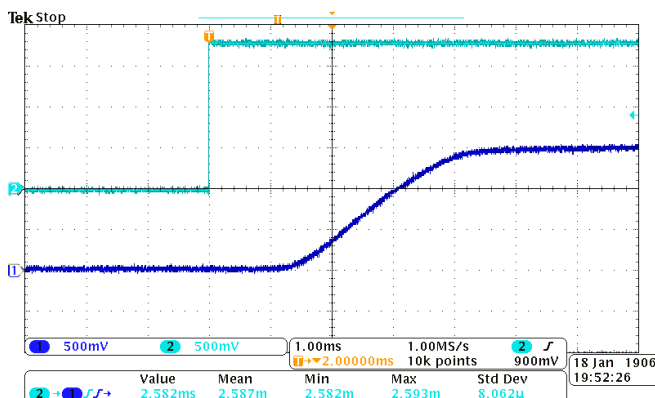


Figure 24.

TURN-OFF RESPONSE TIME

$V_{IN} = 1.5V, T_A = 25^\circ C, C_{IN} = 1\mu F, C_L = 0.1\mu F, R_L = 10\Omega$

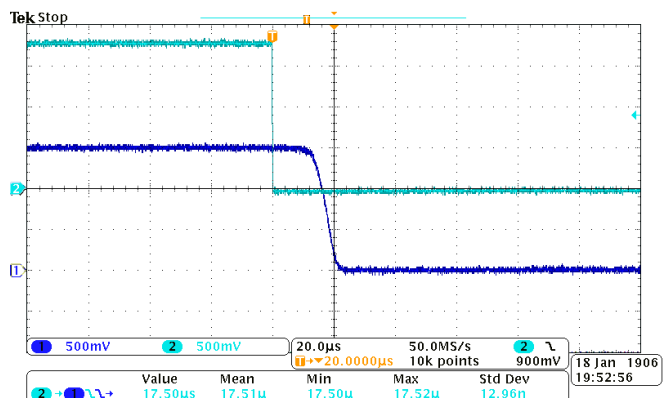


Figure 25.

TYPICAL CHARACTERISTICS (continued)

TURN-ON RESPONSE TIME

$V_{IN} = 1.5V$, $T_A = 25^\circ C$, $C_{IN} = 10\mu F$, $C_L = 1\mu F$, $R_L = 10\Omega$

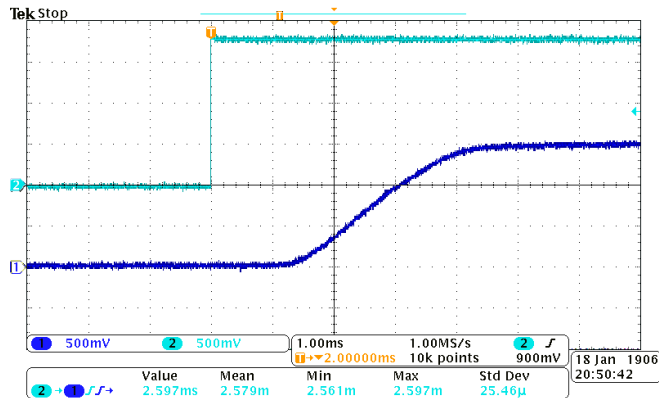


Figure 26.

TURN-OFF RESPONSE TIME

$V_{IN} = 1.5V$, $T_A = 25^\circ C$, $C_{IN} = 10\mu F$, $C_L = 1\mu F$, $R_L = 10\Omega$

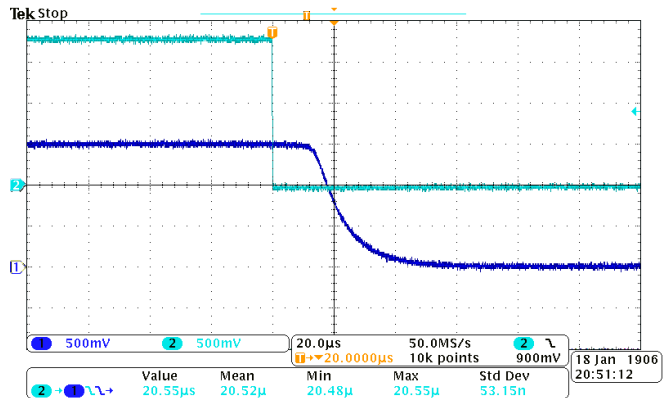


Figure 27.

APPLICATION INFORMATION

On/Off Control

The ON pin controls the state of the switch. Asserting ON high enables the switch. ON is active high and has a low threshold, making the pin capable of interfacing with low-voltage signals. The ON pin is compatible with standard GPIO logic threshold. It can be used with any microcontroller with 1.2-V, 1.8-V, 2.5-V or 3.3-V GPIO.

Input Capacitor

To limit the voltage drop on the input supply caused by transient inrush currents, a capacitor needs to be placed between VIN and GND. A 1- μ F ceramic capacitor, C_{IN} , placed close to the pins is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop.

Output Capacitor

A C_{IN} to C_L ratio of 10 to 1 is recommended for minimizing V_{IN} dip caused by inrush currents during startup. Devices with faster rise times may require a larger ratio to minimize V_{IN} dip.

Under-Voltage Lockout

Under-voltage lockout protection turns off the switch if the input voltage is below the under-voltage lockout threshold. During under-voltage lockout (UVLO), if the voltage level at V_{OUT} exceeds the voltage level at V_{IN} by the Reverse Current Voltage Threshold (V_{RVP}), the body diode will be disengaged to prevent any current flow to V_{IN} . With the ON pin active, the input voltage rising above the under-voltage lockout threshold will cause a controlled turn-on of the switch to limit current over-shoot.

Reverse Current Protection

In a scenario where V_{OUT} is greater than V_{IN} , there is potential for reverse current to flow through the pass FET or the body diode. The TPS22912 monitors V_{IN} and V_{OUT} voltage levels. When the reverse current voltage threshold (V_{RCP}) is exceeded, the switch is disabled (within 10 μ s typ). Additionally, the body diode is disengaged so as to prevent any reverse current flow to V_{IN} . The FET, and the output (V_{OUT}), will resume normal operation when the reverse current scenario is no longer present. The peak instantaneous reverse current is the current it takes to trip the reverse current protection. After the reverse current protection has tripped due to the peak instantaneous reverse current, the DC (off-state) leakage current from V_{OUT} and V_{IN} is referred to as $I_{RCP(LEAK)}$ (see figure below).

Use the following formula to calculate the amount of peak instantaneous reverse current for a particular application:

$$I_{RC} = \frac{V_{RCP}}{R_{ON(VIN)}}$$

Where,

I_{RC} is the amount of reverse current,

$R_{ON(VIN)}$ is the on-resistance at the V_{IN} of the reverse current condition.

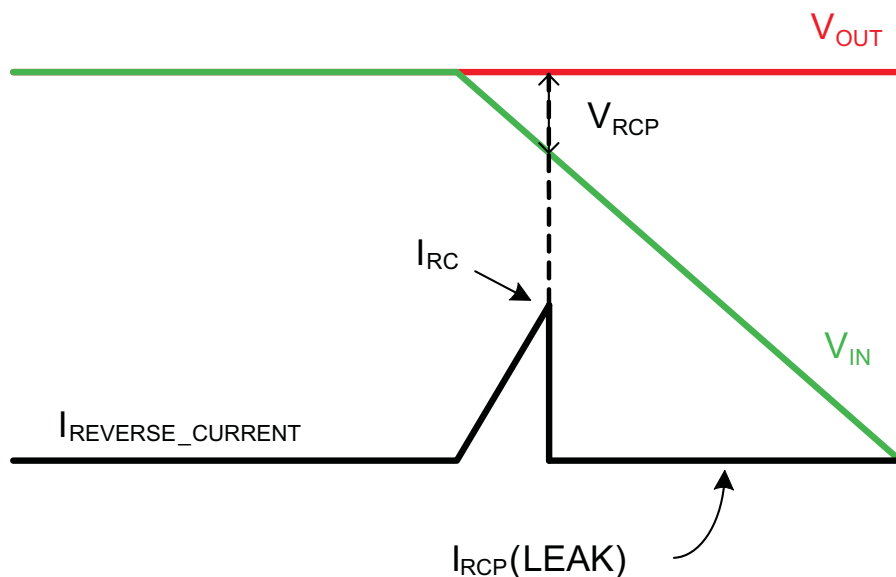


Figure 28. Reverse Current

Board Layout

For best performance, all traces should be as short as possible. The input and output capacitors should be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for V_{IN} , V_{OUT} , and GND helps minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS22912CZVZR	ACTIVE	DSBGA	YZV	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	78	Samples
TPS22912CZVZT	ACTIVE	DSBGA	YZV	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	78	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22912CYZVR	DSBGA	YZV	4	3000	178.0	9.2	1.0	1.0	0.63	4.0	8.0	Q1
TPS22912CYZVT	DSBGA	YZV	4	250	178.0	9.2	1.0	1.0	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS

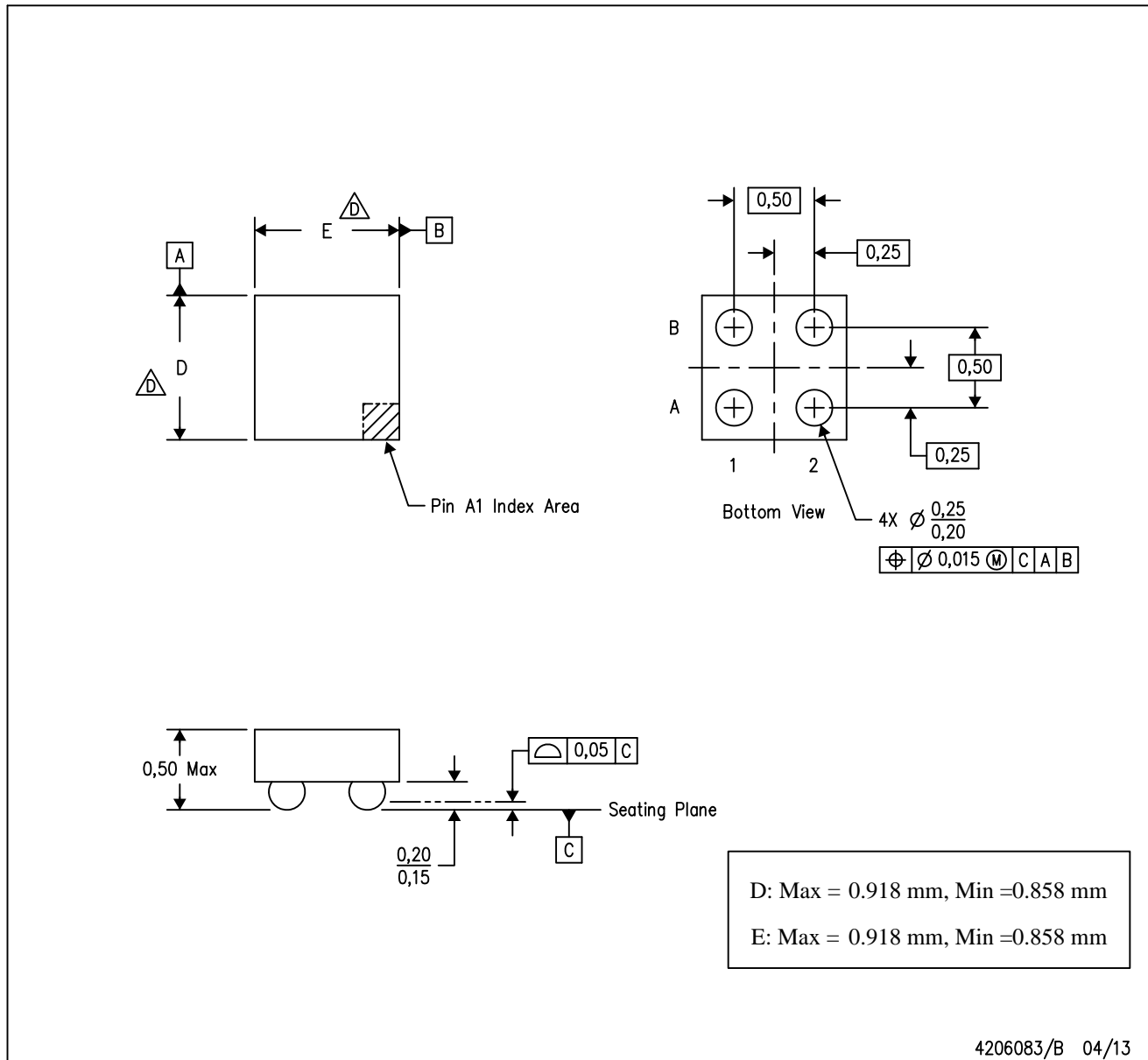

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22912CYZVR	DSBGA	YZV	4	3000	220.0	220.0	35.0
TPS22912CYZVT	DSBGA	YZV	4	250	220.0	220.0	35.0

MECHANICAL DATA

YZV (S-XBGA-N4)

DIE-SIZE BALL GRID ARRAY



4206083/B 04/13

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.
 - $\triangle D$ The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative.
 - E. Reference Product Data Sheet for array population. 2 x 2 matrix pattern is shown for illustration only.
 - F. This package contains Pb-free balls. Refer to the 4 YEV package (drawing 4206082) for tin-lead (SnPb) balls.

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