LOW VOLTAGE H-BRIDGE IC WITH LDO VOLTAGE REGULATOR

Check for Samples: DRV8851

FEATURES

- **H-Bridge Motor Driver**
  - **Drives a DC Motor or One Winding of a Stepper Motor, or Other Loads**
  - **Low MOSFET On-Resistance: HS + LS 280 mΩ**
- **1.8-A Maximum Drive Current**
- **1.8-V to 11-V Motor Operating Supply Voltage Range**
- **Separate Motor and Logic Supply Pins**
- **PWM (IN/IN) Interface**
- **Low-Power Sleep Mode**
- **150-mA LDO Voltage Regulator**
- **12-Pin, 2-mm x 3-mm WSON Package**

APPLICATIONS

- **Cameras**
- **DSLR Lenses**
- **Electronic Locks**
- **Toys**
- **Robotics**
- **Smart Meters (Gas or Water)**
- **Medical Devices**

PRODUCT PREVIEW

DESCRIPTION

The DRV8851 provides a motor driver plus LDO voltage regulator solution for cameras, consumer products, toys, and other low-voltage or battery-powered motion control applications. The device has one H-bridge driver and can drive one DC motor or one winding of a stepper motor, as well as other devices like solenoids. The output driver block consists of N-channel power MOSFET's configured as an H-bridge to drive the motor winding. An internal charge pump generates needed gate drive voltages.

The DRV8851 can supply up to 1.8-A of output current. It operates on a motor power supply voltage from 1.8 V to 11 V, and a device power supply voltage of 1.8 V to 7 V.

The DRV8851 has a PWM (IN/IN) input interface which is compatible with industry-standard devices.

A low-dropout linear voltage regulator (LDO) is integrated with the motor driver, to supply power to microcontrollers or other circuits. The LDO can supply up to 150 mA.

Internal shutdown functions are provided for over current protection, short circuit protection, under voltage lockout and overtemperature.

The DRV8851 is packaged in a 12-pin, 2-mm x 3-mm WSON package with PowerPAD™ (Eco-friendly: RoHS & no Sb/Br).

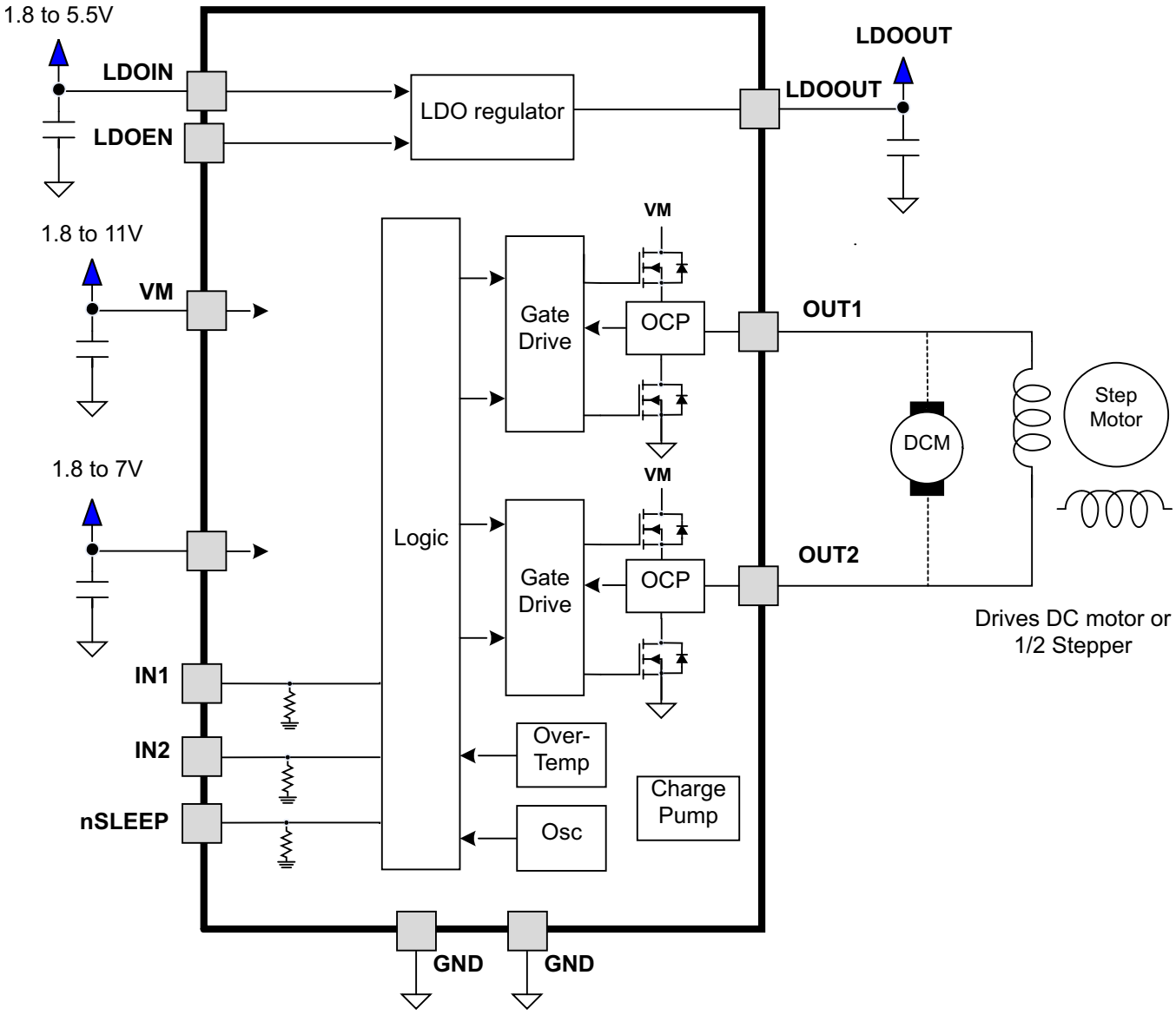
ORDERING INFORMATION(1)

PACKAGE(2)		ORDERABLE PART NUMBER	LDO OUTPUT VOLTAGE(3)	TOP-SIDE MARKING
PowerPAD™ (WSON) - DSS	Reel of 3000	DRV8851-25DSSR	2.5 V	885125
		DRV8851-27DSSR	2.7 V	881527
		DRV8851-33DSSR	3.3 V	881533

(1) For the most current packaging and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(3) Other voltages are available, please consult factory.

DEVICE INFORMATION

Functional Block Diagram



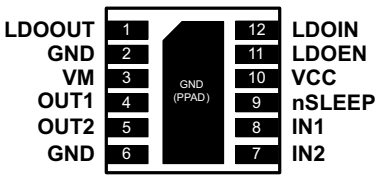
PRODUCT PREVIEW

Table 1. TERMINAL FUNCTIONS

NAME	PIN	I/O(1)	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
POWER AND GROUND				
GND	2, 6	-	Device ground	
VM	3	-	Motor supply	Bypass to GND with a 0.1-µF, 16-V ceramic capacitor.
VCC	10	-	Device supply	Bypass to GND with a 0.1-µF, 16-V ceramic capacitor.
LDOIN	12	-	LDO regulator input	Bypass to GND with a 0.1-µF, 6.3-V ceramic capacitor.
LDOOUT	1	-	LDO regulator output	Bypass to GND with a 1-µF, 6.3-V ceramic capacitor.
CONTROL				
LDOEN	11	I	LDO regulator enable	Logic low disables LDO regulator Logic high enables LDO regulator May be connected to LDOIN to enable LDO Note that there is no pullup or pulldown on this input
IN1	8	I	Input 1	Logic high sets OUT1 high Internal pulldown resistor
IN2	7	I	Input 2	Logic high sets OUT2 high Internal pulldown resistor
nSLEEP	9	I	Sleep mode input	Logic low puts device in low-power sleep mode Logic high for normal operation Internal pulldown resistor
OUTPUT				
OUT1	4	O	Output 1	Connect to motor winding
OUT2	5	O	Output 2	

(1) Directions: I = input, O = output, OZ = tri-state output, OD = open-drain output, IO = input/output

DRV8851
DSS PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

ABSOLUTE MAXIMUM RATINGS(1)(2)

		VALUE	UNIT
VM	Power supply voltage range	–0.3 to 12	V
VCC	Power supply voltage range	–0.3 to 7	V
LDOIN	Power supply voltage range	–0.3 to 6	V
	ENLDO, LDOOUT pin voltage range	–0.3 to 6	V
	Digital pin voltage range	–0.5 to 7	V
	Peak motor drive output current	Internally limited	
	LDO output current	Internally limited	
	LDO output short circuit duration	Indefinite	
	Continuous total power dissipation(3)	See Thermal Information table	
T_J	Operating virtual junction temperature range	–40 to 150	°C
T_{stg}	Storage temperature range	–60 to 150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) Power dissipation and thermal limits must be observed.

PRODUCT PREVIEW

THERMAL INFORMATION

THERMAL METRIC(1)		DRV8851 DSS 12 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	50.4	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	58	
θ_{JB}	Junction-to-board thermal resistance(4)	19.9	
ψ_{JT}	Junction-to-top characterization parameter(5)	0.9	
ψ_{JB}	Junction-to-board characterization parameter(6)	20	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	6.9	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_M	Motor power supply voltage range	1.8		11	V
V_{CC}	Device power supply voltage range	1.8		7	V
I_{OUT}	H-bridge output current(1)	0		1.8	A
f_{PWM}	Externally applied PWM frequency	0		250	kHz
V_{IN}	Logic level input voltage	0		5.5	V

(1) Power dissipation and thermal limits must be observed.

MOTOR DRIVER ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_M = 5 V, V_{CC} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supplies						
I_{VM}	VM operating supply current	V_M = 5 V, V_{CC} = 3 V, no PWM		40	100	µA
		V_M = 5 V, VCC = 3 V, 50-kHz PWM		0.8	1.5	mA
I_{VMQ}	VM sleep-mode supply current	V_M = 5 V, V_{CC} = 3 V, nSLEEP = 0 V		30	95	nA
I_{VCC}	VCC operating supply current	V_M = 5 V, V_{CC} = 3 V, no PWM		300	500	µA
		V_M = 5 V, V_{CC} = 3 V, 50-kHz PWM		0.7	1.5	mA
I_{VCQ}	VCC sleep-mode supply current	V_M = 5 V, V_{CC} = 3 V, nSLEEP = 0 V		5	25	nA
V_{UVLO}	VCC undervoltage lockout voltage	V_{CC} rising			1.8	V
		V_{CC} falling			1.7	
Logic-Level Inputs						
V_{IL}	Input low voltage		0.25 V_{CC}	0.38 V_{CC}		V
V_{IH}	Input high voltage			0.46 V_{CC}	0.5 V_{CC}	V
V_{HYS}	Input hysteresis			0.08 V_{CC}		V
I_{IL}	Input low current	V_{IN} = 0 V	–5		5	µA
I_{IH}	Input high current	V_{IN} = 3.3 V			50	µA
R_{PD}	Pulldown resistance			100		kΩ
H-Bridge FETs						
$R_{DS(ON)}$	HS + LS FET on-resistance	V_{CC} = 3 V, V_M = 5 V, I_O = 800 mA, T_J = 25°C		280	330	mΩ
I_{OFF}	Off-state leakage current	V_{OUT} = 0 V			±200	nA
Protection Circuits						
I_{OCP}	Overcurrent protection trip level		1.9		3.5	A
t_{OCR}	OCP retry time			1		ms
t_{TSD}	Thermal shutdown temperature	Die temperature	150	160	180	ºC

LDO REGULATOR ELECTRICAL CHARACTERISTICS

At V_{IN} = $V_{OUT(TYP)}$ + 0.5 V or 2 V (whichever is greater); I_{OUT} = 10 mA, V_{EN} = 0.9 V, C_{OUT} = 1 µF, and T_J = -40°C to 125°C (unless otherwise noted). Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range		2		5.5	V
V_{OUT}	DC output accuracy	-40°C ≤ T_J ≤ 125°C	-2	0.5	2	%
$\Delta V_O/\Delta V_{IN}$	Line regulation	$V_{OUT(NOM)}$ + 0.5 V ≤ V_{IN} ≤ 5.5 V, I_{OUT} = 10 mA		1	5	mV
$\Delta V_O/\Delta I_{OUT}$	Load regulation	0 mA ≤ I_{OUT} ≤ 150 mA		1	15	mV
V_{DO}	Dropout voltage(1)	V_{IN} = 0.98 x $V_{OUT(NOM)}$, I_{OUT} = 50 mA, V_{OUT} = 2.8 V		37		mV
		V_{IN} = 0.98 x $V_{OUT(NOM)}$, I_{OUT} = 100 mA, V_{OUT} = 2.8 V		75		
I_{CL}	Output current limit	V_{IN} = 0.9 x $V_{OUT(NOM)}$	320	500	860	mA
I_{GND}	Ground pin current	I_{OUT} = 0 mA		35	55	µA
		I_{OUT} = 150 mA, V_{IN} = V_{OUT} = 0.5 V		370		
I_{SHDN}	Ground pin current (shutdown)	V_{EN} ≤ 0.4 V, V_{IN} = 2 V		400		nA
		V_{EN} ≤ 0.4 V, 2 V ≤ V_{IN} ≤ 4.5 V_{IN}, T_J = -40°C to 85°C		1	2	µA
PSRR	Power-supply rejection ratio	V_{IN} = 2.3 V, V_{OUT} = 1.8 V, I_{OUT} = 10 mA, f = 1 kHz		68		dB
V_N	Output noise voltage	BW = 100 Hz to 100 kHz, V_{IN} = 2.3 V, V_{OUT} = 1.8 V, I_{OUT} = 10 mA		48		μV_{RMS}

(1) V_{DO} is measured for devices with $V_{OUT(NOM)}$ ≥ 2.35 V.

PRODUCT PREVIEW

LDO REGULATOR ELECTRICAL CHARACTERISTICS (continued)

At V_{IN} = $V_{OUT(TYP)}$ + 0.5 V or 2 V (whichever is greater); I_{OUT} = 10 mA, V_{EN} = 0.9 V, C_{OUT} = 1 µF, and T_J = -40°C to 125°C (unless otherwise noted). Typical values are at T_J = 25°C.

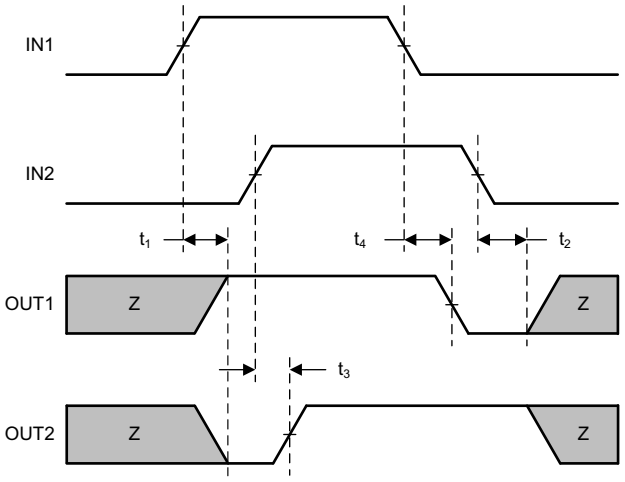
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{STR}	Startup time(2)	C_{OUT} = 1 µF, I_{OUT} = 150 mA		100		µs
$V_{EN(HI)}$	Enable pin high (enabled)		0.9		V_{IN}	V
$V_{EN(LO)}$	Enable pin low (disabled)		0		0.4	V
I_{EN}	Enable pin current	V_{IN} = V_{EN} = 5.5 V		0.04		µA
UVLO	Undervoltage lockout	V_{IN} rising		1.9		V
$R_{DISCHARGE}$	Active pulldown resistance	V_{EN} = 0 V		120		Ω
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		165		°C
		Reset, temperature decreasing		145		

(2) Startup time = time from EN assertion to 0.98 x $V_{OUT(NOM)}$.

TIMING REQUIREMENTS

T_A = 25°C, V_M = 5 V, V_{CC} = 3 V, R_L = 20 Ω

			MIN	MAX	UNIT
1	t_1	Output enable time		120	ns
2	t_2	Output disable time		120	ns
3	t_3	Delay time, INx high to OUTx high		120	ns
4	t_4	Delay time, INx low to OUTx low		120	ns
5	t_5	Output rise time	50	150	ns
6	t_6	Output fall time	50	150	ns



DRV8851

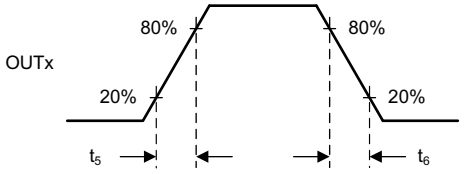


Figure 1. Timing Requirements

FUNCTIONAL DESCRIPTION

Bridge Control

The DRV8851 is controlled using a PWM input interface, also called an IN/IN interface. Each output is controlled by a corresponding input pin..

The following table shows the logic for the DRV8851:

Table 2. DRV8851 Logic

IN1	IN2	OUT1	OUT2	FUNCTION (DC MOTOR)
0	0	Z	Z	Coast
0	1	L	H	Reverse
1	0	H	L	Forward
1	1	L	L	Brake

Sleep Mode

If the nSLEEP pin is brought to a logic-low state, the DRV8851 will enter a low-power sleep mode. In this state all unnecessary internal circuitry is powered down.

Power Supplies and Inputs

The input pins may be driven within their recommended operating conditions with or without the VCC power supply present. No leakage current path will exist to the supply. There is a weak pulldown resistor (approximately 100 kΩ) to ground on each input pin. VCC and VM may be applied and removed in any order. When VCC is removed, the device enters a low-power state and very little current is drawn from VM. If the supply voltage is between 1.8 V and 7 V, VM and VCC may be connected together.

LDO Voltage Regulator

The LDO voltage regulator in the DRV8851 is identical to the TI TLV702xx. Please refer to the TLV702xx datasheet for details and full specifications.

Protection Circuits

The DRV8851 is fully protected against undervoltage, overcurrent and overtemperature events.

Overcurrent Protection (OCP)

An analog current limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than the OCP time, all FETs in the H-bridge will be disabled. After approximately 1 ms, the bridge will be re-enabled automatically.

Overcurrent conditions on both high and low side devices; i.e., a short to ground, supply, or across the motor winding will all result in an overcurrent shutdown.

Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge will be disabled. Once the die temperature has fallen to a safe level operation will automatically resume.

Undervoltage Lockout (UVLO)

If at any time the voltage on the VCC pins falls below the undervoltage lockout threshold voltage, all circuitry in the device will be disabled, and internal logic will be reset. Operation will resume when VCC rises above the UVLO threshold.

PRODUCT PREVIEW

THERMAL INFORMATION

Thermal Protection

The DRV8851 has thermal shutdown (TSD) as described above. If the die temperature exceeds approximately 150°C, the device will be disabled until the temperature drops to a safe level.

Any tendency of the device to enter TSD is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

Power Dissipation

Power dissipation in the DRV8851 is the sum of the motor driver power dissipation and the LDO voltage regulator dissipation.

The LDO dissipation is calculated simply by $(V_{IN} - V_{OUT}) \times I_{OUT}$.

The power dissipation in the motor driver is dominated by the power dissipated in the output FET resistance, or $R_{DS(ON)}$. Average power dissipation when running a stepper motor can be roughly estimated by Equation 1.

$$P_{TOT} = R_{DS(ON)} \bullet (I_{OUT(RMS)})^2 \quad (1)$$

where P_{TOT} is the total power dissipation, $R_{DS(ON)}$ is the resistance of the HS plus LS FETs, and $I_{OUT(RMS)}$ is the RMS output current being applied to the load.

The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

Note that $R_{DS(ON)}$ increases with temperature, so as the device heats, the power dissipation increases.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
DRV8851-25DSSR	PREVIEW	WSON	DSS	12	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	885125	
DRV8851-27DSSR	PREVIEW	WSON	DSS	12	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	885127	
DRV8851-33DSSR	PREVIEW	WSON	DSS	12	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	885133	

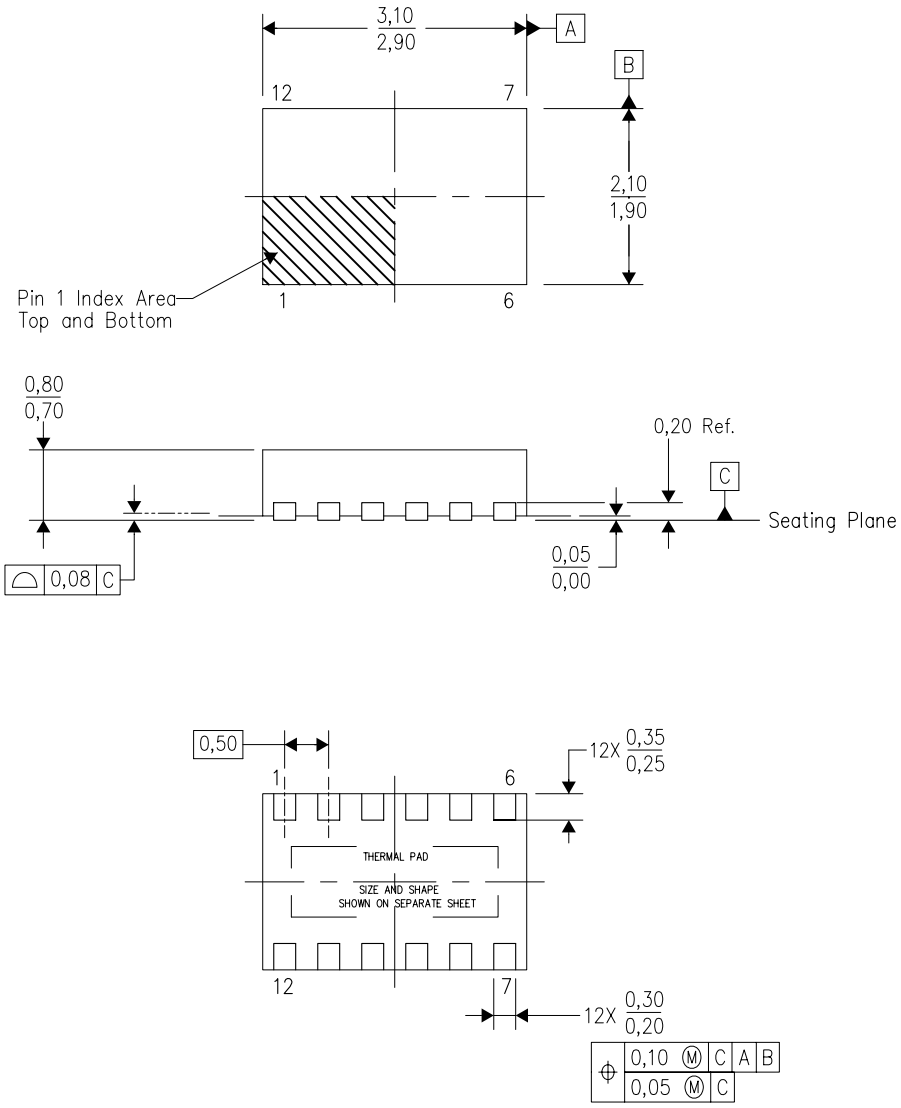
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

DSS (R–PWSON–N12) PLASTIC SMALL OUTLINE NO–LEAD



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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

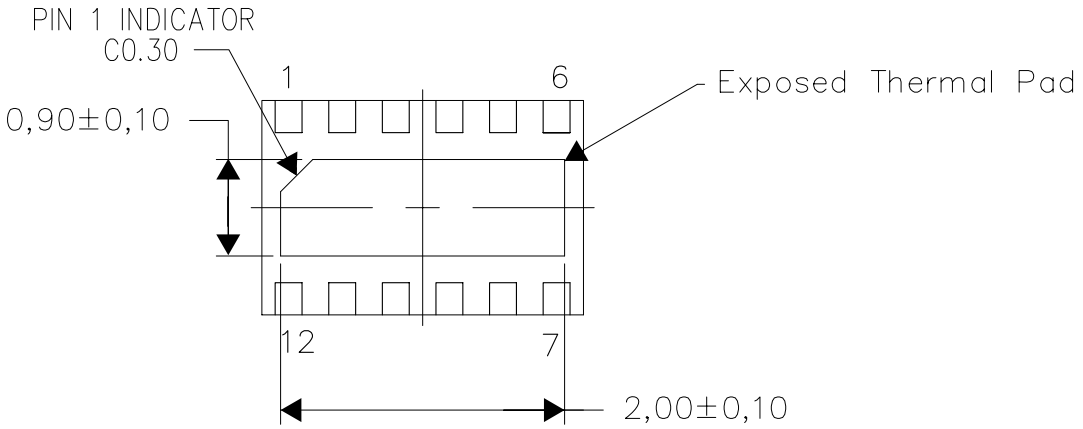
DSS (R–PWSON–N12) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4210135–3/C 02/12

NOTE: All linear dimensions are in millimeters

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