

Thunderbolt™ SUPPLY SELECTION IC

Check for Samples: [TPS22985](#)

FEATURES

- 2.8 V to 19.8 V
- Auto Selects 3.3 V Supply
- > 10-mA Low Power Switch
- > 500-mA High Power Switch
- Reverse Current Blocking From OUT to VDD
- Wake on UART Input Activity
- UART RX and TX Buffers

APPLICATIONS

- Thunderbolt™ Cables
- Notebook Computers
- Desktop Computers
- Power Management Systems

DESCRIPTION

The TPS22985 is a supply selection device for active Thunderbolt™ cables. The device selects a supply that is at 3.3V from two supply inputs and connects this to two non-current limited outputs OUTA and OUTB. When 3.3V is not present at either supply, the outputs become high impedance.

The TPS22985 has two modes of operation, Normal and Control.

In Normal Mode, OUTA is always on when a valid supply is present. OUTB is connected to a valid VDD when the ENB input is high.

In Control Mode, OUTA functions the same as Normal Mode and OUTB is controlled by a combination of monitored inputs and valid supplies on VDD1 and VDD2. When a valid VDD is available, the device waits for a rising input on ENB and then disconnects OUTB until the next falling RXH transition. Once the next falling RXH transition occurs, the device reconnects OUTB.

In either mode, when a valid VDD is not available, the TPS22985 opens all switches and the outputs OUTA and OUTB become high impedance. When the connected VDD exceeds a maximum voltage of 3.6V, it is disconnected from the outputs. VDD2 will only connect when it is in the valid range and VDD1 is greater than 3.6V.

The TPS22985 is available in a 1.6mm x 1.6mm W CSP package.

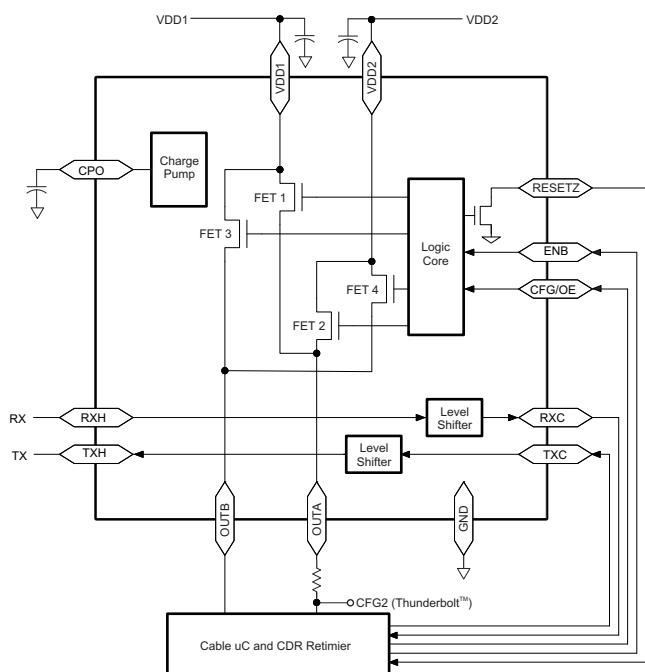


Figure 1. Typical Application



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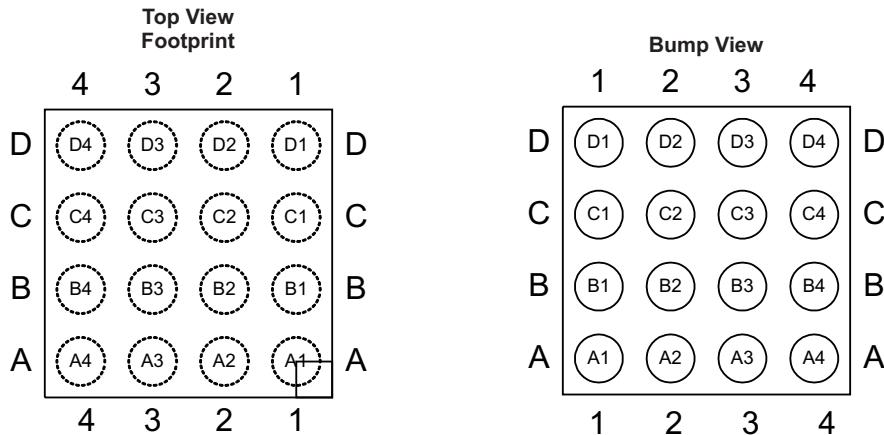


These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

PART NUMBER	PACKAGE MARKING ⁽¹⁾	PACKAGE	DEVICE SPECIFIC FEATURES
TPS22985YFP	YMD9US	YFP	WCSP

(1) Y= Year, M = Month, D = Sequence Code, 9U = TPS22985 Device Code, S = Wafer Fab/Assembly Site Code



Die Size: 1.6mm x 1.6mm

Bump Size: 0.25mm

Bump Pitch: 0.4mm

Table 1. TPS22985 Pin Mapping (Top View)

	4	3	2	1
D	VDD1	VDD1	VDD2	VDD2
C	OUTA	OUTB	OUTB	GND
B	RXH	TXH	RESETZ	CPO
A	RXC	TXC	ENB	CFG/OE

DISSIPATION RATINGS

PACKAGE	THERMAL RESISTANCE θ_{JA}	THERMAL RESISTANCE ⁽¹⁾ θ_{JB}	POWER RATING $T_A = 25^\circ\text{C}$	DERATING FACTOR ABOVE ⁽²⁾ $T_A = 25^\circ\text{C}$
YFP	95°C/W	63°C/W	1050 mW	10.5 mW/°C

(1) Simulated with high-K board

(2) Maximum power dissipation is a function of $T_{J(\text{max})}$, θ_{JA} and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(\text{max})} - T_A) / \theta_{JA}$.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)⁽¹⁾ ⁽²⁾

		VALUE	UNIT
V _I	Voltage range on VDD1, VDD2, OUTA, OUTB ⁽³⁾	–0.3 to 20	V
	Voltage range on RXC, TXC, RESETZ, CFG/OE, ENB ⁽³⁾ (VDD is the active 3.3V input)	–0.3 to VDD+0.3	V
	Voltage range on CPO	–0.3 to 13	V
	Voltage range on RXH, TXH	–0.3 to 4.0	V
T _A	Operating ambient temperature range	–40 to 85	°C
T _{J (MAX)}	Maximum operating junction temperature	125	°C
T _{stg}	Storage temperature range	–65 to 150	°C
	Charge Device Model (JESD 22 C101)	350	V
	Human Body Model (JESD 22 A114)	2	kV
	Contact discharge on VDD1, VDD2 (IEC 61000-4-2) ⁽⁴⁾	4.4	kV

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature [T_{A(max)}] is dependent on the maximum operating junction temperature [T_{J(max)}], the maximum power dissipation of the device in the application [P_{D(max)}], and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: T_{A(max)} = T_{J(max)} – (θ_{JA} × P_{D(max)})
- (3) All voltage values are with respect to network ground terminal.
- (4) IEC tests are run with 0.1 μF on VDD1 and VDD2. IEC rating is non-destructive.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
V _{DD1}	Supply voltage range	2.8	19.8	V
V _{DD2}		2.8	19.8	
I _{LIM1/2}	FET1 and FET2 switch current range	0	10	mA
I _{LIM3/4}	FET3 and FET4 switch current range	0	500	mA
V _{IH}	Input logic high	RXH, TXC, CFG/OE, ENB	2	V
V _{IL}	Input logic low	RXH, TXC, CFG/OE, ENB	0.8	V
V _{OH}	Output logic high	RXC, TXH, RESETZ	2.25	V
V _{OL}	Output logic low	RXC, TXH, RESETZ	0.4	V
C _{OUT}	Output capacitance on OUTA	1	4	μF
	Output capacitance on OUTB	4	22	
C _{CPO}	Output capacitance on CPO	2	10	nF
T _A	Operating temperature range	–40	85	°C

ELECTRICAL CHARACTERISTICS

Unless otherwise noted the specification applies over the V_{DD} range and operating junction temp $-40^\circ\text{C} \leq T_J \leq 85^\circ\text{C}$. Typical values are for $V_{DD} = 3.3\text{V}$ and $T_J = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
POWER SUPPLIES AND CURRENTS						
$V_{DD1/2}$	Input voltage range		2.8	19.8	V	
I_{DD-1}	V_{DD1} Quiescent current	$V_{DD1} = 2.5$ to 15 V	250	500	μA	
I_{DD-2}	V_{DD2} Quiescent current	$V_{DD2} = 3.3\text{ V}$, $V_{DD1} = 3.3\text{ V}$	20		μA	
		$V_{DD2} = 3.3\text{ V}$, $V_{DD1} = 15\text{ V}$	20			
$I_{DDOFF-2}$	V_{DD2} Off current	$V_{DD2} = 3.3\text{ V}$, $V_{DD1} = 0\text{ V}$		1	μA	
I_{IN-ENB}	ENB Input current	$V_{IN} = 1.8\text{ V}$ to 3.6 V		1	μA	
$I_{IN-UART}$	RXH Input current	$V_{IN} = 1.8\text{V}$ to 3.6 V		1	μA	
$I_{IN-CFGOE}$	CFG/OE Input current ⁽¹⁾	$V_{CFG/OE} = 0\text{ V}$	-1	-1.8	-5	μA
$V_{PUCFGOE}$	CFG/OE pull-up voltage ⁽¹⁾		2.3	6.7	V	
$I_{IN-RESETZ}$	RESETZ Input current	$V_{RESETZ} = 100\text{ mV}$	0.8	2	3	mA
SWITCH AND RESISTANCE CHARACTERISTICS						
R_{F1}	FET1 On resistance	$V_{DD} = 3.3\text{ V}$, $I_{OUT} = 10\text{ mA}$		5	Ω	
R_{F2}	FET2 On resistance			5		
R_{F3}	FET3 On resistance	$V_{DD} = 3.3\text{ V}$, $I_{OUT} = 350\text{ mA}$	170	250	$\text{m}\Omega$	
R_{F4}	FET4 On resistance		170	250		
$R_{PDRESETZ}$	RESETZ Pull-down resistance	RESETZ asserted	33	50	100	Ω
$R_{PUCFGOE}$	CFG/OE Pull-up resistance ⁽¹⁾		1.2	2	2.6	$\text{M}\Omega$
R_{PDUART}	TXC Pull-down resistance	See the UART RX and TX Section	80	130	180	$\text{k}\Omega$
VOLTAGE THRESHOLDS AND AMPLITUDES						
V_{HVLO}	High voltage lockout	3.3V Supply rising	3.5	3.55	3.6	V
	Hysteresis		20	40	60	mV
V_{UVLO}	Under voltage lockout	3.3V Supply rising	2.7	2.75	2.8	V
		3.3V Supply falling	2.4	2.45	2.5	
V_{CPO}	Charge pump voltage	$C_{CPO} = 2\text{ nF}$, $I_{CPO} = 0\text{ }\mu\text{A}$	7	8	9	V
V_{os}	Voltage overshoot on OUTA/B	$C_{OUTB} = 4\text{ }\mu\text{F}$, $I_{OUTB} = 0\text{ mA}$, $C_{OUTA} = 1\text{ }\mu\text{F}$, $I_{OUTA} = 0\text{ mA}$ V_{DD1} $\text{SR}_{3.3 \rightarrow 4\text{V}} = 10\text{ mV}/\mu\text{s}$			200	mV

(1) CFG/OE is pulled up to $V_{PUCFGOE}$ through the resistance $R_{PUCFGOE}$.

ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise noted the specification applies over the V_{DD} range and operating junction temp $-40^\circ\text{C} \leq T_J \leq 85^\circ\text{C}$. Typical values are for $V_{DD} = 3.3\text{V}$ and $T_J = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
THERMAL SHUTDOWN					
T_{SD}	Shutdown temperature		110	130	°C
T_{SDHYST}	Shutdown hysteresis		15		°C
TRANSITION TIMING					
t_d	UVLO to FETn open time	$C_{OUTB} = 4 \mu\text{F}$, $C_{OUTA} = 1 \mu\text{F}$	200		μs
t_e	UVLO to FETn closed time		2		ms
t_{dh}	HVLO to FETn open time		20		μs
t_{eh}	HVLO to FETn closed time	See The Supply Switch-Over During HVLO Section			
TRANSITION TIMING (NORMAL MODE)					
t_{eb}	ENB to FET3/4 closed time	$C_{OUTB} = 4 \mu\text{F}$, $C_{OUTA} = 1 \mu\text{F}$	2		ms
t_{db}	ENB to FET3/4 open time		200		μs
TRANSITION TIMING (CONTROL MODE)					
t_{U2R}	UVLO to RESETZ time		5	6	7
t_{E2R}	ENB to RESETZ time		2	10	μs
t_{E2O}	ENB to FET3/4 open time	$C_{OUTB} = 4 \mu\text{F}$, $C_{OUTA} = 1 \mu\text{F}$	100	200	μs
t_{RX2O}	RX to FET3/4 closed time	$C_{OUTB} = 4 \mu\text{F}$, $C_{OUTA} = 1 \mu\text{F}$	0.8	2	ms
t_{RX2R}	RX to RESETZ Time		5	6	7
t_{OE2TX}	OE to TXH Valid Time		20		μs
t_{OE2TXZ}	OE to TXH Hi-Z Time		20		μs
TXC/TXH I/O (CONTROL MODE)					
V_{IH}	TXC Input logic high		2		V
V_{IL}	TXC Input logic low			0.8	V
V_{OH}	TXH Output logic high		2.25		V
V_{OL}	TXH Output logic low			0.4	V
T_R / T_F	TXH Rise and fall time	10-90% CL = 20 pF	5	70	ns
Z_O	TXH Output impedance		35		Ω
f_{MAX}	TX Input signal frequency			1	Mb/s
DC	TX Duty cycle		40%	60%	
RXC/RXH I/O (CONTROL MODE)					
V_{IH}	RXC Input logic high		2		V
V_{IL}	RXC Input logic low			0.8	V
V_{OH}	RXC Output logic high		2.25		V
V_{OL}	RXC Output logic low			0.4	V
T_R / T_F	RXC Rise and fall time	10-90% CL = 20 pF	20	120	ns
f_{MAX}	RX Input signal frequency			1	Mb/s
DC	RX Duty cycle		40%	60%	

FUNCTIONAL BLOCK DIAGRAM

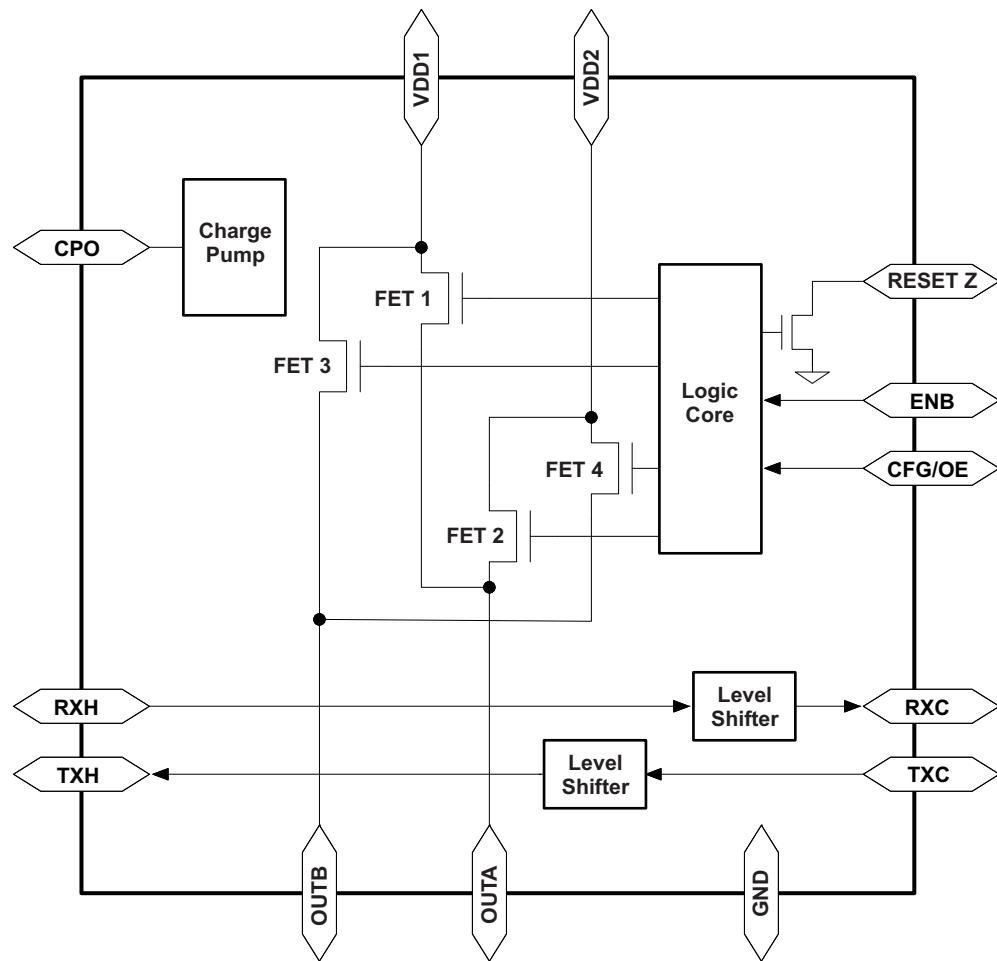


Figure 2. Functional Block Diagram

DEVICE INFORMATION

PIN FUNCTIONS

PIN NAME	TYPE	DESCRIPTION
VDD1	Supply	Device Supply 1. 0V to 19.8-V Input.
VDD2	Supply	Device Supply 2. 0V to 19.8-V Input.
OUTA	Output	Output A. 10-mA capable output. Refer to the Supply Selection section for more information.
OUTB	Output	Output B. 500-mA capable output. Refer to the Normal Mode and Control Mode sections for more information.
CPO	Output	Charge Pump Output. This pin is the output of the internal charge pump. It drives the gates of the internal FET switches. Connect a capacitor of at least 2nF to this pin.
CFG/OE	Input	Mode Configuration/Output Enable. When CFG is floating, the device is in Normal Mode. When CFG is ground, the device is in Control Mode (see the APPLICATION INFORMATION section for more information). The mode is latched at power-up. When the device enters Control Mode, this pin becomes an output enable for the UART TXH output. See the UART RX and TX section for more information. A pull-down resistance between this pin and GND is recommended when Control Mode is desired.
RXH	Input	UART RX Input. Monitored Input for data activity to enable outputs. In Control Mode, this pin is monitored for a high to low transition to enable the outputs. This input is level shifted and driven on RXC. See the UART RX and TX section for more information.
RXC	Output	UART RX Output. This output is a level shifted version of RXH. RXC is referenced to OUTA. See the UART RX and TX section for more information.
TXC	Input	UART TX Input. This input is buffered and level shifted on TXH. See the UART RX and TX section for more information.
TXH	Output	UART TX Output. This output is a buffered and level shifted version of TXC. TXH is referenced to OUTA. See the UART RX and TX section for more information.
RESETZ	Output	Microcontroller Reset. This pin is a delayed reset signal indicating OUTB is connected to a valid VDD. RESETZ in an open-drain pull-down. RESETZ is low when OUTB is high impedance.
ENB	Input	OUTB Enable. In Normal Mode, this pin is the active high OUTB enable. In Control Mode, this pin opens OUTB when asserted high and resets the device until a new transition on RX occurs.
GND	Supply	Device ground.

APPLICATION INFORMATION

Supply Selection

The TPS22985 selects between two separate power supplies, VDD1 or VDD2, and connects these to two outputs (OUTA and OUTB) through non-current limited switches. When a valid VDD ($V_{UVLO} < VDD < V_{HVLO}$) is present on VDD1, VDD1 will be connected to the outputs. When $VDD1 > V_{HVLO}$, the TPS22985 will connect the outputs to VDD2 when a valid VDD is present on this input. OUTB is also opened and closed by other digital inputs, ENB and RXH, depending on the mode of the TPS22985. Refer to the [Normal Mode](#) and [Control Mode](#) sections for more information on the control of OUTB. VDD1 and VDD2 can power up in any order; however, VDD1 always takes priority over VDD2 and only allows VDD2 to connect when the $VDD1 > V_{HVLO}$ condition is present. When the outputs are connected to VDD2, and VDD1 drops below V_{HVLO} , the TPS22985 will disconnect the outputs from VDD2. [Figure 3](#) shows a flow diagram illustrating the selection of VDD1 or VDD2 as the appropriate supply to connect to OUTA and OUTB. Note, this diagram does not show the enabling and disabling of OUTB by ENB and RXH.

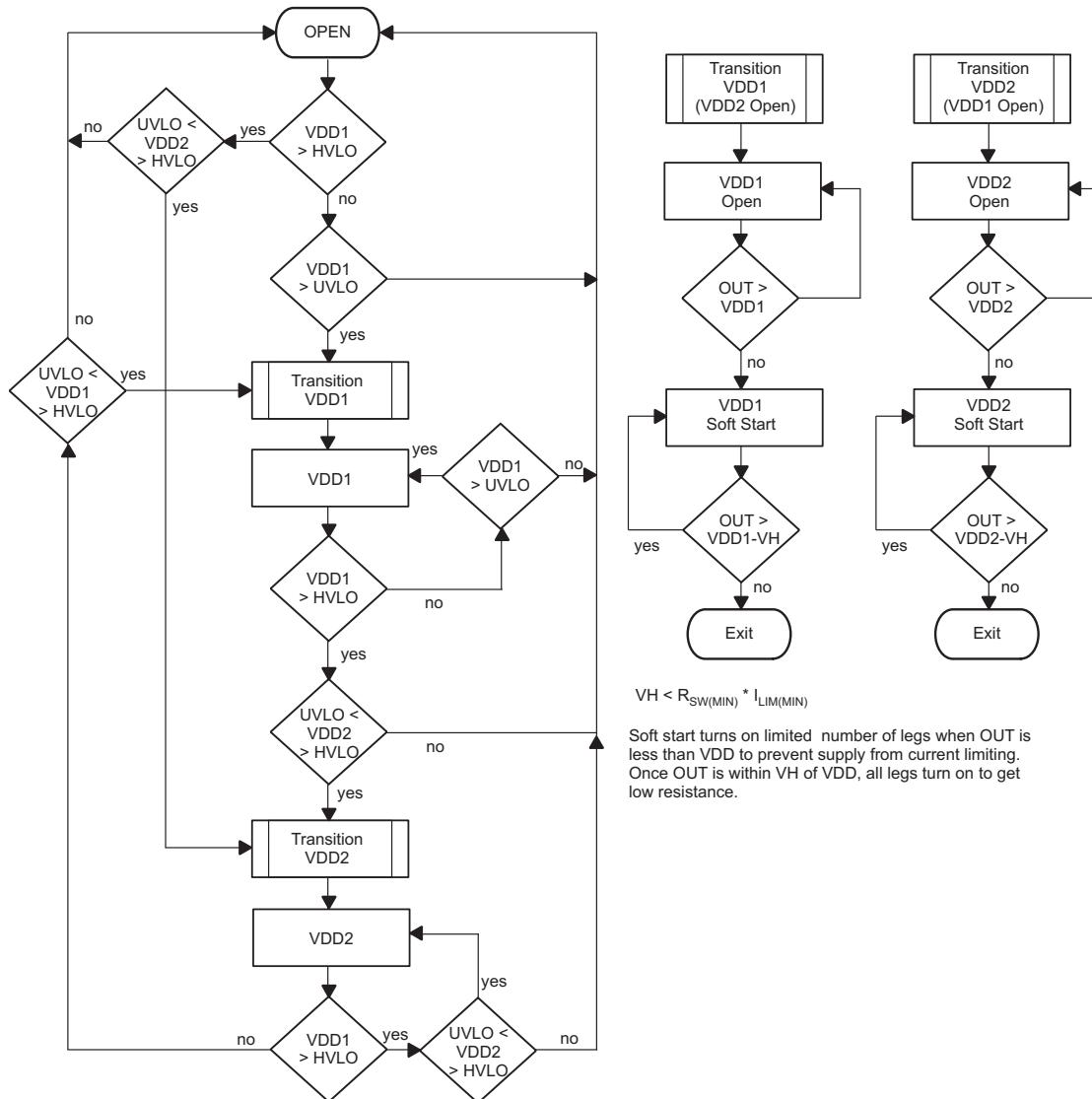


Figure 3. Flow Diagram of Supply Selection and Switch-Over

Normal Mode

When the CFG/OE pin is floating at power-up, the device enters Normal Mode. In Normal Mode, the TPS22985 provides power via OUTA and OUTB.

OUTA is connected whenever a valid VDD is present on VDD1. OUTA may also be connected if VDD1 > V_{HVLO} and a valid VDD is connected to VDD2. When OUTA is connected it will supply ≥ 10 mA to a load. OUTB is connected whenever a valid VDD is present on VDD1. OUTB may also be connected if VDD1 > V_{HVLO}, a valid VDD is connected to VDD2, and the control signal ENB is high. When OUTB is connected it will supply ≥ 500 mA to a load.

When a valid VDD is not present, the TPS22985 enters into a shutdown mode and blocks current flow through the switches.

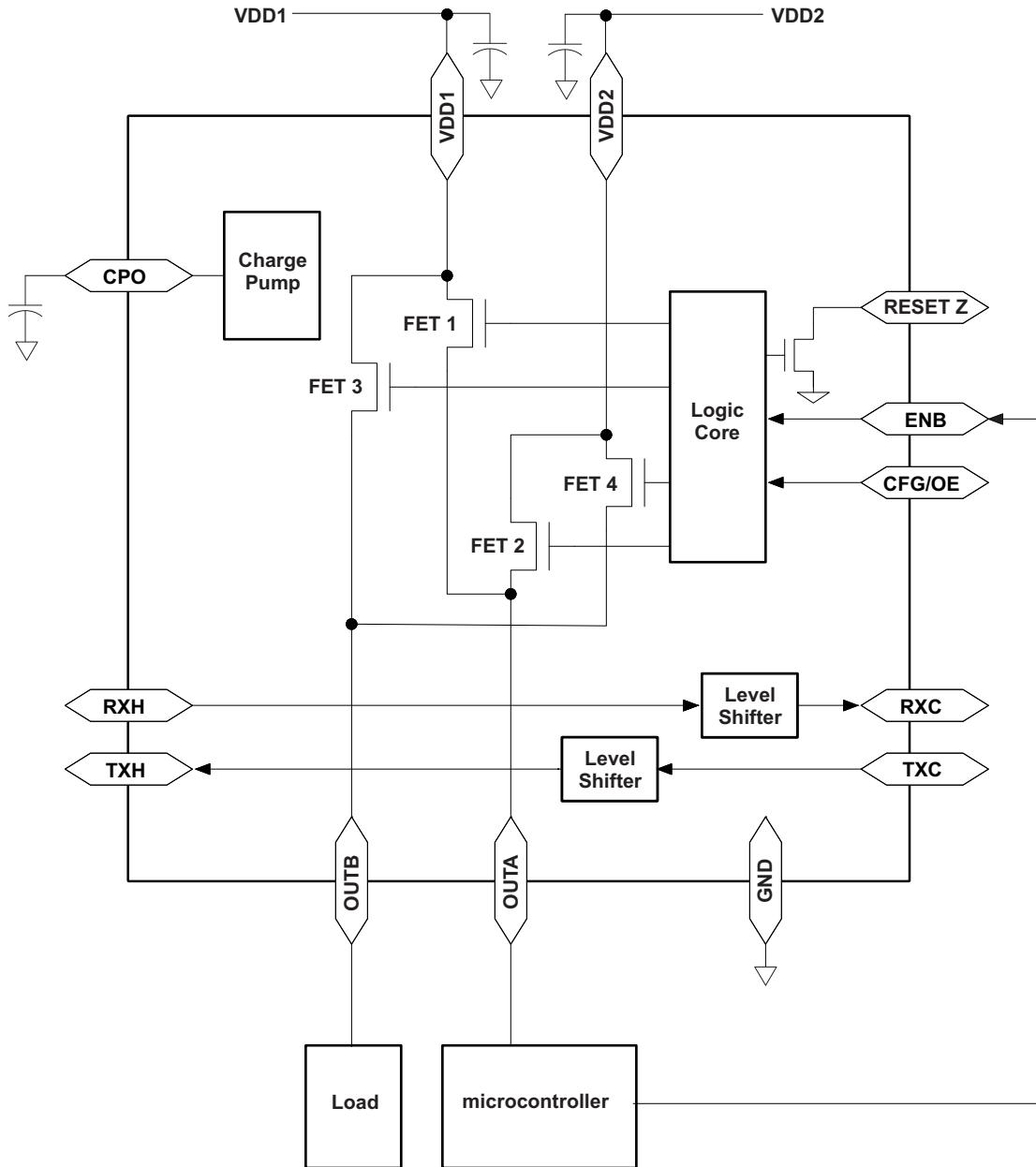


Figure 4. Normal Mode Typical Application

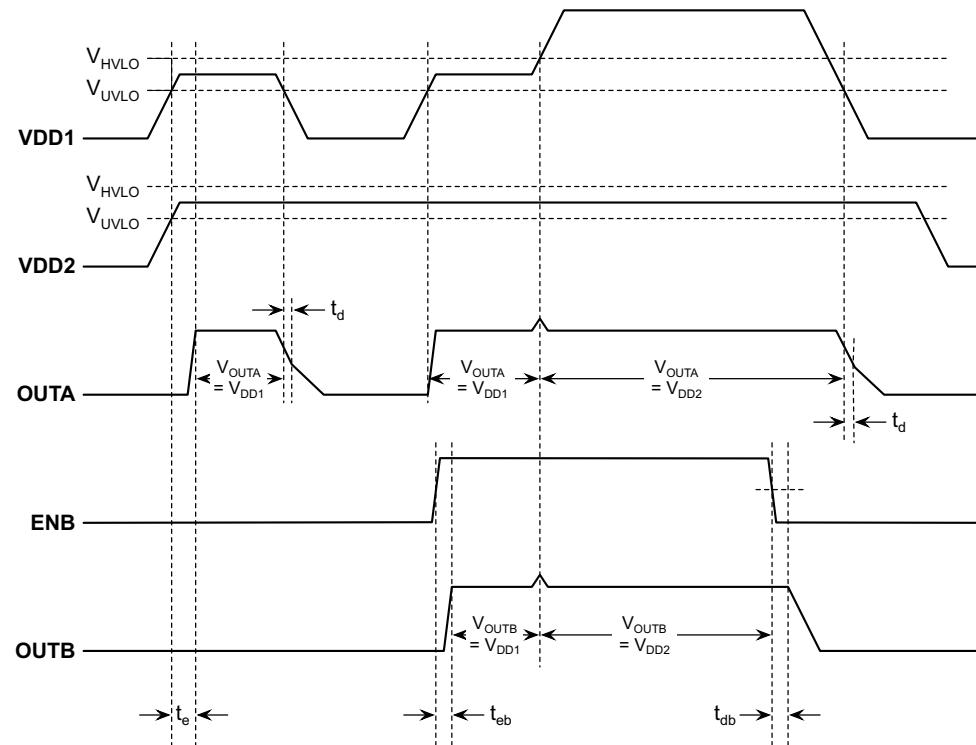


Figure 5. Timing During Normal Mode

Control Mode

When CFG/OE pin is grounded at power-up, the device latches into Control Mode. In Control Mode, the TPS22985 provides power to a microcontroller/CDR device.

When a valid VDD is connected, OUTA and OUTB are connected to the VDD. OUTB remains connected to VDD until ENB transitions high. OUTA remains connected to VDD as long as a valid VDD exists. RESETZ indicates that a valid VDD is available at OUTB. When RESETZ is low, a valid VDD is not available, if RESETZ is high, a valid VDD is available.

When ENB transitions high, RESETZ is asserted low and OUTB is opened until a falling edge on RXH is detected, as illustrated in [Figure 7](#) and [Figure 8](#). When ENB transitions high, RESETZ will assert low after time t_{E2R} and OUTB will open after time t_{E2O} . During the time t_{E2O} , RXH is not monitored. After the time t_{E2O} , the TPS22985 starts monitoring RXH for a falling edge. When a falling edge occurs and a valid VDD is available, RESETZ is transitioned from low to high and OUTB is connected to VDD until ENB transitions high again or until no valid VDD is available. When a valid VDD is not available, RESETZ is asserted low and the TPS22985 blocks current flow through the switches.

After the device is latched into Control Mode, the CFG/OE pin becomes the output enable for the TX buffer/level-shifter. Refer to the [UART RX and TX](#) section for more information.

OUTA can be used as a pull-up for the Thunderbolt™ CFG2 connector pin as an indicator that power is available to the cable active circuitry. Place a resistor greater than $1\text{k}\Omega$ between OUTA and CFG2 in this case.

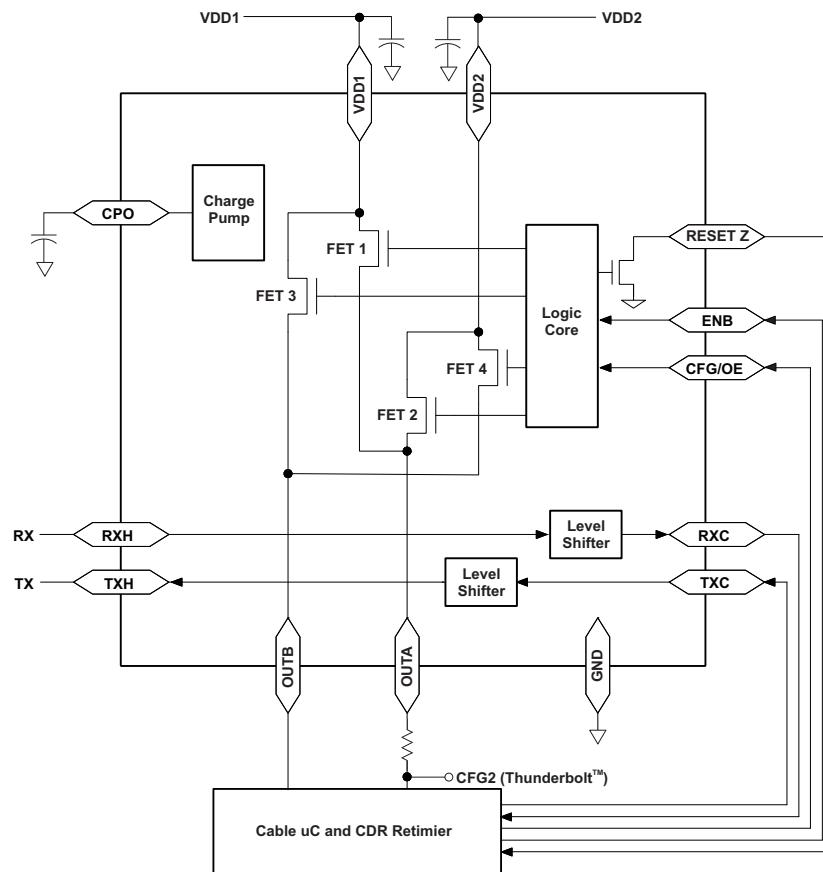


Figure 6. Control Mode Typical Application

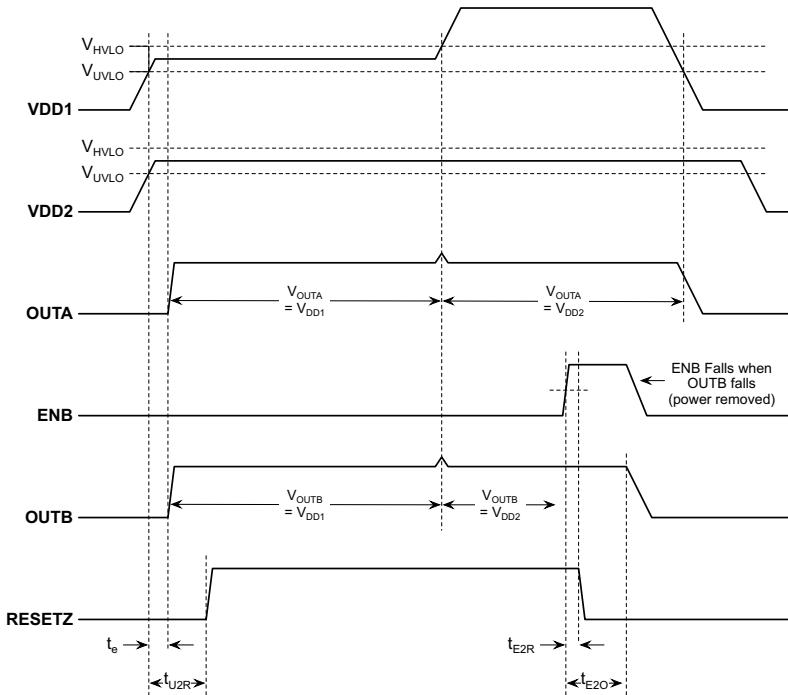


Figure 7. Timing During Control Mode

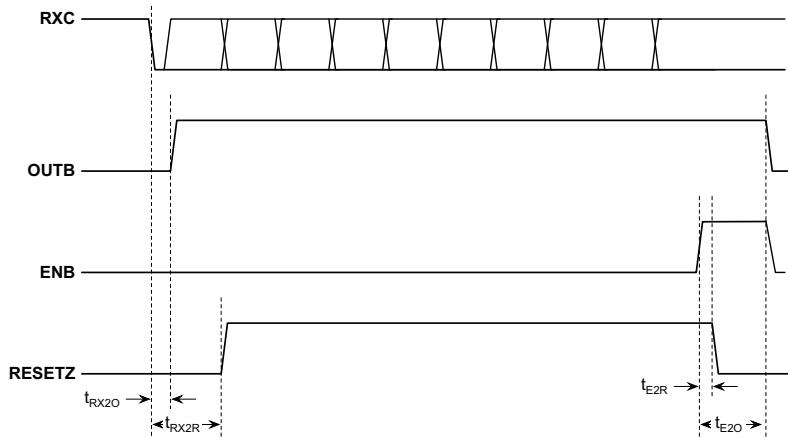


Figure 8. Timing During Control Mode Continued

Typical Startup

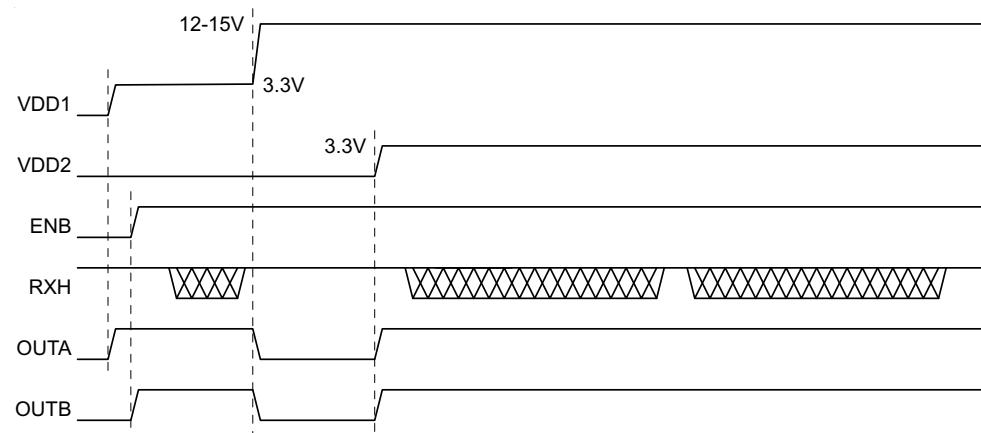


Figure 9. Typical Startup in Normal Mode

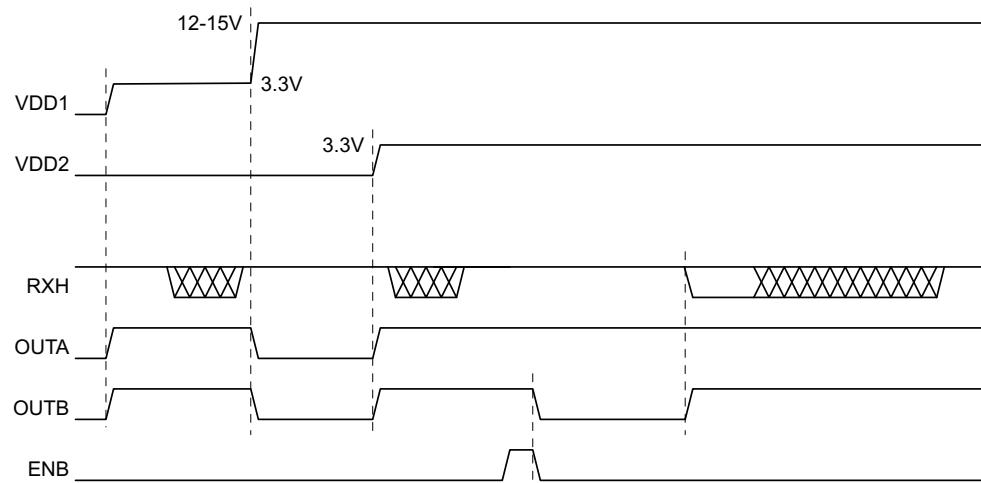


Figure 10. Typical Startup Timing for Control Mode

Figure 10. Typical Startup Timing for Control Mode

Soft Start

To prevent inrush current to the load, the TPS22985 soft starts OUTA and OUTB. When OUTA and OUTB are first enabled, the resistance of the FET switches (FET1, FET2, FET3, and FET4) starts high and reduces every 250 μ s in four steps. Figure 11 shows the nominal resistance ramp profile for OUTB. The resistance shown in this figure is the equivalent resistance through FET3 and FET4 in Figure 2.

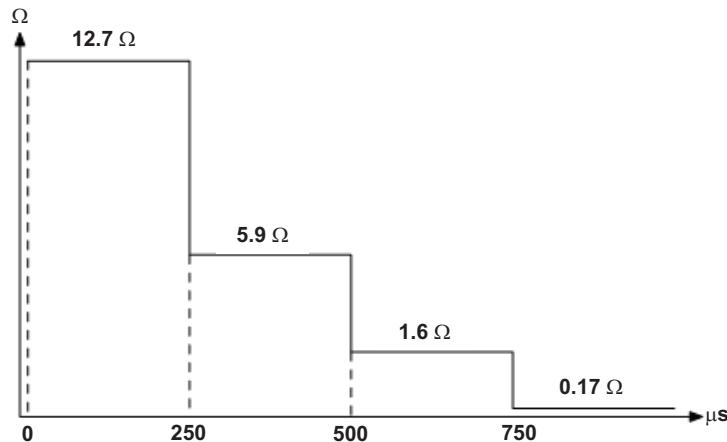


Figure 11. OUTB Soft Start Resistance vs Time Profile

Supply Switch-Over During HVLO

When OUTA and OUTB are connected to VDD1 and VDD1 crosses V_{HVLO} , the TPS22985 will open the FET1/3 switches. Due to the delay t_{dh} , the output will overshoot V_{HVLO} by V_{OS} . When a valid VDD is present on VDD2, OUTA and OUTB will connect to VDD2 after time t_{eh} . Figure 12 illustrates this switch-over event.

The overshoot V_{OS} will occur when the VDD (VDD1 or VDD2) that is connected to the output transitions above V_{HVLO} . V_{OS} is set by the delay t_{dh} and the slew rate of the connected VDD. However, the connection of the outputs to VDD2 will only occur when VDD1 transitions above V_{HVLO} and VDD2 is a valid VDD.

The following equation determines the overshoot V_{OS} .

$$V_{OS} = SR_{VDD} \times t_{DH} \quad (1)$$

SR_{VDD} is the slew rate of the supply that is transitioning above V_{HVLO} . As an example, when SR_{VDD} is 10mV/ μ s and t_{dh} is 20 μ s, V_{OS} is 200mV.

When switching to VDD2 due to an HVLO event on VDD1, the outputs OUTA and OUTB are discharged by their respective loads until they reach the VDD2 voltage. This prevents in-rush current when charging the output caps. The discharge time t_{eh} is variable and is determined by the following equation.

$$t_{eh} = t_{dh} + (V_{HVLO} + V_{OS} - V_{DD2}) \times C_{LOAD}/I_{LOAD} \quad (2)$$

In this equation, V_{OS} is determined by [Equation 1](#), C_{LOAD} is the load capacitance at the respective output, and I_{LOAD} is load current flowing out of the same output. As an example, when VDD2 is 3.3V, t_{dh} is 20 μ s, V_{OS} is 200mV, C_{LOAD} is 4 μ F, and I_{LOAD} is 350mA, the resulting t_{eh} is 25.7 μ s.

Note, when VDD1 transitions above V_{HVLO} and a valid VDD is not present on VDD2, the outputs will open and will discharge through each respective load.

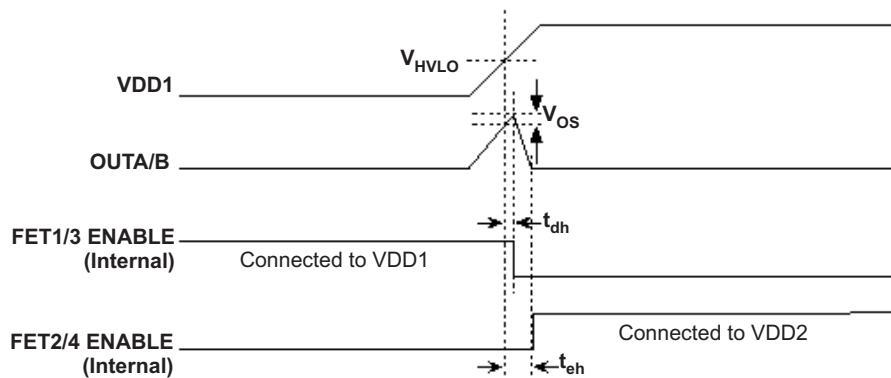


Figure 12. VDD switch-over at VDD1 rising above V_{HVLO}

UART RX and TX

The TPS22985 provides failsafe buffers for digital UART RX and TX lines. The failsafe mechanism prevents the RX and TX lines from being loaded when power is removed from the device. The RX line is divided into a host side RXH input and a cable side RXC output. The TX line is divided into host side TXH output and a cable side TXC input.

The RXH and TXC inputs are used in Control Mode only and must be pulled low when the device is in Normal Mode. In Normal Mode, leave the RXH and TXC pins disconnected from the UART signal lines and pull low through a $> 1\text{k}\Omega$ resistance.

In Control Mode, when the TPS22985 is unpowered or when RESETZ is asserted low, the TXH output is high impedance. This prevents loading the system TX line and allowing other devices on the UART bus to communicate. The RXC output is pulled low through the output driver during this same condition.

Figure 13 illustrates the RXC and TXH control when in Control Mode. When RESETZ is high, CFG/OE controls TXH. When CFG/OE is low, TXH is high impedance. When CFG/OE is high, TXH is a buffered and level-shifted TXC. The CFG/OE, ENB, and TXC inputs are ignored when RESETZ is asserted low. Figure 14 shows the delay from CFG/OE to TXH.

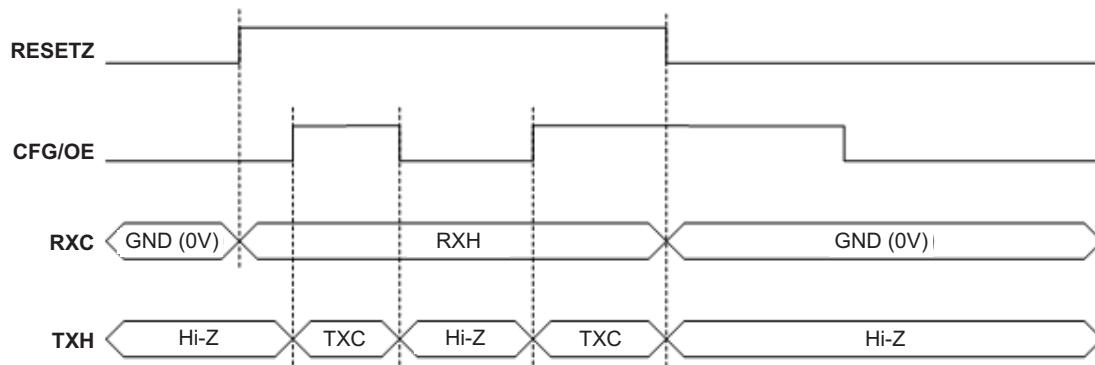


Figure 13. UART RX and TX Buffer Control During Control Mode

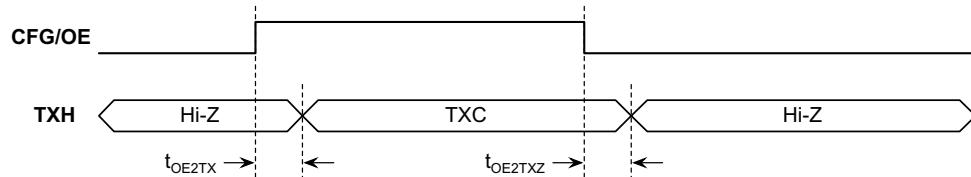


Figure 14. CFG/OE to TXH Timing During Control Mode

THUNDERBOLT™ SYSTEM WITH TPS22980/TPS22985

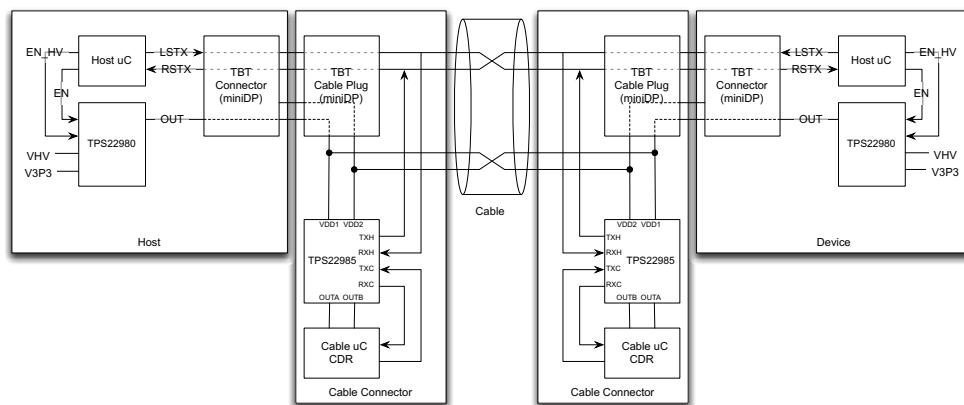
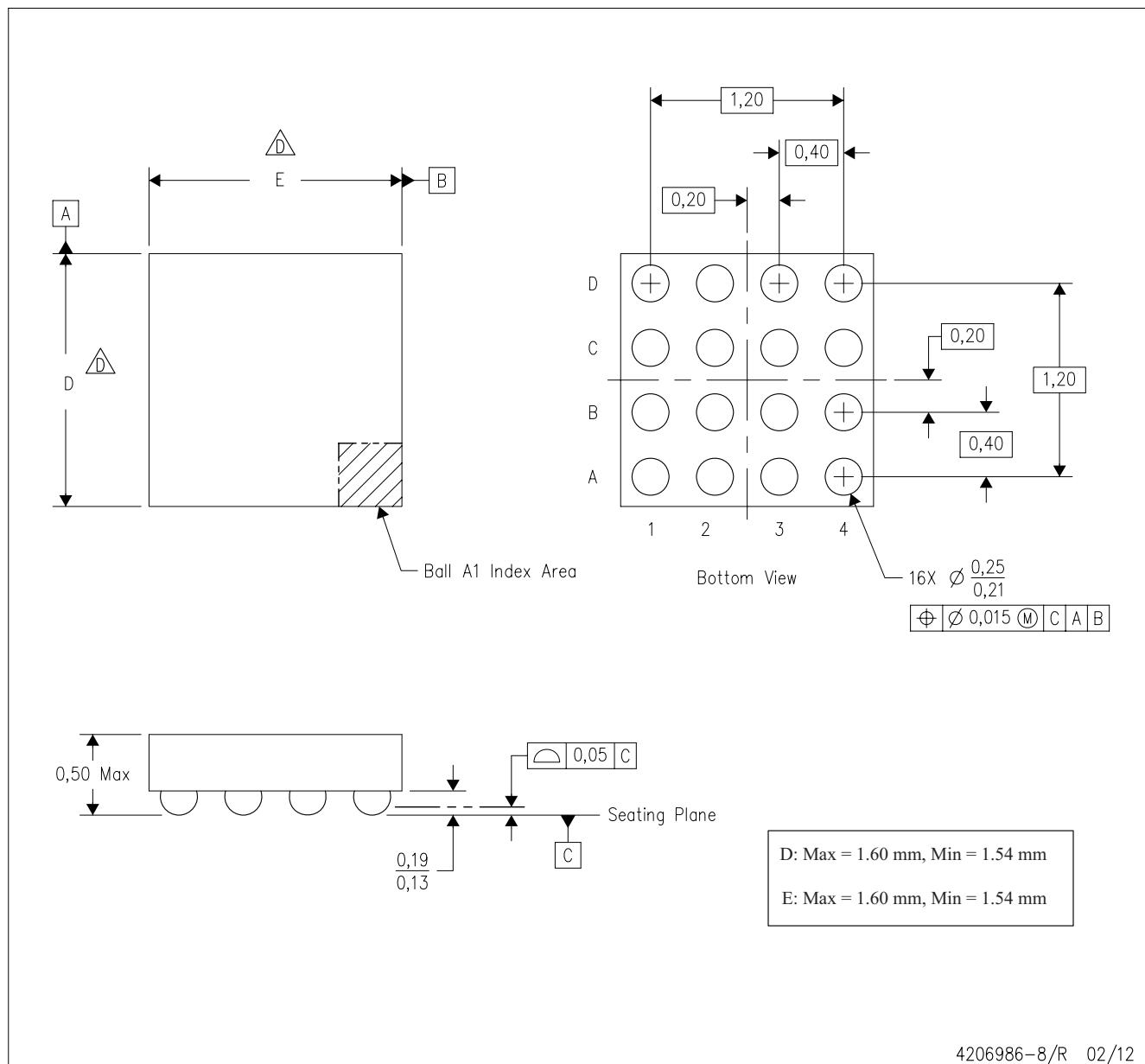


Figure 15. Thunderbolt System with TPS22980/TPS22985

YFP (S-XBGA-N16)

DIE-SIZE BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

C. NanoFree™ package configuration.

 The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative.

E. Reference Product Data Sheet for array population.

4 x 4 matrix pattern is shown for illustration only.

F. This package contains Pb-free balls.

4206986-8/R 02/12

NanoFree is a trademark of Texas Instruments

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS22985YFP	PREVIEW	DSBGA	YFP	16		TBD	Call TI	Call TI	-40 to 85		
TPS22985YFPR	NRND	DSBGA	YFP	16	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 85	9U	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

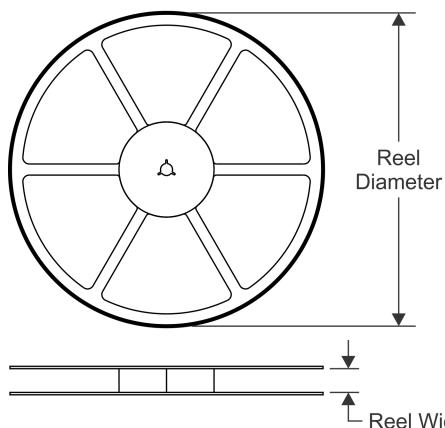
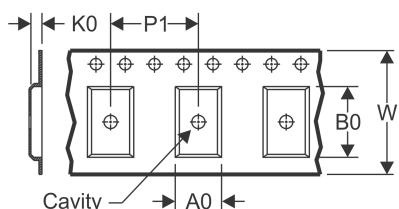
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

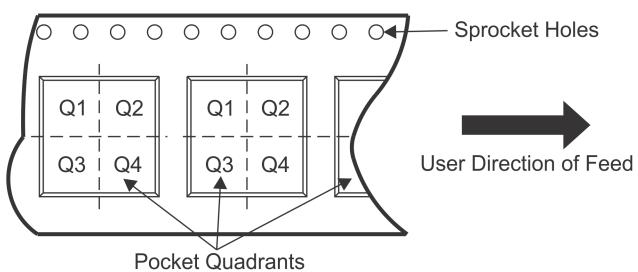
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22985YFPR	DSBGA	YFP	16	3000	180.0	8.4	1.71	1.71	0.81	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22985YFPR	DSBGA	YFP	16	3000	210.0	185.0	35.0

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