3 Phase Motor Driver-IC for Automotive Safety Applications

Check for Samples: DRV3201-Q1

FEATURES

- **Qualified for Automotive Applications**
- **AEC-Q100 Test Guidance With the Following Results:**
  - **Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature**
  - **Device HBM ESD Classification Level H2**
  - **Device CDM ESD Classification Level C2**
- **3 Phase Bridge Driver for Motor Control**
- **Drives 6 Separate N-Channel Power MOSFETs up to 250 nC Gate Charge**
- **Programmable 140 mA–1 A Gate Current Drive (Source/Sink) for Easy Output Slope Adjustment**
- **–7 V to 40 V Compliance on All FET Driver Pins to Handle Inductive Under/Overshooting**
- **Separate Control Input for Each Power MOSFET**
- **PWM Frequency up to 30 kHz**
- **Supports 100% Duty Cycle Operation**
- **Operating Voltage: 4.75 to 30 V**
- **Proper Low Supply Voltage Operation Due to Integrated Boost Converter for Gate-Driver Voltage Generation**
- **Logic Functional Down to 3 V**
- **Short Circuit Protection With VDS-Monitoring and Adjustable Detection Level**
- **Two Integrated High Accuracy Current Sense Amplifiers With Two Gain-Programmable Second Stage for Higher Resolution at Low Load Current Operation**
- **Over and Undervoltage Protection**
- **Shoot Through Protection With Programmable Dead Time**
- **Three Real Time Phase Comparators**
- **Over Temperature Warning and Shut Down**
- **Sophisticated Failure Detection and Handling Through SPI Interface**
- **Sleep Mode Function**
- **Reset and Enable Function**
- **Package: 64-pin HTQFP PowerPAD™**

APPLICATIONS

- **Automotive Safety Critical Motor-Control Applications**
  - **Electrical Power Steering (EPS, EHPS)**
  - **Electrical Brake/Brake Assist**
  - **Transmission**
  - **Oil-Pump**
- **Industrial Safety Critical Motor-Control Applications**

DESCRIPTION

The bridge driver is dedicated to automotive 3 phase brushless DC motor control including safety relevant applications. It provides six dedicated drivers for normal level N-Channel MOSFET transistors. The driver capability is designed to handle gate charges of 250 nC, and the driver source/sink currents are programmable for easy output slope adjustment. The device also incorporates sophisticated diagnosis, protection and monitoring features through an SPI interface. A boost converter with integrated FET provides the overdrive voltage, allowing full control on the power-stages even for low battery voltage down to 4.75 V.

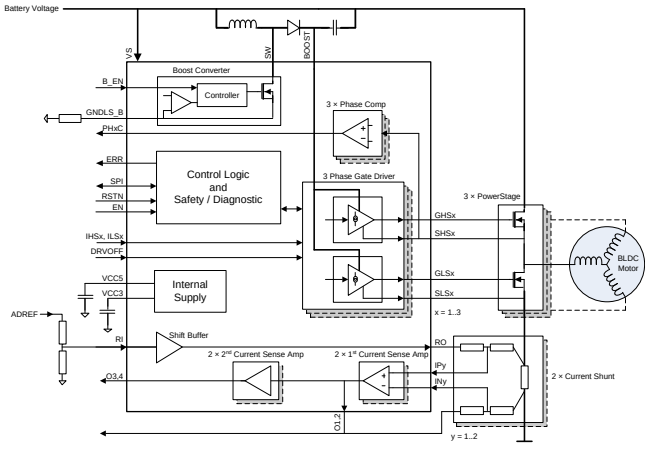


Figure 1. Typical Application Diagram

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

THERMAL INFORMATION

THERMAL METRIC(1)		DRV3201 HTQFP PAP - 64 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	21.6	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	10.9	
θ_{JB}	Junction-to-board thermal resistance	4.5	
ψ_{JT}	Junction-to-top characterization parameter	0.1	
ψ_{JB}	Junction-to-board characterization parameter	4.4	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	0.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

ABSOLUTE MAXIMUM RATINGS(1)(2)

over operating temperature T_J = –40°C to 150°C

SYMBOL	PARAMETER	CONDITIONS	VALUE		UNIT
			MIN	MAX	
VS, VSH	DC	VS, negative voltages with minimum serial resistor 5 Ω	–5	38	V
		VS, negative voltages with external protection NMOS	–1	38	V
VS, VSH	Supply voltage, transient 1s	VS, negative voltages with minimum serial resistor 5 Ω	–5	42	V
		VS, negative voltages with external protection NMOS driven by device internal circuit	–1	42	V
GHSx	Gate high-side voltage		–7	47	V
SHSx	Source high-side voltage		–7	42	V
GHSx-SHSx	Gate-source high-side voltage difference	External driven, internal limited (see $V_{GS,HS,high}$ in ELECTRICAL CHARACTERISTICS)	–0.3	15	V
GLSx	Gate low-side voltage		–7	20	V
SLSx	Source low-side voltage		–7	7	V
GLSx-SLSx	Gate-source low-side voltage difference	External driven, internal limited (see $V_{GS,LS,high}$ in ELECTRICAL CHARACTERISTICS)	–0.3	15	V
BOOST, SW	Boost converter	Negative voltage with minimum serial resistor 5 Ω	–0.3	60	V
		Negative voltage with external protection NMOS	–1	60	V
INx, IPx	Current sense input voltage		–0.3	42	V
INx, IPx clamping current	Current sense input current	Clamping current	–5	5	mA
Ox	Current sense output voltage		–0.3	ADREF +0.3	V
Ox forced input current			–10	10	mA
VDDIO, ADREF	Analog input voltage		–0.3	8	V
ILSx,IHSx, EN, DRVOFF, SCLK, NCS, SDI, RSTN, CSM, B_EN	Digital input voltage		–0.3	18	V
SCTH	Analog input voltage		–0.3	18	V
GNDA, GNDL, GNDLS_B, PGND, NC	Difference one GND or NC to any other GND or NC		–0.3	0.3	V
T_J	Operating virtual junction temperature range		–40	150	°C
T_S	Storage temperature range		–40	165	°C
ESD all pins	ESD performance of all pins to any other pin	HBM model AEC-Q100-002D Classification Level H2	–2	2	kV
ESD pin SHSx	ESD performance of SHSx to SHSx and GND	HBM model AEC-Q100-002D Classification Level H2	–4	4	kV
ESD all pin	ESD performance of all pins to any other pin	CDM Model AEC-Q100-011B Classification Level C2	–500	500	V
SR_{SHS}	Maximum slew rate of SHSx pins		–150	150	V/µs
ERR, SDO, PHxC, RO	Analog/digital output voltages		–0.3	8	V
ERR, SDO, PHxC, RO	Forced input/output current		–10	10	mA
TEST, AMUX, NC	Unused pins. Connect to GND		–0.3	0.3	V
RI	Analog input voltage		–0.3	18	V
VCC5	Internal supply voltage		–0.3	8	V
I_VCC5	Short-to-ground current	Internal current limit		40	mA
VCC3	Internal supply voltage		–0.3	3.6	V
VCC3	Short-to-ground current	Limited by VCC5		40	mA

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network ground terminal, unless otherwise specified.

RECOMMENDED OPERATING CONDITIONS

Over operating temperature T_J = -40°C to 150°C. Over recommended operating conditions VS = 4.75 to 30 V, f_{PWM} < 30 kHz (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage, normal voltage operation, VS	Full device functionality. Operation at VS = 4.75V only when coming from higher VS. Min. VS for startup = 4.85V	4.75		30	V
Supply voltage, logic operation, VSLO	Logic functional (during battery cranking after coming from full device functionality)	3		40	V
Supply voltage for digital IOs, VDDIO		2.7		5.5	V
Duty cycle of bridge drivers, D		0		100	%
PWM switching frequency, f_{PWM}		0		30	kHz
Junction temperature, T_J		–40		150	°C
Operating ambient free-air temperature, T_A	With proper thermal connection	–40		125	°C
Current sense input voltage range, V_{INx},V_{IPx}	Relative to GNDA	–0.14		1.6	V
Clamping voltage for current sense amplifier outputs O 1/ 2/ 3/ 4, ADREF		0.7		5	V
VCC3 output current, $I_{\_VCC3}$	Intended for MCU ADC input	0		100	µA
VCC3 decoupling capacitance, $C_{\_VCC3}$		1	4.7	22	nF
VCC5 output current, $I_{\_VCC5}$	Intended for MCU ADC input	0		100	µA
VCC5 decoupling capacitance, $C_{\_VCC5}$		1	4.7	470	nF

ELECTRICAL CHARACTERISTICS

over operating temperature T_J = –40°C to 150°C and recommended operating conditions, VS = 4.75 to 30 V, f_{PWM}< 30 kHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply						
I_{VSq}	VS quiescent current shut down (sleep mode)	VS = 14 V, no operation, T_J < 85°C EN = low, RSTN = high(1) total leakage current on all supply connected pins			30	µA
I_{VSn}	VS quiescent current normal operation (boost converter enabled, drivers not switching)	See Figure 18 and Figure 19.		65	90	mA
VCC5	Internal supply voltage	VS > 6 V, external load current < 100µA. Decoupling capacitance is typically 4.7nF.	4.7		5.3	V
VCC3	Internal supply voltage	VS > 3 V, external load current < 100µA. Decoupling capacitance is typically 4.7nF.	2.1(2)		3.6	V
		VS >4.75 V, external load current < 100µA. Decoupling capacitance is typically 4.7nF.	3.15		3.45	V
Current Sense Amplifier First Stages						
$V_{off1/2}$	Initial input offset of amplifiers at T_J = 25°C		–1	0	1	mV
$V_{off1/2\_d}$	Temperature and aging offset		–1	0	1	mV
$I_{leak,INxIPx}$	Input leakage current INx, IPx	0 V < INx, IPx < 1 V pin-to-pin and pin-to-ground	–0.5		0.5	µA
		–0.3 V < INx, IPx < 0 V pin-to-pin and pin-to-ground	–50		0.5	µA
$G_{o1/2}$	DC open loop gain	See Note (3)	80			dB
$V_{O1/2\_N}$	Nominal output voltage range	Normal voltage operation, VS ≥ 6 V, ADREF = 5 V; 0.5 mA load current	0.5		4.5	V
$V_{O1/2\_L}$	Output voltage range during low voltage operation	Low voltage operation, 4.75 V ≤ VS ≤ 6 V, ADREF = 5 V; 0.5 mA load current	0.5		4	V
$GBP_{1/2}$	Gain bandwidth product (GBP)	0.5 V ≤ O1/2 ≤ 4.5 V (3)	5			MHz
$SR_{1/2}$	Slew rate	0.5 V ≤ O1/2 ≤ 4.5 V, cap load = 25 pF	2.9		15	V/µs
$PSRR_{1/2}$	Power supply rejection ratio	VS to O1/2. Decoupling capacitance is typically 4.7 nF on VCC5 and VCC3. (3)		80		dB
$CMRR_{1/2}$	Common mode rejection ratio	IN1/2 or IP1/2 to O1/2 (3)		80		dB
Current Sense Amplifier Second Stages						
$V_{off3/4}$	Initial input offset of amplifiers at T_J = 25 °C	VRO = 2.5V	–5	0	5	mV
$V_{off3/4\_d}$	Temperature and aging offset		–3	0	3	mV
$V_{O3/4\_N}$	Nominal output voltage range	Normal voltage operation, VS ≥ 6 V, ADREF = 5 V; 0.5 mA load current	0.5		4.5	V
$V_{O3/4\_L}$	Output voltage range during low voltage operation	Low voltage operation, 4.75 V ≤ VS ≤ 6 V, ADREF = 5 V; 0.5 mA load current	0.5		4	V
$GBP_{3/4}$	Gain bandwidth product (GBP)	0.5 V ≤ O3/4 ≤ 4.5 V, gain = 8 (3)	5			MHz
$SR_{3/4}$	Slew rate	0.5 V ≤ O3/4 ≤ 4.5 V, cap load = 25 pF	2.9		15	V/µs
G1	Gain1		1.98	2	2.02	V/V
G2	Gain2		3.96	4	4.04	V/V
G3	Gain3		5.82	6	6.18	V/V
G4	Gain4		7.84	8	8.16	V/V
$PSRR_{3/4}$	Power supply rejection ratio	VS to O3/4 decoupling capacitance is typically 4.7 nF on VCC5 and VCC3. (3)		80		dB
Shift Buffer						
VRI	Shift input voltage range		0.1		2.6	V
VRO	Shift output voltage range		0.1		2.6	V
VR_{offset}	Shift voltage offset		–5		5	mV
I_{RO}	Shift output current capability		–5		5	mA
$I_{leak,RI}$	Input leakage current RI	VRI = 2.5 V, pin-to-ground	–0.2		0.2	µA

(1) The DRV3201 can only enter Sleep Mode when EN is set to low while RSTN is kept high. Once the device is in Sleep Mode (100 µs after EN has been set low), the RSTN pin can be set low without affecting the Sleep Mode.
(2) Lower limit of functional range dependent of internal PowerOnReset level for internal digital logic. It is specified by VS > 3 V the internal digital logic is operational and not put into PowerOnReset.
(3) Specified by design

ELECTRICAL CHARACTERISTICS (continued)

over operating temperature T_J = –40°C to 150°C and recommended operating conditions, VS = 4.75 to 30 V, f_{PWM}< 30 kHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADREF						
V_{oxm}	Maximum DC voltage of O1/2/3/4 relative to ADREF	ADREF = 3.3/ 5 V; Ox-ADREF	–0.25	0.03	0.25	V
V_{oxos}	Overshoot of O1/2/3/4 over ADREF	Ox-ADREF; for < 1 µs; never higher than 5 V over GND (3)			1.2	V
I_{ADREF}	Bias current for voltage clamping circuit	ADREF = 3.3/5V, pin-to-ground			150	µA
Gate-Driver						
$V_{GS,low}$	Gate-source voltage low high/low-side driver	Active pulldown, I_{load} = –2 mA	0		0.2	V
R_{GSp}	Passive gate-source resistance	V_{gs} ≤ 200 mV	80	500	700	kΩ
R_{GSsa}	Semi-active gate-source resistance	In sleep mode, V_{gs} > 2 V		7	8	kΩ
R_{GSa2}	Active gate-source resistance	V_{gs} < 1 V, gate driven low by gate-driver, Regyx = 100			2.3	Ω
R_{GSa1}	Active gate-source resistance	V_{gs} < 1 V, gate driven low by gate-driver, Regyx = 010			4.5	Ω
R_{GSa0}	Active gate-source resistance	V_{gs} < 1 V, gate driven low by gate-driver, Regyx = 001			9	Ω
$V_{GS,HS,high}$	high-side output voltage	I_{load} = –2 mA	9		12.8	V
$V_{GS,LS,high}$	low-side output voltage	I_{load} = –2 mA	9		12.8	V
IGC2C	Gate charge current high/low-side driver 2	2V ≤ (VGLSx-VSLSx) ≤ 5V, Regyx = 100, if not disabled in CFG1	0.4	0.57	0.74	A
IGC1C	Gate charge current high/low-side driver 1	2V ≤ (VGLSx-VSLSx) ≤ 5V , Regyx = 010, if not disabled in CFG1	0.2	0.29	0.37	A
IGC0C	Gate charge current high/low-side driver 0	2V ≤ (VGLSx-VSLSx) ≤ 5V, Regyx = 001, if not disabled in CFG1	0.1	0.14	0.18	A
IGD2D	Gate discharge current high/low-side driver 2	2V ≤ (VGLSx-VSLSx) ≤ 5V, Regyx = 100, if not disabled in CFG1	0.4	0.57	0.74	A
IGD1D	Gate discharge current high/low-side driver 1	2V ≤ (VGLS-VSLS) ≤ 5V, Regyx = 010, if not disabled in CFG1	0.2	0.29	0.37	A
IGD0D	Gate discharge current high/low-side driver 0	2V ≤ (VGLS-VSLS) ≤ 5V, Regyx = 001, if not disabled in CFG1	0.1	0.14	0.18	A
t_{Don}	Propagation on delay time	After ILx/IHx rising edge		200	250	ns
t_{Dondif}	Propagation on delay time difference	LSx to LSy and HSx to HSy			70	ns
t_{Doff}	Propagation off delay time	After ILx/IHx falling edge		200	350	ns
$t_{Doffdiff}$	Propagation off delay time difference	LSx to LSy and HSx to HSy			50	ns
$t_{Don\_Doff\_diff}$	Difference between propagation on delay time and propagation off delay time	For each Gate-Driver in each channel			150	ns
t_{DRVoff}	Propagation off (DRVOFF) delay time	After rising edge on DRVOFF		200	400	ns
t_{ENoff}	Propagation off (EN) deglitching time	After falling edge on EN		6		µs
t_{SD}	Time until device enters shutdown	After falling edge on EN	20		35	µs
$t_{RSTNoff}$	Propagation off (RSTN) delay time	After falling edge on RSTN		200	400	ns
A_{dt}	Accuracy of dead time	If not disabled in CFG1	-15		15	%
Boost Converter						
I_{BOOSTn}	BOOST pin quiescent current normal operation (drivers not switching)	4.75 V < VS <32 V			20	mA
$I_{BOOST,sw}$	BOOST pin additional load current due to switching gate-drivers	Without external power FETS (pure internal switching current, 30kHz all gate-drivers switching at the same time)			3	mA
V_{BOOST}	Boost output voltage	BOOST-VS voltage	13.8	15	16	V
I_{BOOST}	Output current capability	For device internal use only	40			mA
f_{BOOST}	Switching frequency	BOOST-VS > $V_{BOOSTUV}$ (4)	2	2.5	3	MHz
$V_{BOOSTUV}$	Undervoltage shutdown Level	BOOST-VS voltage	11		11.9	V
t_{BCSD}	Filter time for undervoltage shutdown		5		6	µs
$V_{GNDLS\_B,off}$	Voltage at GNDLS_B pin at which boost FET switches off due to current limit		70	100	130	mV

(4) During startup when BOOST-VS < $V_{BOOSTUV}$, f_{BOOST} is typically 1.25 MHz.

ELECTRICAL CHARACTERISTICS (continued)

over operating temperature T_J = –40°C to 150°C and recommended operating conditions, VS = 4.75 to 30 V, f_{PWM}< 30 kHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{SW,off}$	Delay of the GNDLS_B current limit comparator	See Note (5)			20	ns
$I_{SW,fail}$	Internal second level current limit		420		700	mA
$R_{DS(on)}$	Resistance BOOST FET		0.48		1.2	Ω
Digital Inputs						
INL	Input low threshold	All digital inputs: RSTN, B_EN, NCS, DRVOFF, ILSx, IHSx, CSM, SDI, SCLK			0.9	V
ENL	EN input low threshold				0.27 x VDDIO	V
INH	Input high threshold	All digital inputs: RSTN, B_EN, NCS, DRVOFF, ILSx, IHSx, CSM, SDI, SCLK	2.3			V
ENH	EN input high threshold		0.65 x VDDIO			V
Inhys	Input hysteresis	All digital inputs: RSTN, B_EN, NCS, DRVOFF, ILSx, IHSx, CSM, SDI, SCLK	0.3	0.8	1	V
EN Inhys	EN input hysteresis		0.18 x VDDIO	0.25 x VDDIO	0.48 x VDDIO	V
$R_{pd,EN}$	Input pull down resistor at EN pin	EN	170	200	300	kΩ
$t_{deg,ENon}$	Power-up time after EN pin high from sleep mode to active mode	After rising edge on EN, time until logic out-of-reset		1		ms
R_{pullup}	Input pull up resistance	RSTN, B_EN, NCS, DRVOFF	100	140	200	kΩ
$R_{pulldown}$	Input pull down resistance	ILSx, IHSx, CSM, SDI	100	140	200	kΩ
Digital Outputs						
OH	Output high voltage	All digital outputs: ERR, SDO, PHxC, I = ±2 mA; VDDIO in functional range (6)	VDDIO –0.2			V
OL	Output low voltage				0.2	V
VDS Monitoring						
V_{SCTH}	VDS short circuit threshold input range	If not disabled in CFG1	0		2.5	V
A_{vds}	Accuracy of VDS monitoring		-250		250	mV
t_{VDS}	Detection filter time	Only rising edge of VDS comparators are filtered		5		µs
THERMAL SHUTDOWN						
T_{msd0}	Thermal recovery	See Note (7)	140	150		°C
T_{msd1}	Thermal warning		160	170		°C
T_{msd2}	Thermal global reset		175	190	205	°C
T_{hmsd}	Thermal shutdown hysteresis			40		°C
t_{TSD}	Thermal warning filter time		40	45	50	µs
t_{TSD}	Thermal shutdown filter time		40	45	50	µs
Phase Comparator						
V_{PCHth}	Phase comparator high threshold		0.65 x VSH		0.88 x VSH	
V_{PCLth}	Phase comparator low threshold		0.15 x VSH		0.4 x VSH	
t_{DHL}	Delay time high–low	C_{out} = 50 pF		80	120	ns
t_{DLH}	Delay time low–high	C_{out} = 50 pF		80	120	ns
t_D	Matching between two channels		–30		30	ns
	Matching between rising and falling edge for each channel		–30		30	ns
R_{VSH}	Resistance of internal voltage divider to ground		170		330	kΩ
VS Monitoring						
V_{VSOV}	Overvoltage shutdown level, OV = OFF	If not disabled in CFG1	29.3		30.7	V
	Recovery level from Overvoltage shutdown, OV = ON		27.5		29.3	V

(5) Specified by design
(6) All digital outputs have a push-pull output stage between VDDIO and ground.
(7) Specified by design

ELECTRICAL CHARACTERISTICS (continued)

over operating temperature T_J = –40°C to 150°C and recommended operating conditions, VS = 4.75 to 30 V, f_{PWM}< 30 kHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{VSUV}	Undervoltage shutdown level, UV = OFF	When coming from higher VS voltage	4.5		4.75	V
	Recovery level form Undervoltage shutdown, UV = ON	Min. VS for device startup	4.6		4.85	V
Hys	Overvoltage hysteresis		1.2		1.8	V
	Under voltage hysteresis		50		300	mV
$t_{VS,SHD}$	Filter time for voltage shutdown		5		6	µs
Serial Peripheral Interface Timing						
f_{SPI}	SPI clock (SCLK) frequency				4 (8)	MHz
T_{SPI}	SPI clock period		250			ns
t_{high}	High time: SCLK logic high duration		90			ns
t_{low}	Low time: SCLK logic low duration		90			ns
t_{sMCUs}	Setup time NCS: time between falling edge of NCS and rising edge of SCLK		90			ns
t_{d1}	Delay time: time delay from falling edge of NCS to data valid at SDO				60	ns
t_{susi}	Setup time at SDI: setup time of SDI before the rising edge of SCLK		30			ns
t_{d2}	Delay time: time delay from falling edge of SCLK to data valid at SDO		0		45	ns
t_{hcs}	Hold time: time between the falling edge of SCLK and rising edge of NCS		45			ns
t_{hlcs}	SPI transfer inactive time: time between two transfers		250			ns
t_{tri}	3-state delay time: time between rising edge of NCS and SDO in 3-state				15	ns

(8) MAX SPI clock tolerance is ± 10%.

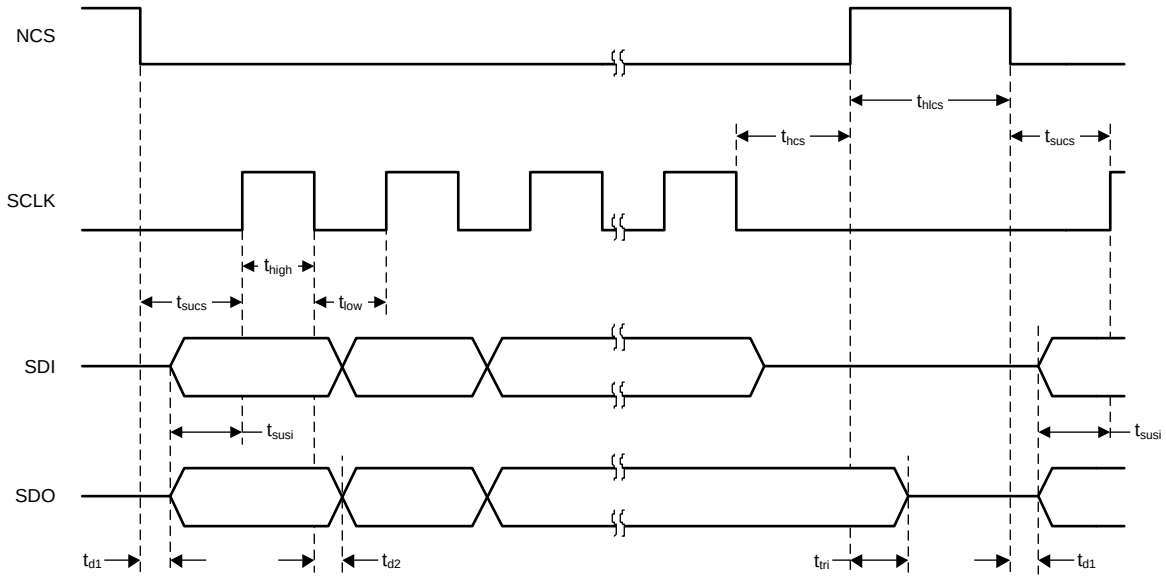


Figure 2. SPI Timing Parameters

PIN FUNCTIONS

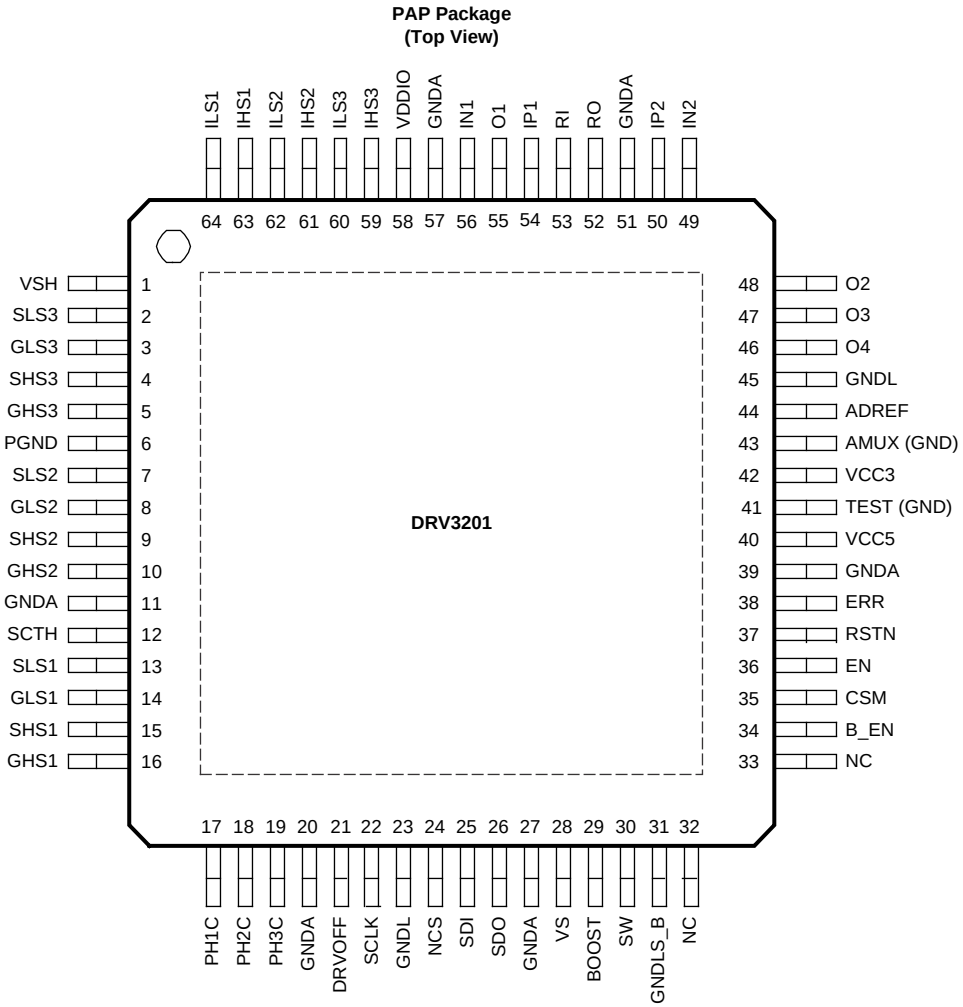


Figure 3. Pin Assignment (HTQFP-64 Package)

PIN FUNCTIONS

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
VSH	1	HVI_A	Sense high-side, sensing VS connection of the external power MOSFETs for VDS monitoring.
SLS3	2	PWR	Source low-side 3, connected to external power MOSFET for gate discharge and VDS monitoring.
GLS3	3	PWR	Gate low-side 3, connected to gate of external power MOSFET.
SHS3	4	PWR	Source high-side 3, connected to external power MOSFET for gate discharge and VDS monitoring.
GHS3	5	PWR	Gate high-side 3, connected to gate of external power MOSFET.
PGND	6	GND	Sense low-side (ground), sensing ground connection of the external power MOSFETs for phase comparators.
SLS2	7	PWR	Source low-side 2, connected to external power MOSFET for gate discharge and VDS monitoring.
GLS2	8	PWR	Gate low-side 2, connected to gate of external power MOSFET.
SHS2	9	PWR	Source high-side 2, connected to external power MOSFET gate discharge and VDS monitoring.
GHS2	10	PWR	Gate high-side 2, connected to gate of external power MOSFET.

(1) Description of pin type: GND = Ground, HVI_A = High-Voltage Input Analog, HVI_D = High-Voltage Input Digital, LVI_A = Low-Voltage Input Analog, LVO_A = Low-Voltage Output Analog, LVO_D = Low-Voltage Output Digital, NC = NoConnect, PWR = Power Output, Supply = Supply Input.

PIN FUNCTIONS (continued)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
GNDA	11	GND	Analog ground
SCTH	12	HVI_A	Short circuit threshold, reference input voltage for VDS monitoring.
SLS1	13	PWR	Source low-side 1, connected to external power MOSFET for gate discharge and VDS monitoring.
GLS1	14	PWR	Gate low-side 1, connected to gate of external power MOSFET.
SHS1	15	PWR	Source high-side 1, connected to external power MOS transistor for gate discharge and VDS monitoring.
GHS1	16	PWR	Gate high-side 1, connected to gate of external power MOS transistor.
PH1C	17	LVO_D	Phase comparator output1
PH2C	18	LVO_D	Phase comparator output2
PH3C	19	LVO_D	Phase comparator output3
GNDA	20	GND	Analog ground
DRVOFF	21	HVI_D	Driver OFF (high active), secondary bridge driver disable
SCLK	22	HVI_D	SPI clock
GNDL	23	GND	Logic ground
NCS	24	HVI_D	SPI chip select
SDI	25	HVI_D	SPI data input
SDO	26	LVO_D	SPI data output
GNDA	27	GND	Analog ground
VS	28	Supply	Power supply voltage
BOOST	29	Supply	Boost output voltage, used as supply for the gate-drivers.
SW	30	PWR	Boost converter switching node connected to external coil and external diode.
GNDLS_B	31	GND	Boost GND to set current limit. Boost switching current goes through this pin via exterior resistor to GND.
NC	32	NC	NC pin, connected to GND during normal application.
NC	33	NC	NC pin, connected to GND during normal application.
B_EN	34	HVI_D	Boost enable. Enable boost operation or disable during e.g. sensitive measurement.
CSM	35	HVI_D	Configurable safety mode (high active), defines the level of safety.
EN	36	HVI_D	Enable (high active) of the device
RSTN	37	HVI_D	Reset (low active)
ERR	38	LVO_D	Error (low active). Error pin to indicate detected error.
GNDA	39	GND	Ground analog
VCC5	40	LVO_A	VCC5 regulator, for internal use only. Recommended external decoupling capacitance: 4.7 nF. External load < 100 µA
TEST	41	HVI_A	TEST mode input, connected to GND during normal application.
VCC3	42	LVO_A	VCC3 regulator, for internal use only. Recommended external decoupling capacitance: 4.7 nF. External load < 100 µA
AMUX (GND)	43	LVO_A	Analog TEST output MUX, connected to GND during normal application.
ADREF	44	LVI_A	ADC reference of MCU, used as maximum voltage clamp for O1-O4.
GNDL	45	GND	Logic ground
O4	46	LVO_A	Output second stage current sense amplifier 2
O3	47	LVO_A	Output second stage current sense amplifier 1
O2	48	LVO_AO	Output first stage current sense amplifier 2
IN2	49	HVI_A	Current sense input N 2
IP2	50	HVI_A	Current sense input P 2
GNDA	51	GND	Ground analog
RO	52	LVO_A	Current sense reference output for the shift voltage.
RI	53	HVI_A	Current sense reference input for the shift voltage.

PIN FUNCTIONS (continued)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
IP1	54	HVI_A	Current sense input P 1
O1	55	LVO_A	Output first stage current sense amplifier 1
IN1	56	HVI_A	Current sense input N 1
GNDA	57	GND	Ground analog
VDDIO	58	Supply	IO supply voltage, defines the interface voltage of digital I/O e.g. SPI.
IHS3	59	HVI_D	Input HS 3, digit input to drive the HS3
ILS3	60	HVI_D	Input LS 3, digit input to drive the LS3
IHS2	61	HVI_D	Input HS 2, digit input to drive the HS2
ILS2	62	HVI_D	Input LS 2, digit input to drive the LS2
IHS1	63	HVI_D	Input HS 1, digit input to drive the HS1
ILS1	64	HVI_D	Input LS 1, digit input to drive the LS1

FUNCTIONAL BLOCK DIAGRAM

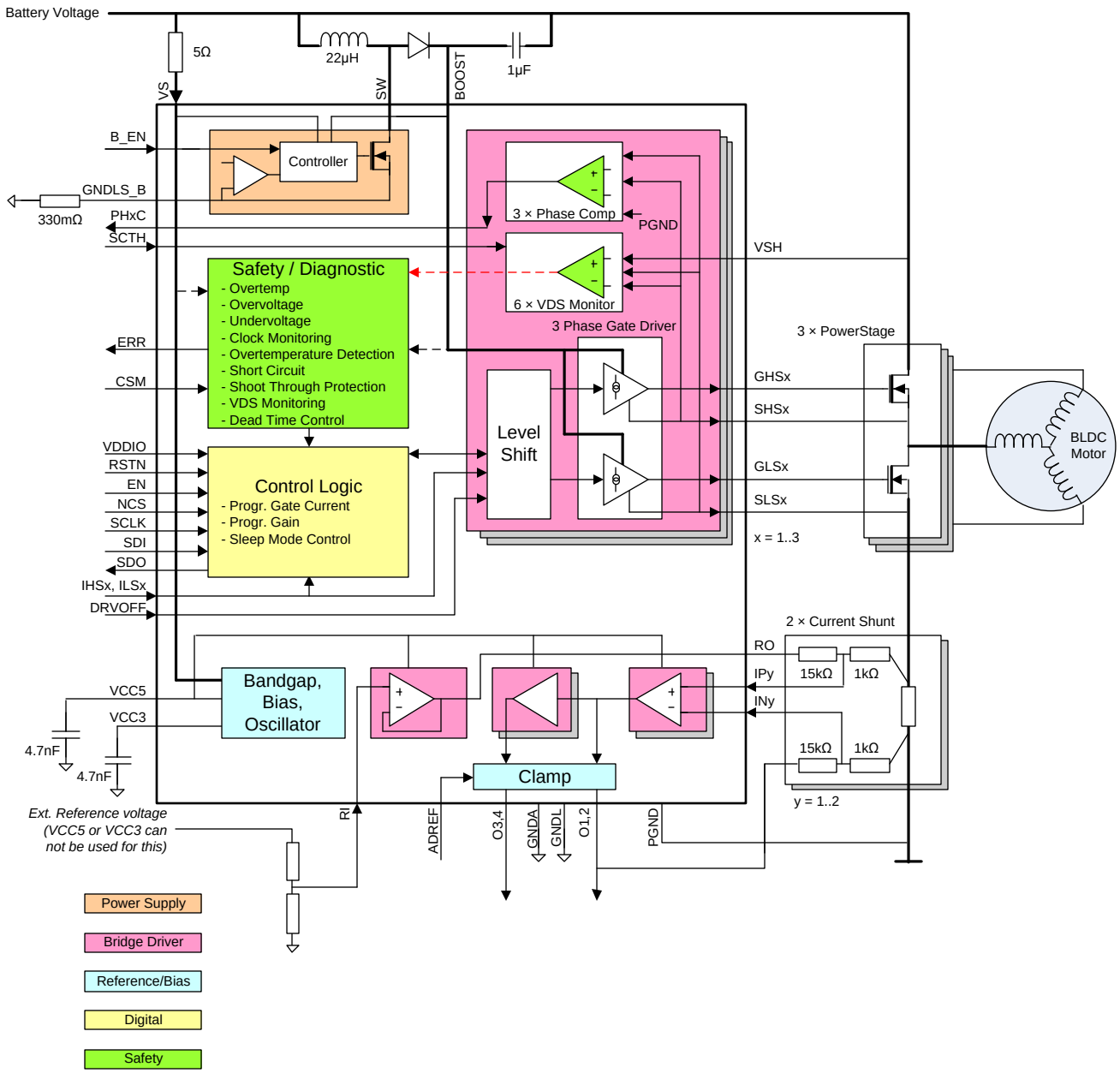


Figure 4. DRV3201-Q1 Functional Block Diagram

DETAILED DESCRIPTION

The DRV3201-Q1 is designed to control 3 phase brushless DC motors in automotive applications using pulse width modulation. Three high-side and three low-side gate-drivers can be switched individually with low propagation delay. The input logic prevents simultaneous activation of high and low-side driver of the same channel. A configuration and status register can be accessed through the SPI communication interface.

SUPPLY CONCEPT

The battery voltage functional operation range for the DRV3201-Q1 is between 4.85 V and 30 V. The DRV3201-Q1 operates with either 3.3 V or 5 V MCUs, which can be achieved by connecting the IO voltage of the MCU to the VDD_IO pin of the DRV3201-Q1, and by connecting the ADC reference voltage of the MCU to the ADREF pin of the DRV3201-Q1. All digital outputs are related to VDDIO, and all analog outputs are related (clamped) to ADREF. All digital inputs are related to the internal supply VCC3, except the EN pin. The gate-drivers for the external power FETs operate even during battery voltage drops down to 4.75V when coming from full functional battery voltage range. For supply voltage falling below 4.75 V, the gates of the external FETs are pulled down actively. For supply voltage below 3 V, these gates are pulled down semi-actively. The minimum start-up battery voltage for the gate-drivers and the internal logic is 4.85 V.

Coming from full functional battery voltage range (that is, between 4.85 V and 30 V) the internal logic, including the SPI interface, operates even during battery voltage drops down to 3 V. When the battery drops below 3 V, the DRV3201-Q1 triggers a complete internal reset, clearing all internal status bits and registers. Also, the SPI communication to the MCU is disabled when the DRV3201-Q1 logic is put in reset.

The VCC5 is an internal supply for the current sense amplifiers and other internal analog circuitry. The VCC5 pin needs to be externally decoupled with a typical 4.7 nF capacitance. The VCC5 has an internal current limit to avoid any internal damage due to an external short-to-ground on the VCC5 pin.

The VCC3 is an internal supply for the internal logic. The VCC3 pin needs to be externally decoupled with a typical 4.7 nF capacitance. Since the VCC3 is supplied from the VCC5 regulator, its output is current limited by the VCC5 current limit so any internal damage is avoided in case of an external short-to-ground on the VCC3 pin. In case of a short-to-ground on either the VCC5 pin or the VCC3 pin, the internal logic is put in reset, which is detectable by the MCU because of disabled SPI communication. In this situation it is strongly recommended that the MCU takes necessary action to bring down the EN pin and shut off the DRV3201-Q1 to avoid VCC5 and/or VCC3 overloading for too long.

Boost Converter

The boost converter is configured to supply an add-on voltage to the supply voltage. The boost converter requires an external inductance, capacitor, Schottky-diode, and a series resistance in its ground for current sensing. Both the high-side and the low-side gate-drivers are supplied from the boost converter. This allows the DRV3201-Q1 to achieve full-range gate-source driving voltage for all external power FETs even at battery voltage down to 4.75 V. The boost converter has a separate B_EN pin to enable/disable. When the device is put in sleep mode, the boost converter cannot be enabled.

Sleep Mode, Active Mode

The EN (Enable) pin puts the device into sleep mode, in which it consumes less than 35 µA. At the falling edge on the EN pin, after a typical 6 µs deglitch time, the gates of the external power FETs are actively pulled low by the gate-drivers. Afterwards (min 20 µs, max 35 µs later) the internal supplies VCC5, VCC3, the boost converter, and the current sense amplifiers are switched off and the gates of the external power FETs are pulled low with a semi-active pulldown resistor (see Semi-Active Pull-Down Resistor). The internal logic is put in reset state, and all internal registers are cleared. No diagnostic information is available during sleep mode. When putting the device into Sleep Mode, the RSTN pin must be kept high. Once the device is in Sleep Mode (100 µs after EN has been set low), the RSTN pin can be set low without affecting the Sleep Mode.

A rising edge on the EN pin puts the device in active mode after typically 3 ms power-up time. In active mode, the supplies VCC5 and VCC3 are present, and the boost converter can be enabled or disabled with the B_EN pin. Since all internal registers are cleared in sleep mode, the MCU must program the DRV3201-Q1 in the desired settings after each wake-up from sleep mode to active mode.

DIGITAL INPUT, OUTPUT PINS

All digital input pins (marked HVI_D in terminal function table), except the EN pin, have a threshold voltage related to the internal VCC3 supply. Therefore, the state of these input pins is effective regardless of whether the VDDIO level is out of limits. These digital input pins have a fail-safe ESD structure with only a reverse diode path to ground, and no reverse diode path to any supply voltage. Depending on the function, these input pins have an internal passive pulldown or pullup. All digital output pins (marked LVO_D) have a push-pull stage between VDDIO and ground. Therefore, the logic high-levels are related to VDDIO.

RESET

The DRV3201-Q1 can be reset by switching the RSTN to low. When RSTN is low, all status bits and register settings are cleared, the boost converter and the current sense amplifiers are off, and the gate-driver outputs are actively pulled low with the maximum setting for the sink current, hence turning off the external power FETs. The internal supplies VCC3 and VCC5 are still active when RSTN is forced low. The input high and low thresholds of RSTN are related to VCC3, and therefore independent of VDDIO, hence the state of the RSTN pin is effective regardless of whether the VDDIO level is out of limits. Once the RSTN pin has been set low, the device cannot enter Sleep Mode.

GATE-DRIVERS

The DRV3201-Q1 has three high-side and low-side gate-drivers. Each high-side and low-side gate-driver contains a programmable sourcing and sinking current to charge and discharge the gate of the external power FETs.

The digital logic prevents the simultaneous activation of high and low-side gate-driver of one power-stage. If a command from the MCU for simultaneous activation is detected, the failure is flagged in the status register.

Gate-Driver Slope Control

The DRV3201-Q1 has been designed to support adaptive slope control by programmable sink and source currents to charge and discharge the gates of the external power FETs. Table 1 gives the slope registers which are supported to program the sink and source currents of the gate-drivers.

Table 1. Slope Configuration Registers

Affected Gate-Drivers	Register	Slope	Current Range	Number of steps
HS1 and HS2	HS1/2 Slope Register (CURR0)	Rising Edge	140mA–1A	8
HS1 and HS2	HS1/2 Slope Register (CURR0)	Falling Edge	140mA–1A	8
LS1 and LS2	LS1/2 Slope Register (CURR1)	Rising Edge	140mA–1A	8
LS1 and LS2	LS1/2 Slope Register (CURR1)	Falling Edge	140mA–1A	8
HS3	HS3 Slope Register (CURR2)	Rising Edge	140mA–1A	8
HS3	HS3 Slope Register (CURR2)	Falling Edge	140mA–1A	8
LS3	LS3 Slope Register (CURR3)	Rising Edge	140mA–1A	8
LS3	LS3 Slope Register (CURR3)	Falling Edge	140mA–1A	8

To reduce the risk of a distorted slope due to changing the slope setting, a new slope setting for a rising edge only becomes active after the next falling edge of the affected gate-driver and vice versa for the falling edge. This does not apply directly after wake-up to active mode. As long as no low-side or high-side gate-driver has been switched after wake-up to active mode, the programmed slope settings are active immediately.

To allow a high scalability of the output FETs and switching speed, there is also one general reduced current mode setting, in which all gate charge/discharge currents are 25% of the programmed settings. Furthermore it is possible to set the drivers to switching mode by setting bit 7 in configuration register 1 (CFG1) to 1. In this setting the drivers are not current limited and limiting the switching speed can be done externally with resistors in the gate lines. In this mode it is strongly recommended to set the slope registers (CURR0–3) to 0x3F to get the maximum current setting and have the current limiting only from the external resistors.

Direct Mode (6 x Inputs Operation)

The direct mode is the default operation mode after each wake-up from sleep mode to active mode. In direct mode, all gate-drivers can be controlled individually via the digital input pins IHSx/ILSx.

PWM Mode (3 x Inputs Operation)

Alternatively, the gate-drivers can be operated in PWM mode by setting bit 6 in Configuration Register 1 (CFG1) to 1. PWM Mode controls all six gate-drivers with only three PWM signals. The valid controls in PWM mode are the IHSx inputs. The low-side controls are derived from the corresponding IHSx signals while all safety features remain active. In PWM mode, the ILSx inputs may be used as SPI-readable general purpose inputs.

DRVOFF Gate-Driver Shutoff

When the DRVOFF pin is high, the gate-driver outputs are actively pulled low with the programmed setting for the sink current to turn off the external power FETs. Meanwhile, the IHSx/ILSx inputs can be read back through SPI. The VDS comparators, and flag errors (if VDS is too high) are enabled which can be used to ensure functionality of these blocks. The boost converter, the current sense amplifiers, and the internal VCC3 and VCC5 supplies are still active when DRVOFF is forced low. The input high and low thresholds of DRVOFF are related to VCC3, and are independent of VDDIO, so the state of the DRVOFF pin is effective regardless of whether the VDDIO level is out of limits.

Active Pulldown

When the external power FETs need to be turned off and the DRV3201-Q1 is in active mode (either by normal control signal, DRVOFF signal, RSTN signal or by any error handling), the gate-drivers provide a low-ohmic active pulldown. Once the gate-source voltage of the power FETs reaches less than 2 V, the programmed current sink behavior changes into an Rdson behavior to increase the pulldown strength.

Semi-Active Pull-Down Resistor

Each high and low-side driver has a typical 500 kΩ resistor from gate to source acting as passive pulldown to keep the external power FET turned off in unsupplied conditions. In addition a semi-active pulldown circuit is reducing the gate impedance at a typical voltage of 2 V to about 7 kΩ. This semi-active pulldown circuit is turned off in normal operation to avoid higher DC current consumption for the gate-driver.

Gate-Driver Shutoff Paths

Table 2 summarizes the possible states of the EN, RSTN and DRVOFF pins and the effect on the gate-drivers.

Table 2. Gate-Driver Shutoff Paths

EN	RSTN	DRVOFF	Any Non-Masked Error	Gate-Driver Shutoff	Logic
Unpowered device (1)				Semi-active pulldown + passive pulldown	
0	X	X	X	Semi-active pulldown + passive pulldown	Reset
1	0	X	X	Active pulldown	Reset
	1	1	X	Active pulldown	Enabled
		0	1 (1)	Active pulldown	Enabled
		0	0	Active, controlled by inputs	Enabled
1 ≥ 0	X	X	X	Active pulldown, afterwards device enters sleep mode ≥ semi-active pulldown + passive pulldown	Enabled during active pulldown, afterwards reset in sleep mode

(1) For 3 V < VS < 4.75 V, the VS undervoltage detection actively pulls down the gates of the external FETs. For VS < 3 V, these gates are pulled down semi-actively.

SAFETY

The DRV3201-Q1 has a wide range of safety features that helps the application to grant a high safety level.

Monitored Errors

The following sections describe the monitored errors. The handling of these errors is described in Configurable Safety Mode.

Drain Source Voltage Monitoring

The DRV3201-Q1 provides a drain-source voltage monitoring feature for each external power MOSFET. After input pin IHSx/ILSx goes high to turn on the external power MOSFET, its drain-source voltage is monitored. If this voltage stays higher than the VDS threshold for filter-time (t_{vds}) then the error is raised and the status flag for this power MOSFET is set.

The internal VDS threshold for the VDS monitoring can be set by an external analog input level on the SCTH pin, and can be scaled in eight steps with a factor between 0 and 1 through SPI in configuration register 0 (CFG0), bits 5:3.

The VDS comparator configuration for each gate-driver is shown in Figure 5. As shown in Figure 5, the VSH pin is used as sense input voltage for the high-side VDS comparators. Externally, this VSH pin should be connected to the star-point of the positive supply of the power-stages.

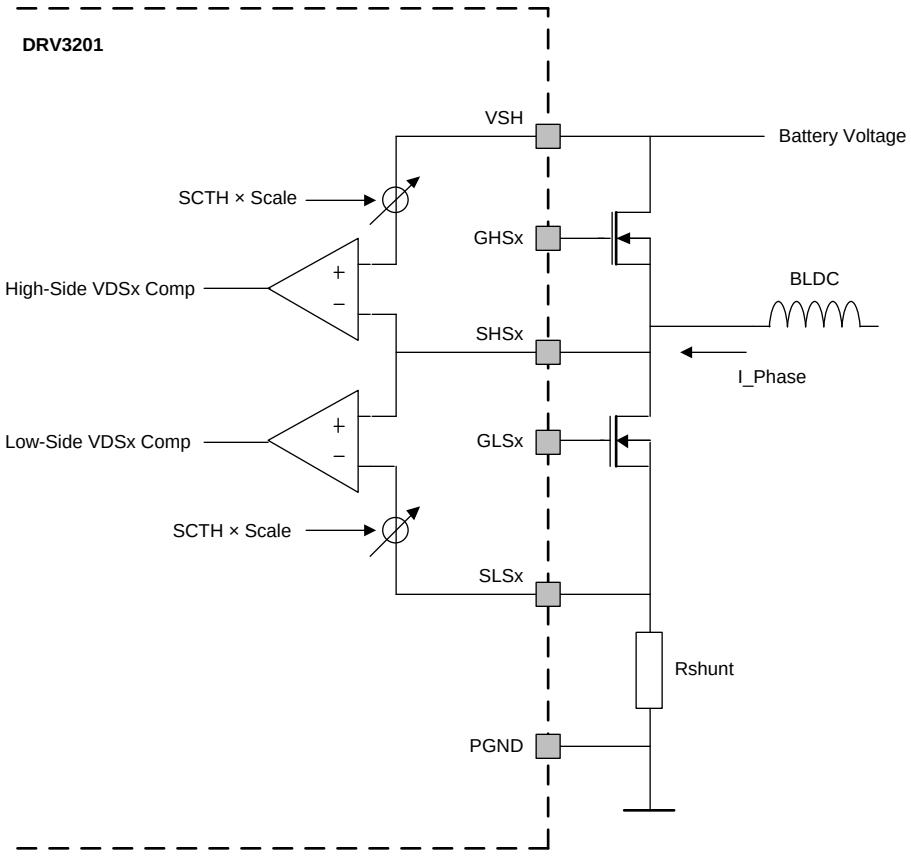


Figure 5. VDS Comparator Configuration for Each Driver-Stage

To verify the proper operation of the VDS comparators during normal operation, either the scale factor can be lowered through SPI, or the SCTH voltage can be externally lowered. This sets a lower VDS threshold (depending mostly on the random comparator offset < ± 100 mV) which causes the comparators to toggle at relative low current through the external power FETs (during normal operation without overcurrent). This is shown in Figure 6. During this verification, the error-handling of the VDS errors can be disabled as described in Configurable Safety Mode (configuration register 1 (CFG1), bits 3:4), such that the VDS errors are flagged in the SPI status register 0 (STAT0) and at the ERR pin only. The SCTH pin is a high-impedance input to a MOS gate with internal ESD protection to ground. There is no reverse pullup path present to any supply (fail-safe ESD structure).

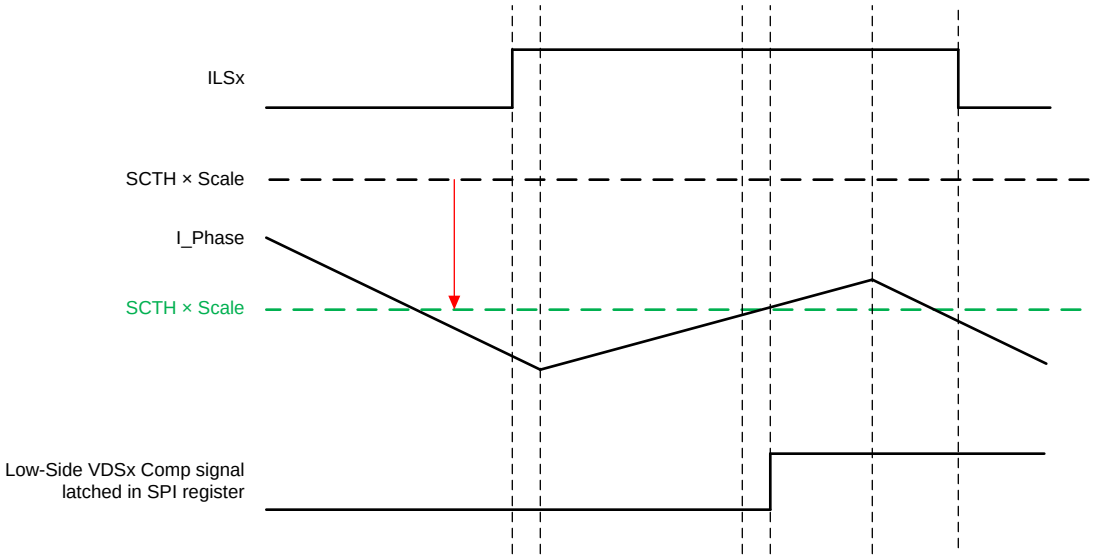


Figure 6. Checking VDS Comparators During Normal Operation (Low-Side Given as Example, Principle Also Applies to High-Side)

Shoot Through Detection and Programmable Dead Time

The DRV3201-Q1 provides a mechanism that prevents both external MOSFETs of each power-stage from switching on at the same time connecting VS directly to GND. If the digital inputs try to force the device to switch on high-side and low-side gate-drivers of one power-stage, the error is raised in the status register and the bridges are switched according to Figure 7.

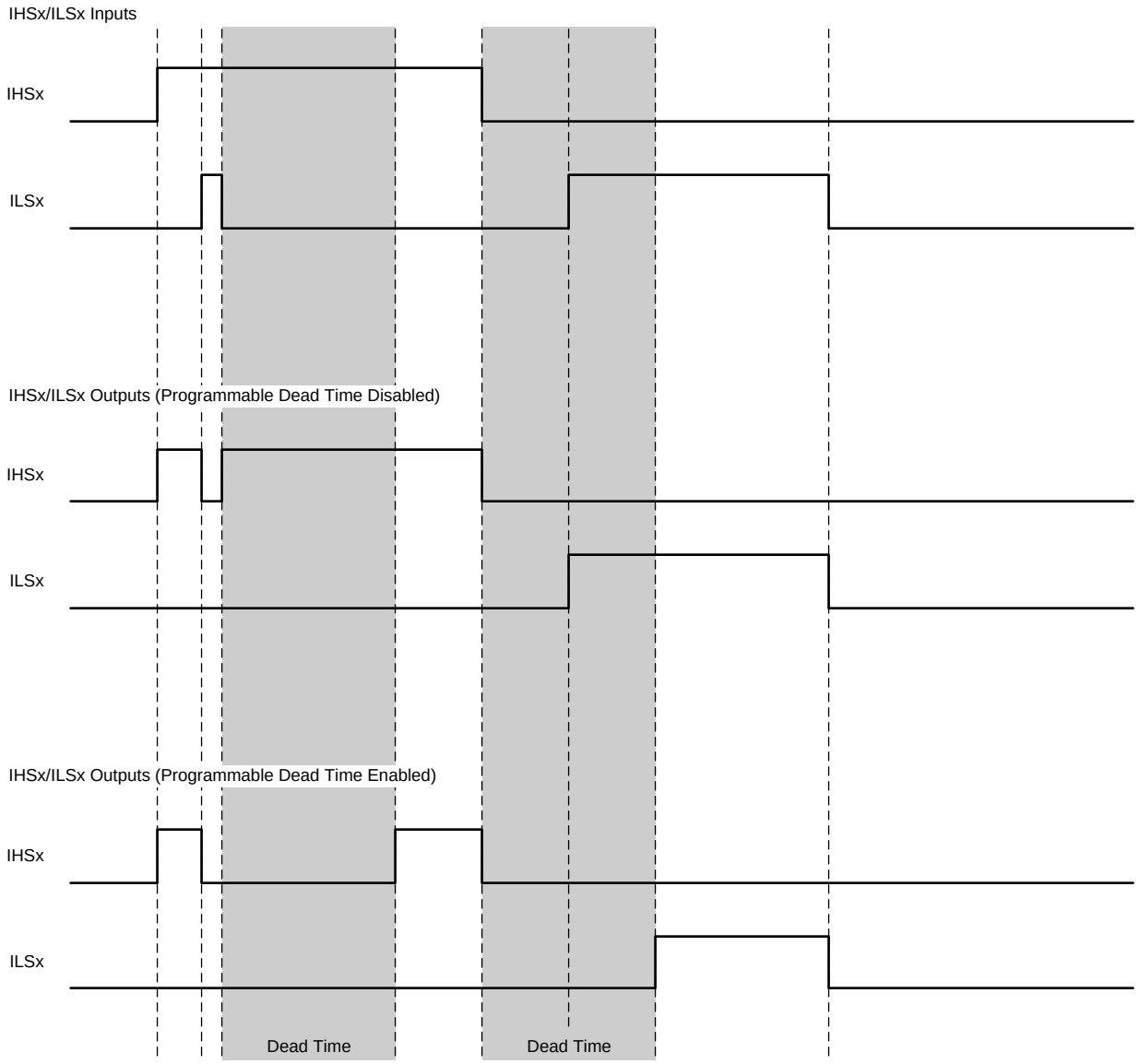


Figure 7. Driver Output During Input Failures

The dead time can be programmed in eight steps between 200 ns and 3000 ns in configuration register 0, bits 2:0. The programmed dead time is valid for all three power-stages. An internal 10 MHz oscillator is used as a time reference for creating the dead-time steps.

The dead time can be disabled in the configurable safety mode (see Configurable Safety Mode) when operating in direct mode. PWM mode does not support disabling the programmable dead time.

Boost Undervoltage Error

If the boost converter output voltage is below the undervoltage threshold level $V_{VBOOST,UV}$ (11 V–11.9 V) for t_{BCSD} (5 µs–6 µs), the boost undervoltage flag is set accordingly in SPI status register 1 (STAT1). Depending on the configured safety mode (see Configurable Safety Mode), all gate-driver outputs are pulled low, and the ERR pin is pulled low.

VS Undervoltage Shutdown

If the VS voltage drops below the undervoltage threshold level $V_{VS,UV}$ (4.5 V–4.75 V) for $t_{VS,SHD}$ (5 µs–6 µs), the VS undervoltage flag is set in SPI status register 1 (STAT1), the gate-driver outputs are pulled low, and the ERR pin is pulled low. This happens regardless of the configured safety mode (see Configurable Safety Mode). The SPI interface works down to 3 V. Below 3 V on VS, internal reset occurs.

VS Overvoltage Error

If the VS voltage exceeds the overvoltage threshold level $V_{VS,OV}$ (29.3 V–30.7 V) for $t_{VS,SHD}$ (5 µs–6 µs), the VS overvoltage flag is set in SPI status register 1 (STAT1). Depending on the configured safety mode (see Configurable Safety Mode), all gate-driver outputs are pulled low, and the ERR pin is pulled low.

VS Comparator Check

The VS undervoltage and overvoltage comparators can be checked by using the loss of clock (LOC) test/VS comparator bit in configuration register 0 (CFG0). As long as this bit is set the comparators toggle and flag the undervoltage and the overvoltage at the same time. The error handling is active, so the bridges shut down and the ERR pin is pulled low. To reset the flags the LOC test /VS comparator bit needs to be reset and then the flags need to be read via SPI. After this, the ERR pin goes up again. This self-check is combined with the loss of clock self-test (see Loss of Clock).

Overtemperature Warning and Shutdown

The thermal overload detection and protection of the device is based on five temperature sensors and two thresholds T_{msd1} (thermal warning) and T_{msd2} (thermal global reset):

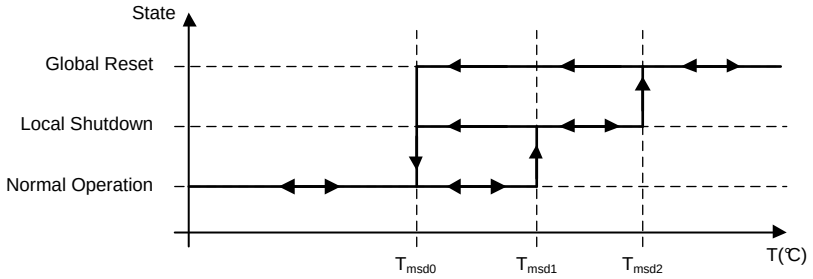


Figure 8. Thermal Shutdown

Normal operation of the device:

- Gate-drivers and boost converter are fully operational.

Thermal warning – overtemperature warning flag is set to 1:

- Thermal warning, stored in overtemperature warning bit in status register 0 (STAT0). This bit is reset after a read out of this register by the MCU.

Global reset - device in shutdown:

- An internal reset is generated.
- The boost converter is stopped.
- However, the temperature monitor block monitors the temperature and does not release the reset until the temperature drops below T_{msd0}.
- Thermal hysteresis avoids any oscillation between shutdown and restart.
- The overtemperature shutdown is filtered with t_{TSD} (no unwanted shutdown by noise).

SPI Error

If the DRV3201-Q1 receives an invalid write or read access, the SPI OK bit in status register 1 (STAT1) is set to 0. This bit is set to 1 after a read out of this register by the MCU.

EEPROM CRC Check

After each wake up to active mode, the DRV3201-Q1 performs an EEPROM CRC check. If the calculated CRC8 checksum does not match the CRC8 checksum stored in the EEPROM, the EEPROM Data CRC Failed flag is set in status register 1 (STAT1).

Configuration Data CRC Check

The DRV3201-Q1 offers a security feature to permanently ensure configuration integrity employing a CRC8 checksum mechanism. The MCU can start a CRC8 checksum calculation within the DRV3201-Q1 over all configuration registers by setting bit 0 in the CRC control register (CRCCTL) to 1. This bit stays set until the CRC calculation is finished. There may not be any write access while the CRC engine is running, otherwise the CRC8 checksum becomes corrupt. The CRC8 checksum value calculated by the DRV3201-Q1 is stored in the CRC calculated checksum register (CRCCALC).

The MCU itself can also calculate the expected CRC8 checksum value, based on the vector given below, and store this expected value in the CRC expected checksum register (CRCEXP). This should be done before the MCU initiates the CRC8 checksum calculation within the DRV3201-Q1. After the DRV3201-Q1 does the CRC calculation, if the expected CRC stored in the CRCEXP register does not match the calculated CRC in CRCCALC register, the Configuration Data CRC Failed flag is set in status register 1 (STAT1).

The MCU may then read back all configuration registers to search for the bit error and perform corrective actions.

The CRC8 calculation mechanism is a generic one with following presets:

- The polynomial used is: (0 1 2 8)
- Initial value is: 11111111

See Table 3 for CRC data vector.

Table 3. CRC Data Vector

Bit Number	CRC8 Data Bus Values
[47:40]	CFG0
[39:32]	CFG1
[31:28]	CFG2
[27:22]	CURR0
[21:16]	CURR1
[15:10]	CURR2
[9: 4]	CURR3
[3: 0]	0000

Loss of Clock

If the internal clock gets stuck, the loss of clock monitor pulls the ERR pin low. During a test of this block the ERR is also low. This self-check is combined with the VS comparator self-test (see VS Comparator Check)

Configurable Safety Mode

The DRV3201-Q1 can work in two different safety modes controlled by the external pin CSM, as described in Table 4. This pin can be read back via SPI register RB0.

Table 4. Safety Modes

CSM	Description
LOW	Full safety mode: All internal protection features are activated.
HIGH	Configurable safety mode: Protective actions as selected in configuration register CFG_REG_1 are enabled and they set diagnostic flags, deselected actions only set diagnostic flags without protective action. With this mode the device can be used outside the normal operation range but below Absolute Maximum Range (see ABSOLUTE MAXIMUM RATINGS(1)(2)) under responsibility of user.

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network ground terminal, unless otherwise specified.

Table 5 defines the protective actions taken on certain error conditions. When the device is in full safety mode, all internal protection features are activated, and all protective actions listed below are taken if the respective error condition is detected. When the device is in configurable safety mode (CSM), the error conditions for which CSM is available, the protective action and ERR pin indication (see Error Indication on ERR Pin) can be configured with the corresponding bit in CFG1. The diagnostic flags are always set if the respective error condition is present, regardless of the CSM setting.

Table 5. Error Conditions and Protective Actions

Error Condition	Protective Action	Recovery	Selectable Through CFG_REG_1 in CSM	Error Indication ERR Pin
VS undervoltage	Switch all gate-driver outputs to low (active pulldown)	Flags are cleared with MCU reading the status register or through RESET. If the failure remains after read out of the register, it is immediately be reported again.	No	Always
VS overvoltage			Yes	Selectable by CFG_REG_1
Boost converter undervoltage			Yes	
HS VDS error			Yes	
LS VDS-error			Yes	
Programmable dead time window failure	Enforce programmable dead time		Yes	
Shoot through protection violated	Switch high-side and low-side gate-driver outputs of affected power-stage to low (active pulldown). If enabled, enforce dead time to high-side and low-side.		No	Always
SPI error	SPI command is ignored		No	None
Configuration data CRC error	Reported via SPI		No	None
EEPROM data CRC error			No	None
Overtemperature first threshold			No	Always
Overtemperature second threshold	Shutdown of device	After thermal recovery device performs power on reset	No	Always
LOC error	ERR pin low		No	Always

Error Indication on ERR Pin

The ERR pin is an indicator for a detected error condition. It may act as interrupt to the external MCU, after which the MCU reads all status registers to determine which error condition is detected. After entering active mode this pin remains high as long as no error condition is detected, in case of a detected error condition the ERR pin goes low. Error reporting occurs according to Table 6.

Table 6. Error Reporting in the Safety Modes

CSM	ERR pin configuration (CFG1)	Description
LOW	Do not care	All error conditions are flagged on ERR pin
HIGH	1	ERR pin only shows errors for protective actions that are enabled in CSM
	0	All error conditions are flagged on ERR pin

The ERR pin goes up again after a read out of the respective error flag in the status register once the respective violation condition disappears. In case the MCU reads out the respective error flag in the status register while the respective error condition is still present, the ERR pin shows a short positive pulse (pulse width typically 100 ns).

This behavior helps show the distinction between a loss of clock error and a VS undervoltage or overvoltage error flag during self-tests of these safety features. After activation of these self-tests in configuration register 0 (CFG0) bit 6, the ERR pin goes down. After an MCU read out of the VS undervoltage/overvoltage flags in status register 1 (STAT1) bits 1:0, the ERR pin should stay low if the loss of clock self-test is working properly. If the ERR pin shows a positive pulse (pulse width typically 100 ns), this is an indication of a failure in the loss of clock self-test.

Additional Safety Features

IHSx/ILSx Input Readback/Edge Counter

To verify the signal path to the DRV3201-Q1, the device allows reading back the logic level of all IHSx and ILSx inputs from the RB0 address. These values directly reflect the state of the pin and are not registered. It is required to ensure that the state of the IHSx and ILSx pins do not change while reading back their levels via SPI.

IHSx/ILSx Input Readback remains operational even if PWM Mode is chosen. In this case the ILSx Readback may be used to read any logic level signal.

The edge counter allows a more robust and less time critical verification of the ILSx/IHSx signal chain and may be more convenient to use during normal operation. This counter can be used to count the number of edges on one or more IHSx/ILSx inputs. The MCU selects the inputs to be observed and arms the counter by writing to the SPI register RB1. When the start bit is removed the counter stops counting edges. The obtained counter value can be read from the SPI register RB2 and it resets by setting the CLEAR bit in SPI register RB1.

When the counter has reached its maximum value of 255 it stops counting and remains in this state.

IHSx/ILSx edge counter remains operational even if PWM Mode is chosen, and in this case it may be used to count edges at any connected input.

Gate-Source Voltage Monitoring

The DRV3201-Q1 provides a gate-source voltage monitoring feature for the external MOSFETs. For each external MOSFET, the VGS is monitored by a comparator with 1 V as a lower threshold, and 9 V as a higher threshold.

For each external MOSFET, a status flag is set in SPI status register 2 (STAT2), bits 0:5. Each status bit is set to 1 when the respective VGS rises above 9 V and they are set to 0 when the respective VGS drops below 1 V. This feature is intended for diagnostic use after startup to turn on/off the external MOSFETs and check the respective status bits.

Ultima Ratio Support

Under certain circumstances it may be required to turn on all FETs simultaneously, which is supported by this device. However, to minimize risk of accidental triggering two requirements need to be satisfied:

1. The MCU is required to perform an unlock sequence of three different consecutive SPI transfers.
2. When the last SPI command is sent all IHSx and ILSx inputs need to be at a high level already.

This feature is only available when operating in direct mode.

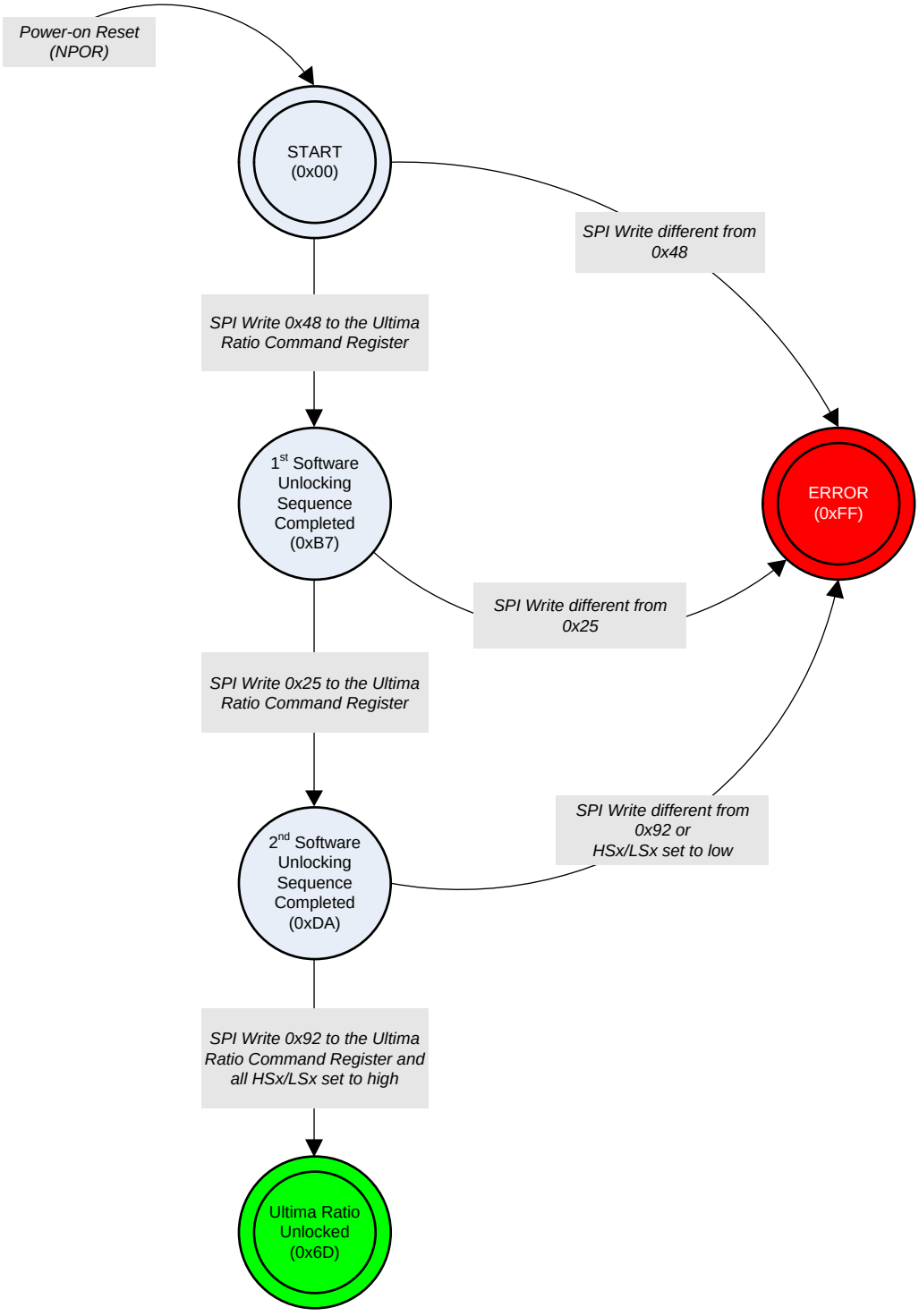


Figure 9. State Diagram for Unlocking Ultima Ratio

CURRENT MEASUREMENT

The two channel current measurement is measured by the voltage drop across two external shunt resistors. It contains one shift buffer, two first and two second stages.

Shift Buffer

The DRV3201-Q1 offers a unity gain amplifier that is normally used to support a shift voltage with lower output impedance. This allows each current sense path to handle negative common-mode voltages across the external shunt resistor. The shift voltage is applied externally on the RI pin, with the actual shift voltage buffered on the RO pin.

The RI input pin is a high-impedance input to a MOS gate with internal ESD protection to ground. There is no reverse pullup path present to any supply (fail-safe ESD structure).

Two First Stage Amplifiers

A first stage operational amplifier operates with an external resistor network for higher flexibility to adjust the current measurement to the application requirements.

In the recommended application, a shift voltage that may be based on an external reference (e.g. an external voltage regulator) can be added to move the transfer curve. Each channel of the first amplifier has its own output going to the input of the MCU ADC.

The input of the first stage is high voltage compatible, so the device can be used to measure the voltage drop across the low-side MOSFET for low requirement applications. The maximum output voltage of the O1 and O2 pins is clamped to the ADREF voltage.

The input pins INx and IPx pin are high-impedance inputs to a MOS gate with internal ESD protection to ground. There is no reverse pullup path present to any supply (fail-safe ESD structure).

Two Second Stage Amplifiers

The second stage amplifiers with a separately programmable gain enable a higher resolution measurement at low current. They can be directly connected to inputs of the MCU ADC.

The gain of the second stage amplifiers is programmable by SPI in steps two, four, six and eight using the CFG2 register.

The maximum output voltage of the O3 and O4 pins is clamped to the ADREF voltage.

ADREF Voltage Clamp

The maximum output voltage of pins O1–O4 is clamped to the voltage applied to ADREF by an active clamp. The ADREF voltage is the reference supply voltage for the ADC in the MCU, so the outputs O1–O4 have a maximum signal range related to the input range of the ADC in the MCU. The active clamp consumes a maximum of 100 µA from the ADREF pin.

Current Sense Application Circuit

The standard configuration for the current sense amps are given in Figure 10.

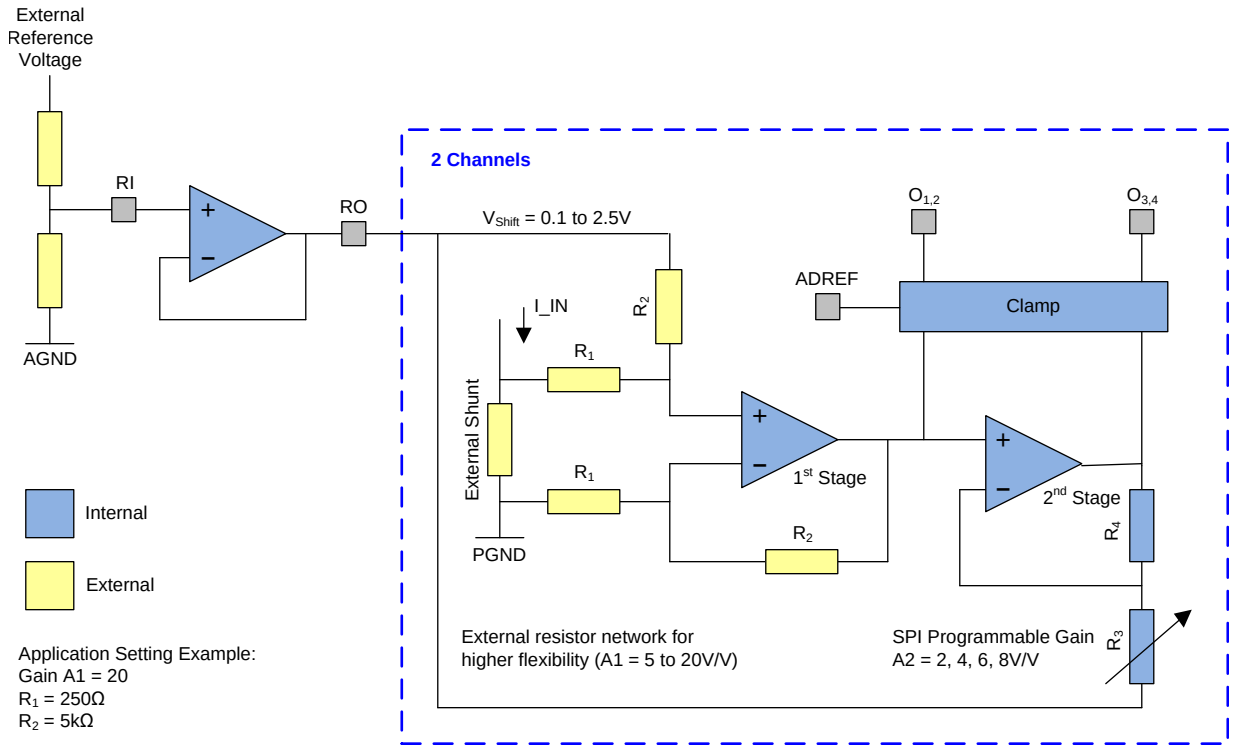


Figure 10. Application Circuit for Current Sense

The output voltage at O1/2 is: $O_{1/2} = IR_S \frac{R_2}{R_1} + V_{RO}$

The output voltage at O3/4 is: $O_{3/4} = g \times (O_{1/2} - V_{RO}) + V_{RO}$
where g is the SPI adjusted gain in the second stage.

PHASE COMPARATORS

The device contains three real time phase comparators usable for sensorless commutation and diagnostics. Each comparator is switching at typically 75% and 25% of the supply voltage, and has an individual digital output going to the MCU. The phase comparators are always active as long as EN is high.

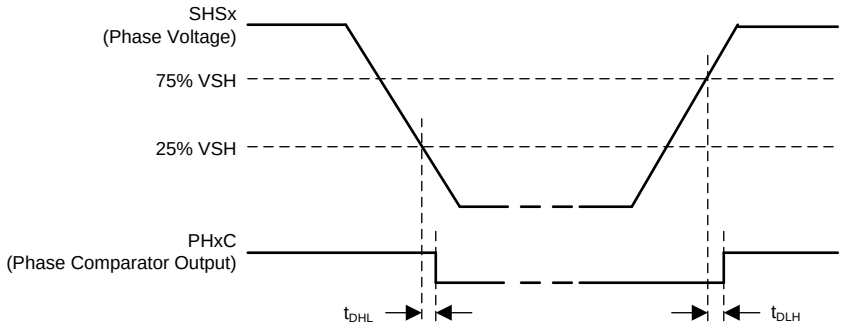


Figure 11. Phase Comparator Rise and Fall Thresholds

Phase Comparators Application Diagram

The phase comparator configuration is given in Figure 12.

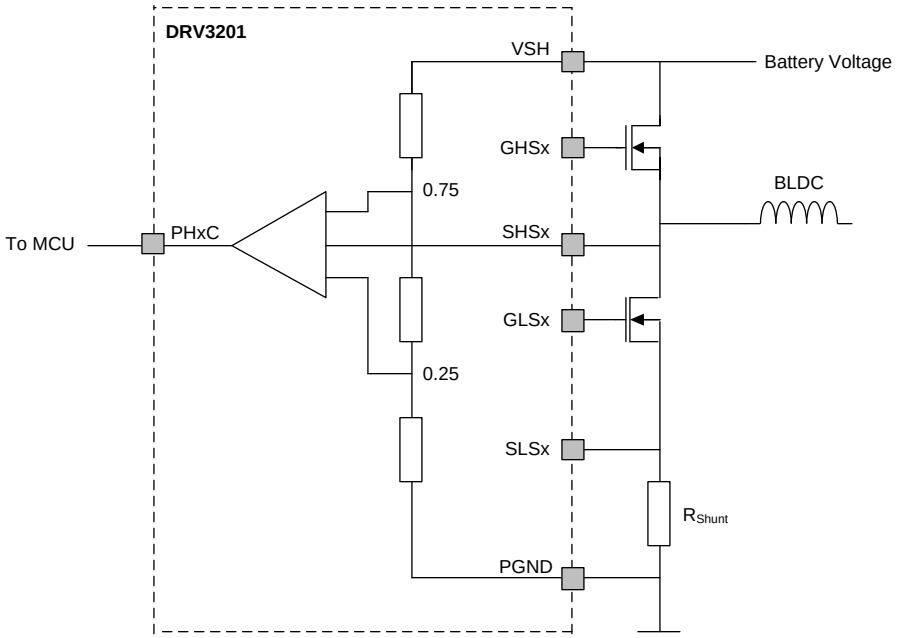


Figure 12. Application Diagram for Phase Comparators

The phase comparators allow:

- Real time observation of the phase switching on node SHSx
- Measurement of the time between the Input IHSx/ILSx and the phase comparator output PHxC
- Verification of time drift in previous measurements and/or other driver-stages

As Figure 12 shows, the VSH and PGND pins are used as sense inputs to create the high-side and low-side threshold levels for the phase comparators. Connect the VSH pin externally to the star-point of the positive supply of the power-stages. The PGND pin is to be connected to the power-ground star-point of the power-stages. The total resistance of the internal voltage divider is typically 248 kΩ.

BOOST CONVERTER

The boost converter is based on a burst mode fixed frequency controller. During the on-time, the internal low-side boost FET is turned on until the current limit level is detected. The off-time is calculated proportionally from an independent 2.5 MHz time-reference by sensing the supply voltage VS and the output voltage VBOOST. A hysteretic comparator (low-level VBOOST-VS = 14 V, high level VBOOST-VS = 16 V) determines starting/stopping the burst pulsing. The nominal switching frequency during the burst pulsing is 2.5 MHz.

The maximum current in the coil can be adjusted by the resistor Rboost_shunt such that the maximum coil current is limited to 0.1 V/Rboost_shunt. This current limit is used by the controller to switch off the internal low-side boost FET. It is recommended to choose a coil with a current saturation level of at least 30% above the current limit level set with the resistor Rboost_shunt.

A second internal current limit is implemented that triggers at higher currents and acts as a second level of protection for the internal low-side boost FET in case the resistor R1 is shorted. If the Rboost_shunt is shorted, the second current limit is used by the controller to switch off the internal low-side boost FET. Since the second internal current limit is higher than the normal current limit set by Rboost-shunt and only meant for protecting the internal boost FET, the external coil may saturate if the second internal current limit becomes active. To allow the external MCU to detect this possible failure condition, the second internal current limit sets the boost undervoltage flag (register STAT1, bit 2). This causes a shutdown of the gate-drivers depending on the configured safety mode.

To reduce noise level on the chip the boost converter can be switched off during sensitive current measurements with the B_EN pin. As long as the disable time interval is short enough, the boost output capacitor can keep the boost output voltage high enough. When the boost converter is disabled, the boost undervoltage monitor is active to ensure the driver-stages are still operating correctly. During the boost undervoltage condition, the boost switching frequency folds back to around half the normal operating frequency. This does not affect the current limit.

Application Circuit for Boost Converter

The recommended application for the boost converter is given in Figure 13. For the best performance, a Schottky diode and a 22 µH coil is required. The current limit for the internal FET (and the maximum current in the coil) can be adjusted and in the recommended application it is set to 0.1 V/0.33 Ω = 300 mA.

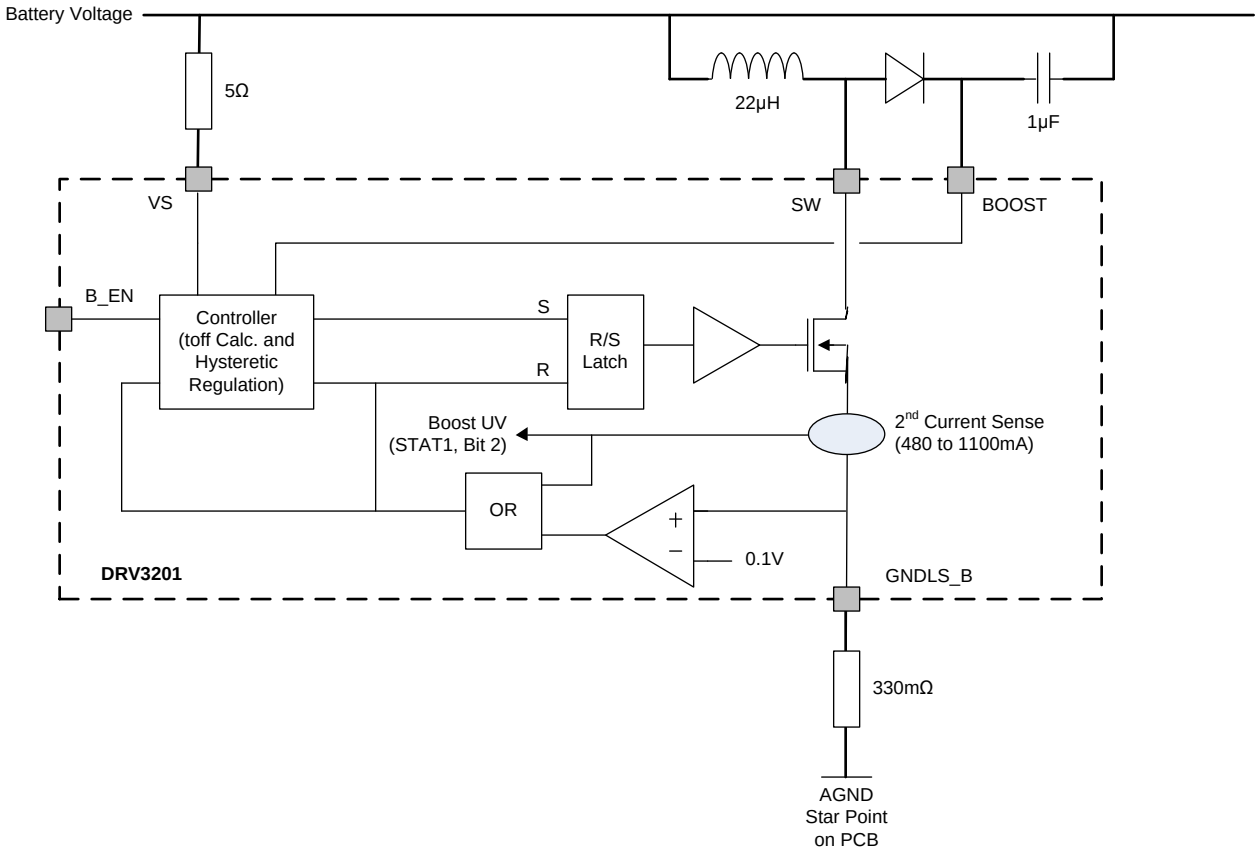


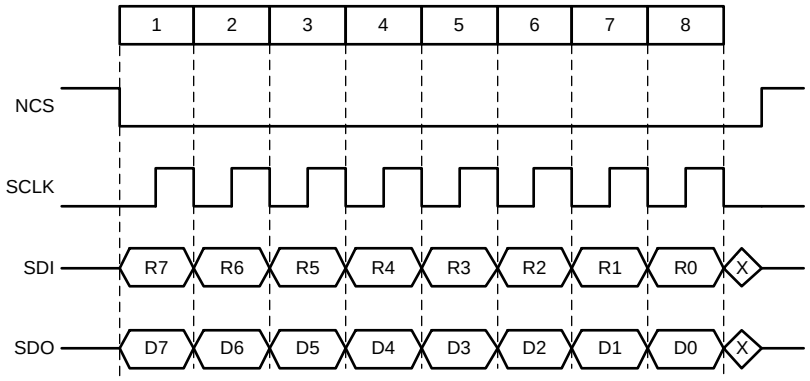
Figure 13. Recommended Application Circuit for Boost Converter

SPI INTERFACE

The SPI slave interface is used for serial communication with external SPI master (external MCU). The SPI communication starts with the NCS falling edge, and ends with NCS rising edge. The NCS high level keeps SPI slave interface in reset state, and SDO output 3-stated.

Address Mode Transfer

The address mode transfer is an 8-bit protocol. Both SPI slave and SPI master transmit the MSB first.



NOTE: SPI Master (MCU) and SPI Slave (DRV3201) sample received data on the falling SCLK edge, and transmit on rising SCLK edge

Figure 14. Single 8-bit SPI Frame/Transfer

After the NCS falling edge, the first word of 7 bits are address bits followed by the RW bit. During the first address transfer, the device returns the STAT1 register on SDO. Each complete 8-bit frame is processed. The bits are ignored if NCS goes high before a multiple of 8 bits is transferred.

SPI Address Transfer Phase

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Function	ADDR6	ADDR5	ADDR4	ADDR3	ADDR2	ADDR1	ADDR0	RW

FIELD NAME	BIT DEFINITION
ADDR [6:0]	Register Address
RW	RW = 1: Write access
	RW = 0: Read access

When RW = 0, the SPI master performs a read access to the selected register. During the following SPI transfer, the device returns the requested register read value on SDO, and interprets SDI bits as a next address transfer. When RW = 1, the master performs a write access on the selected register. The slave updates the register value during the next SPI transfer (if followed immediately) and returns the current register value on SDO.

SPI Data Transfer Phase

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Function	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

FIELD NAME	BIT DEFINITION
DATA [7:0]	Data value for write access (8-bit)

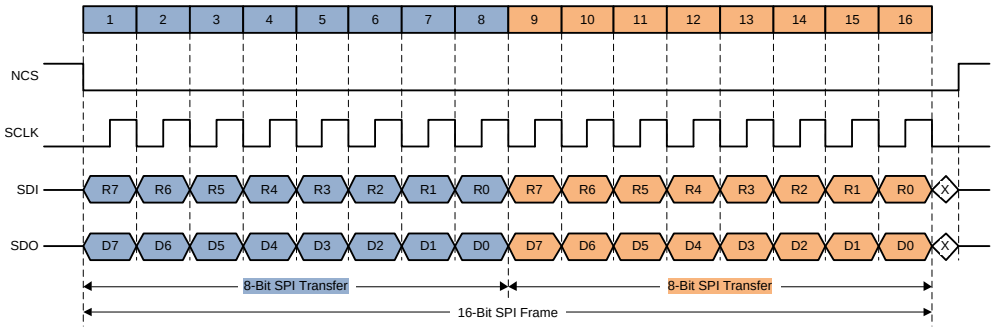
The table shows a data value encoding scheme during a write access.
It is possible to mix the two access modes (write and read access) during one SPI communication sequence (NCS = 0). The SPI communication can be terminated after a single 8-bit SPI transfer by asserting NCS = 1. The device returns STAT1 register (for the very first SPI transfer after power-up) or current register value addressed during the SPI transfer address phase.

Device Data Response

Bit	R7	R6	R5	R4	R3	R2	R1	R0
Function	REG7	REG6	REG5	REG4	REG3	REG2	REG1	REG0

FIELD NAME	BIT DEFINITION
REG [7:0]	Internal register value

All unused bits are set to zero.



NOTE: SPI Master (MCU) and SPI Slave (DRV3201) sample received data on the falling SCLK edge, and transmit on rising SCLK edge

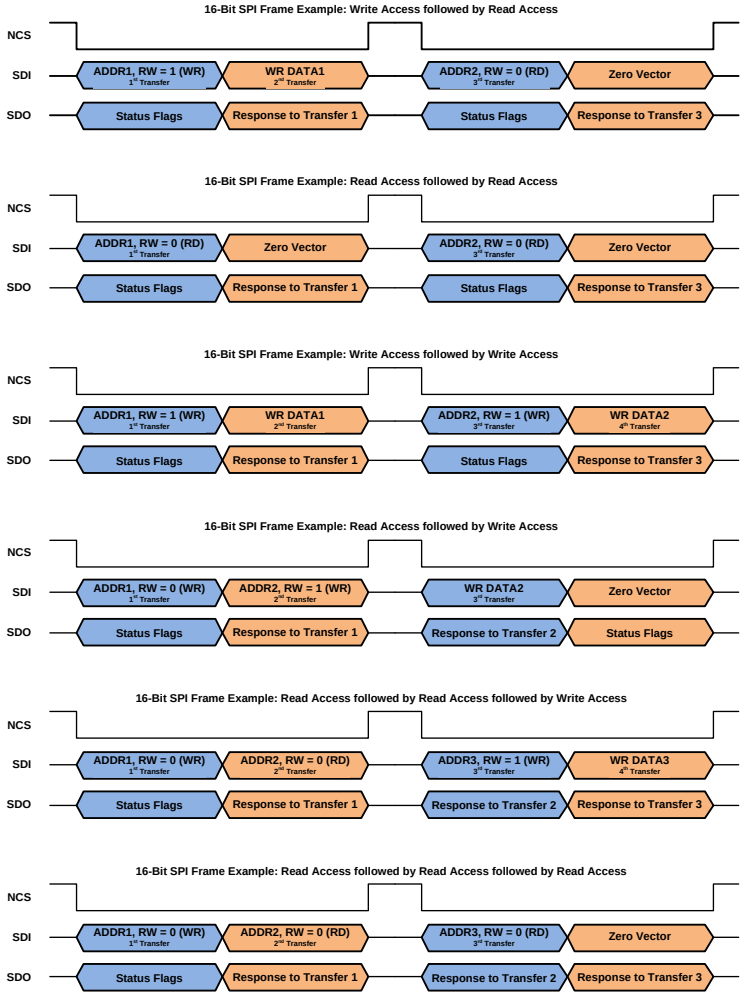


Figure 15. SPI Frame examples

Register Address Map

Address	Name	RW	Reset Value
0x00	Reserved		
0x01	Configuration Register 0 (CFG0)	RW	8'h3F
0x02	Configuration Register 1 (CFG1)	RW	8'h3F
0x03	Configuration Register 2 (CFG2)	RW	4'h0
0x04	HS1/2 Slope Register (CURR0)	RW	6'h3F
0x05	LS1/2 Slope Register (CURR1)	RW	6'h3F
0x06	HS3 Slope Register (CURR2)	RW	6'h3F
0x07	LS3 Slope Register (CURR3)	RW	6'h3F
0x08-0x0F	Reserved		
0x10	Status Register 0 (STAT0)	RO	8'h00
0x11	Status Register 1 (STAT1)	RO	8'h80
0x12	Status Register 2 (STAT2)	RO	6'h00
0x13-0x1F	Reserved		
0x20	CRC Control Register (CRCCTL)	RW	1'h0
0x21	CRC Calculated (CRCCALC)	RO	8'h0
0x22	CRC Expected (CRCEXP)	RW	8'h0
0x23	HS/LS Read Back (RB0)	RO	6'h0
0x24	HS/LS Count Control (RB1)	RW	6'h0
0x25	HS/LS Count (RB2)	RO	8'h0
0x26-0x2F	Reserved		
0x30	Ultima Ratio Command (UR)	RW	8'h0
0x31-7F	Reserved		

Detailed Register Definitions

Table 7. Configuration Register 0 (CFG0) (Addr. 0x01)

Bits	R/W	Reset	Definition
7	RW	1'h0	Current capability 1: Reduced current mode (all gate charge/discharge currents are 25%) 0: Full current mode
6	RW	1'h0	Loss of clock detection test/VS comparator test If this bit is set, the clock for LOC monitor is permanently set to high. Additionally, the VS comparators show a VS undervoltage and a VS overvoltage at the same time in status register 1 (STAT1), bits 1:0. Both LOC and VS undervoltage/overvoltage are indicated on the ERR pin. A way to distinguish between LOC and VS undervoltage/overvoltage is described in VS Comparator Check. Once the bit is cleared, the error-flag disappears after read out.
5:3	RW	3'h7	VDS monitoring scale factor VSCTH/VDS threshold 000: 0 001: 1/7 010: 2/7 011: 3/7 100: 4/7 101: 5/7 110: 6/7 111: 1 (Voltage follower)
2:0	RW	3'h7	Programmable dead time 000: 200-300 ns 001: 300-400 ns 010: 500-600 ns 011: 900-1000 ns 100: 1400-1500 ns 101: 1900-2000 ns 110: 2400-2500 ns 111: 2900-3000 ns

Table 8. Configuration Register 1 (CFG1) (Addr. 0x02)

Bits	R/W	Reset	Definition
7	RW	1'h0	0: Adjustable HS/LS currents for rising/falling edges according to registers CURR0–3 1: Unlimited HS/LS currents for rising/falling edges
6	RW	1'h0	Set PWM mode All gate-drivers can be driven with 3 PWM signals
5	RW	1'h1	ERR pin configuration In CSM, ERR pin only shows errors that are actually handled in CSM if this bit is set or else all errors are flagged
4	RW	1'h1	Enable LS VDS error handling in CSM
3	RW	1'h1	Enable HS VDS error handling in CSM
2	RW	1'h1	Enable programmable dead time in CSM
1	RW	1'h1	Enable boost undervoltage handling in CSM
0	RW	1'h1	Enable VS overvoltage handling in CSM

Table 9. Configuration Register 2 (CFG2) (Addr. 0x03)

Bits	R/W	Reset	Definition
7:4	RO	1'h0	Reserved
3:2	RW	2'h0	Current amplifier gain for second stage second amplifier (O4/O2) 00: 2 01: 4 10: 6 11: 8
1:0	RW	2'h0	Current amplifier gain for second stage first amplifier (O3/O1) 00: 2 01: 4 10: 6 11: 8

Table 10. HS1/2 Slope Register (CURR0) (Addr. 0x04)

Bits	R/W	Reset	Definition
7:6	RO	2'h0	Reserved
5:3	RW	3'h7	Adjust HS0/1 current for rising edge 000: 140 mA 001: 140 mA 010: 290 mA 011: 430 mA 100: 570 mA 101: 710 mA 110: 850 mA 111: 1 A
2:0	RW	3'h7	Adjust HS0/1current for falling edge 000: 140 mA 001: 140 mA 010: 290 mA 011: 430 mA 100: 570 mA 101: 710 mA 110: 850 mA 111: 1 A

Table 11. LS1/2 Slope Register (CURR1) (Addr. 0x05)

Bits	R/W	Reset	Definition
7:6	RO	2'h0	Reserved
5:3	RW	3'h7	Adjust LS0/1 current for rising edge 000: 140 mA 001: 140 mA 010: 290 mA 011: 430 mA 100: 570 mA 101: 710 mA 110: 850 mA 111: 1 A
2:0	RW	3'h7	Adjust LS0/1 current for falling edge 000: 140 mA 001: 140 mA 010: 290 mA 011: 430 mA 100: 570 mA 101: 710 mA 110: 850 mA 111: 1 A

Table 12. HS3 Slope Register (CURR2) (Addr. 0x06)

Bits	R/W	Reset	Definition
7:6	RO	2'h0	Reserved
5:3	RW	3'h7	Adjust HS2 current for rising edge 000: 140 mA 001: 140 mA 010: 290 mA 011: 430 mA 100: 570 mA 101: 710 mA 110: 850 mA 111: 1A
2:0	RW	3'h7	Adjust HS2 current for falling edge 000: 140 mA 001: 140 mA 010: 290 mA 011: 430 mA 100: 570 mA 101: 710 mA 110: 850 mA 111: 1 A

Table 13. LS3 Slope Register (CURR3) (Addr. 0x07)

Bits	R/W	Reset	Definition
7:6	RO	2'h0	Reserved
5:3	RW	3'h7	Adjust LS2 current for rising edge 000: 140 mA 001: 140 mA 010: 290 mA 011: 430 mA 100: 570 mA 101: 710 mA 110: 850 mA 111: 1 A

Table 13. LS3 Slope Register (CURR3) (Addr. 0x07) (continued)

Bits	R/W	Reset	Definition
2:0	RW	3'h7	Adjust LS2 current for falling edge 000: 140 mA 001: 140 mA 010: 290 mA 011: 430 mA 100: 570 mA 101: 710 mA 110: 850 mA 111: 1 A

Table 14. Status Register 0 (STAT0) (Addr. 0x10)

Bits	R/W	Reset	Definition
7	RO	1'h0	Reserved
6	RO	1'h0	Over temperature warning
5	RO	1'h0	HS2 VDS error
4	RO	1'h0	HS1 VDS error
3	RO	1'h0	HS0 VDS error
2	RO	1'h0	LS2 VDS error
1	RO	1'h0	LS1 VDS error
0	RO	1'h0	LS0 VDS error

Table 15. Status Register 1 (STAT1) (Addr. 0x11)

Bits	R/W	Reset	Definition
7	RO	1'h1	SPI OK flag
6	RO	1'h0	Configuration data CRC failed
5	RO	1'h0	EEPROM data CRC failed
4	RO	1'h0	Programmable dead time violated
3	RO	1'h0	Shoot through protection violated
2	RO	1'h0	Boost undervoltage
1	RO	1'h0	VS overvoltage
0	RO	1'h0	VS undervoltage

Table 16. Status Register 2 (STAT2) (Addr. 0x12)

Bits	R/W	Reset	Definition
7:6	RO	2'h0	Reserved
5	RO	1'h0	HS2 VGS comparator (0 if VGS < 1 V, 1 if VGS > 9 V)
4	RO	1'h0	HS1 VGS comparator (0 if VGS < 1 V, 1 if VGS > 9 V)
3	RO	1'h0	HS0 VGS comparator (0 if VGS < 1 V, 1 if VGS > 9 V)
2	RO	1'h0	LS2 VGS comparator (0 if VGS < 1 V, 1 if VGS > 9 V)
1	RO	1'h0	LS1 VGS comparator (0 if VGS < 1 V, 1 if VGS > 9 V)
0	RO	1'h0	LS0 VGS comparator (0 if VGS < 1 V, 1 if VGS > 9 V)

Table 17. CRC Control Register (CRCCTL) (Addr. 0x20)

Bits	R/W	Reset	Definition
7:1	RO	7'h0	Reserved
0	RO	1'h0	Starts configuration data CRC8 calculation. Bit gets cleared when calculation is finished To perform CRC check: 1.Calculate CRC checksum 2.Store calculated checksum in CRCEXP register 3.Set bit 0 CRC control register (CRCCTL) to 1 4.Bit gets cleared when calculation is finished 5.Failing checksum is indicated in STAT1 register 6.Calculated checksum can be read from CRCCALC register

Table 18. CRC Calculated Checksum Register (CRCCALC) (Addr. 0x21)

Bits	R/W	Reset	Definition
7:0	RO	8'h0	Checksum generated by internal CRC engine

Table 19. CRC Expected Checksum Register (CRCEXP) (Addr. 0x22)

Bits	R/W	Reset	Definition
7:0	RW	8'h0	Checksum externally calculated by microcontroller

Table 20. Input Read Back (RB0) (Addr. 0x23)

Bits	R/W	Reset	Definition
7	RO	1'h0	Reserved
6	RO	1'h0	CSM input
5	RO	1'h0	LS2 input
4	RO	1'h0	LS1 input
3	RO	1'h0	LS0 input
2	RO	1'h0	HS2 input
1	RO	1'h0	HS1 input
0	RO	1'h0	HS0 input

Table 21. HS/LS Count Control (RB1) (Addr. 0x24)

Bits	R/W	Reset	Definition
7	RW	1'h0	Clear edge counter This bit has priority over 6 down to 0
6	RW	1'h0	Start/stop counter 0: Counter stopped 1: Counter running
5	RW	1'h0	Enable LS2 edge count
4	RW	1'h0	Enable LS1 edge count
3	RW	1'h0	Enable LS0 edge count
2	RW	1'h0	Enable HS2 edge count
1	RW	1'h0	Enable HS1 edge count
0	RW	1'h0	Enable HS0 edge count

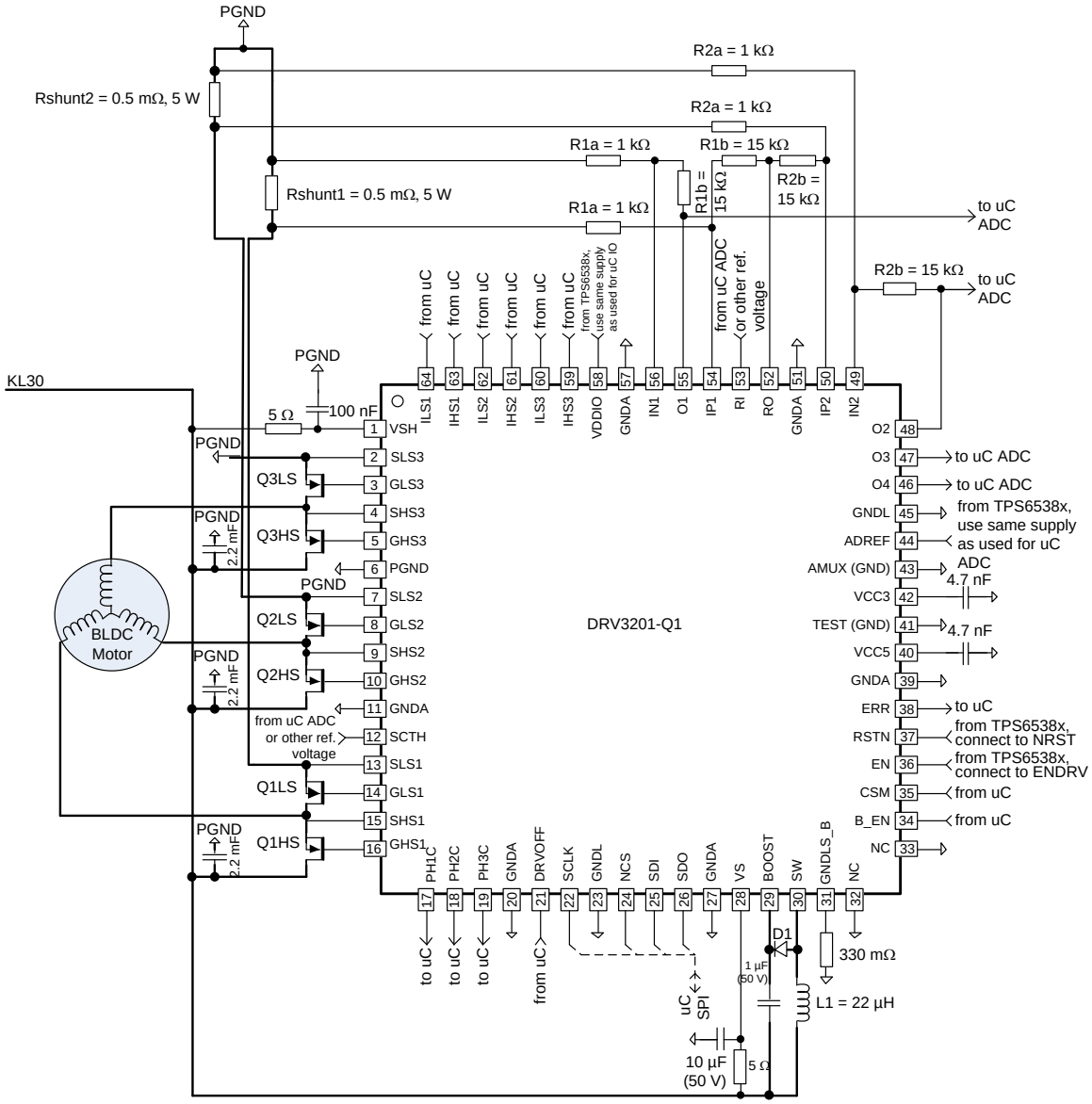
Table 22. HS/LS Count (RB2) (Addr. 0x25)

Bits	R/W	Reset	Definition
7:0	RO	8'h0	HS/LS edge count Counter stops counting at 0xFF

Table 23. Ultima Ratio Command (UR) (Addr. 0x30)

Bits	R/W	Reset	Definition
7:0	RO	8'h0	Ultima ratio command See specification for command sequence

APPLICATION INFORMATION



L1 = B82442A1223K000 INDUCTOR, SMT, 22 µH, 10%, 480 mA)
D1 = SS28 (DIODE, SMT, SCHOTTKY, 80 V, 2 A)
QxHS, QxLS = IRFS3004PBF (HEXFET, N-CHANNEL, POWER MOSFET, D2PACK)
Rshunt1, 2 = BVR-Z-R0005 (RES, SMT, 4026, PRECISION POWER, 0.0005 OHMS, 1%, 5 W)

Figure 16. DRV3201-Q1 Typical Application Diagram

TYPICAL SYSTEM APPLICATION DIAGRAMS

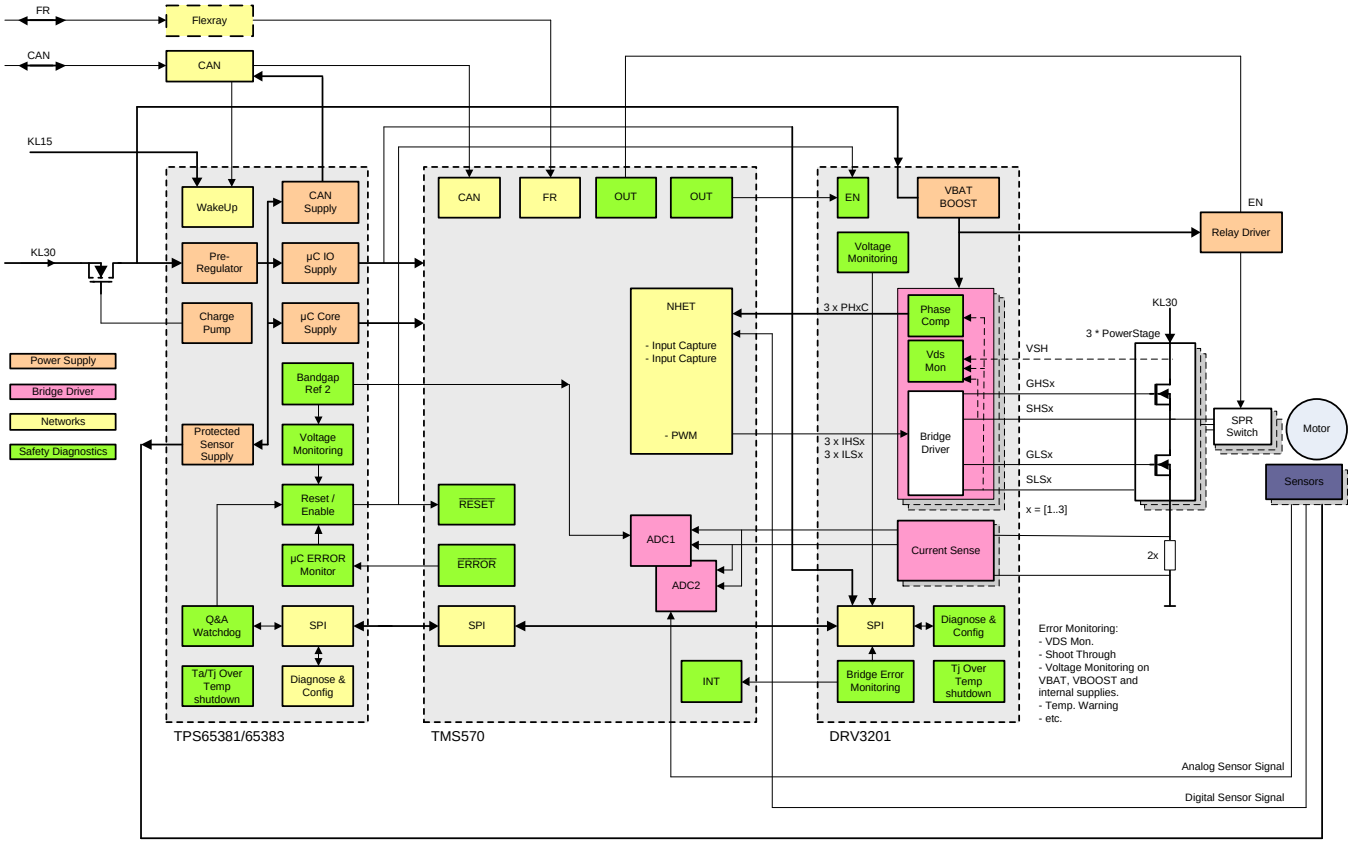


Figure 17. Electrical Power Steering Example

POWER CONSUMPTION

The DRV3201-Q1 has been designed to drive six external power FETs with 250 nC gate charge at 30 kHz PWM frequency. The necessary current for charging the gates of these external power FETs is delivered by the boost converter. The three internal high-side gate-drivers and the three internal low-side gate-drivers are supplied out of the boost converter. The following graphs show the total supply current consumption against the supply voltage for varying boost load current.

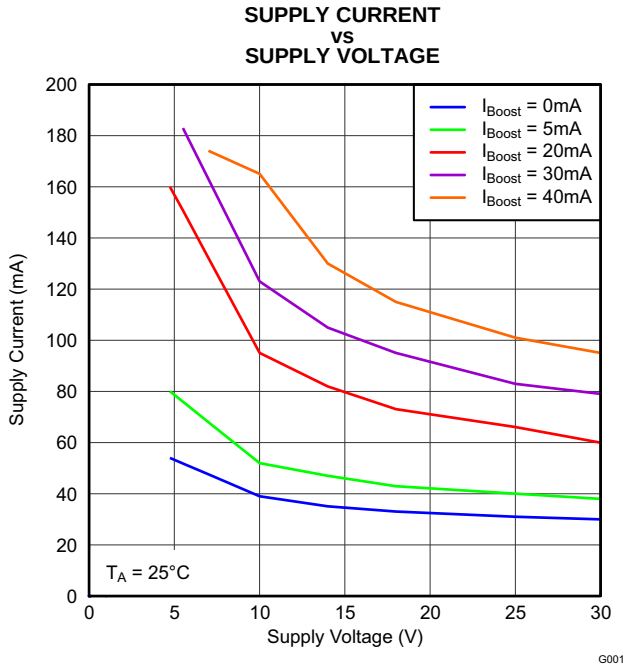


Figure 18. Supply Current vs. Supply Voltage for Varying Boost Load Current at T_A = 25°C

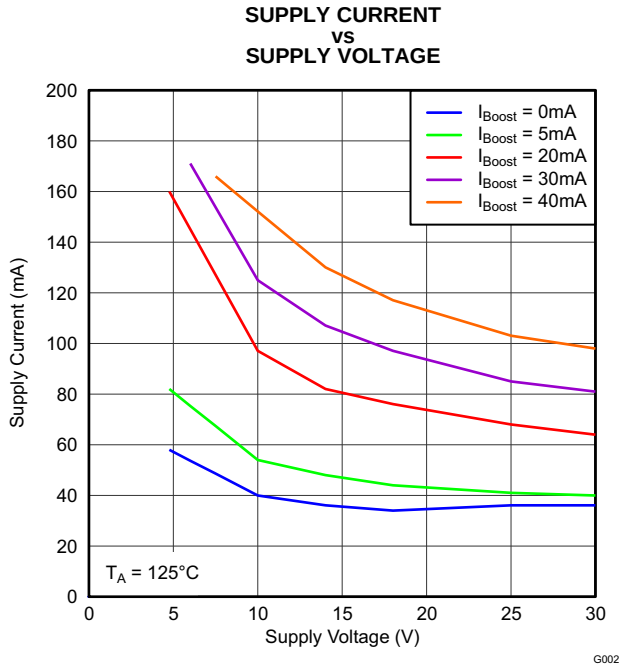


Figure 19. Supply Current vs. Supply Voltage for Varying Boost Load Current at T_A = 125°C

In these graphs, the quiescent current consumption from the boost converter taken by the non-switching gate-drivers is taken into account (see, parameter R_{GSa2} in ELECTRICAL CHARACTERISTICS). However, the current consumption from the boost converter due to gate-driver switching is not taken into account. This gate-driver switching current, which forms the actual load current of the boost converter, consists of two components: the internal gate-driver switching currents, and the external FET gate charging currents.

The switching current from the internal gate-drivers (without the external power FETs) is given in parameter $V_{GS,HS,high}$ in ELECTRICAL CHARACTERISTICS, for 30 kHz PWM frequency and all six gate-drivers.

The total load current Iboost is given by the sum of Equation 1 and Equation 2:
rivers switching. The expected current consumption from the boost converter due to switching gate-drivers (without the external power FETs) can be calculated as follows:

$$I_{boost,sw} = \frac{f_{PWM} \bullet \#FETs \bullet I_{boost,swmax}}{30\ kHZ \bullet 6} = \frac{f_{PWM} \bullet \#FETs \bullet 3\ mA}{30\ kHZ \bullet 6} \quad (1)$$

The switching current formed by charging the gates of the external FETs at the given PWM frequency can be calculated as follows:

$$I_{boost,qg} = f_{PWM} \bullet \#FETs \bullet Q_{gate} \quad (2)$$

$$I_{boost} = I_{boost,sw} + I_{boost,qg} \quad (3)$$

Calculation example 1:

f_{PWM} = 25 kHz

Q_{gate} = 250 nC

Number of FETs = 6

$I_{boost,sw}$ = 25 kHz•6•3 mA/30 kHz•6 = 2.5 mA

$I_{boost,qg}$ = 25 kHz•6•250 nC = 37.5 mA

I_{boost} = 2.5 mA + 37.5 mA = 40 mA

Using the IBOOST = 40 mA from Figure 18 and Figure 19, the total current consumption from VS is 130 mA at T_A = 25°C and for T_A = 125°C. This gives a total power consumption of 1.82 Watt at T_A = 25°C and at T_A = 125°C for VS = 14 V.

Calculation example 2:

f_{PWM} = 20kHz

Q_{gate} = 200nC

Number of FETs = 6

$I_{boost,sw}$ = 20 kHz•6•3 mA/30 kHz•6 = 2 mA

$I_{boost,qg}$ = 20 kHz•6•200 nC = 24 mA

I_{boost} = 2 mA + 24 mA = 27 mA

To estimate the total current consumption from the VS battery supply, the curve IBOOST = 30 mA from Figure 18 and Figure 19 can be used. From this curve, it follows that for VS = 14 V, the total current consumption from VS is 105 mA at T_A = 25°C respectively 107 mA at T_A = 125°C. This gives a total power consumption of 1.47 Watt at T_A = 25°C respectively, 1.50 Watt at T_A = 125°C for VS = 14 V.

From these examples, it can be seen how the gate-charge and the PWM frequency impact the load current for the boost converter and the total battery current consumption in Figure 18 and Figure 19. The total power consumption can be calculated from this.

BOOST CONVERTER

The output current capability of the boost converter can be configured with the external Rshunt_boost resistor to 0.1 V/Rshunt_boost (please note that this resistor needs to be able to conduct the boost switching current). The output current capability can be dimensioned to the needed current determined by the PWM switching frequency and the gate-charge of the external power FETs. It is recommended to choose a coil having a current saturation level of at least 30% above the current limit level set with the resistor Rboost_shunt. The operation principle of the boost converter is based on a burst mode fixed frequency controller. During the on-time, the internal low-side boost FET is turned on until the current limit level is detected. The off-time is calculated proportionally from a 2.5 MHz time-reference by sensing the supply voltage VS and the output voltage VBOOST. The formula for the calculated off-time is given in Equation 4, with f_{boost} = 2.5 MHz.

$$t_{off} = \frac{VS}{V_{BOOST} \cdot f_{BOOST}} \tag{4}$$

For steady state, the current in the coil looks like Figure 20.

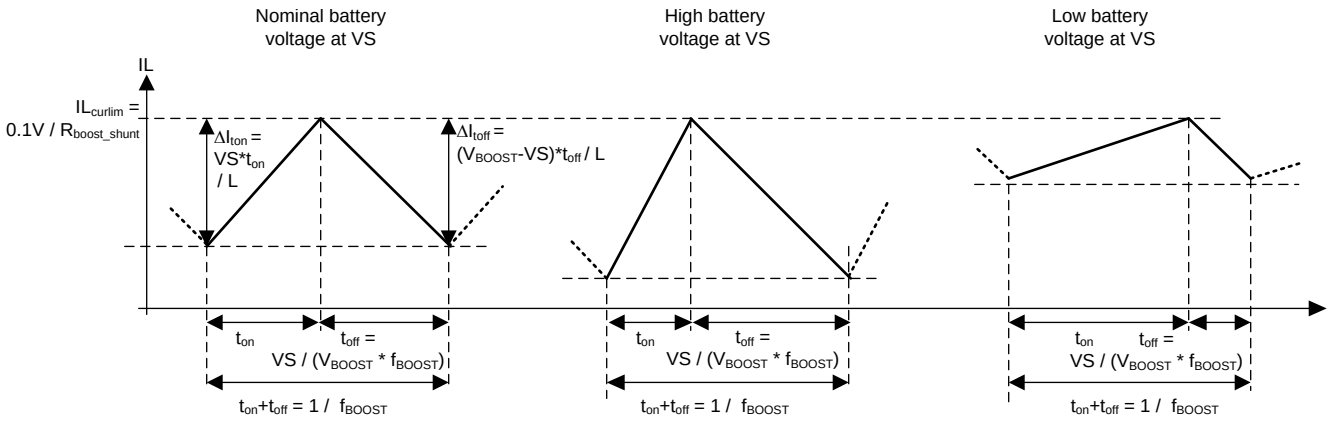


Figure 20. Coil Current Waveforms in Steady State for Nominal, High and Low Battery Voltage

From this figure, the ripple current and the boost output current can be calculated as follows:

$$IL_{ripple} = \frac{VS}{L \cdot f_{BOOST}} \cdot \left(1 - \frac{VS}{V_{BOOST}}\right) = \frac{(V_{BOOST} - VS) \cdot VS}{L \cdot f_{BOOST} \cdot V_{BOOST}} \tag{5}$$

$$I_{BOOST} = \frac{VS}{V_{BOOST}} \cdot IL_{curlim} - \frac{1}{2} \cdot \left(\frac{(V_{BOOST} - VS) \cdot VS}{L \cdot f_{BOOST} \cdot V_{BOOST}}\right) \tag{6}$$

$$f_{BOOST} = 2.5\ MHz;\ (V_{BOOST} - VS) = 15\ V;\ IL_{curlim} = \left(\frac{0.1\ V}{R_{shunt\_boost}} \right) \quad (7)$$

As can be seen from Equation 6, the boost output current capability for a given IL_curlim is the lowest for the minimum supply voltage VS. The boost output current capability should be dimensioned (by setting IL_curlim with external Rshunt_boost) so the needed output current (based on PWM frequency and gate-charge of the external power FETs) can be delivered at the needed minimum supply voltage for the application. The following equation gives IL_curlim as a function of IBOOST and VS:

$$IL_{curlim} = I_{BOOST} \cdot \frac{V_{BOOST}}{VS} + 1/2 \cdot \left(\frac{V_{BOOST} - VS}{L \cdot f_{BOOST}} \right) \quad (8)$$

To set the IL_curlim, the minimum application supply should be used in this equation and IBOOST according to Equation 3.The minimum application supply voltage the DRV3201-Q1 can support is 4.75 V.

As shown in Equation 6, the boost output current capability increases for higher supply voltage VS. If the boost output current capability is dimensioned so it can deliver the necessary output current for the minimum supply voltage, it actually delivers more current than needed for nominal supply voltage and the boost voltage increases. Therefore, a hysteretic comparator (low level VBOOST-VS = 14 V, high level VBOOST-VS = 16 V) determines starting/stopping the burst pulsing as shown in Figure 21.

The nominal switching frequency during the burst pulsing is 2.5 MHz once the boost has reached steady state. During startup of the boost, the internal time reference is slower by a factor of three, resulting in three times longer off-times to allow the coil current to decrease sufficiently compared to Equation 4.

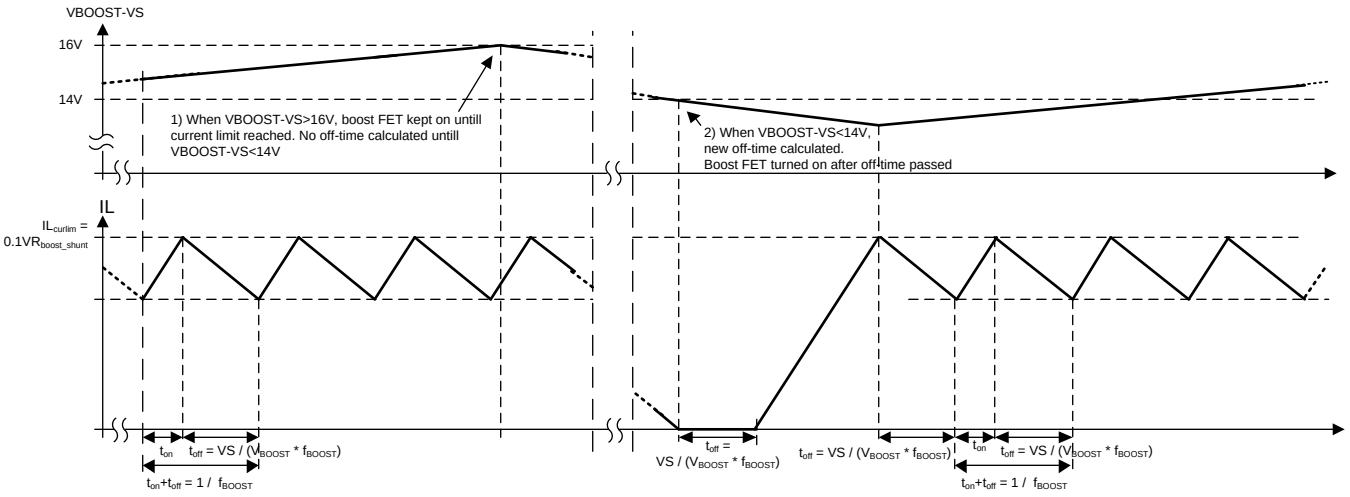


Figure 21. Boost Waveforms Showing Burst Pulsing Controlled by Hysteretic Comparator Levels

REVISION HISTORY

Changes from Revision B (March 2013) to Revision C **Page**

- Changed From: PWM Frequency up to 20kHz To: PWM Frequency up to 30kHz 1
- Changed min value for VS, negative voltages with external protection NMOS (DC) from -14 to -1. 3
- Changed min value for VS, negative voltages with external protection NMOS driven by device internal circuit (transient 1s) from -14 to -1. 3
- Changed I_{BOOST} to $V_{GS,HS,high}$, and corrected the cross reference. 3
- Changed $I_{BOOST,SW}$ to $V_{GS,LS,high}$, and corrected the cross reference. 3
- Added "Negative voltage with minimum serial resistor 5 Ω" to boost converter conditions. 3
- Added another row for "Negative voltage with external protection NMOS" to boost converter conditions. Added –1 to the min value, 60 to the max value, and V to the units. 3
- Changed min value for supply voltage for digital IOs, VDDIO from 1.72 to 2.7. 4
- Changed max value for VCC3 decoupling capacitance, $C_{\_VCC3}$ from 10 to 22, and moved typically 4.7 nF to the normal value. 4
- Changed max value for VCC5 decoupling capacitance, $C_{\_VCC5}$ from 10 to 470, and moved typically 4.7 nF to the nomal value. 4
- Moved I_{VSq}, I_{VSn}, VCC5 (internal supply voltage), and VCC3 (internal supply voltage) from the Recommended Operating Conditions table to Electrical Characteristics table. 5
- Moved typically 65mA (boost converter enabled) to the typical value, and corrected the cross reference. 5
- Moved I_{BOOST} and $I_{BOOST,sw}$ from the Recommended Operating Conditions table to the Electrical Characteristics table, and changed I_{BOOST} to I_{BOOSTn}. 6
- Added SCLK to conditions for INL, changed max value from 0.3 x VDDIO to 0.9. 7
- Added SCLK to conditions for INH, changed min value from 0.7 x VDDIO to 2.3. 7
- Added ENH parameter symbol, removed VDDIO = 3.3 V from parameter and conditions, changed min value from 2 to 0.65 x VDDIO, removed EN input high threshold VDDIO = 5 V row below. 7
- Removed EN from Input hysteresis conditions, added SCLK. Changed typ value from 0.4 to 0.8, changed max value from 0.78 to 1. 7
- Added row for EN input hysteresis with min typ and max values of 0.18 x VDDIO, 025 x VDDIO, and 0.48 x VDDIO, respectively. 7
- Changed t_{SHDOWN} to t_{TSD}. 20
- Updated connections and units in image 36
- Changed $I_{boost,sw}$ to $I_{boost,qg}$ in Equation 2. 38
- Corrected the cross reference 39
- Removed VS and V_{BOOST} from Equation 8. 40

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
DRV3201QPAPQ1	ACTIVE	HTQFP	PAP	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV3201	Samples
DRV3201QPAPRQ1	ACTIVE	HTQFP	PAP	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV3201	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

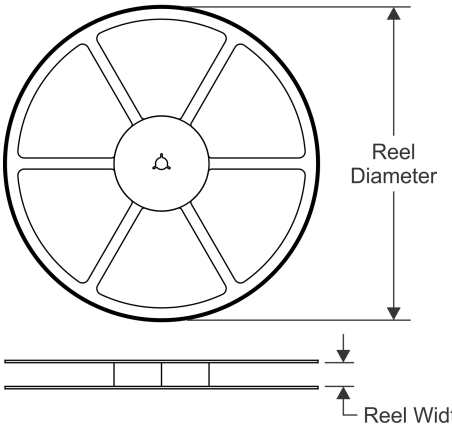
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

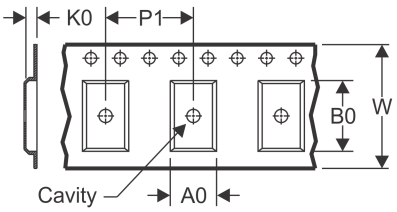
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

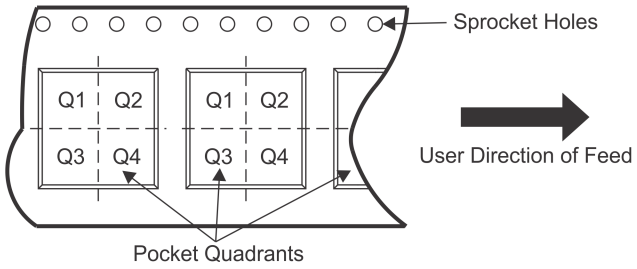


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

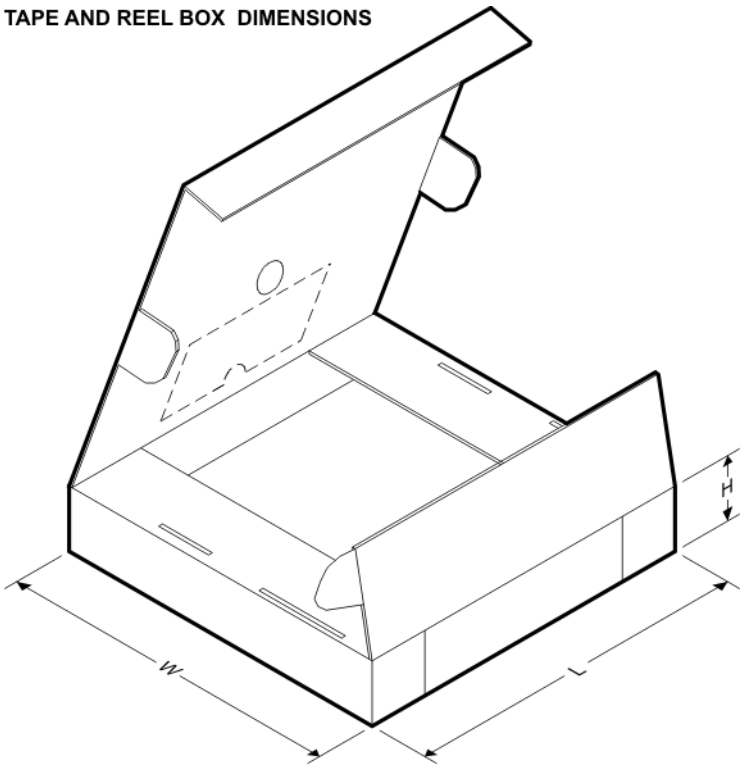
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV3201QPAPRQ1	HTQFP	PAP	64	1000	330.0	24.4	13.0	13.0	1.5	16.0	24.0	Q2

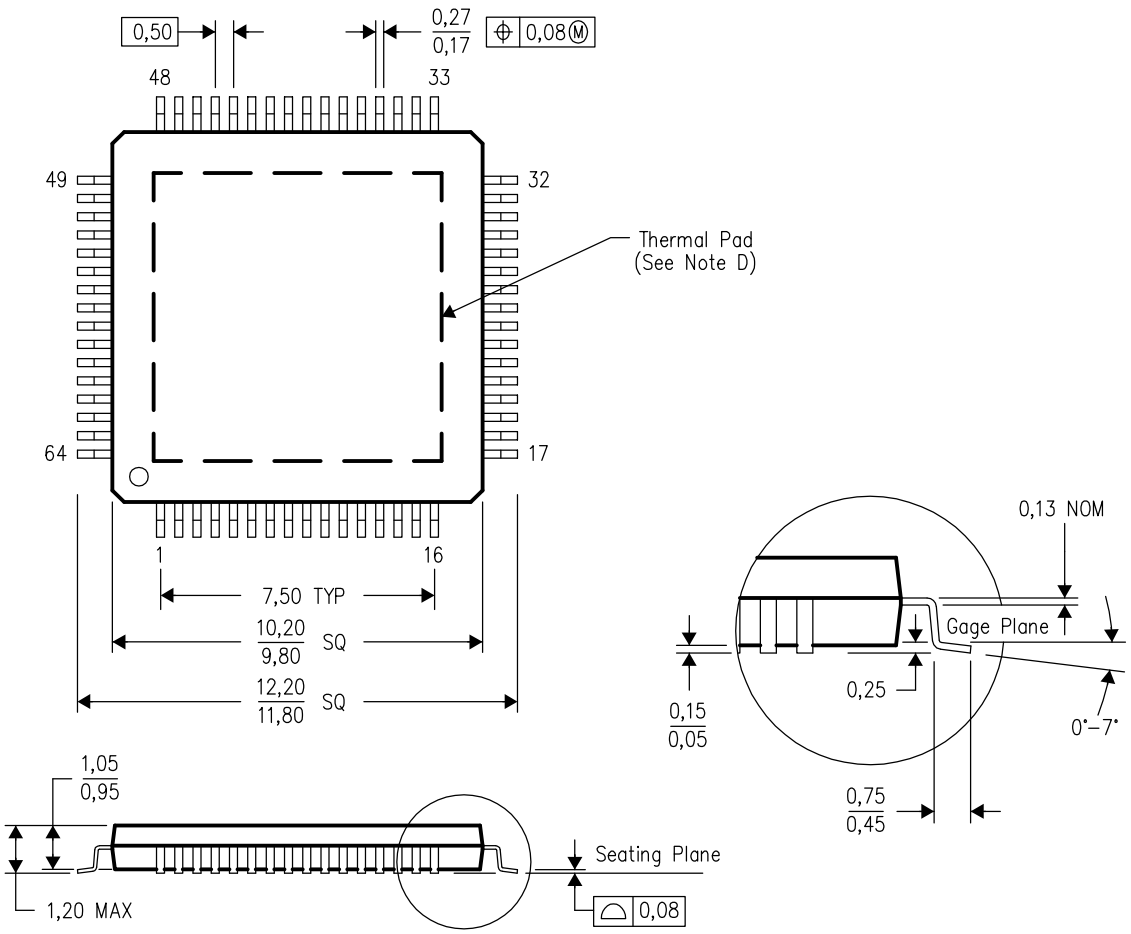
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV3201QPAPRQ1	HTQFP	PAP	64	1000	367.0	367.0	45.0

PAP (S–PQFP–G64) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MS–026

PowerPAD is a trademark of Texas Instruments.

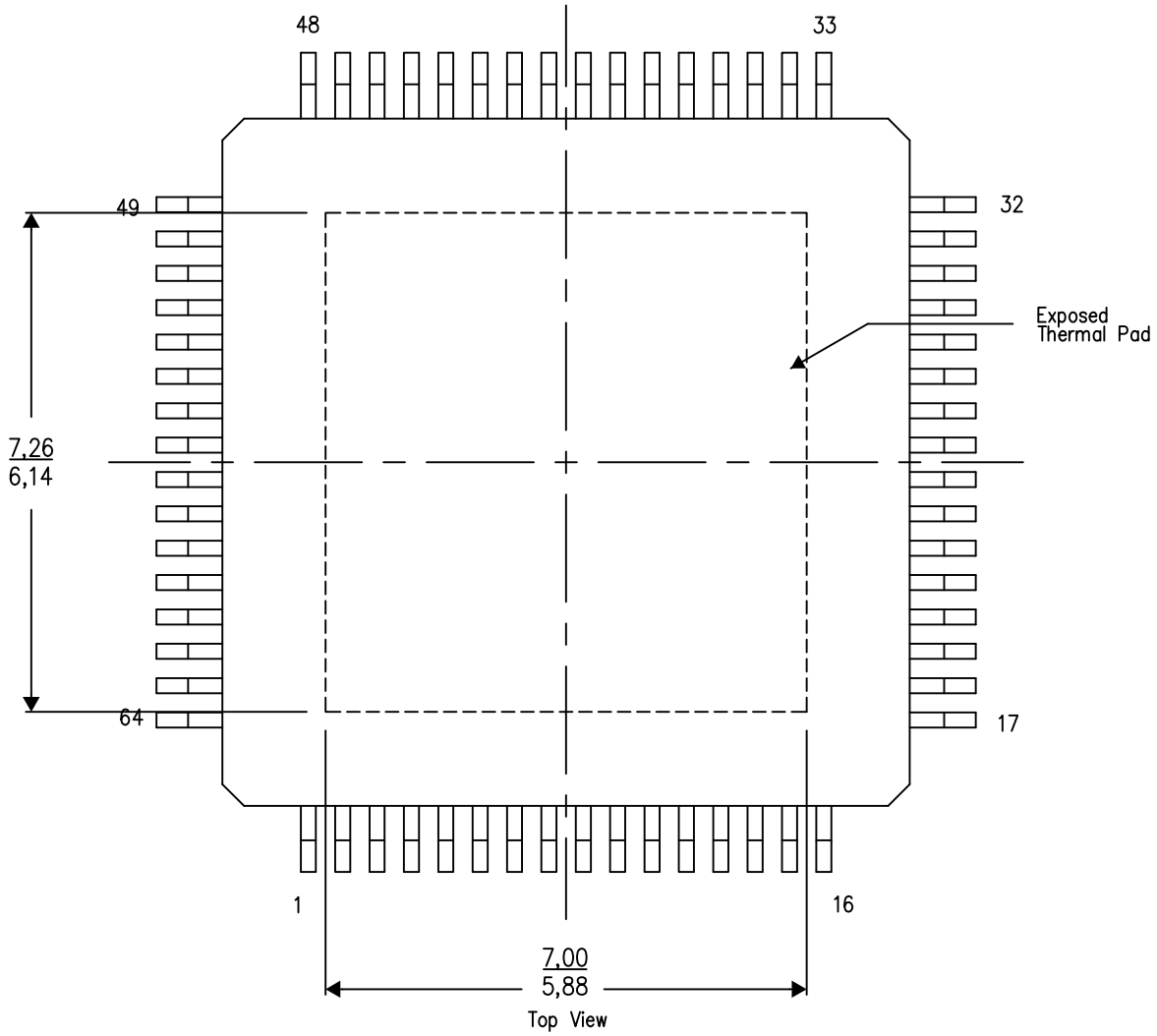
PAP (S–PQFP–G64) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



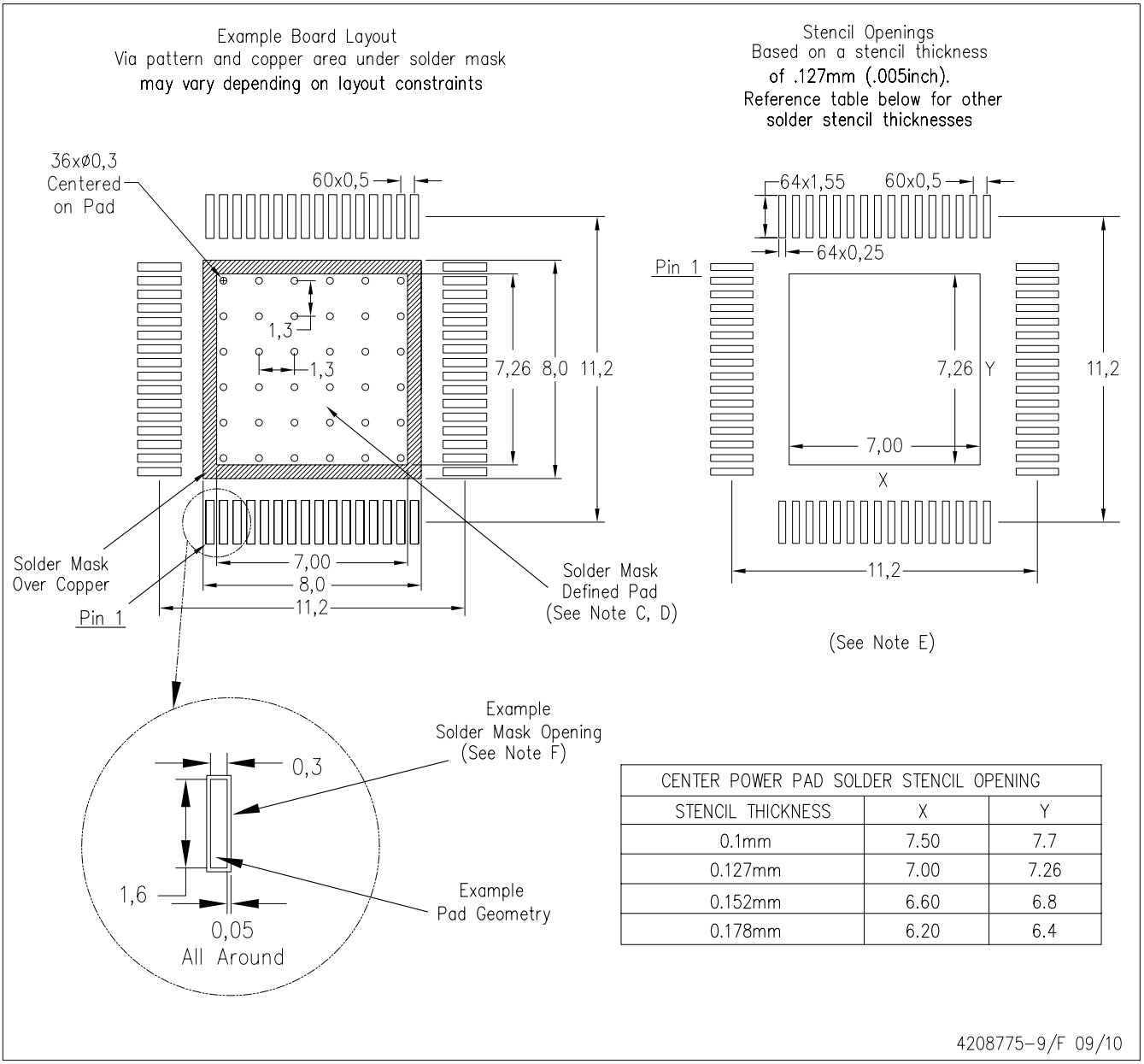
Exposed Thermal Pad Dimensions

4206326–9/N 02/13

NOTES: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

PAP (S–PQFP–G64) PowerPAD™ PLASTIC QUAD FLATPACK



CENTER POWER PAD SOLDER STENCIL OPENING		
STENCIL THICKNESS	X	Y
0.1mm	7.50	7.7
0.127mm	7.00	7.26
0.152mm	6.60	6.8
0.178mm	6.20	6.4

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265