2.95 V to 6 V INPUT, 6 A OUTPUT, 2 MHz, SYNCHRONOUS STEP DOWN SWITCHER WITH INTEGRATED FET (SWIFT™)

Check for Samples: TPS54678

FEATURES

- **Two 12 mΩ (typical) MOSFETs for High Efficiency 6 A Continuous Output Current**
- **200 kHz to 2 MHz Switching Frequency**
- **0.6 V ±1% Voltage Reference Over Temperature (-40°C to 150°C)**
- **Synchronizes to External Clock**
- **Start up with Pre-Biased Voltage**
- **Power Good Output**
- **Adjustable Slow Start and Sequencing**
- **Cycle-by-Cycle Current Limit and Hiccup Current Protection**
- **Adjustable Input Voltage UVLO**
- **Thermally Enhanced 16-Pin 3 mm x 3 mm QFN (RTE)**

APPLICATIONS

- **Low-Voltage, High-Density Power Systems**
- **Point of Load Regulation for High Performance DSPs, FPGAs, ASICs and Microprocessors**
- **Broadband, Networking and Optical**
- **Communications Infrastructure**
- **Gaming, DTV and Set-Top Boxes**

DESCRIPTION

TPS54678 device is a full featured 6 V, 6 A, synchronous step down current mode converter with two integrated MOSFETs.

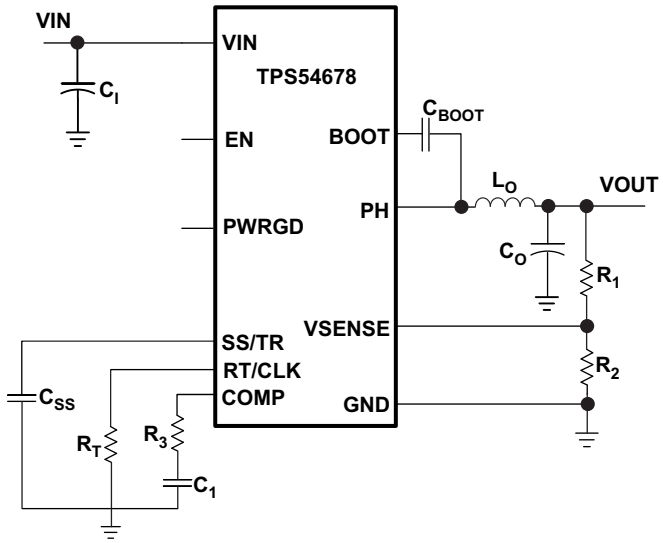
TPS54678 enables small designs by integrating the MOSFETs, implementing current mode control to reduce external component count, reducing inductor size by enabling up to 2 MHz switching frequency, and minimizing the IC footprint with a small 3 mm x 3 mm thermally enhanced QFN package.

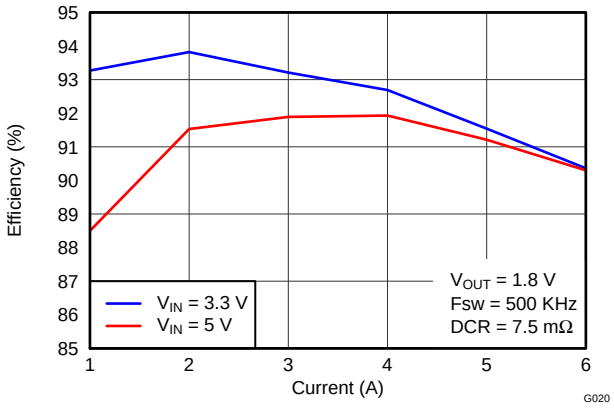
TPS54678 provides accurate regulation for a variety of loads with an accurate ±1% Voltage Reference (V_{REF}) over temperature.

Efficiency is maximized through the integrated 12 mΩ MOSFETs. Using the enable pin, shutdown supply current is reduced by disabling the device.

The output voltage startup ramp is controlled by the soft start pin that can also be configured for sequencing or tracking. Monotonic startup is achieved with pre-biased voltage. Under voltage lockout can be increased by programming the threshold with a resistor divider on the enable pin. An open drain power good signal indicates the output is within 93% to 105% of its nominal voltage.

Cycle-by-cycle current limit, hiccup overcurrent protection and thermal shutdown protect the device during an overcurrent condition.





Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_J	PACKAGE	PART NUMBER
-40°C to 150°C	3 x 3 mm QFN	TPS54678RTE

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE		UNIT
		MIN	MAX	
Input Voltage	VIN	-0.3	7	V
	EN	-0.3	7	V
	BOOT		PH + 7	V
	VSENSE	-0.3	3	V
	COMP	-0.3	3	V
	PWRGD	-0.3	6	V
	SS/TR	-0.3	3	V
	RT/CLK	-0.3	6	V
Output Voltage	BOOT-PH		7	V
	PH	-0.7	7	V
	PH 20ns Transient	-2	10	V
	PH 5ns Transient	-4	12	V
Source Current	EN		100	µA
	RT/CLK		100	µA
Sink Current	COMP		100	µA
	PWRGD		10	mA
	SS/TR		100	µA
Electrostatic Discharge	Human Body Model (HBM)		2	kV
	Charged device Model (CDM)		500	V
Operating Junction Temperature		-40	150	ºC
Storage Temperature		-65	150	ºC

(1) Stresses beyond those listed under “ABSOLUTE MAXIMUM RATINGS” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “ELECTRICAL SPECIFICATIONS” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability

THERMAL INFORMATION

THERMAL METRIC(1)		TPS54678	UNITS
		RTE (16 PINS)	
θ_{JA}	Junction-to-ambient thermal resistance	43.2	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	38.5	
θ_{JB}	Junction-to-board thermal resistance	14.5	
ψ_{JT}	Junction-to-top characterization parameter	0.4	
ψ_{JB}	Junction-to-board characterization parameter	14.5	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	3.4	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

ELECTRICAL CHARACTERISTICS

T_J = –40°C to +150°C, VIN = 2.95 to 6 V (unless otherwise noted)

DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN PIN)					
Operating Input Voltage		2.95		6	V
Shutdown Supply Current	EN = 0 V, 25°C, 2.95 V ≤ VIN ≤ 6 V		1	3	µA
Operating– Non switching Supply Current	VSENSE = 0.6 V, VIN = 5 V, 25°C, f_{SW} = 500 kHz		570	800	µA
ENABLE AND UVLO (EN PIN)					
Enable threshold	Rising		1.3		V
Enable threshold	Falling		1.18		V
Input current	Enable threshold + 50 mV		-3.5		µA
Input current	Enable threshold – 50 mV		-0.70		µA
VOLTAGE REFERENCE					
Voltage Reference	2.95 V ≤ VIN ≤ 6 V, –40°C < T_J < 150°C	0.594	0.600	0.606	V
MOSFET					
High Side Switch Resistance	BOOT-PH = 5 V		12	25	mΩ
High Side Switch Resistance	BOOT-PH = 2.95 V		17	33	
Low Side Switch Resistance	BOOT-PH = 5 V		12	25	mΩ
Low Side Switch Resistance	BOOT-PH = 2.95 V		17	33	
ERROR AMPLIFIER					
Input Current			7		nA
Error amplifier Transconductance (gm)	–2 µA < $I_{(COMP)}$ < 2 µA $V_{(COMP)}$ = 1 V		245		umhos
Error amplifier Transconductance (gm) during slow start	–2 µA < $I_{(COMP)}$ < 2 µA $V_{(COMP)}$ = 1 V, $V_{(VSENSE)}$ = 0.4 V		80		umhos
Error amplifier source and sink	$V_{(COMP)}$ = 1V 100 mV Overdrive		±20		µA
COMP to I_{switch} gm			20		A/V
CURRENT LIMIT					
Current limit threshold	Fs = 500 KHz	9.5	10.5	11.5	A
Cycles before entering hiccup during OC			512		cycles
Hiccup cycles			16384		cycles
Low side sourcing current threshold		7	8.5	10.5	A
Low side Fet reverse current protection			4		A
THERMAL SHUTDOWN					
Thermal Shutdown			170		°C
Hysteresis			15		°C
TIMING RESISTOR AND EXTERNAL CLOCK (RT/CLK PIN)					
Switching Frequency Range using RT mode		200		2000	kHz
Switching Frequency	R_t = 82.5 kΩ	400	500	600	kHz
Switching Frequency Range using CLK mode		300		2000	kHz
Minimum CLK Pulse width			75		ns
RT/CLK voltage	$R_{(RT/CLK)}$ = 82.5 kΩ		0.5		V
RT/CLK high threshold			1.6	2.2	V
RT/CLK low threshold		0.4	0.6		V
RT/CLK falling edge to PH rising edge delay	Measure at 500 kHz with RT resistor in series		55		ns
PLL lock in time	Measure at 500 kHz		40		us

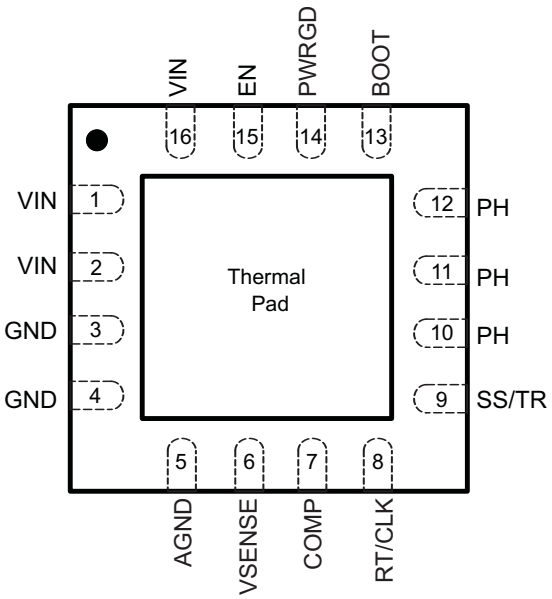
ELECTRICAL CHARACTERISTICS (continued)

T_J = –40°C to +150°C, VIN = 2.95 to 6 V (unless otherwise noted)

DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
PH (PH PIN)					
Minimum On time	Measured at 50% points on PH. I_{OUT} = 3 A		85	110	ns
	Measured at 50% points on PH. I_{OUT} = 0 A		100		ns
Minimum Off time	Prior to skipping off pulses, BOOT-PH = 3 V, I_{OUT} = 3 A		70		ns
Rise and fall dV/dT	BOOT-PH = 3V; I_O = 6 A		1.5		V/ns
BOOT (BOOT PIN)					
Charging Resistor	VIN = 6V, BOOT-PH = 6 V		7		Ω
BOOT-PH UVLO	VIN = 3.3 V		2.2		V
SLOW START AND TRACKING (SS/TR PIN)					
Charge Current	$V_{(SS/TR)}$ < 0.15 V		47		µA
	$V_{(SS/TR)}$ > 0.15 V		2.2		
SS/TR to VSENSE matching	V_{IN} = 3.3 V		60		mV
SS/TR to Reference Crossover	98% nominal		0.8		V
SS/TR Discharge Voltage (Overload)	VSENSE = 0 V		4.5		mV
SS/TR Discharge to current (Overload)	VSENSE = 0 V; $V_{(SS/TR)}$ = 4 V;		95		µA
SS/TR Discharge Current (UVLO, EN, Thermal Fault)	V_{IN} = 3 V; $V_{(SS/TR)}$ = 4 V;		925		µA
POWER GOOD (PWRGD PIN)					
VSENSE Threshold	VSENSE falling (Fault)		91		% V_{REF}
	VSENSE rising (Good)		93		% V_{REF}
	VSENSE rising (Fault)		105		% V_{REF}
	VSENSE falling (Good)		103		% V_{REF}
Output high leakage	VSENSE = V_{REF}, $V_{(PWRGD)}$ = 5.5 V		2		nA
On Resistance	V_{IN} = 5 V		65	120	Ω
Output low	$I_{(PWRGD)}$ = 2.5 mA		0.2	0.3	V
Minimum VIN for valid output	$V_{(PWRGD)}$ < 0.5V at 100 µA		1.2	1.5	V

DEVICE INFORMATION

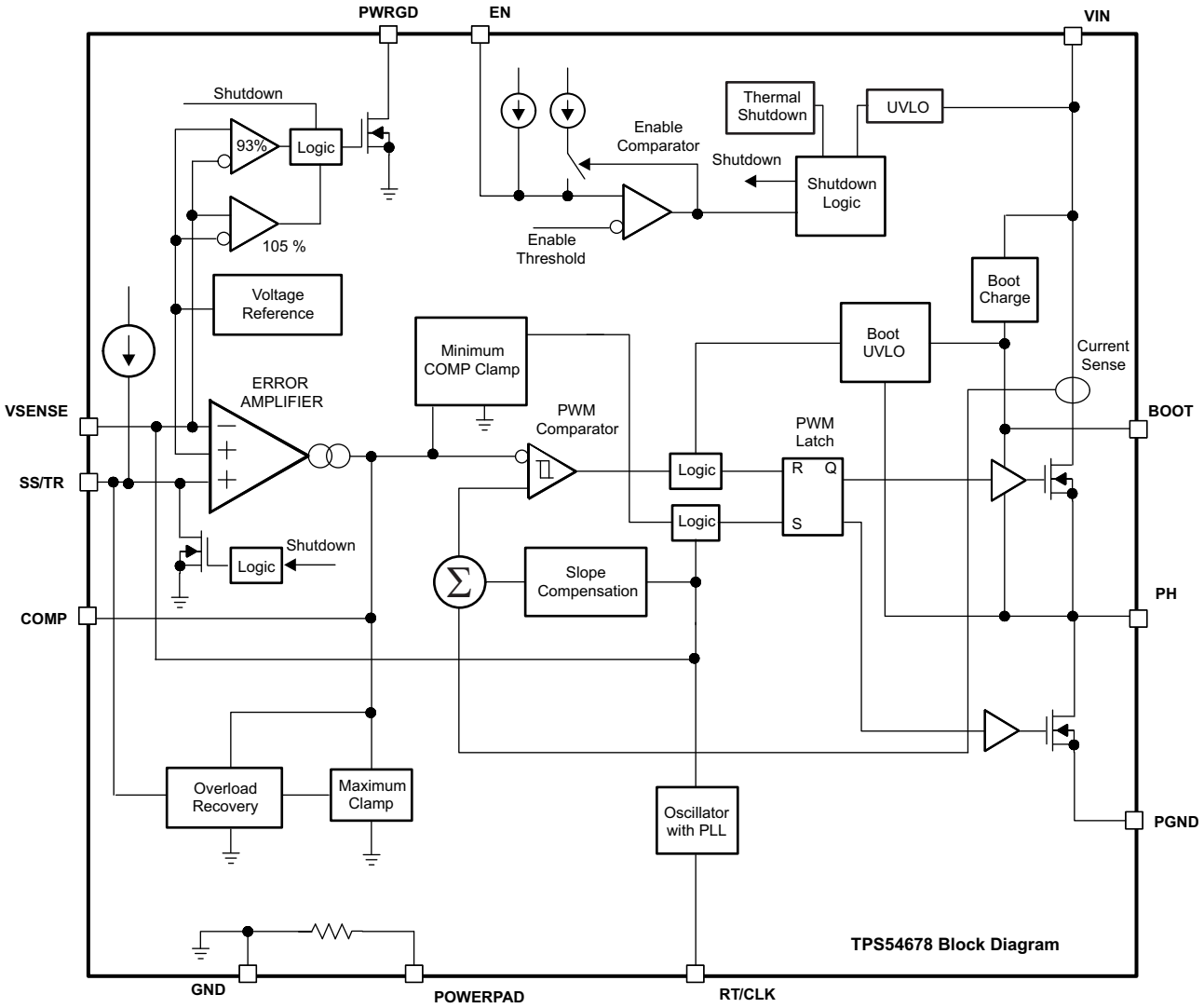
RTE PACKAGE
(TOP VIEW)



PIN FUNCTIONS

PIN NAME	NUMBER	DESCRIPTION
AGND	5	Analog Ground should be tied to GND close to the device.
BOOT	13	A bootstrap capacitor is required between BOOT and PH. If the voltage on this capacitor is below the minimum required by the output device, the output is forced to switch off until the capacitor is refreshed.
COMP	7	Error amplifier output, and input to the output switch current comparator. Connect frequency compensation components to this pin.
EN	15	Enable pin, internal pull-up current source. Pull below 1.18 V to disable. Float to enable. Adjust the input under voltage lockout with two additional resistors.
GND	3, 4	Ground. This pin should be tied directly to the power pad under the IC.
PH	10, 11, 12	The source of the internal high side power MOSFET, and drain of the internal low side (synchronous)MOSFET.
PowerPAD™	17	GND pin must be connected to the exposed power pad for proper operation. This power pad should be connected to any internal PCB ground plane using multiple vias.
PWRGD	14	An open drain output. Active if output voltage is low due to thermal shutdown, dropout, over-voltage or EN shut down.
RT/CLK	8	Resistor Timing and External Clock input pin.
SS/TR	9	Slow-start and Tracking. An external capacitor connected to this pin sets the output rise time. Since the voltage on this pin overrides the internal reference, it can be used for tracking and sequencing.
VIN	1, 2, 16	Input supply voltage, 2.95 V to 6 V.
VSENSE	6	Inverting node of the (gm) error amplifier.

FUNCTIONAL BLOCK DIAGRAM



Overview

The TPS54678 is a 6-V, 6-A, synchronous step-down (buck) converter with two integrated n-channel MOSFETs. To improve the performance during line and load transients the device implements a constant frequency, peak current mode control which reduces output capacitance and simplifies external frequency compensation design. The wide switching frequency range of 200 kHz to 2000 kHz allows for efficiency and size optimization when selecting the output filter components. The switching frequency is adjusted using a resistor to ground on the RT/CLK pin. The device has an internal phase lock loop (PLL) on the RT/CLK pin that is used to synchronize the power switch turn on to a falling edge of an external system clock.

The TPS54678 has a typical default start up voltage of 2.4 V. The EN pin has an internal pull-up current source that can be used to adjust the input voltage under voltage lockout (UVLO) with two external resistors. In addition, the pull up current provides a default condition when the EN pin is floating for the device to operate. The total operating current for the TPS54678 is typically 570 µA when not switching and under no load. When the device is disabled, the supply current is less than 3 µA.

The integrated 12 mΩ MOSFETs allow for high efficiency power supply designs with continuous output currents up to 6 amperes. The TPS54678 reduces the external component count by integrating the boot recharge diode. The bias voltage for the integrated high side MOSFET is supplied by a capacitor between the BOOT and PH pins. The boot capacitor voltage is monitored by an UVLO circuit and turns off the high side MOSFET when the voltage falls below a preset threshold. This BOOT circuit allows the TPS54678 to operate approaching 100%. The output voltage can be stepped down to as low as the 0.60 V reference.

TPS54678 features monotonic startup under pre-bias conditions. The low side Fet turns on for a short time period every cycle before the output voltage reaches the pre-biased voltage. This ensures the boot cap has enough charge to turn on the top Fet when the output voltage reaches the pre-biased voltage.

The TPS54678 has a power good comparator (PWRGD) with 2% hysteresis.

The TPS54678 minimizes excessive output overvoltage transients by taking advantage of the overvoltage power good comparator. When the regulated output voltage is greater than 105% of the nominal voltage, the overvoltage comparator is activated, and the high side MOSFET is turned off and masked from turning on until the output voltage is lower than 103%.

The SS/TR (slow start or tracking) pin is used to minimize inrush currents or provide power supply sequencing during power up. A small value capacitor should be coupled to the pin for slow start. The SS/TR pin is discharged before the output power up to ensure a repeatable restart after an overtemperature fault, UVLO fault or disabled condition. To optimize the output startup waveform, two levels of SS current are implemented.

To reduce the power dissipation of TPS54678 during overcurrent event, the hiccup protection is implemented beyond the cycle-by-cycle protection.

DETAILED DESCRIPTION

Fixed Frequency PWM Control

The TPS54678 uses a settable fixed frequency, peak current mode control. The output voltage is compared through external resistors on the VSENSE pin to an internal voltage reference by an error amplifier which drives the COMP pin. An internal oscillator initiates the turn on of the high side power switch. The error amplifier output is compared to the high side power switch current. When the power switch current reaches the COMP voltage level the high side power switch is turned off and the low side power switch is turned on. The COMP pin voltage will increase and decrease as the output current increases and decreases. The device implements a current limit by clamping the COMP pin voltage to a maximum level and implements a sleep mode with a minimum clamp.

Slope Compensation and Output Current

The TPS54678 adds a compensating ramp to the switch current signal. This slope compensation prevents sub-harmonic oscillations. The available peak inductor current maintains constant over the full duty cycle range.

Bootstrap Voltage (BOOT) and Low Dropout Operation

The TPS54678 has an integrated boot regulator and requires a small ceramic capacitor between the BOOT and PH pin to provide the gate drive voltage for the high side MOSFET. The value of the ceramic capacitor should be 0.1 µF. A ceramic capacitor with an X7R or X5R grade dielectric is recommended because of the stable characteristics over temperature and voltage.

To improve drop out, the TPS54678 is designed to operate at 100% duty cycle as long as the BOOT to PH pin voltage is greater than 2.2 V. The high side MOSFET is turned off using an UVLO circuit, allowing for the low side MOSFET to conduct, when the voltage from BOOT to PH drops below 2.2 V. Since the supply current sourced from the BOOT pin is low, the high side MOSFET can remain on for more switching cycles than are required to refresh the capacitor, thus the effective duty of the switching regulator is high.

Error Amplifier

The TPS54678 has a transconductance amplifier for the error amplifier. The error amplifier compares the VSENSE voltage to the lower of the SS/TR pin voltage or the internal 0.6 V voltage reference. The transconductance of the error amplifier is 245 µA/V during normal operation. During the slow start operation, the transconductance is a fraction of the normal operating gm. The frequency compensation components are added to the COMP pin to ground.

Voltage Reference

The voltage reference system produces a precise ±1% voltage reference over temperature by scaling the output of a temperature stable bandgap circuit. During production, the bandgap and scaling circuits are trimmed to produce 0.6 V at the amplifier output.

Adjusting the Output Voltage

The output voltage is set with a resistor divider from the output node to the VSENSE pin. It is recommended to use 1% tolerance or better divider resistors. Start with a 20 KΩ for the R1 resistor and use the Equation 1 to calculate R2. To improve efficiency at light loads consider using larger value resistors. If the values are too high the regulator will be more susceptible to noise and voltage errors from the VSENSE input current will be noticeable.

$$R2 = R1 \times \left(\frac{0.6\ V}{V_O - 0.6\ V} \right) \quad (1)$$

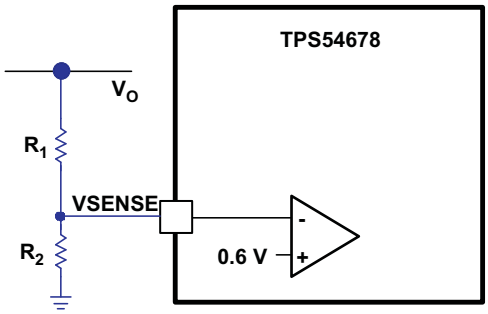


Figure 1. Voltage Divider Circuit

Enable and Set Up Adjusting Undervoltage Lockout

The EN pin provides electrical on and off control of the device. Once the EN pin voltage exceeds the threshold voltage, the device starts operation. If the EN pin voltage is pulled below the threshold voltage, the regulator stops switching and enters low Iq state. If an application requires controlling the EN pin, use open drain or open collector output logic to interface with the pin.

For input undervoltage lockout (UVLO), use the EN pin as shown in Figure 2 to set up the UVLO by using the two external resistors. Once the EN pin voltage exceeds 1.3 V, an additional 2.8 µA of hysteresis is added. This additional current facilitates input voltage hysteresis. Use Equation 2 to set the external hysteresis for the input voltage. Use Equation 3 to set the input startup voltage. It is recommended that the minimum input shutdown voltage be set at 2.45 V or higher to ensure proper operation before shutdown.

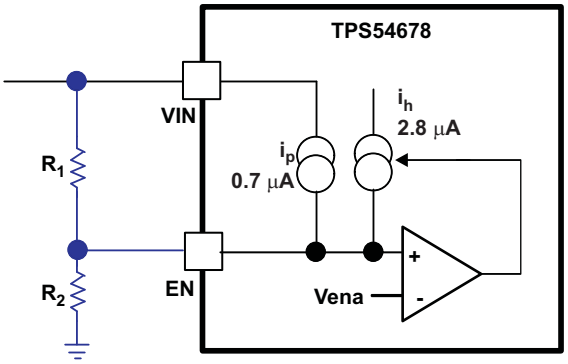


Figure 2. Set Up Input Undervoltage Lock Out.

$$R1 = \frac{V_{START}\left(\frac{V_{EN\_FALLING}}{V_{EN\_RISING}}\right) - V_{STOP}}{I_p\left(1 - \frac{V_{EN\_FALLING}}{V_{EN\_RISING}}\right) + I_h} \quad (2)$$

$$R2 = \frac{R1 \times V_{EN\_FALLING}}{V_{STOP} - V_{EN\_FALLING} + R1 \times (I_p + I_h)} \quad (3)$$

Where R_1 and R_2 are in Ω, I_h = 2.8 µA, I_p = 0.7 µA, V_{EN_RISING} = 1.3 V, $V_{EN\_FALLING}$ = 1.18 V.

Slow Start or Tracking Pin (SS/TR)

TPS54678 effectively uses the lower voltage of the internal voltage reference or the SS/TR pin voltage as the power supply's reference voltage and regulates the output accordingly. A capacitor on the SS/TR pin to ground will implement a slow start time. The TPS54678 has an internal pull-up current source of 47 µA when $V_{(SS/TR)}$ is less than 0.15 V and 2.2 µA when $V_{(SS/TR)}$ is higher than 0.15 V. The I_{SS} charges the external slow start capacitor. The equation for the slow start time is shown in Equation 4 considering the fact the first 47 µA charges the SS to 0.15 V. The 2.2 µA then charges the SS from 0.15 V to about 0.8 V for the handoff of the SS voltage to reference voltage.

$$Css(nF) = 3 \times Tss(mS) \quad (4)$$

If during normal operation, the VIN UVLO is exceeded, EN pin pulled below 1.2 V, or a thermal shutdown event occurs, the TPS54678 will stop switching and the SS/TR must be discharged to about 60 mV before reinitiating a powering up sequence.

The VSENSE voltage will follow the SS/TR pin voltage up to 90% of the internal voltage reference. When the SS/TR voltage is greater than 90% of the internal voltage, the effective system reference voltage will transit from the SS/TR voltage to the internal voltage reference.

Sequencing

Many of the common power supply sequencing methods can be implemented using the SS/TR, EN and PWRGD pins. The sequential method can be implemented using an open drain or collector output of a power on reset pin of another device. The sequential method is illustrated in Figure 3. The power good is coupled to the EN pin on the TPS54678 which will enable the second power supply once the primary supply reaches regulation.

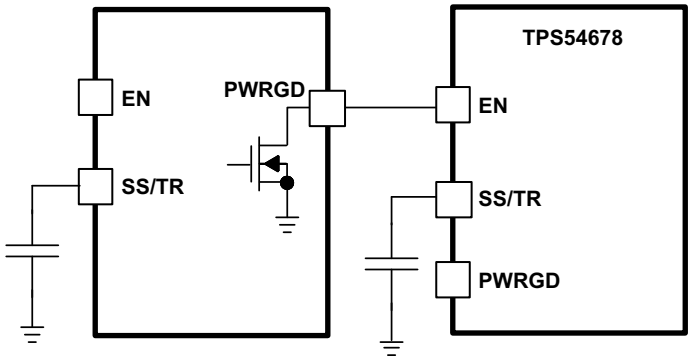


Figure 3. Sequential Start-Up Sequence

Constant Switching Frequency and Timing Resistor (RT/CLK Pin)

The switching frequency of the TPS54678 is adjustable over a wide range from approximately 200 kHz to 2000 kHz by placing a maximum of 210 kΩ and minimum of 18 kΩ, respectively, on the RT/CLK pin. The RT/CLK is typically 0.5 V. To determine the timing resistance for a given switching frequency, use the curve in Figure 4. To reduce the solution size one would typically set the switching frequency as high as possible, but tradeoffs of the supply efficiency, maximum input voltage and minimum controllable on time should be considered.

The minimum controllable on time is typically 85 ns at 3 A current load and 100 ns at no load, and will limit the maximum operating input voltage or output voltage.

$$R_T(k\Omega) = \frac{56183}{\left[F_{SW}(KHz)\right]^{1.052}} \quad (5)$$

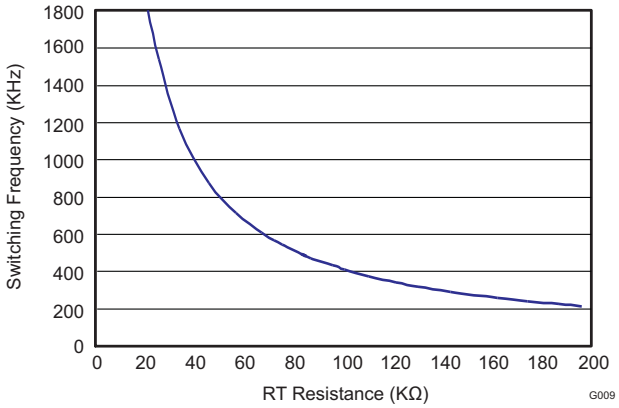


Figure 4. Switching Frequency vs RT Set Resistor

Overcurrent Protection

The TPS54678 implements current mode control which uses the COMP pin voltage to turn off the high side MOSFET and turn on the low side MOSFET on a cycle-by-cycle basis. Each cycle the switch current and the COMP pin voltage are compared, when the peak switch current intersects the COMP voltage the high side switch is turned off.

High-Side Overcurrent Protection

During overcurrent conditions that pull the output voltage low, the error amplifier will respond by driving the COMP pin high, increasing the switch current. The error amplifier output is clamped internally. This clamp functions as a high-side switch current limit. When the high-side switch current limit occurs consecutively for 512 CLK cycles, the converter enters hiccup mode in which no switching action happens for about 16000 cycles. This helps to reduce the power consumption during an overcurrent event.

Low-Side Overcurrent Protection

The low-side MOSFET's conduction current is also monitored by TPS54678. During normal operation, the low-side sources current into the load. When the sourcing current reaches the internally set low-side sourcing (forward) current limit, the high-side is not turned on and skipped during the next clock cycle. Under this condition, the low-side is kept on until the sourcing current becomes less than the internally set current limit and then the high-side is turned on at the beginning of the following clock cycle. This ensures protection under an output short condition; thereby, preventing current run-away.

The low-side can also sink current from the load. If the low-side sinking (reverse) current limit is exceeded, the low-side is turned off immediately for the rest of the clock cycle. Under this condition, both the high-side and low-side are off until the start of the next cycle.

Safe Start-Up into Pre-Biased Outputs

The TPS54678 allows monotonic startup into pre-biased output. The low side Fet turns on for a short time period every cycle before the output voltage reaches the pre-biased voltage. This ensures the boot cap has enough charge to turn on the top Fet when the output voltage reaches the pre-biased voltage.

The TPS54678 also implements low side current protection by detecting the voltage over the low side MOSFET. When the converter sinks current through the low side FET and if the current exceeds 4 A, the control circuit turns the low side Fet off. Due to the implemented prebias function, the low side Fet reverse current protection should not be reached, but it provides another layer of protection.

Synchronize using the RT/CLK pin

The RT/CLK pin is used to synchronize the converter to an external system clock. See Figure 5. To implement the synchronization feature in a system connect a square wave to the RT/CLK pin with on time at least 75 ns. The square wave amplitude at this pin must transition lower than 0.6 V and higher than 1.6 V. The synchronization frequency range is 300 kHz to 2000 kHz. The rising edge of the PH will be synchronized to the falling edge of RT/CLK pin.

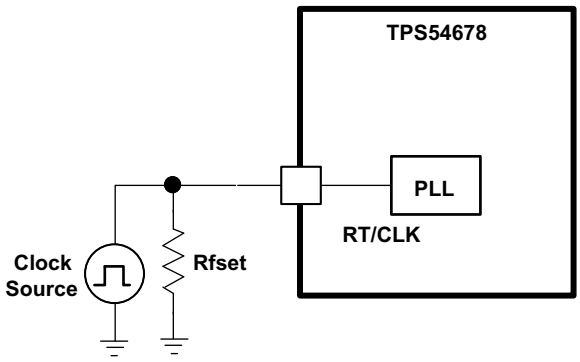


Figure 5. Synchronizing to a System Clock

Power Good (PWRGD Pin)

The PWRGD pin is an open drain output and pulls the PWRGD pin low when the VSENSE voltage is less than 91% or greater than 105% of the nominal internal reference voltage.

There is a 2% hysteresis, so once the VSENSE pin is within 93% to 103% of the internal voltage reference the PWRGD pin is de-asserted and the pin floats. It is recommended to use a pull-up resistor between the values of 1 kΩ and 100 kΩ to a voltage source that is 5.5 V or less. The PWRGD is in a valid state once the VIN input voltage is greater than 1.2 V.

Overvoltage Transient Protection

The TPS54678 incorporates an overvoltage transient protection (OVTP) circuit to minimize voltage overshoot when recovering from output fault conditions or strong unload transients. The OVTP feature minimizes the output overshoot by implementing a circuit to compare the VSENSE pin voltage to OVTP threshold which is 105% of the internal voltage reference. If the VSENSE pin voltage is greater than the OVTP threshold, the high side MOSFET is disabled preventing current from flowing to the output and minimizing output overshoot. When the VSENSE voltage drops lower than the OVTP threshold the high side MOSFET is allowed to turn on the next clock cycle.

Thermal Shutdown

The device implements an internal thermal shutdown to protect itself if the junction temperature exceeds 170°C. The thermal shutdown forces the device to stop switching when the junction temperature exceeds thermal trip threshold. Once the die temperature decreases below 155°C, the device reinitiates the power up sequence by discharging the SS/TR pin to about 60 mV. The thermal shutdown hysteresis is 15°C.

Small Signal Model for Loop Response

The Figure 6 shows an equivalent model for the TPS54678 control loop which can be modeled in a circuit simulation program to check frequency response and dynamic load response. The error amplifier is a transconductance amplifier with a gm of 245 µA/V. The error amplifier can be modeled using an ideal voltage controlled current source. The resistor R_O and capacitor C_O model the open loop gain and frequency response of the amplifier.

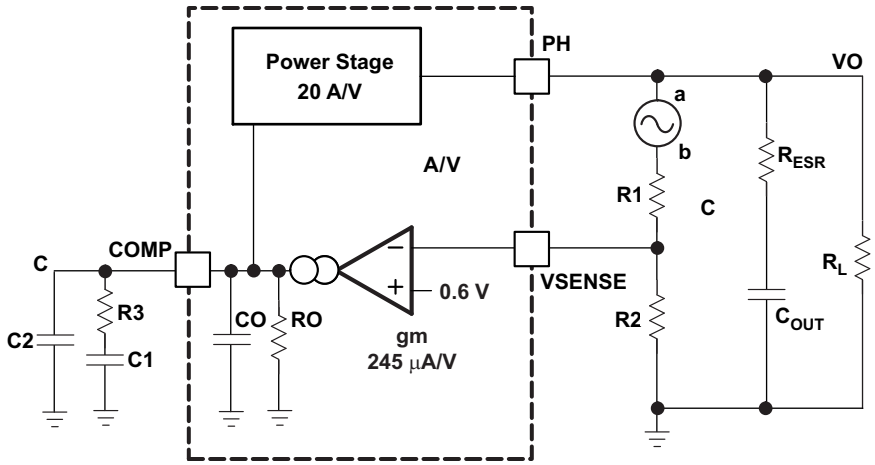


Figure 6. Small Signal Model for Loop Response

Simple Small Signal Model for Peak Current Mode Control

Figure 6 is a simple small signal model that can be used to understand how to design the frequency compensation. The TPS54678 power stage can be approximated to a voltage controlled current source (duty cycle modulator) supplying current to the output capacitor and load resistor. The control to output transfer function is shown in Equation 6 and consists of a dc gain, one dominant pole and one ESR zero. The quotient of the change in switch current and the change in COMP pin voltage (node c in figure) is the power stage transconductance. The gm for the TPS54678 is 20 A/V. The low frequency gain of the power stage frequency response is the product of the transconductance and the load resistance as shown in Equation 7. As the load current increases and decreases, the low frequency gain decreases and increases, respectively. This variation with load may seem problematic at first glance, but fortunately the dominant pole moves with load current (see Equation 8). The combined effect is highlighted by the dashed line in the right half of Figure 7. As the load current decreases, the gain increases and the pole frequency lowers, keeping the 0-dB crossover frequency the same for the varying load conditions which makes it easier to design the frequency compensation.

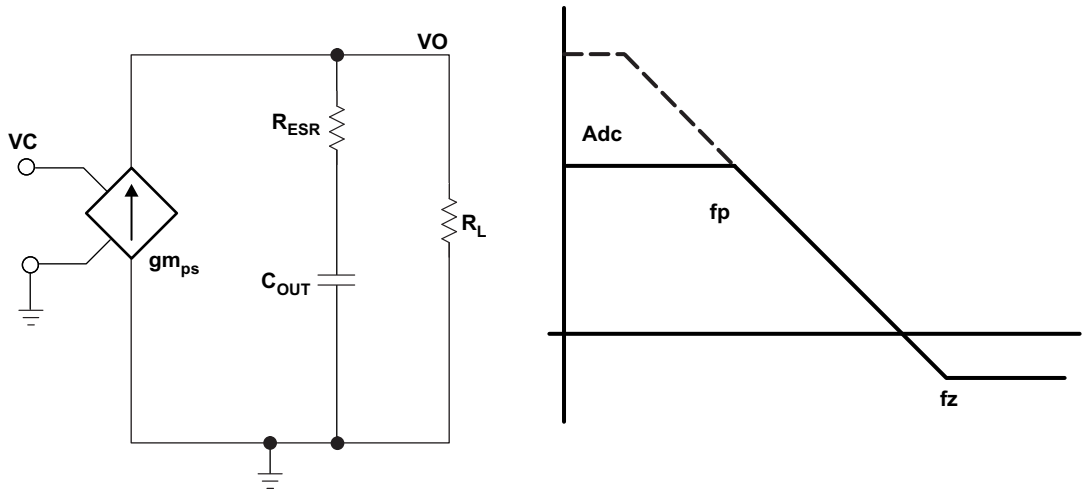


Figure 7. Simple Small Signal Model and Frequency Response for Peak Current Mode Control

$$\frac{V_O}{V_C} = Adc \times \frac{\left(1 + \frac{s}{2\pi \times fz}\right)}{\left(1 + \frac{s}{2\pi \times fp}\right)} \quad (6)$$

$$Adc = gm_{ps} \times R_L \quad (7)$$

$$fp = \frac{1}{C_{OUT} \times R_L \times 2\pi} \quad (8)$$

$$fz = \frac{1}{C_{OUT} \times R_{ESR} \times 2\pi} \quad (9)$$

Small Signal Model for Frequency Compensation

The TPS54678 uses a transconductance amplifier for the error amplifier and readily supports two of the commonly used frequency compensation circuits. The compensation circuits are shown in Figure 8. The Type 2 circuits are normally implemented in high bandwidth power supply designs using low ESR output capacitors. In Type 2A, one additional high frequency pole is added to attenuate high frequency noise.

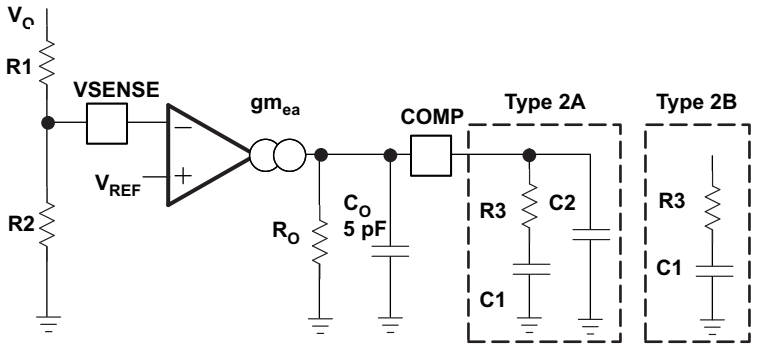


Figure 8. Types of Frequency Compensation

The design guidelines for TPS54678 loop compensation are as follows:

1. Set up cross over frequency fc.
2. R3 can be determined by

$$R3 = \frac{2\pi \times fc \times V_O \times C_{OUT}}{gm_{ea} \times V_{REF} \times gm_{ps}} \quad (10)$$

   Where gm_{ea} is the GM amplifier gain, gm_{PS} is the power stage gain (20 A/V).

3. Place a compensation zero at the dominant pole $fp = \frac{1}{C_{OUT} \times R_L \times 2\pi}$ C1 can be determined by

$$C1 = \frac{R_L \times C_{OUT}}{R3} \quad (11)$$

4. C2 is optional. It can be used to cancel the zero from Co's ESR.

$$C2 = \frac{R_{ESR} \times C_{OUT}}{R3} \quad (12)$$

Typical Characteristics

SHUTDOWN SUPPLY CURRENT vs TEMPERATURE

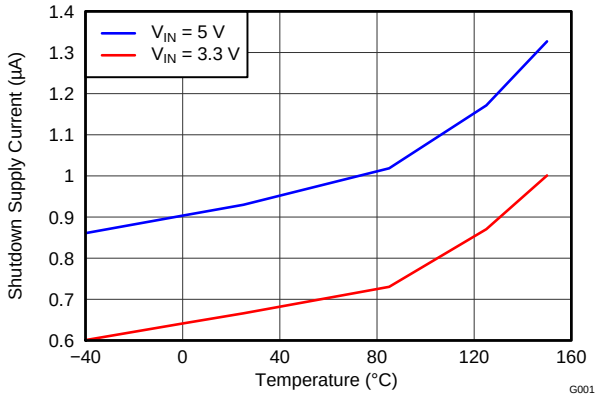


Figure 9.

VIN OPERATING CURRENT vs TEMPERATURE

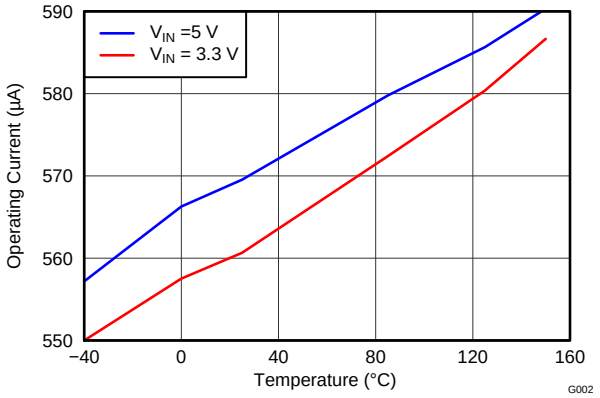


Figure 10.

EN PIN VOLTAGE vs TEMPERATURE

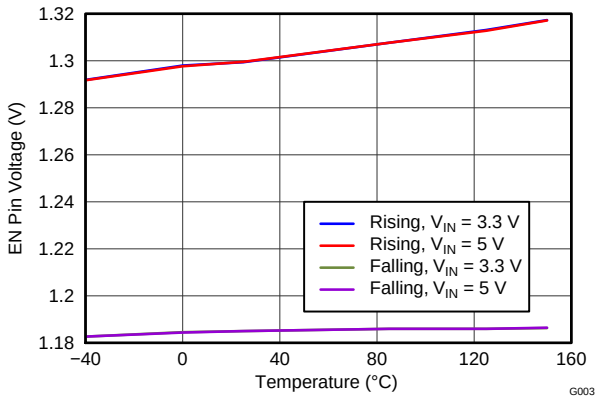


Figure 11.

EN PIN CURRENT vs TEMPERATURE

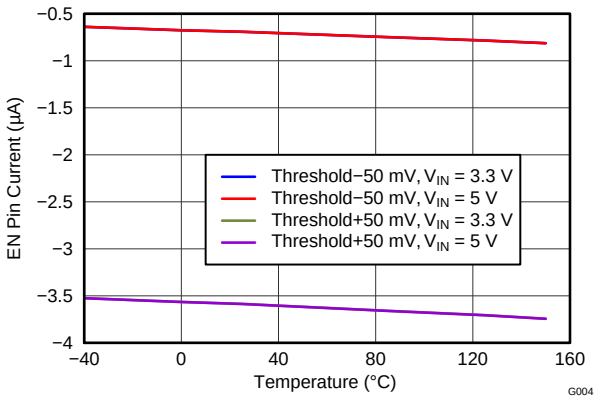


Figure 12.

VOLTAGE REFERENCE vs TEMPERATURE

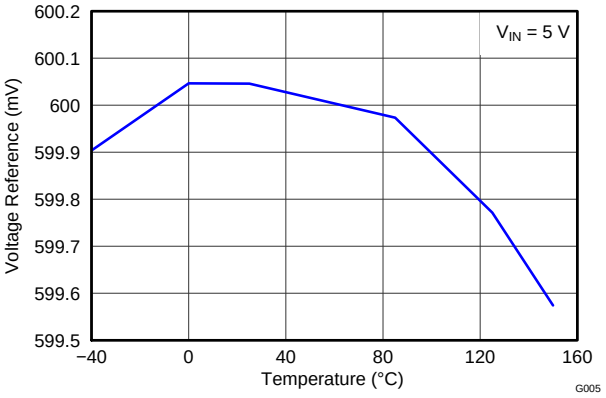


Figure 13.

MOSFET $R_{DS(on)}$ vs TEMPERATURE

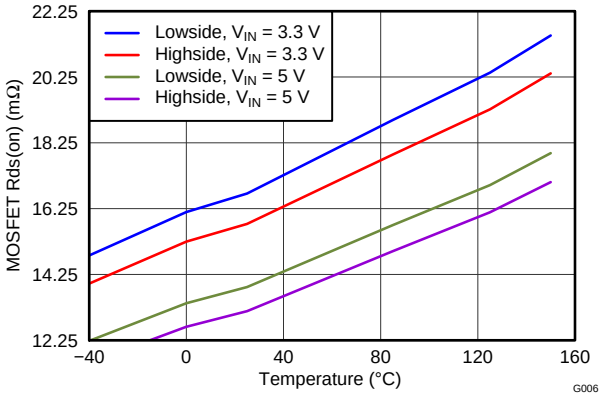


Figure 14.

Typical Characteristics (continued)

TRANSCONDUCTANCE vs TEMPERATURE

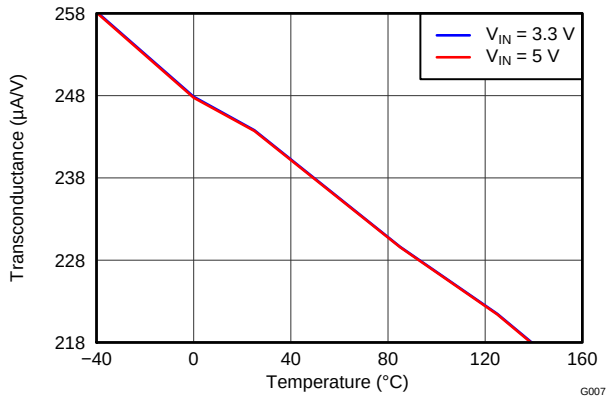


Figure 15.

HIGH SIDE FET CURRENT LIMIT vs TEMPERATURE

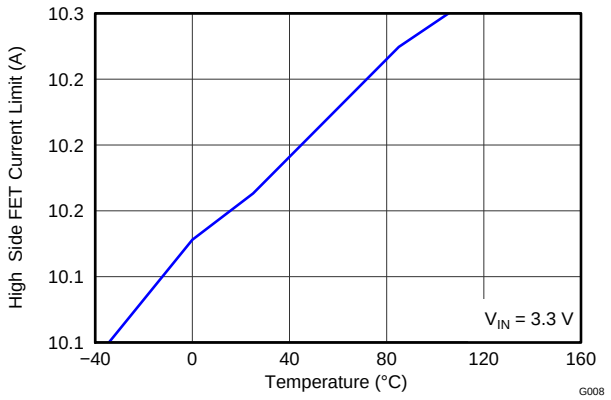


Figure 16.

SWITCHING FREQUENCY vs RT RESISTANCE

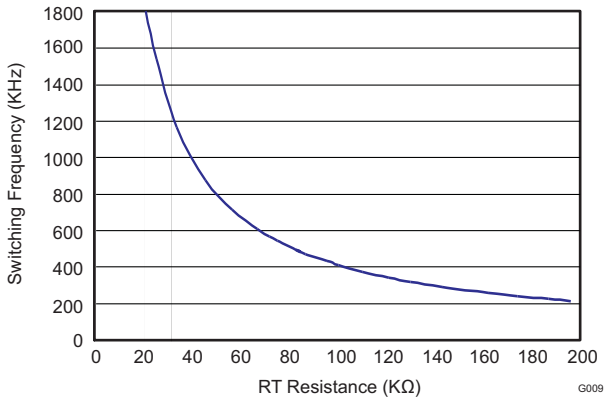


Figure 17.

SWITCHING FREQUENCY vs TEMPERATURE

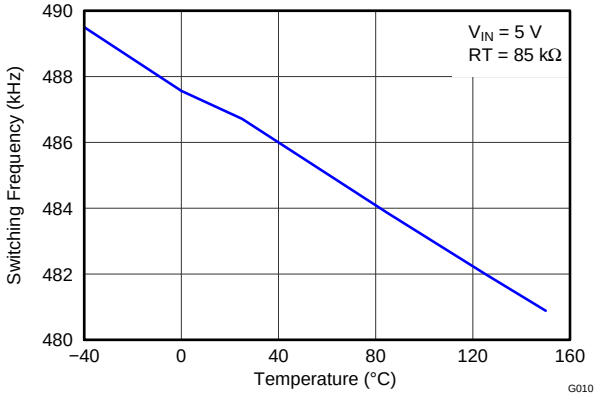


Figure 18.

VSS VOLTAGE THRESHOLD VSSTHR vs TEMPERATURE

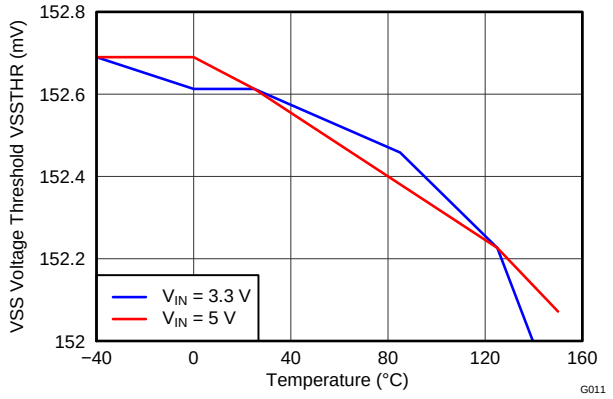


Figure 19.

SS CHARGE CURRENT vs TEMPERATURE

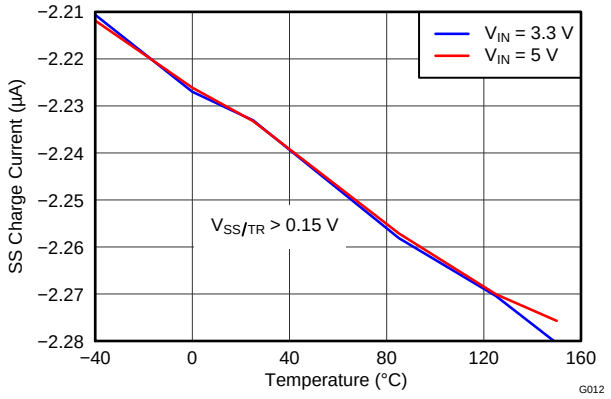


Figure 20.

Typical Characteristics (continued)

SS CHARGE CURRENT vs TEMPERATURE

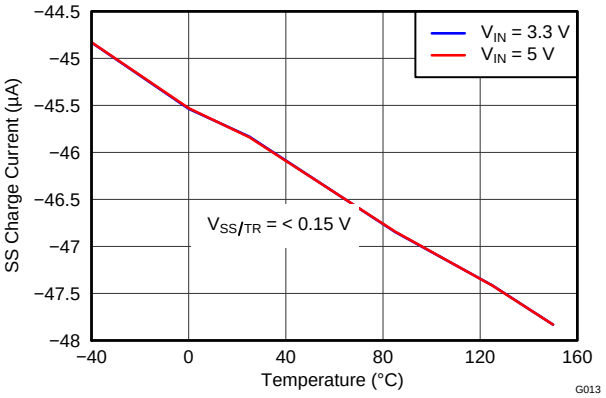


Figure 21.

PWRGD $R_{DS(on)}$ vs TEMPERATURE

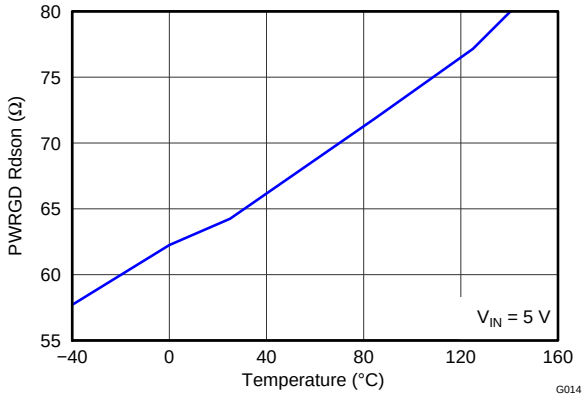


Figure 22.

PWRGD THRESHOLD vs TEMPERATURE

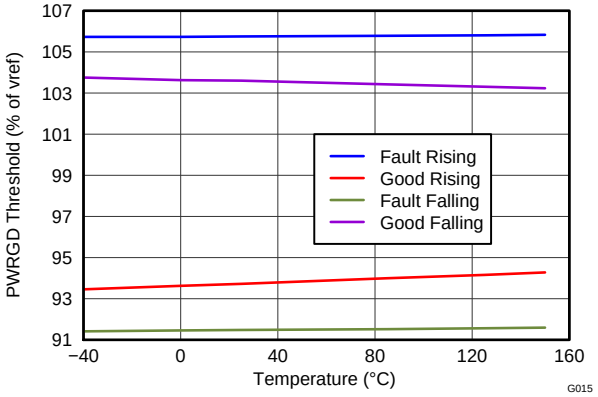


Figure 23.

PWRGD LEAKAGE CURRENT vs TEMPERATURE

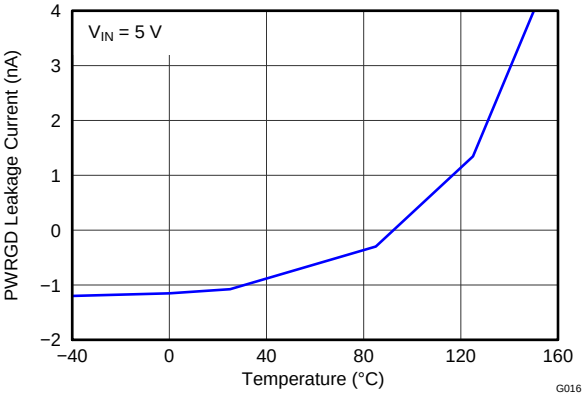


Figure 24.

EFFICIENCY vs CURRENT

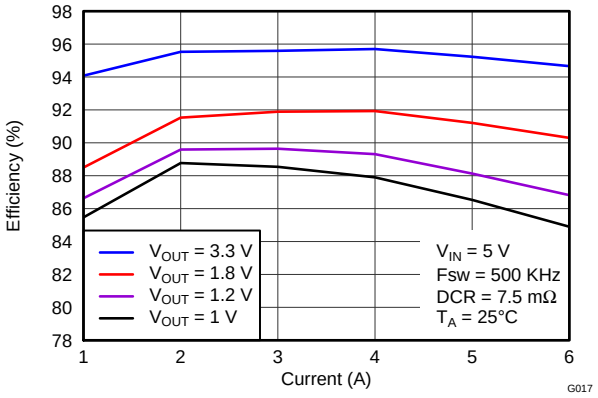


Figure 25.

EFFICIENCY vs CURRENT

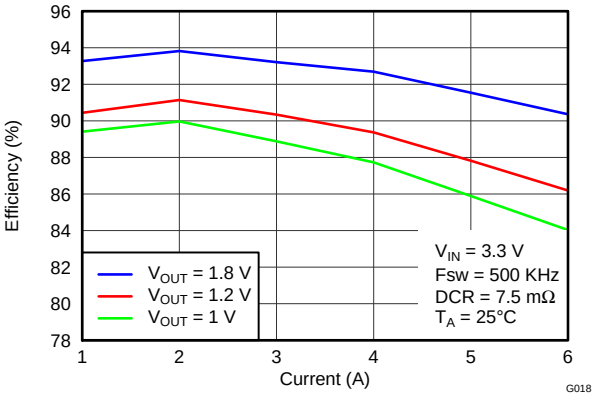


Figure 26.

Typical Characteristics (continued)

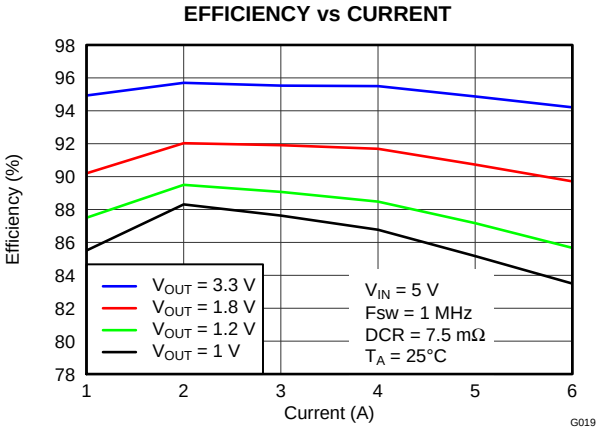


Figure 27.

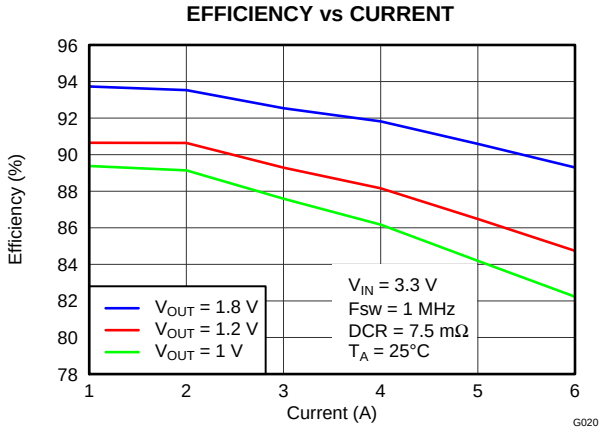


Figure 28.

APPLICATION INFORMATION

DESIGN GUIDE – STEP-BY-STEP DESIGN PROCEDURE

This example details the design of a high frequency switching regulator design using ceramic output capacitors. This design is available as the TPS54678EVM-155 (PWR155) evaluation module (EVM). A few parameters must be known in order to start the design process. These parameters are typically determined at the system level. For this example, we start with the following known parameters:

PARAMETER	VALUE
Output Voltage	1.2V
Transient Response 50% load step	ΔV_{OUT} < 5%
Maximum Output Current	6A
Input Voltage	3 V to 6 V, 5 V nominal
Output Voltage Ripple	< 30 mV_{PP}
Switching Frequency (Fsw)	500 kHz

Step by Step Design

1. SELECTING THE SWITCHING FREQUENCY

   The first step is to decide on a switching frequency for the regulator. Typically, it is desirable to choose the highest switching frequency possible since this produces the smallest component solution size. The high switching frequency allows for lower value inductors and smaller output capacitors compared to a power supply that switches at a lower frequency. However, the higher switching frequency causes extra switching losses, which degrade the performance of the converter. This SWIFT™ converter is capable of running from 200 kHz to 2 MHz. Unless a small solution size is the top priority, a moderate switching frequency of 500kHz is selected to achieve both a small solution size and high efficiency operation. Using Equation 13, R_T is calculated to be 81.34 kΩ. A standard 1% 82.5 kΩ value was chosen for the design.

$$R_T(k\Omega) = \frac{56183}{(F_{SW})^{1.052}} = \frac{56183}{(500)^{1.052}} = 81.34\ k\Omega \quad (13)$$

   Where:

   – R_T is in kΩ
   – F_{SW} is in kHz

2. OUTPUT INDUCTOR SELECTION

   The inductor selected works for the entire TPS54678 input voltage range. To calculate the value of the output inductor, use Equation 14. K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. The inductor ripple current is filtered by the output capacitor. Therefore, choosing high inductor ripple currents impacts the selection of the output capacitor since the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current. In general, the inductor ripple value is at the discretion of the designer, however K_{IND} is usually chosen between 0.1 to 0.3 for the majority of applications.

   For this design example, a value of K_{IND} = 0.3 was used at 6 V_{IN} and 6 A_{OUT}, and the inductor value is calculated to be 1.06 µH. For this design, the nearest standard value of 1.2 µH was chosen. For the output filter inductor, it is important that the RMS current and saturation current ratings not be exceeded. The RMS and peak inductor current can be found from Equation 16 and Equation 17.

   For this design, the RMS inductor current is 6.02 A and the peak inductor current is 6.8 A. The chosen inductor is a Coilcraft XAL5030-122ME. It has a saturation current rating 0f 11.8 A (20% inductance loss) and a RMS current rating of 8.7 A (20°C temperature rise). The series resistance is 6.78 mΩ typical.

   The current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults or transient load conditions, the inductor current can increase above the calculated peak inductor current level calculated above. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the switch current limit rather than the peak inductor current.

$$L1 = \frac{V_{IN\_MAX} - V_{OUT}}{I_o \times K_{IND}} \times \frac{V_{OUT}}{V_{IN\_MAX} \times F_{SW}} \quad (14)$$

$$I_{RIPPLE} = \frac{V_{IN\_MAX} - V_{OUT}}{L1} \times \frac{V_{OUT}}{V_{IN\_MAX} \times F_{SW}} \quad (15)$$

$$I_{IND\_RMS} = \sqrt{I_o^2 + \frac{1}{12} \times \left(\frac{V_{OUT} \times \left(V_{IN\_MAX} - V_{OUT} \right)}{V_{IN\_MAX} \times L1 \times F_{SW}} \right)^2} \quad (16)$$

$$I_{IND\_peak} = I_o + \frac{I_{RIPPLE}}{2} \quad (17)$$

3. OUTPUT CAPACITOR

There are three primary considerations for selecting the value of the output capacitor. Along with the inductor, the output capacitor determines the output voltage ripple, and also how the regulator responds to a large change in load current. The output capacitance needs to be selected based on the more stringent of these two criteria.

The desired response to a large change in the load current is the first criteria. The output capacitor needs to supply the load with current when the regulator can not due to limited control speed. The regulator is temporarily not able to supply sufficient change in output current if there is a large, fast increase or decrease in the current needs of the load such as transitioning from no load to full load. The regulator usually needs two or more clock cycles for the control loop to see the change in load current and output voltage and adjust the duty cycle to react to the change. The output capacitor must be sized to supply the extra current to the load until the control loop responds to the load change, or conversely, absorb the excess current from the inductor. Since the output voltage is less than half the input voltage, the worst case deviation in output voltage occurs when the load has an extremely rapid reduction in current, or a load dump. The desired specification is a 50% or 3A load step, and a resulting voltage deviation of no more than 5%, or 60mV. When a load dump occurs, the excess stored current in the inductor will tend to charge the output capacitors, and the best the converter can achieve to limit the increase in output voltage is to fold back the duty cycle to zero. Under these circumstances, the amount of rise in output voltage is defined by the energy from the choke being fully absorbed by the capacitor bank. Equation 18 through Equation 20 can be used to calculate the required capacitor bank value.

For this example, the transient load response is specified as a 5% change in Vout for a 50% load step from 3 A to 0 A. So, ΔI_{OUT} = 3 A and ΔV_{OUT} = 0.05 × 1.2 = 0.06 V. Using these numbers gives a minimum capacitance of 73.2 µF. This calculation does not take the ESR of the output capacitor into account in the output voltage change, and it does not account for latency in control loop speed. For ceramic capacitors, the ESR is usually small enough to ignore in this calculation.

$$Energy_{IND} = 0.5 \times L \times I^2 = 0.5 \times 1.2\mu \times 3^2 = 5.4\mu Joule \quad (18)$$

$$Energy_{CAP\,Initial} = 0.5 \times C \times V^2 = 0.5 \times C \times 1.2^2$$

$$Energy_{CAP\,Final} = 0.5 \times C \times 1.2^2 + Energy_{IND} = 0.5 \times C \times (1.2 + 0.06)^2 \quad (19)$$

Solving for C:

$$C_{Bank} = \frac{5.4\mu J}{(0.7938 - 0.72)} = 73.17\mu F \quad (20)$$

This 73.17 µF defines the minimum capacitance required to meet the transient spec, however, since the control loop speed is finite, more capacitance than this will be required to meet desired performance.

Equation 21 calculates the minimum output capacitance needed to meet the output voltage ripple specification. Where F_{SW} is the switching frequency, V_{RIPPLE} is the maximum allowable output voltage ripple, and Iripple is the inductor ripple current. In this case, the maximum output voltage ripple is 60 mV. Under this requirement, Equation 21 yields 13.33 µF.

$$C_{Bank} = \frac{1}{(8 \times F_{SW})} \times \frac{1}{\frac{V_{RIPPLE}}{I_{RIPPLE}}} = 13.33\mu F \quad (21)$$

Equation 22 calculates the maximum ESR for the capacitor bank to meet the output voltage ripple specification. Equation 22 indicates the ESR should be less than 37.5 mΩ. In this case, the ESR of the ceramic capacitor bank is less than 37.5 mΩ.

$$R_{ESR} < \frac{V_{RIPPLE}}{I_{RIPPLE}} \quad (22)$$

Additional capacitance de-ratings for aging, temperature and DC bias should be factored in which increases the minimum value calculated in Equation 20. For this example, five 47 µF 10 V X5R ceramic capacitors with 3 mΩ of ESR are used. The estimated capacitance after derating is 5 x 47 µF x 0.9 = 211.5 µF.

4. INPUT CAPACITOR

The TPS54678 requires a high quality ceramic, type X5R or X7R, input decoupling capacitor of at least 10 µF of effective capacitance and in some applications a bulk capacitance. The effective capacitance includes any DC bias effects. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the TPS54678. The input ripple current can be calculated using Equation 23.

$$I_{RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN\_MIN}} \times \frac{\left(V_{IN\_MIN} - V_{OUT}\right)}{V_{IN\_MIN}}} \quad (23)$$

The value of a ceramic capacitor varies significantly over temperature and the amount of DC bias applied to the capacitor. The capacitance variations due to temperature can be minimized by selecting a dielectric material that is stable over temperature. X5R and X7R ceramic dielectrics are usually selected for power regulator capacitors because they have a high capacitance to volume ratio and are fairly stable over temperature. The output capacitor must also be selected with the DC bias taken into account. The capacitance value of a capacitor decreases as the DC bias across a capacitor increases.

For this example design, a ceramic capacitor with at least a 10V voltage rating is required to support the maximum input voltage. For this example, three 47 µF and one 0.1 µF 10 V capacitors in parallel have been selected. In addition to these low ESR capacitors, an input bulk cap of 220 µF electrolytic is included so as to provide low source impedance at low frequencies for instances where the input voltage source is connected with a lossy feed.

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 24. Using the design example values, I_{OUT_MAX} = 6 A, C_{IN} = 141 µF (neglecting the electrolytic due to high ESR), F_{SW} = 500 kHz, yields an input voltage ripple of 21.3 mV and an rms input ripple current of 2.94 A.

$$\Delta V_{IN} = \frac{I_{OUT\_MAX} \times 0.25}{C_{IN} \times F_{SW}} \quad (24)$$

5. SLOW START CAPACITOR

The slow start capacitor determines the minimum amount of time it takes for the output voltage to reach the nominal programmed value during power up. This is useful if a load requires a controlled voltage slew rate. This is also used if the output capacitance is very large and would require large amounts of current to quickly charge the capacitor to the output voltage level. The large currents necessary to charge the capacitor may cause the TPS54678 to trip OCP, or excessive current draw from the input power supply may cause the input voltage rail to sag. Limiting the output voltage slew rate mitigates both of these issues.

The slow start capacitor value can be calculated using Equation 25. For the example circuit, the slow start time is not critical since the output capacitor value is 5 x 47 µF which does not require much current to charge to 1.2 V. The example circuit has the slow start time set to an arbitrary value of 3.33 ms which requires a 10nF capacitor.

$$C_{SS} = 3 \times T_{SS} \quad (25)$$

6. BOOTSTRAP CAPACITOR SELECTION

A 0.1 µF ceramic capacitor must be connected between the BOOT and PH pins for proper operation. It is recommended to use a ceramic capacitor with X5R or better grade dielectric. The capacitor should have 10 V or higher voltage rating.

7. OUTPUT VOLTAGE AND FEEDBACK RESISTOR SELECTION

For the example design, 20 kΩ was selected for R10. Using Equation 26, R9 is calculated also as 20 kΩ.

$$R_9 = R_{10} \times \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \tag{26}$$

Due to the internal design of the TPS54678, there is a minimum output voltage limit for any given input voltage. The output voltage can never be lower than the internal voltage reference of 0.6 V. Above 0.6 V, the output voltage may be limited by the minimum controllable on time. The minimum output voltage in this case is given by Equation 27.

$$V_{OUT\_MIN} = t_{ON\_MIN} \times F_{SW\_MAX} \left(V_{IN\_MAX} - I_{OUT\_MIN} \times R_{DS(ON)MIN} \right) - I_{OUT\_MIN} \times \left(R_L + R_{DS(ON)MIN} \right) \tag{27}$$

Where:

V_{OUT_MIN} = minimum achievable output voltage
t_{ON_MIN} = minimum controllable on-time (100 ns typical, 120 ns no load)
F_{SW_MAX} = maximum switching frequency including tolerance
V_{IN_MAX} = maximum input voltage
I_{OUT_MIN} = minimum load current
$R_{DS(ON)\_MIN}$ = minimum high-side MOSFET on resistance (See Electrical Characteristics)
R_L = series resistance of output inductor

There is also a maximum achievable output voltage which is limited by the minimum off time. The maximum output voltage is given by Equation 28

$$V_{OUT\_MAX} = V_{IN} \times \left(1 - \frac{t_{OFF\_MAX}}{Period} \right) - I_{OUT\_MAX} \times \left(R_{DS(ON)MAX} + R_L \right) - \left(0.7 - I_{OUT\_MAX} \times R_{DS(ON)MAX} \right) \times \left(\frac{t_{DEAD}}{Period} \right) \tag{28}$$

Where:

V_{OUT_MAX} = maximum achievable output voltage
V_{IN} = minimum input voltage
t_{OFF_MAX} = maximum off time (180 ns typical for adequate margin)
Period = 1/Fs
I_{OUT_MAX} = maximum current
$R_{DS(ON)\_MAX}$ = maximum high-side MOSFET on resistance (See Electrical Characteristics)
R_L = DCR of the inductor
t_{DEAD} = dead time (40 ns)

8. COMPENSATION

There are several possible methods to design closed loop compensation for dc/dc converters. For the ideal current mode control, the design equations can be easily simplified. The power stage gain is constant at low frequencies, and rolls off at –20 dB/decade above the modulator pole frequency. The power stage phase is 0 degrees at low frequencies and starts to fall one decade below the modulator pole frequency reaching a minimum of –90 degrees one decade above the modulator pole frequency. In this case the modulator pole is a simple pole shown in Equation 29.

$$F_{PMOD} = \frac{1}{2\pi C_{OUT} R_{LOAD}} \tag{29}$$

For the TPS54678 most circuits will have relatively high amounts of slope compensation. As more slope compensation is applied, the power stage characteristics will deviate from the ideal approximations. The phase loss of the power stage will extend beyond –90 degrees and can approach –180 degrees, making compensation more difficult. The power stage transfer function can be solved but it is a tedious hand calculation that does not lend itself to simple approximations. It is easier to either simulate the circuit or to actually measure the plant transfer function so that a reliable compensation circuit can be designed. The latter technique used in this design procedure. The power stage plant was measured and is shown below in Figure 29.

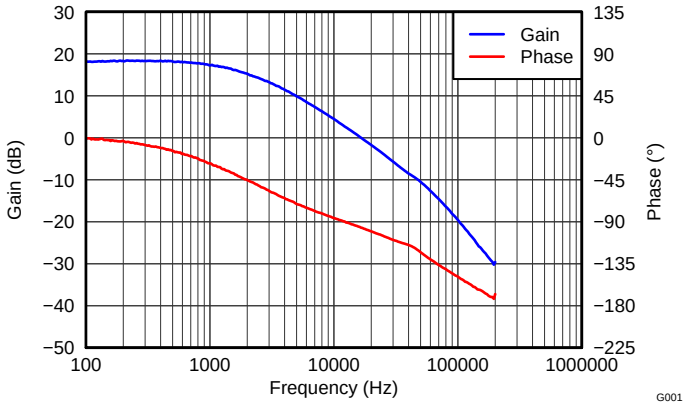


Figure 29. Measured Plant Bode

For this design, the desired crossover frequency Fc is 50 kHz. From the power stage gain and phase plot above, the gain at 50 kHz is -10.6 dB and the phase is –123.3 degrees. Since the plant phase loss is greater than -90 degrees, to achieve at least 60 degrees of phase margin, additional phase boost from a feed forward capacitor in parallel with the upper resistor of the voltage set point divider is required.

See the Schematic in Figure 47. R3 sets the gain of the compensated error amplifier to be equal and opposite (in dB) to the power stage gain at Fc, so +10.6 dB is needed. The required value of R3 can be calculated from Equation 30.

$$R_3 = \frac{10^{\left(\frac{-G_{Plant}}{20}\right)}}{gm_{EA}} \times \sqrt{\frac{V_{OUT}}{V_{REF}}} \tag{30}$$

The compensator zero formed by R3 and C6 is placed at the plant pole, as shown approximately 2.5 kHz. The required value for C6 is given by Equation 31.

$$C_6 = \frac{1}{2\pi R_3 F_{plant\,pole}} \tag{31}$$

The high frequency noise pole formed by C5 and R3 is not used in this design. If the resulting design shows noise susceptibility, the value of C5 can be calculated per Equation 32.

$$C_5 = \frac{1}{2\pi R_3 F_{pole}} \tag{32}$$

To avoid a penalty in loop phase, the Fpole in Equation 32 should be placed a decade above Fc or higher, and is intended to reject noise at F_{SW}.

The feed forward capacitor C15 is used to increase the phase boost at crossover above what is normally available from Type II compensation. It places an additional zero/pole pair with the zero located at Equation 33 and the pole at Equation 34.

$$F_z = \frac{1}{2\pi C_{15} R_9} \tag{33}$$

$$F_p = \frac{1}{2\pi C_{15} \left(R_9 \,||\, R_{10}\right)} \tag{34}$$

This zero and pole pair is not independent since R9 and R10 are set by the desired V_{OUT}. Once the zero location is chosen, the pole is fixed as well. For optimum performance, the zero and pole should be located symmetrically about the intended crossover frequency. The required value for C15 can be calculated from Equation 35.

$$C_{15} = \frac{1}{2\pi R_9 F_c \sqrt{\frac{V_{REF}}{V_{OUT}}}} \quad (35)$$

The above compensation equations yield the following values:

REF DES	CALCULATED VALUE	CHOSEN VALUE
R3	19.6 kΩ	26.7 kΩ
C6	2.38 nF	2.2 nF
C15	225 pF	150 pF

Application Curves

All following measurements are given for an ambient temperature of 25°C.

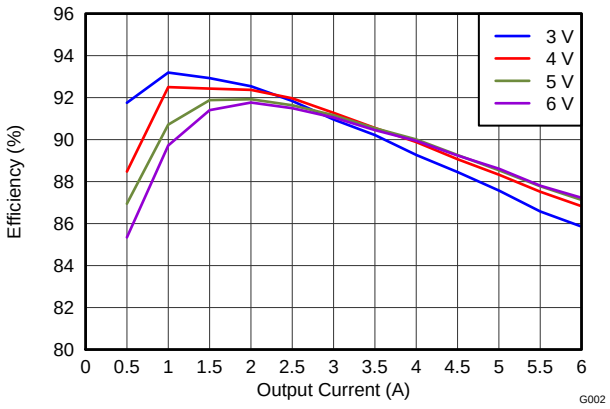


Figure 30. TPS54678EVM-155 Efficiency

The efficiency may be lower at higher ambient temperatures, due to temperature variation in the drain-to-source resistance $R_{DS(ON)}$ of the internal MOSFETs.

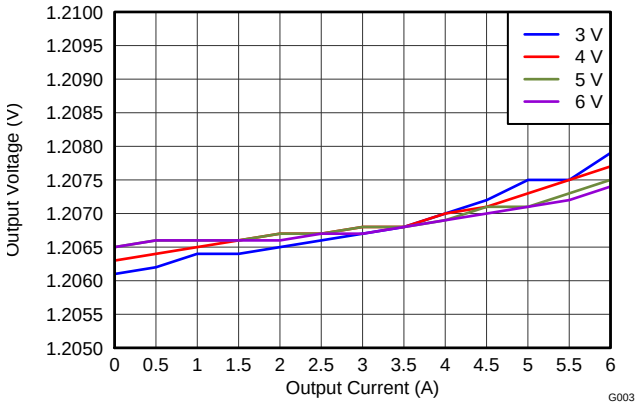


Figure 31. TPS54678EVM-155 Load Regulation

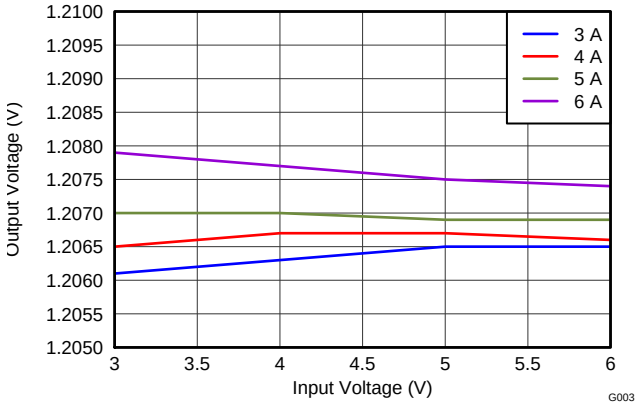


Figure 32. TPS54678EVM-155 Line Regulation

Figure 33 shows the TPS54678EVM-155 response to load transients. The current step is from 0% to 50% of maximum rated load at 3 V input. Total peak-to-peak voltage variation is as shown.

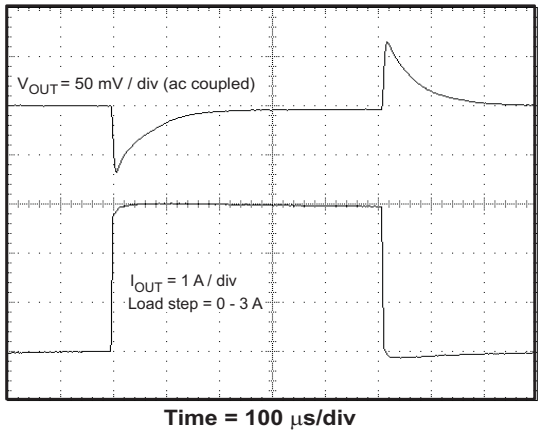


Figure 33. TPS54678EVM-155 Transient Response

Figure 34 shows the TPS54678EVM-155 loop-response characteristics. Gain and phase plots are shown for V_{IN} voltage of 5 V. Load current for the measurement is 6 A.

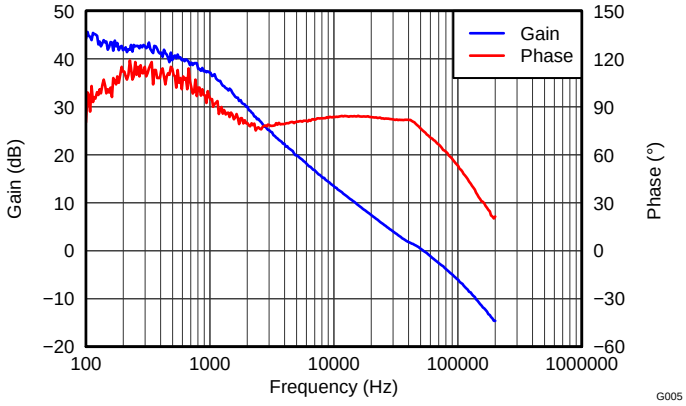


Figure 34. TPS54678EVM-155 Loop Response

Figure 35 shows the TPS54678EVM-155 output voltage ripple. The output current is the rated full load of 6 A and V_{IN} = 3 V. Figure 36 shows the ripple at 6 A and V_{IN} = 6 V. The voltage is measured directly across the output capacitors.

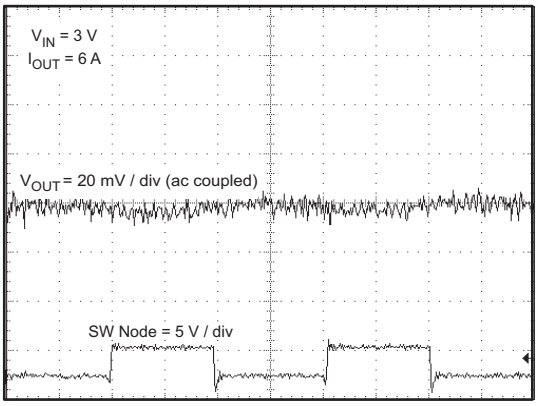


Figure 35. TPS54678EVM-155 Output Ripple, 3 V 6 A

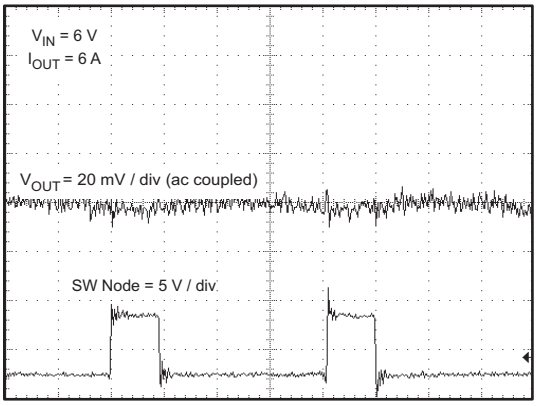


Figure 36. TPS54678EVM-155 Output Ripple, 6 V 6 A

Figure 37 shows the TPS54678EVM-155 input voltage ripple. The output current is the rated full load of 6 A and V_{IN} = 3 V. The ripple voltage is measured directly across the input capacitors.

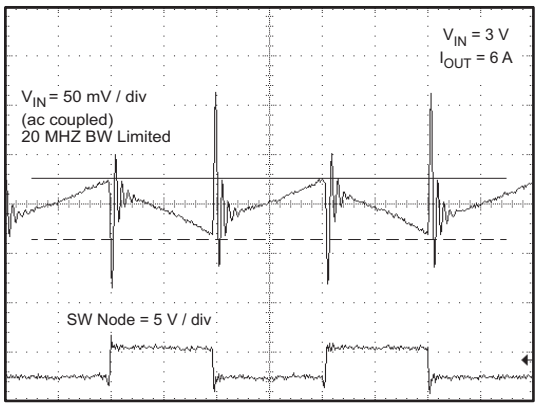


Figure 37. TPS54678EVM-155 Input Ripple at 3 V_{IN} and 6 A

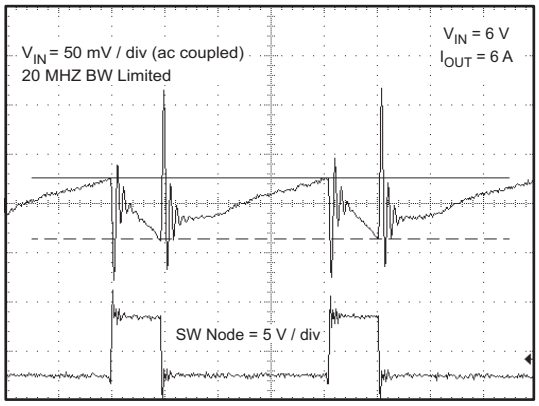


Figure 38. TPS54678EVM-155 Input Ripple at 6 V_{IN} and 6 A

Figure 39 and Figure 40 show the start-up waveforms for the TPS54678EVM-155. In Figure 39, the output voltage ramps up as soon as the input voltage reaches the UVLO threshold as set by the R1 and R2 resistor divider network. In Figure 40, the input voltage is initially applied and the output is inhibited by using a jumper at JP1 to tie EN to GND. When the jumper is removed, EN is released. When the EN voltage reaches the enable-threshold voltage, the start-up sequence begins and the output voltage ramps up to the externally set value of 1.2 V.

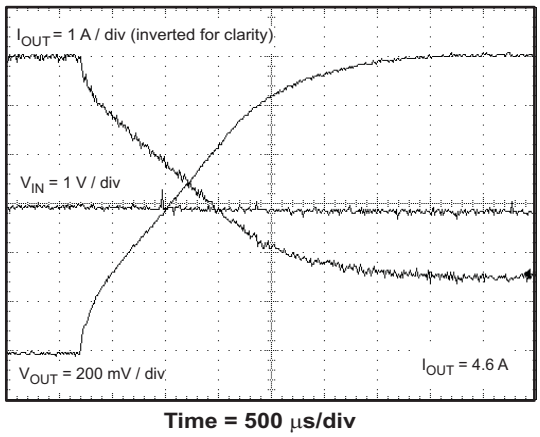


Figure 39. FTPS54678EVM-155 Start-Up Relative to V_{IN}

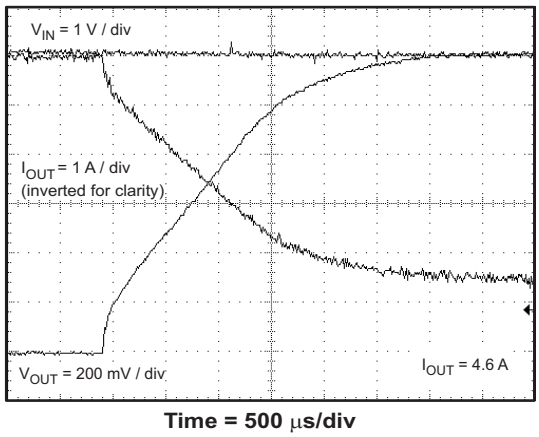


Figure 40. TPS54678EVM-155 Start-up Relative to Enable

The TPS54678 is designed to start up into pre-biased outputs. Figure 41 shows the output voltage start up waveform when the output is prebiased with 550 mV at no load.

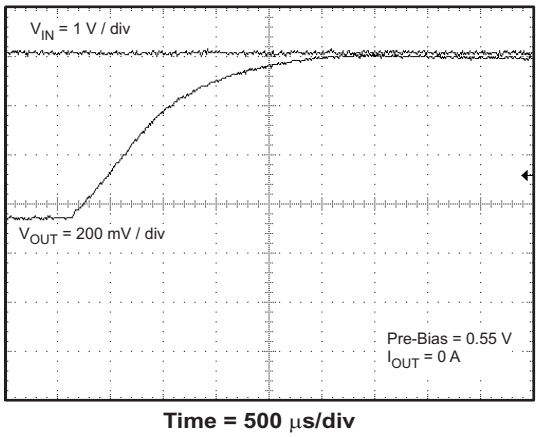


Figure 41. TPS54678EVM-155 Start-up into Pre-bias at no load

Figure 42 and Figure 43 show the shut down waveforms for the TPS54678EVM-155. In Figure 42, the output voltage ramps down as soon as the input voltage falls below the UVLO stop threshold as set by the R1 and R2 resistor divider network. At the point of shutdown, the input voltage rises slightly due to the resistive drop in the input feed impedance. In Figure 43, the output is inhibited by using a jumper at JP1 to tie EN to GND.

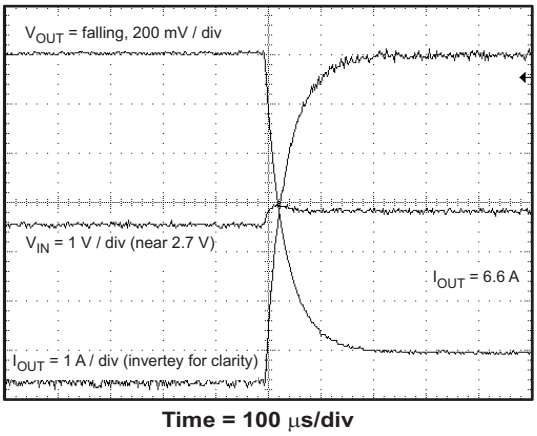


Figure 42. TPS54678EVM-155 Shut-down Relative to V_{IN}

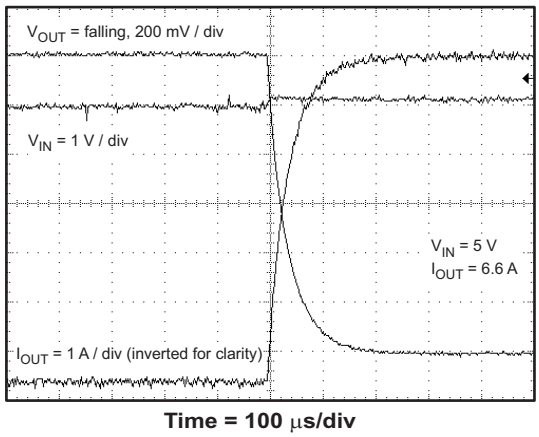


Figure 43. TPS54678EVM-155 Shut-down Relative to EN

The TPS54678 has hiccup mode current limit. When the peak switch current exceeds the current limit threshold, the device shuts down and restarts. Hiccup mode current limit operation is shown in Figure 44 and Figure 45. Figure 44 shows the hiccup mode current limit with a slight resistive overload. When the peak current limit is exceeded, the output voltage is disabled. Figure 45 shows the operation of the TPS54678 with the output shorted to ground. The device continuously resets until the fault condition is removed.

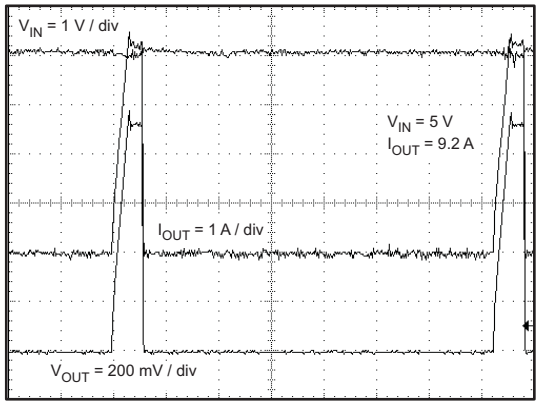


Figure 44. TPS54678EVM-155 Hiccup Mode Current Limit Shut-down

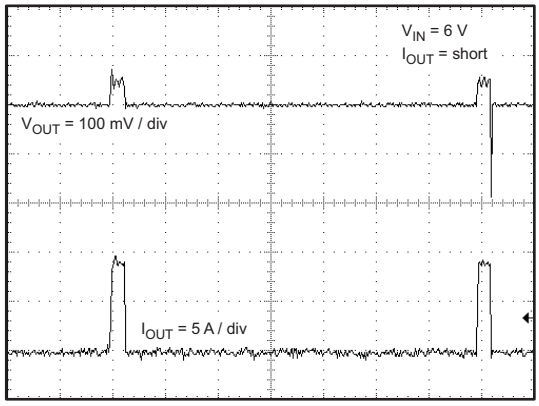


Figure 45. TPS54678EVM-155 Hiccup Mode Current Limit Re-start into Short Circuit

POWER DISSIPATION ESTIMATE

The following formulas show how to estimate the IC power dissipation under continuous conduction mode (CCM) operation. The power dissipation of the IC (Ptot) includes conduction loss (P_{con}), dead time loss (P_d), switching loss (P_{sw}), gate drive loss (P_{gd}) and supply current loss (P_q).

$P_{con} = I_O^2 \times R_{DS(on)}$ (temperature dependent)

$Pd = f_{sw} \times I_O \times 0.7 \times (20\ nS + 20\ nS)$

$P_{sw} = 0.5 \times V_{IN} \times I_O \times f_{sw} \times 7 \times 10^{-9}$

$P_{gd} = 2 \times V_{IN} \times f_{sw} \times 6 \times 10^{-9}$

$P_q = V_{IN} \times 500 \times 10^{-6}$

Where:

I_O is the output current (A).
$R_{DS(on)}$ is the on-resistance of the high-side MOSFET with given temperature (Ω).
V_{IN} is the input voltage (V).
f_{sw} is the switching frequency (Hz).

So

$P_{tot} = P_{con} + P_d + P_{sw} + P_{gd} + P_q$

For given T_A,

$T_J = T_A + R_{th} \times P_{tot}$

For given T_J max = 150°C

T_A max = T_J max – $R_{th} \times P_{tot}$

Where:

P_{tot} is the total device power dissipation (W).
T_A is the ambient temperature (°C).
T_J is the junction temperature (°C).
Rth is the thermal resistance of the package (°C/W).
T_J max is maximum junction temperature (°C).
T_A max is maximum ambient temperature (°C).

There are additional power losses in the regulator circuit due to the inductor AC and DC losses and trace resistance that impact the overall efficiency of the regulator.

LAYOUT

Component placement and copper layout are two of the most critical portions of good power supply design. Unfortunately, these two design parameters do not show up in the schematic, so proper layout rules must be described and followed. There are several signal paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supply's performance. Care should be taken to minimize the loop area formed by the bypass capacitor connections and the VIN pins. See Figure 46 for a PCB layout example. The GND pins and AGND pin should be tied directly to the power pad under the IC. The power pad should be connected to any internal PCB ground planes using multiple vias directly under the IC. Additional vias can be used to connect the top side ground area to the internal planes near the input and output capacitors. For operation at full rated load, the top side ground area along with any additional internal ground planes must provide adequate heat dissipating area.

Locate the input bypass capacitor as close to the IC as possible. The PH pin should be routed to the output inductor. Since the PH connection is the switching node, the output inductor should be located close to the PH pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling. The boot capacitor must also be located close to the device. The sensitive analog ground connections for the feedback voltage divider, compensation components, slow start capacitor and frequency set resistor should be connected to a

separate analog ground trace as shown. The RT/CLK pin is particularly sensitive to noise so the RT resistor should be located as close as possible to the IC and routed with minimal trace lengths. The additional external components can be placed approximately as shown. It may be possible to obtain acceptable performance with alternate PCB layout; however, this layout has been shown to produce good results and is intended as a guideline.

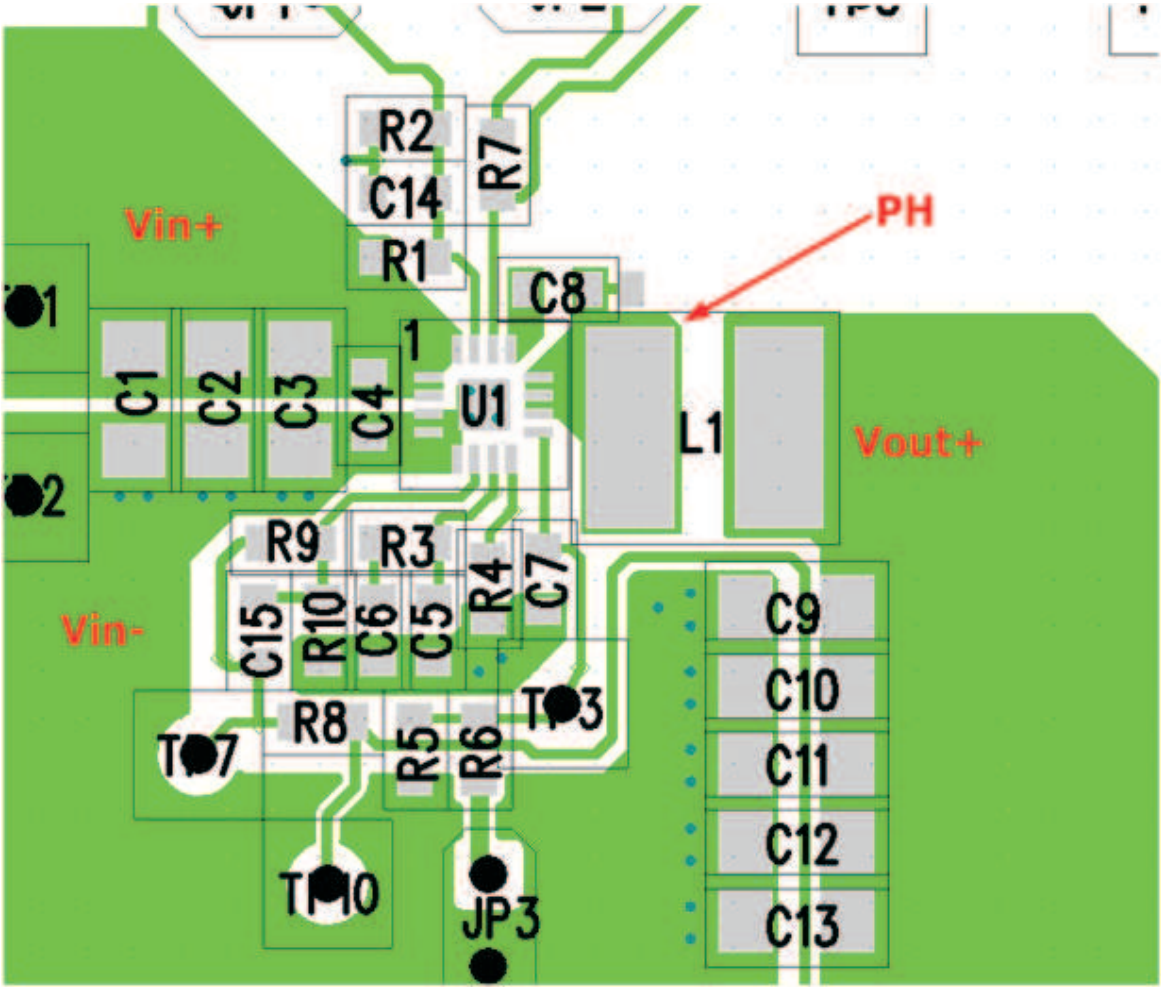


Figure 46. TPS54678EVM-155 Top-Side Assembly

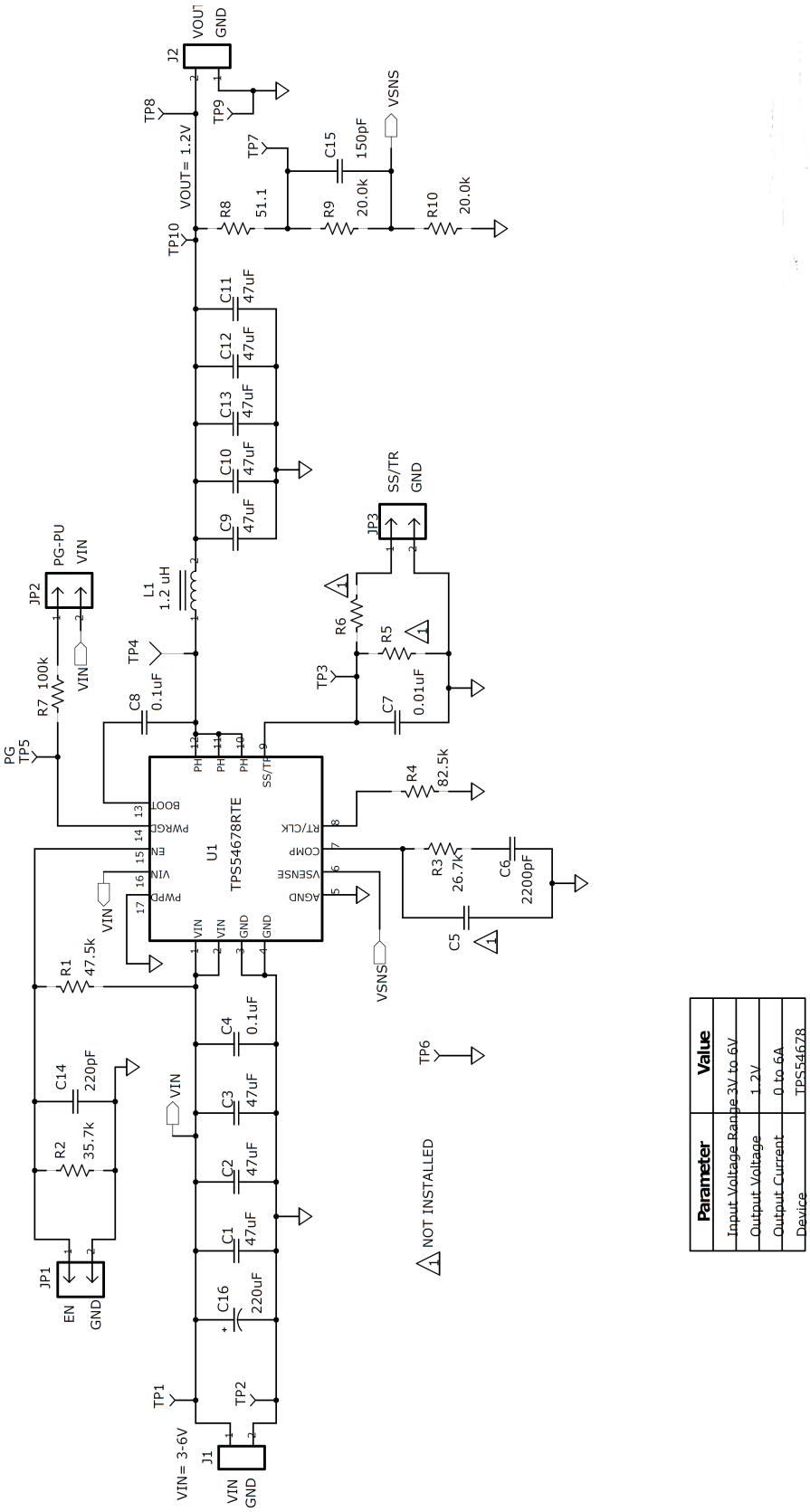


Figure 47. TPS54678 Schematic

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS54678RTER	ACTIVE	WQFN	RTE	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 150	54678	Samples
TPS54678RTET	ACTIVE	WQFN	RTE	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 150	54678	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

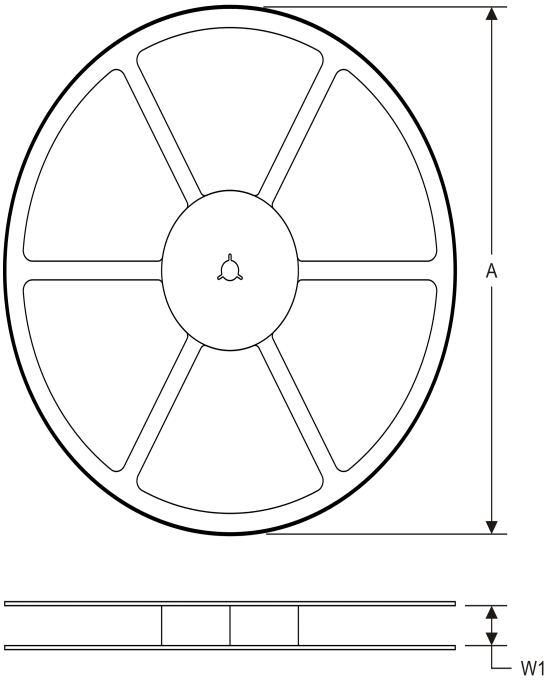
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

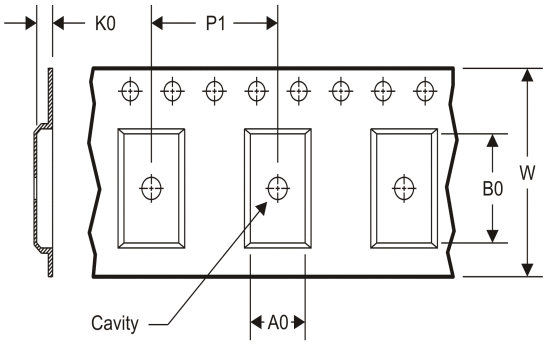
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



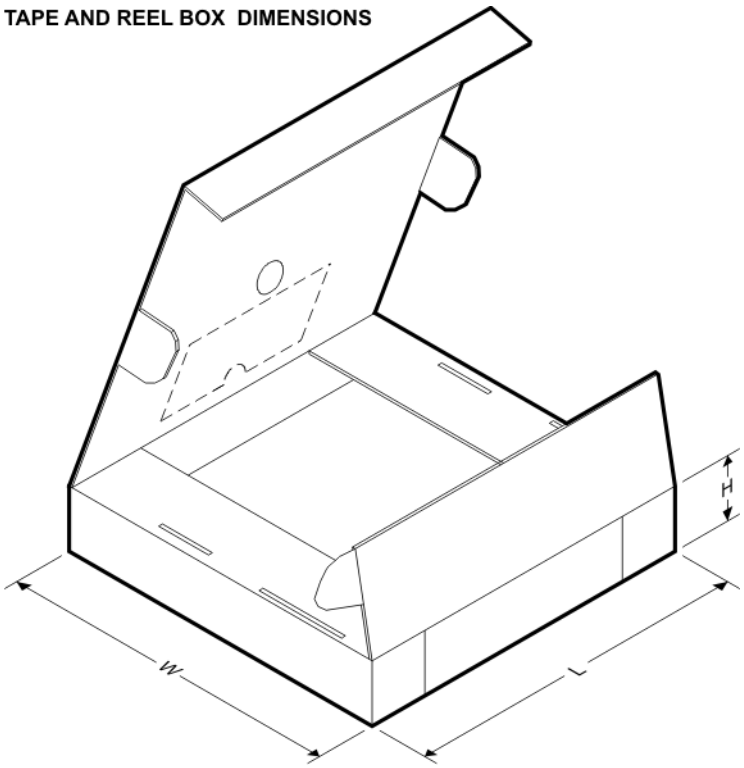
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54678RTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS54678RTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

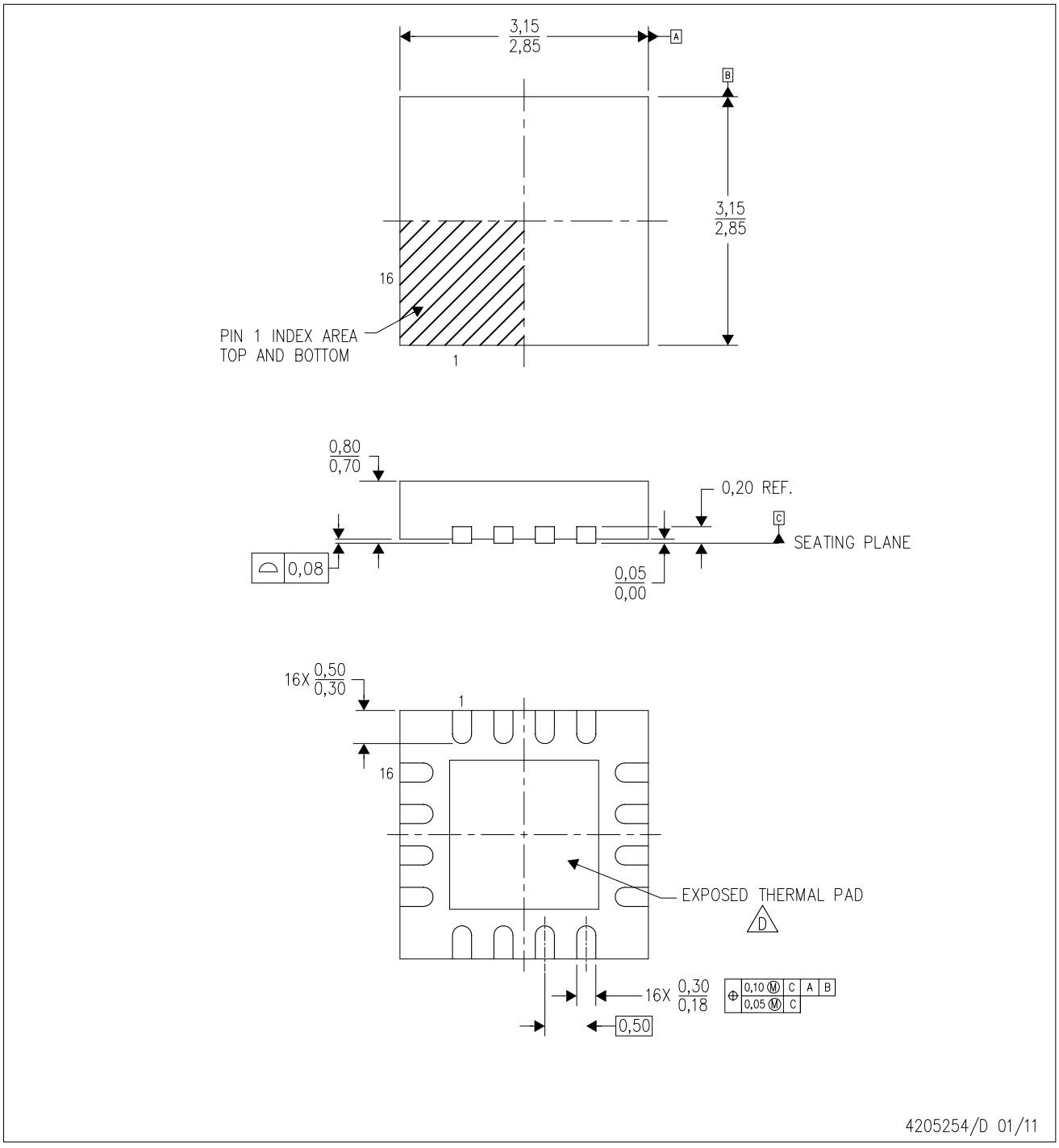
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54678RTER	WQFN	RTE	16	3000	367.0	367.0	35.0
TPS54678RTET	WQFN	RTE	16	250	210.0	185.0	35.0

RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

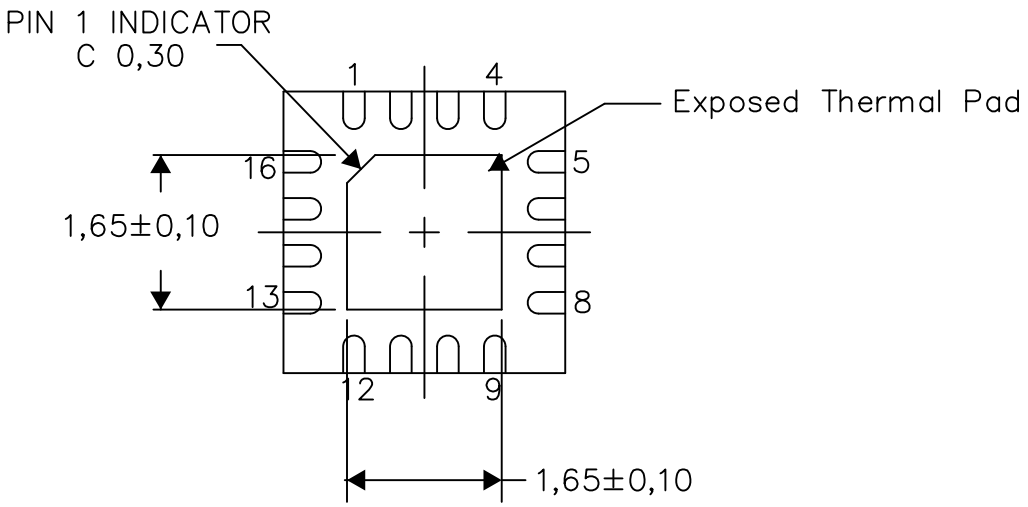
RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



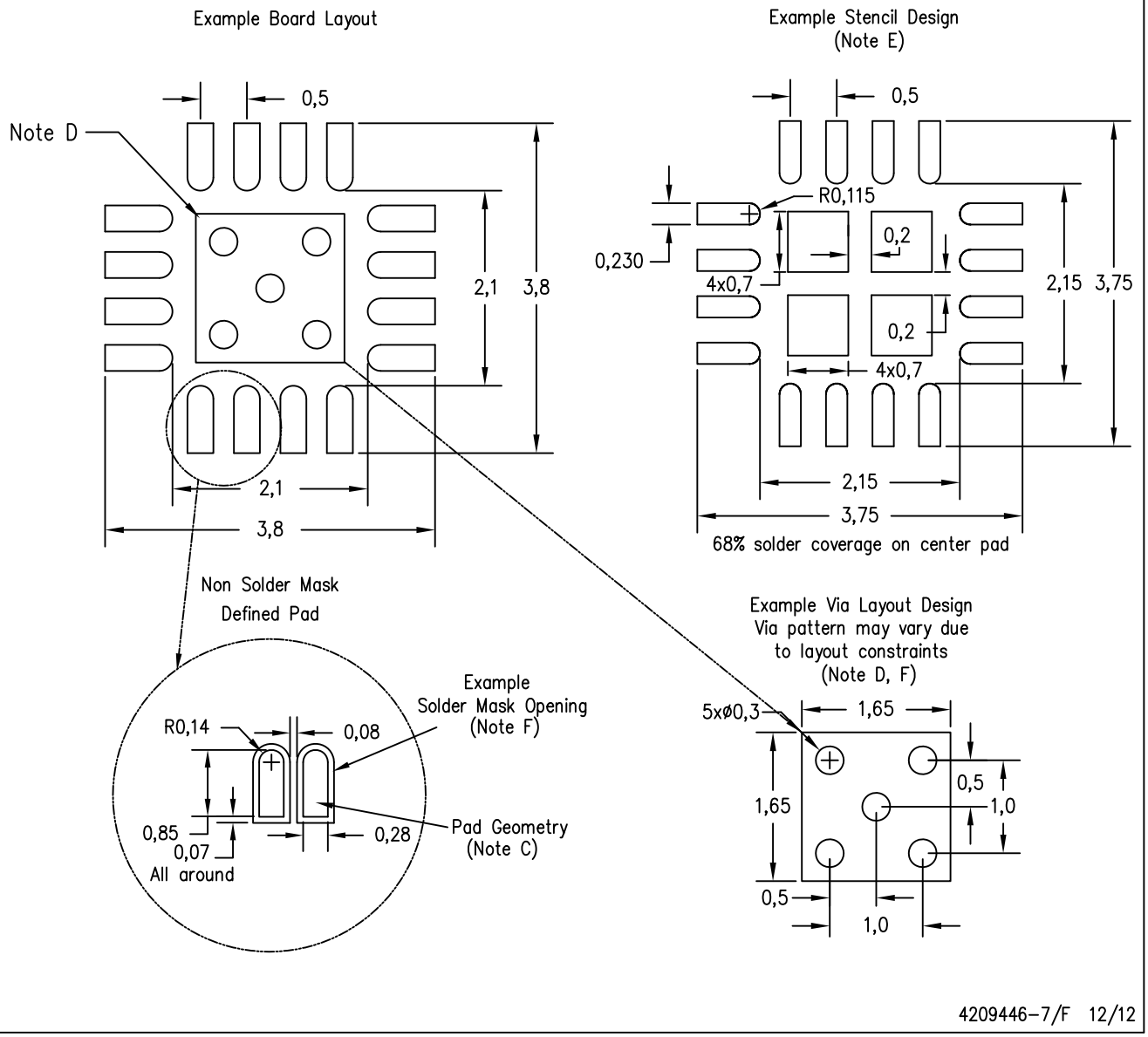
Bottom View

Exposed Thermal Pad Dimensions

4206446–4/L 04/13

NOTE: A. All linear dimensions are in millimeters

RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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