HDMI COMPANION CHIP WITH STEP-UP DC-DC CONVERTER, LEVEL-SHIFTER, AND ESD CLAMP

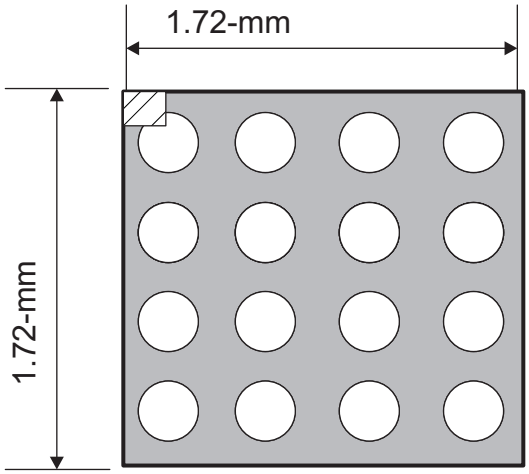
Check for Samples: TPD5S115

FEATURES

- **Conforms to HDMI Compliance Tests Without any External Components**
- **Supports HDMI 1.4 and HDMI 1.3 Standards**
- **Matches HDMI Connector Pin Mapping**
- **Internal DC-DC Converter to Generate 5 V From a Battery Voltage as Low as 2.3 V**
- **Auto-direction Sensing Level Shifting and Buffering in the CEC, SDA, and SCL Paths**
- **IEC 61000-4-2 (Level 4) System Level ESD Compliance**
- **Reverse Current Blocking and Short-circuit Protection to Protect Against Fault Conditions**
- **Industrial Temperature Range: –40°C to 85°C**

APPLICATIONS

- **Smart Phones**
- **eBook**
- **Digital Camcorders**
- **Portable Game Console**
- **Digital Still Cameras**



TPD5S115YFFR Pin Mapping (TOP VIEW)

16-YFF Pin Mapping

	1	2	3	4
A	SCL_B	GND	HPD_B	VCCA
B	CEC_B	SDA_B	LS_OE	HPD_A
C	5VOUT	SW	EN	SD_A
D	PGND	VBAT	CEC_A	SCL_A

DESCRIPTION

The TPD5S115 is an integrated HDMI companion chip solution. The device provides a regulated 5 V output (5VOUT) for sourcing the HDMI power line. The regulated 5 V output supplies up to 55 mA to the HDMI receiver. The TPD5S115 features two control signals EN and LS_OE. The control of 5VOUT and the hot plug detect (HPD) circuitry is independent of the LS_OE control signal and is controlled by the EN pin. The EN pin allows the detection scheme (5VOUT + HPD) to be active before turning on the whole HDMI link. The LS_OE activates the internal LDO, CEC, SCL, and SDA buffers only when EN is also activated. This dual stage enable scheme ensures optimized power saving for portable applications.

There are three non-inverting bi-directional translation circuits for the SDA, SCL, and CEC lines. Each have a common power rail (VCCA) on the A side from 1.1 V to 3.6 V. On the B side, the SCL_B and SDA_B each have an internal 1.75 kΩ pull-up connected to the regulated 5 V rail (5VOUT). The DDC (SCL_B and SDA_B) pins meet the I2C specification and drive up to 750 pF loads. The CEC_B pin has an internal 27 kΩ pull-up to an internal 3.3 V supply. The TPD5S115 exceeds the IEC61000-4-2 (Level 4) ESD protection level. This device is offered in a space saving 1.72 mm × 1.72 mm WCSP package with 0.4 mm pitch.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_A	PACKAGE(1)(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	YFF	Tape and reel	TPD5S115YFFR	RE115

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

SYSTEM LEVEL BLOCK DIAGRAM

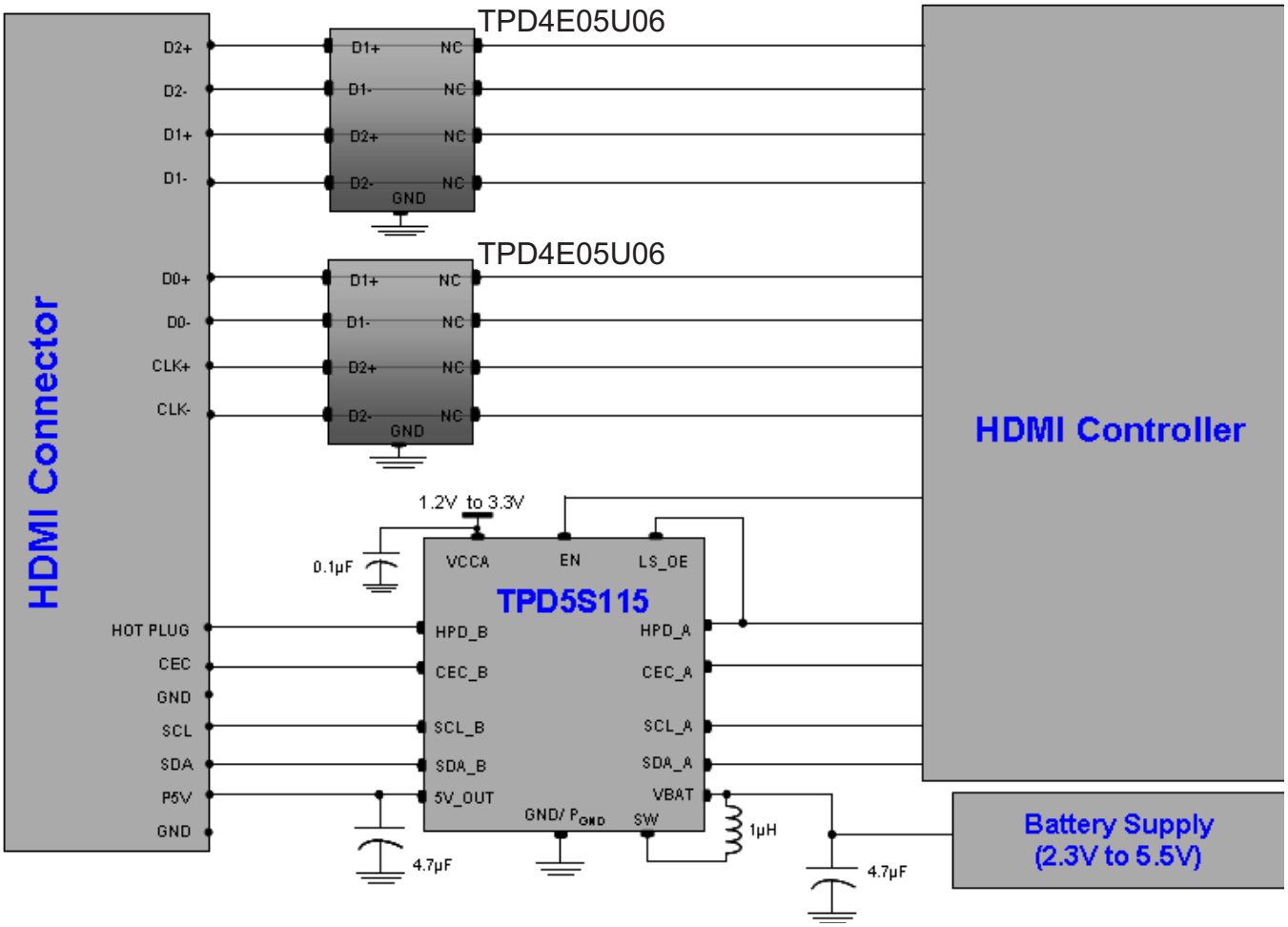


Figure 1. Application Schematics for HDMI Controllers with one GPIO for HDMI Interface Control

Some HDMI controllers may have only one GPIO to control the HDMI interface. Refer to Figure 1, HDMI Driver Chip is controlling the TPD5S115 via only one control line (EN). In this mode the HPD_A to LS_OE pin are connected shown in the above oval dotted line.

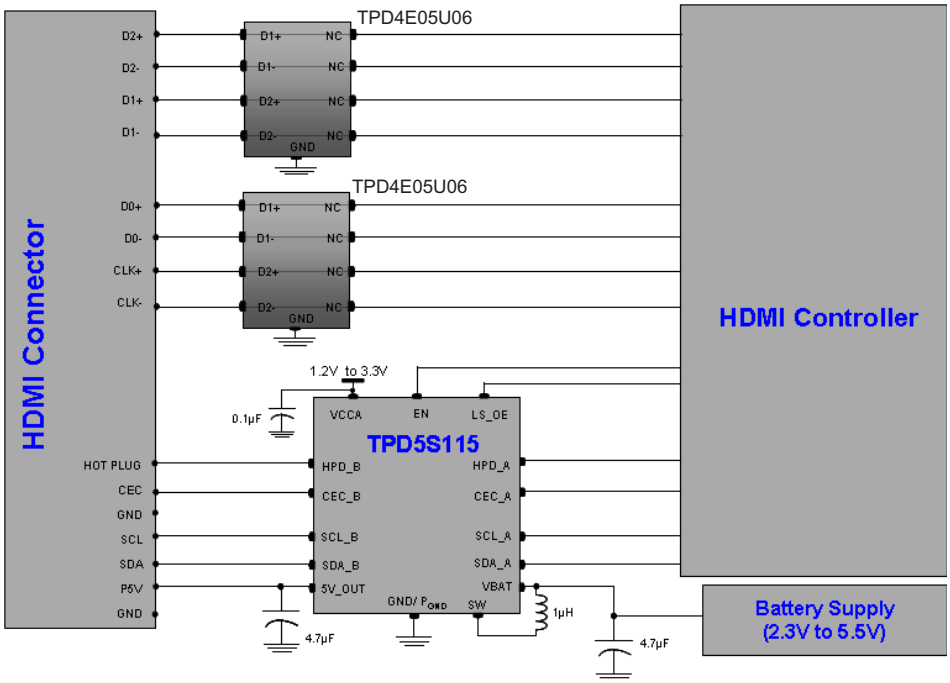


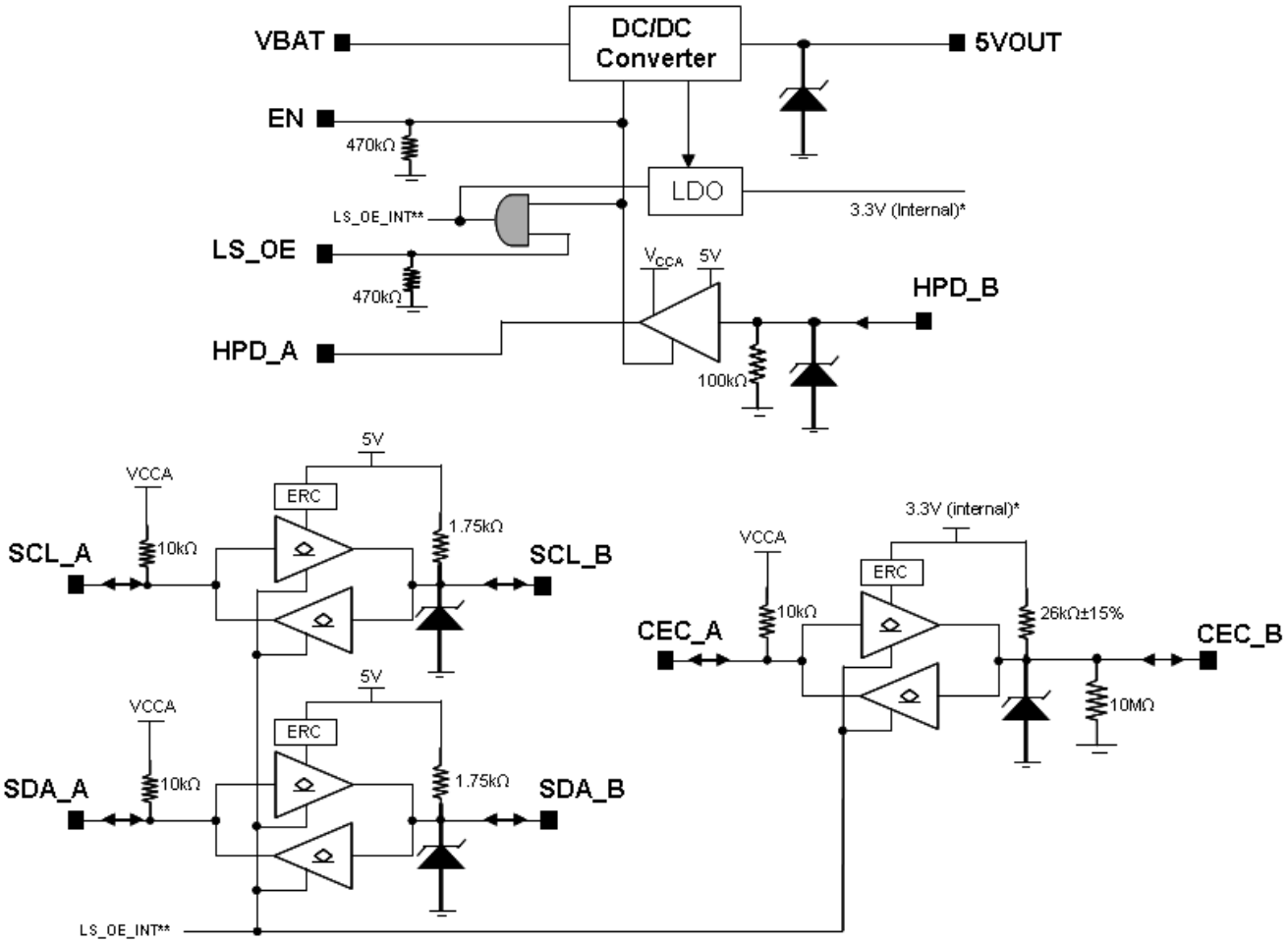
Figure 2. Application Schematics for HDMI Controllers with Two GPIOs for HDMI Interface Control

Some HDMI driver chips may have two GPIOs to control the HDMI interface chip. In this case a flexible power saving mode can be implemented. The LS_OE and EN are active-high enable pins. They control the TPD5S115 power saving options according to the following tables:

LS_OE	EN	VCCA	VBAT	5VOUT	A-Side Pull-ups	DCC, B-Side Pull-ups	CEC, B-Side Pull-ups
L	**L**	1.8 V	5.0 V	Off	Off	Off	Off
L	**H**	1.8 V	5.0 V	On	On	On	Off
H	**L**	1.8 V	5.0 V	Off	Off	Off	Off
H	**H**	1.8 V	5.0 V	On	On	On	On
X	**X**	0 V	0 V	High-Z	High-Z	High-Z	High-Z
X	**X**	1.8 V	0 V	Low	Low	High-Z	High-Z
X	**X**	0 V	5.0 V	High-Z	High-Z	High-Z	High-Z

LS_OE	EN	CEC LDO	DC/DC & HPD	DDC/CEC VLTs	ICCA Typ	ICC VBAT Typ	Comment
L	**L**	Off	Off	Off & High-Z	1 µA	1 µA	Fully Disabled
L	**H**	Off	On	Off & High-Z	1 µA	30 µA	DC/DC (30 µA) on
H	**L**	Off	Off	Off & High-Z	1 µA	1 µA	Not Valid State
H	**H**	On	On	On	13 µA	225 µA	Fully On
X	**X**	Off	Off	High-Z	0	0	Power down
X	**X**	Off	Off	High-Z	0	0	Power down
X	**X**	Off	Off	High-Z	0	0	Power down

CIRCUIT BLOCK DIAGRAMS



* 3.3V (Internal) is an internal 3.3V supply rail which is generated from 5VOUT when EN=H and LS_OE=H

** LS_OE_INT is an internal control signal generated from EN and LS__OE signals. LS_OE_INT is active when both EN=H and LS_OE=H

PIN FUNCTIONS

TERMINAL NAME	TYPE	DESCRIPTION
SCL_A, SDA_A	LS System side IO	**System Side Input/Output for I2C Bus**. These pins are bi-directional and referenced to V_{CCA}.
CEC_A	LS System side IO	**System Side CEC Bus I/O.** This pin is bi-directional and referenced to V_{CCA}.
HPD_A	Output	**System Side Output for the Hot Plug Detect.** This pin is unidirectional and is referenced to V_{CCA}.
SCL_B, SDA_B	LS HDMI Connector side IO	**HDMI side Input/Output for I2C Bus.** These pins are bi-directional and referenced to 5VOUT.
CEC_B	LS HDMI Connector side IO	**HDMI Side CEC Bus I/O.** This pin is bi-directional and referenced to the 3.3V internal supply.
HPD_B	Input	**HDMI Side Input for the Hot Plug Detect.** This pin is unidirectional and is referenced to 5VOUT.
EN	Control Pin	**DC/DC Enable.** Enables the DC/DC converter and HPD circuitry when EN = H. The EN is referenced based off V_{CCA}.

PIN FUNCTIONS (continued)

TERMINAL NAME	TYPE	DESCRIPTION
LS_OE	Control Pin	**Level Shifter Enable.** This pin is referenced to VCCA. Enables level shifters and LDO when EN = H and LS_OE = H.
VBAT	Supply	**Battery Supply.** This voltage is typically 2.3 V - 5.5 V.
5VOUT	Power Output Pin	**DC/DC Output.** The +5 V Power pin can supply 55 mA regulated current to the HDMI receiver. Separate dc/dc converter control pin EN disables the dc/dc converter when operating at low-power mode.
SW	Power Input	**Switch Input.** This pin is the inductor input for the dc/dc converter.
VCCA	Supply	**System Side Supply.** This voltage is typically 1.2 V to 3.3 V from the core microcontroller.
GND	Ground	**Device Ground.**
PGND	Analog Ground	**DC/DC Converter Ground.** These pins are isolated from the GND pins. This pin should be tied to system GND.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CCA}	Supply voltage range			4.0	V
V_{BAT}	Supply voltage range		–0.3	6.0	V
V_I	Input voltage range(2)	SCL_A, SDA_A, CEC_A	–0.3	4.0	V
		SCL_B, SDA_B, CEC_B, HPD_B	–0.3	6.0	
		EN, LS_OE	–0.3	4.0	
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)	SCL_A, SDA_A, CEC_A	–0.3	4.0	V
		SCL_B, SDA_B, CEC_B	–0.3	6.0	
V_O	Voltage range applied to any output in the high or low state(2)(3)	SCL_A, SDA_A, CEC_A	–0.3	VCCA + 0.3	V
		SCL_B, SDA_B, CEC_B	–0.3	5VOUT + 0.3	
I_{IK}	Input clamp current	IV < 0		–50	mA
I_{OK}	Output clamp current	VO < 0		–50	mA
I_{OUTMAX}	Continuous current through 5VOUT, or GND			±100	mA

(1) Stresses beyond those listed under "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

PARAMETER			SUPPLY	MIN	TYP	MAX	UNIT
V_{CCA}	Supply voltage			1.2		3.6	V
V_{BAT}	Supply voltage			2.3		5.5	V
V_{IH}	High-level input voltage	SCL_A, SDA_A	V_{CCA} = 1.2 V to 3.6 V	0.7 × V_{CCA}		V_{CCA}	V
		CEC_A	V_{CCA} = 1.2 V to 3.6 V	0.7 × V_{CCA}		V_{CCA}	
		EN, LS_OE	V_{CCA} = 1.2 V to 3.6 V	1.0		V_{CCA}	
		SCL_B, SDA_B	5VOUT = 5.0 V	0.7 × 5VOUT		5VOUT	
		CEC_B	5VOUT = 5.0 V	0.7 × 3.3 V (internal) (1)		3.3 V (internal) (1)	
		HPD_B	5VOUT = 5.0 V	2.0			
V_{IL}	Low-Level input voltage	SCL_A, SDA_A	V_{CCA} = 1.2 V to 3.6 V	–0.5		0.082 × V_{CCA}	V
		CEC_A	V_{CCA} = 1.2 V to 3.6 V	–0.5		0.082 × V_{CCA}	
		EN, LS_OE	V_{CCA} = 1.2 V to 3.6 V	–0.5		0.4	
		SCL_B, SDA_B	5VOUT = 5.0 V	–0.5		0.3 × 5VOUT	
		CEC_B	5VOUT = 5.0 V	–0.5		0.3 × 3.3V (internal) (1)	
		HPD_B	5VOUT = 5.0 V	0		0.8	
V_{ILC}	(contention) Low-level input voltage			–0.5		0.065 × V_{CCA}	V
V_{OL}- V_{ILC}	Delta between V_{OL} and V_{ILC}		V_{IO} = 2.5 V		0.1 × V_{CCA}		V
T_A	Operating free-air temperature			–40		85	°C
Passive Components							
L_{IN}	External Inductor, 0805 foot-print				1		µH
C_{IN}	Input Capacitor, 0603 foot-print				4.7		µF
C_{OUT}	Output Capacitor, 0603 foot-print				4.7		µF
C_{VCCA}	Input Capacitor, 0402 foot-print				0.1		µF

(1) "3.3V (internal)" is an internally generated voltage node for the CEC_B output buffer supply reference. An LDO generates this 3.3 V from 5VOUT when LS_OE = H & EN = H.

ESD Table

PARAMETER	SIGNALS	TYP	UNIT
HBM JESD22A114-B	SCL_A, SDA_A, CEC_A, EN, LS_OE, VCCA	2	kV
CDM JESD22 C101	ALL	1000	V
IEC 61000-4-2 Contact Discharge	SCL_B, SDA_B, CEC_B, HPD_B, 5VOUT	±14	kV
IEC 61000-4-2 Air-gap Discharge	SCL_B, SDA_B, CEC_B, HPD_B, 5VOUT	±16	V

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I_{CCA}	Standby	VCCA	I/O's = High			2	µA
	Active	VCCA	I/O's = High			15	µA
I_{CCB}	Standby	VBAT	EN = L LS_OE = L		0.5		µA
	DC/DC and HPD Active	VBAT	EN = H LS_OE = L		30	50	µA
	DC/DC, HPD, DDC, CEC Active	VBAT	EN = H LS_OE = L I/O's = H		225	300	µA
DC-DC Converter							
V_{BAT}	Input Voltage Range			2.3		5.5	V
5VOUT	Total DC Output Voltage		Includes voltage references, DC load / line regulations, process and temperature	4.90	5.0	5.13	V
T_{OVA}	Total Output Voltage Accuracy		Includes voltage references, DC load / line regulations, transient load / line regulations, ripple, process and temperature	4.80	5.0	5.3	V
V_{IO_Ripple}	Output Voltage Ripple, Loaded		I_O = 65 mA		50.6		mV (p-p)
			I_O = 150 mA		16		
F_clk	Internal operating frequency		V_{BAT} = 2.3 V - 5.5 V		3.5		MHz
t_{start}	Startup time		From EN input to 5 V Power Output 90% point.		187		µs
IO	Output Current		V_{BAT} = 2.3 V to 5.5 V	55			mA
	Reverse Leakage Current V_O		EN= L, VO = 5.5 V			2.5	µA
	Leakage Current from Battery to V_O		EN= L			5.0	µA
V_{BATUV}	Under voltage Lockout Threshold		Falling		2.0		V
			Rising		2.1		V
	Line Transient Response		V_{BAT} = 3.4 V, a pulse of 217 Hz 600 mVp-p square wave. IO = 20/ 65 mA		17.1		mVpk
	Load Transient Response		V_{BAT} = 3.4 V, IO = 5 - 65 mA, pulse of 10 µSec, TRise = TFall = 0.1 µs		63.5		mVpk
I_inrush (startup)	inrush current, average over T_startup time		Vbat = 2.3 V - 5.5 V Iout = 65 mA		168		mA
I_{SC}	Short Circuit Current Limit from Output				90		mA

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CCA}	–40°C to 85°C			UNIT
					MIN	TYP	MAX	
V_{OHA}		I_{OH} = –10 µA	$V_I = V_{IH}$	1.2 V to 3.6 V	V_{CCA} × 0.80			V
V_{OLA}		I_{OL} = 10 µA	$V_I = V_{IL}$	1.2 V to 3.6 V		V_{CCA} × 0.16		V
V_{OHB}		I_{OH} = –10 µA	$V_I = V_{IH}$					V
V_{OLB}		I_{OL} = 3 mA	$V_I = V_{IL}$				0.4	V
RPU	Internal pull-up	SCL_A, SDA_A	Pull-up connected to VCCA rail			10		kΩ
		SCL_B, SDA_B	Pull-up connected to 5 V rail			1.75		
$I_{PULLUPAC}$	Transient Boosted Pull-up Current (rise-time accelerator)	SCL_B, SDA_B	Pull-up connected to 5 V rail			15		mA
I_{off}	A port	VCCA = 0 V, V_I or V_O = 0 to 3.6 V		0 V			±5	µA
	B port	5VOUT = 0 V, V_I or V_O = 0 to 5.5 V		0 V to 3.6 V			±5	
I_{OZ}	A port	$V_O = V_{CCO}$ or GND		1.2 V to 3.6 V			±5	
	B port	$V_I = V_{CCI}$ or GND		1.2 V to 3.6 V			±5	
Voltage Level Shifter CEC Line (x_A & x_B ports)								
V_{OHA}		I_{OH} = –10 µA	$V_I = V_{IH}$	1.2 V to 3.6 V	V_{CCA} × 0.80			V
V_{OLA}		I_{OL} = 10 µA	$V_I = V_{IL}$	1.2 V to 3.6 V		V_{CCA} × 0.16		V
V_{OHB}		I_{OH} = –20 µA	$V_I = V_{IH}$		V_{CCA} × 0.80			V
V_{OLB}		I_{OL} = 3 mA	$V_I = V_{IL}$				0.4	V
R_{PU}	Internal pull-up	CEC_A	Pull-up connected to VCCA rail			10		kΩ
		CEC_B	Pull-up connected to 3.3 V rail		22	26	30	
R_{PD}	Internal pull-down	CEC_B	Pull-up connected to GND			14		MΩ
I_{off}	A port	VCCA = 0 V, V_I or V_O = 0 to 3.6 V		0 V			±5	µA
	B port	5VOUT = 0 V, V_I or V_O = 0 to 5.5 V		0 V to 3.6 V			±1.8	
I_{OZ}	A port	$V_O = V_{CCO}$ or GND		1.2 V to 3.6 V			±5	
	B port	$V_I = V_{CCI}$ or GND		1.2 V to 3.6 V			±5	

ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CCA}	–40°C to 85°C			UNIT
					MIN	TYP	MAX	
Voltage Level Shifter - HPD Line (X_A & x_B)								
V_{OHA}		I_{OH} = –3 mA	$V_I = V_{IH}$	1.2 V to 3.6 V	V_{CCA} × 0.7			V
V_{OLA}		I_{OL} = 3 mA	$V_I = V_{IL}$	1.2 V to 3.6 V			0.4	V
R_{PD}	Internal pull-down	HPD_B	Pull-up connected to GND			100		kΩ
I_{OZ}	A port	$V_I = V_{CCI}$ or GND		3.6 V			±5	µA
LS_OE, EN								
I_I		$V_I = V_{CCA}$ or GND		1.2 V to 3.6 V			±12	

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	Supply & EN Signal	–40°C to 85°C			UNIT
				MIN	TYP	MAX	
I/O Capacitances							
C	EN, LS_OE	V_{BIAS} = 1.8 V, f = 1 MHz, 30 mVp-p ac signal	V_{CCA} = 3.6 V VBAT= 5 V		7.1	9.5	pF
	SCL_A, SDA_A, CEC_A	V_{BIAS} = 1.8 V, f = 1 MHz, 30 mVp-p ac signal	V_{CCA} = 3.6 V VBAT = 5 V, EN = L		7		pF
	HPD_A, HPD_B	V_{BIAS} = 1.8 V, f = 1 MHz, 30 mVp-p ac signal	V_{CCA} = 3.6 V VBAT = 5 V, EN = L		4		pF
	SCL_B, SDA_B	V_{BIAS} = 2.5 V, f = 100 kHz, 3.5 Vp-p ac signal	V_{CCA} = 3.6 V VBAT = 5 V, EN = L, LS_OE = H		10		pF
	CEC_B	V_{BIAS} = 1.65 V, f = 100 kHz, 2.5 Vp-p ac signal	V_{CCA} = 3.6 V VBAT = 5 V, EN=L, LS_OE = H		7		pF
	CEC_B	V_{BIAS} = 1.65 V, f = 100 kHz, 2.5 Vp-p ac signal	V_{CCA} = 0 V 5V_IN = 0 V		7		pF

SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_L	Bus Load Capacitance (B side)				750	pF
	Bus Load Capacitance (A side)				15	

SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Voltage Level Shifter- SCL, SDA Lines (x_A & x_B ports) VCCA = 1.2V							
TPHL	Propagation delay	A to B	DDC channels enabled		394		ns
		B to A	DDC channels enabled		347		ns
TPLH	Propagation delay	A to B	DDC channels enabled		504		ns
		B to A	DDC channels enabled		171		ns
T_{FALL}	A port fall time	A-Port	DDC channels enabled		146		ns
T_{FALL}	B port fall time	B-Port	DCC channels enabled		135		ns
T_{RISE}	A port rise time	A-Port	DCC channels enabled		190		ns
T_{RISE}	B port rise time	B-Port	DCC channels enabled		93		ns
FMAX	Maximum switching frequency		DCC channels enabled	400			kHz
Voltage Level Shifter- CEC Line (x_A & x_B ports) VCCA = 1.2V							
TPHL	Propagation delay	A to B	CEC channels enabled		550		ns
		B to A	CEC channels enabled		350		ns
TPLH	Propagation delay	A to B	CEC channels enabled		13		µs
		B to A	CEC channels enabled		290		ns
T_{FALL}	A port fall time	A-Port	CEC channels enabled		146		ns
T_{FALL}	B port fall time	B-Port	CEC channels enabled		200		ns
T_{RISE}	A port rise time	A-Port	CEC channels enabled		190		ns
T_{RISE}	B port rise time	B-Port	CEC channels enabled		16.4		µs
Voltage Level Shifter- HPD Line (x_A & x_B ports) VCCA = 1.2V							
TPHL	Propagation delay	B to A	CEC channels enabled		10.4		ns
TPLH	Propagation delay	B to A	CEC channels enabled		9.9		ns
T_{FALL}	A port fall time	A-Port	CEC channels enabled		0.7		ns
T_{RISE}	A port rise time	A-Port	CEC channels enabled		0.8		ns
Voltage Level Shifter- SCL, SDA Lines (x_A & x_B ports) VCCA = 1.5V							
TPHL	Propagation delay	A to B	DDC channels enabled		375		ns
		B to A	DDC channels enabled		272		ns
TPLH	Propagation delay	A to B	DDC channels enabled		488		ns
		B to A	DDC channels enabled		166		ns
T_{FALL}	A port fall time	A-Port	DDC channels enabled		114		ns
T_{FALL}	B port fall time	B-Port	DCC channels enabled		135		ns
T_{RISE}	A port rise time	A-Port	DCC channels enabled		186		ns
T_{RISE}	B port rise time	B-Port	DCC channels enabled		93		ns
FMAX	Maximum switching frequency		DCC channels enabled	400			kHz
Section 3.2B (Voltage Level Shifter- CEC Line (x_A & x_B ports) VCCA = 1.5V							
TPHL	Propagation delay	A to B	CEC channels enabled		536		ns
		B to A	CEC channels enabled		272		ns
TPLH	Propagation delay	A to B	CEC channels enabled		13		µs
		B to A	CEC channels enabled		285		ns
T_{FALL}	A port fall time	A-Port	CEC channels enabled		113		ns
T_{FALL}	B port fall time	B-Port	CEC channels enabled		201		ns
T_{RISE}	A port rise time	A-Port	CEC channels enabled		187		ns

SWITCHING CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{RISE}	B port rise time	B-Port	CEC channels enabled		16		µs
Section 3.2C (Voltage Level Shifter- HPD Line (x_A & x_B ports) VCCA = 1.5V							
TPHL	Propagation delay	B to A	CEC channels enabled		10		ns
TPLH	Propagation delay	B to A	CEC channels enabled		10		ns
T_{FALL}	A port fall time	A-Port	CEC channels enabled		0.46		ns
T_{RISE}	A port rise time	A-Port	CEC channels enabled		0.5		ns
Section 3.3A (Voltage Level Shifter- SCL, SDA Lines (x_A & x_B ports) VCCA = 1.8V							
TPHL	Propagation delay	A to B	DDC channels enabled		370		ns
		B to A	DDC channels enabled		230		ns
TPLH	Propagation delay	A to B	DDC channels enabled		480		ns
		B to A	DDC channels enabled		163		ns
T_{FALL}	A port fall time	A-Port	DDC channels enabled		100		ns
T_{FALL}	B port fall time	B-Port	DCC channels enabled		135		ns
T_{RISE}	A port rise time	A-Port	DCC channels enabled		180		ns
T_{RISE}	B port rise time	B-Port	DCC channels enabled		93		ns
FMAX	Maximum switching frequency		DCC channels enabled	400			kHz
Section 3.3B (Voltage Level Shifter- CEC Line (x_A & x_B ports) VCCA = 1.8V							
TPHL	Propagation delay	A to B	CEC channels enabled		530		ns
		B to A	CEC channels enabled		230		ns
TPLH	Propagation delay	A to B	CEC channels enabled		13		µs
		B to A	CEC channels enabled		280		ns
T_{FALL}	A port fall time	A-Port	CEC channels enabled		98		ns
T_{FALL}	B port fall time	B-Port	CEC channels enabled		200		ns
T_{RISE}	A port rise time	A-Port	CEC channels enabled		180		ns
T_{RISE}	B port rise time	B-Port	CEC channels enabled		16		µs
Section 3.3C (Voltage Level Shifter- HPD Line (x_A & x_B ports) VCCA = 1.8V							
TPHL	Propagation delay	B to A	CEC channels enabled		10		ns
TPLH	Propagation delay	B to A	CEC channels enabled		10		ns
T_{FALL}	A port fall time	A-Port	CEC channels enabled		0.41		ns
T_{RISE}	A port rise time	A-Port	CEC channels enabled		0.41		ns
Section 3.4A (Voltage Level Shifter- SCL, SDA Lines (x_A & x_B ports) VCCA = 2.5V							
TPHL	Propagation delay	A to B	DDC channels enabled		370		ns
		B to A	DDC channels enabled		185		ns
TPLH	Propagation delay	A to B	DDC channels enabled		467		ns
		B to A	DDC channels enabled		160		ns
T_{FALL}	A port fall time	A-Port	DDC channels enabled		80		ns
T_{FALL}	B port fall time	B-Port	DCC channels enabled		135		ns
T_{RISE}	A port rise time	A-Port	DCC channels enabled		179		ns
T_{RISE}	B port rise time	B-Port	DCC channels enabled		93		ns
FMAX	Maximum switching frequency		DCC channels enabled	400			kHz

SWITCHING CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		PINS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Section 3.4B (Voltage Level Shifter- CEC Line (x_A & x_B ports) VCCA = 2.5V							
TPHL	Propagation delay	A to B	CEC channels enabled		530		ns
		B to A	CEC channels enabled		185		ns
TPLH	Propagation delay	A to B	CEC channels enabled		13		µs
		B to A	CEC channels enabled		275		ns
T_{FALL}	A port fall time	A-Port	CEC channels enabled		80		ns
T_{FALL}	B port fall time	B-Port	CEC channels enabled		200		ns
T_{RISE}	A port rise time	A-Port	CEC channels enabled		180		ns
T_{RISE}	B port rise time	B-Port	CEC channels enabled		16		µs
Section 3.4C (Voltage Level Shifter- HPD Line (x_A & x_B ports) VCCA = 2.5V							
TPHL	Propagation delay	B to A	CEC channels enabled		10		ns
TPLH	Propagation delay	B to A	CEC channels enabled		10		ns
T_{FALL}	A port fall time	A-Port	CEC channels enabled		0.35		ns
T_{RISE}	A port rise time	A-Port	CEC channels enabled		0.35		ns
Section 3.5A (Voltage Level Shifter- SCL, SDA Lines (x_A & x_B ports) VCCA = 3.3V							
TPHL	Propagation delay	A to B	DDC channels enabled		370		ns
		B to A	DDC channels enabled		160		ns
TPLH	Propagation delay	A to B	DDC channels enabled		460		ns
		B to A	DDC channels enabled		155		ns
T_{FALL}	A port fall time	A-Port	DDC channels enabled		75		ns
T_{FALL}	B port fall time	B-Port	DCC channels enabled		135		ns
T_{RISE}	A port rise time	A-Port	DCC channels enabled		180		ns
T_{RISE}	B port rise time	B-Port	DCC channels enabled		93		ns
FMAX	Maximum switching frequency		DCC channels enabled	400			kHz
Section 3.5B (Voltage Level Shifter- CEC Line (x_A & x_B ports) VCCA = 3.3V							
TPHL	Propagation delay	A to B	CEC channels enabled		530		ns
		B to A	CEC channels enabled		160		ns
TPLH	Propagation delay	A to B	CEC channels enabled		13		µs
		B to A	CEC channels enabled		275		ns
T_{FALL}	A port fall time	A-Port	CEC channels enabled		73		ns
T_{FALL}	B port fall time	B-Port	CEC channels enabled		200		ns
T_{RISE}	A port rise time	A-Port	CEC channels enabled		180		ns
T_{RISE}	B port rise time	B-Port	CEC channels enabled		16		µs
Section 3.5C (Voltage Level Shifter- HPD Line (x_A & x_B ports) VCCA = 3.3V							
TPHL	Propagation delay	B to A	CEC channels enabled		10		ns
TPLH	Propagation delay	B to A	CEC channels enabled		10		ns
T_{FALL}	A port fall time	A-Port	CEC channels enabled		0.34		ns
T_{RISE}	A port rise time	A-Port	CEC channels enabled		0.36		ns

TYPICAL CHARACTERISTICS

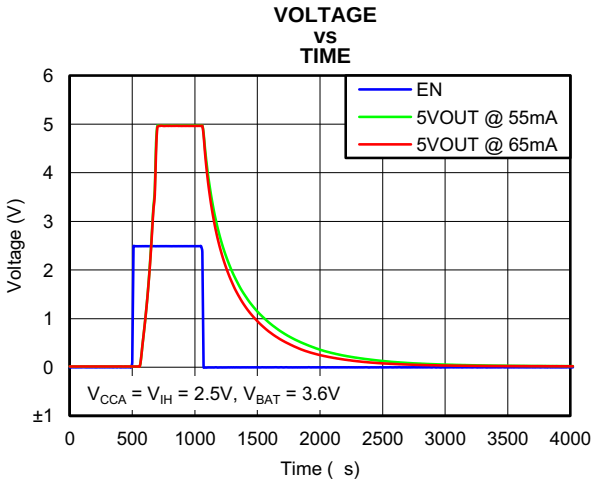


Figure 3.

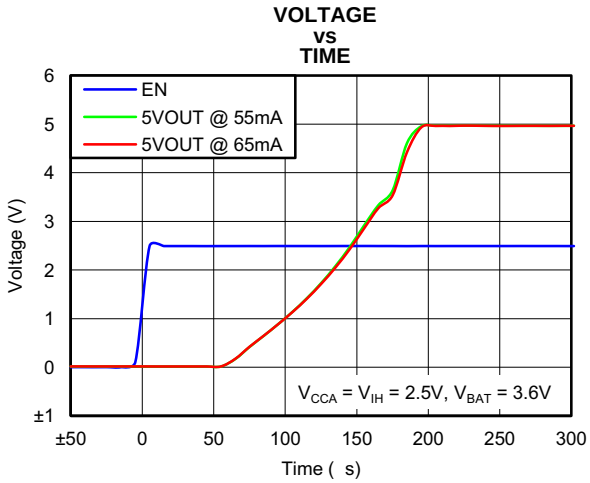


Figure 4.

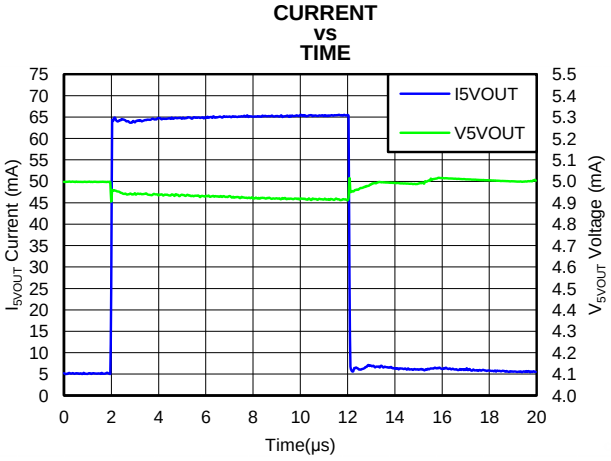


Figure 5.

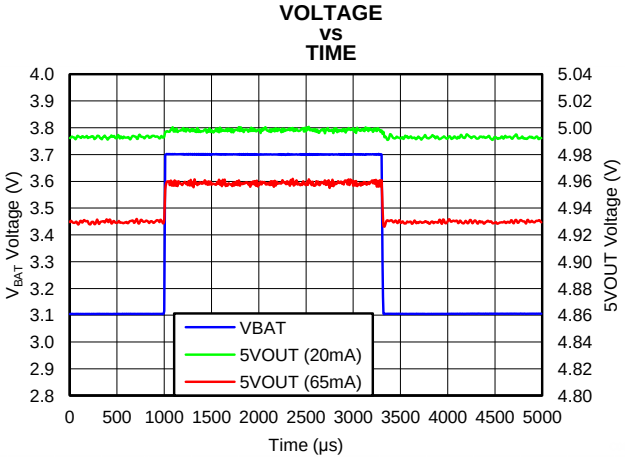


Figure 6.

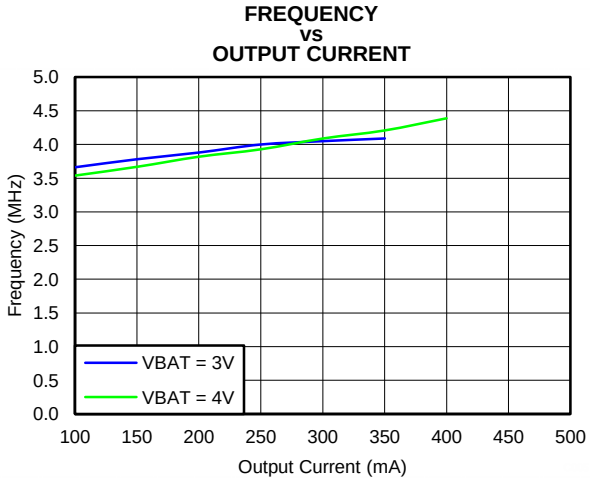


Figure 7.

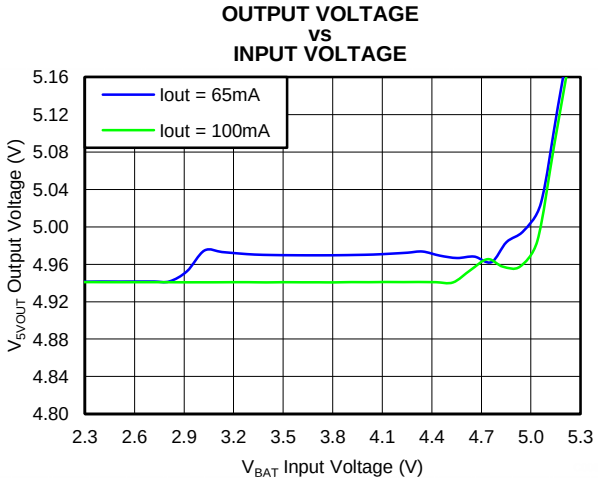


Figure 8.

TYPICAL CHARACTERISTICS (continued)

SUPPLY CURRENT vs SUPPLY VOLTAGE

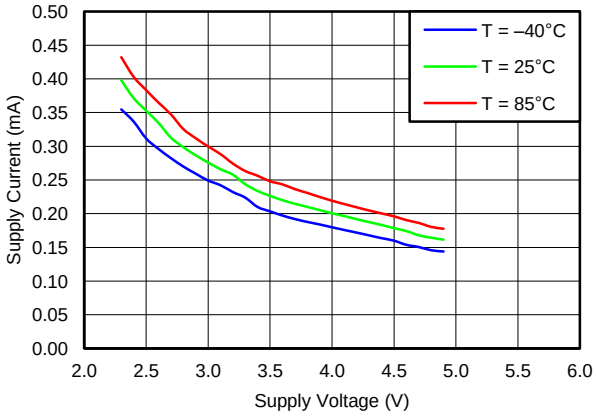


Figure 9.

VOLTAGE AND CURRENT vs TIME

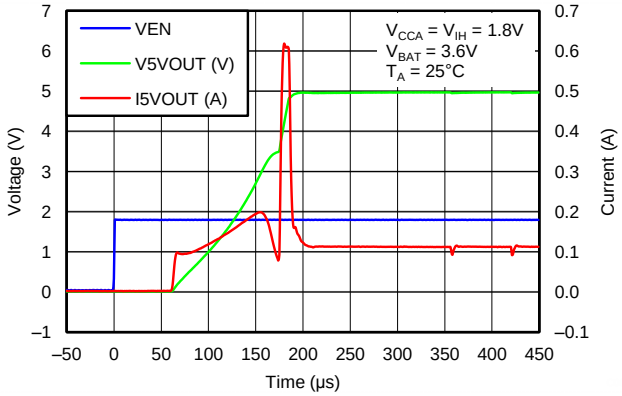


Figure 10.

OUTPUT VOLTAGE vs OUTPUT CURRENT

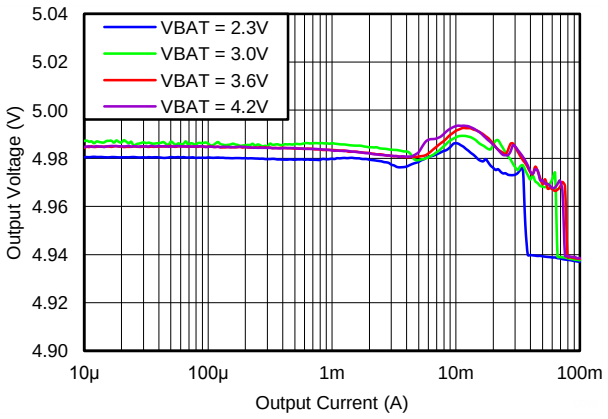


Figure 11.

EFFICIENCY vs INPUT VOLTAGE

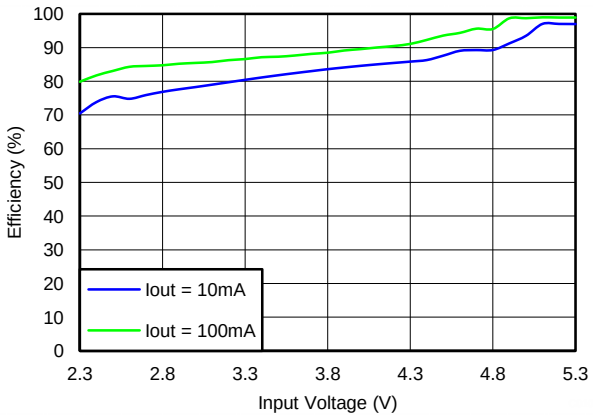


Figure 12.

EFFICIENCY vs OUTPUT CURRENT

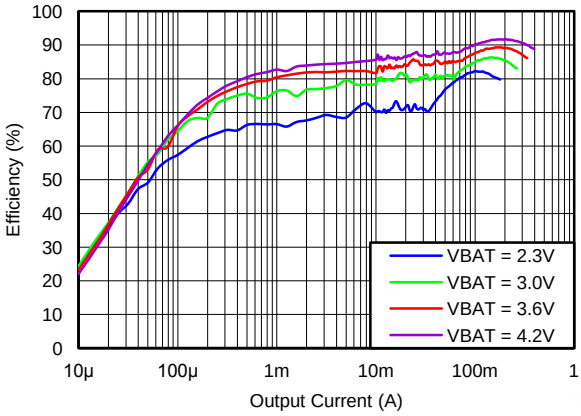


Figure 13.

APPLICATION INFORMATION

DDC/CEC Level Shift Circuit Operation

The TPD5S115 enables DDC translation from VCCA (system side) voltage levels to 5 V (HDMI cable side) voltage levels without degradation of system performance. The TPD5S115 contains 2 bidirectional open-drain buffers specifically designed to support up-translation/down-translation between the low voltage, VCCA side DDC-bus and the 5 V DDC-bus. The port B I/Os are over-voltage tolerant to 5.5 V even when the device is un-powered. After power-up and with the LS_OE and EN pins HIGH, a LOW level on port A (below approximately V_{ILC} = 0.08 × VCCA V) turns the corresponding port B driver (either SDA or SCL) on and drives port B down to VOLB V. When port A rises above approximately 0.10 × VCCA V, the port B pull-down driver is turned off and the internal pull-up resistor pulls the pin HIGH. When port B falls first and goes below 0.3 × 5VOUT, a CMOS hysteresis input buffer detects the falling edge, turns on the port A driver, and pulls port A down to approximately VOLA = 0.16 × VCCA V. The port B pull-down is not enabled unless the port A voltage goes below VILC. If the port A low voltage goes below VILC, the port B pull-down driver is enabled until port A rises above (V_{ILC} + $\Delta V_{T-HYSTA}$), then port B, if not externally driven LOW, will continue to rise being pulled up by the internal pull-up resistor.

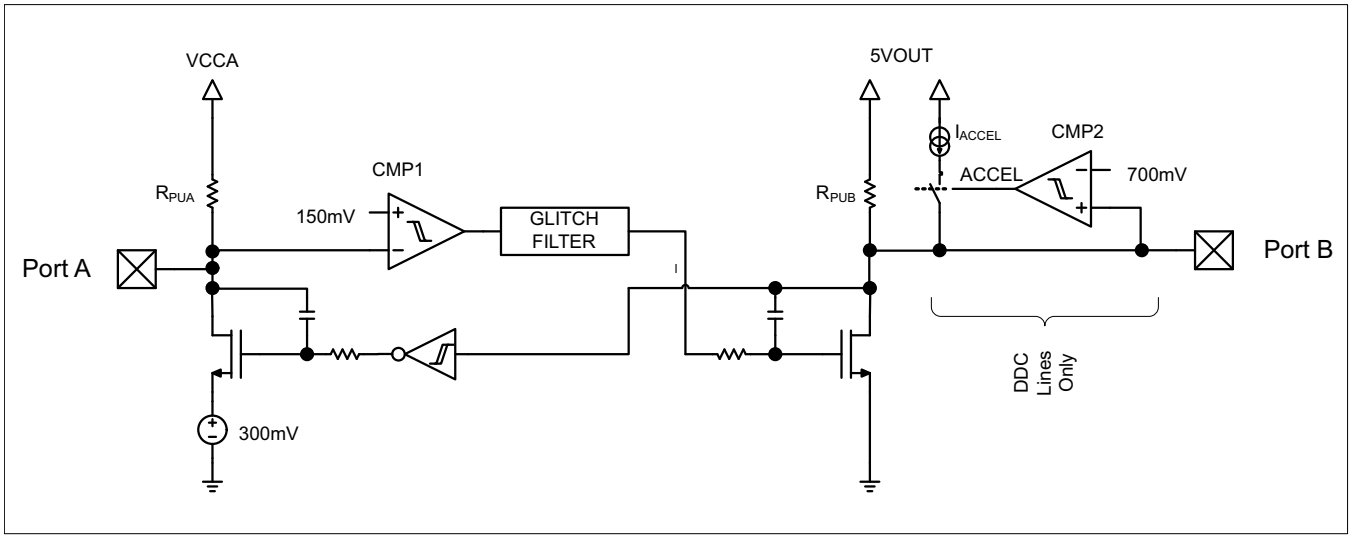


Figure 14. DDC/CEC Level Shifter Block Diagram

DDC/CEC Level Shifter Operational Notes for VCCA=1.8V

- The threshold of CMP1 is ~150 mV ± the 40 mV of total hysteresis.
- The comparator will trip for a falling waveform at ~130 mV
- The comparator will trip for a rising waveform at ~170 mV
- To be recognized as a zero, the level at Port A must first go below 130 mV (V_{ILC} in spec) and then stay below 170 mV (V_{ILA} in spec)
- To be recognized as a one, the level at A must first go above 170mV and then stay above 130 mV
- V_{ILC} is set to 110 mV in Electrical Characteristics Table to give some margin to the 130 mV
- V_{ILA} is set to 140 mV in the Electrical Characteristics Table to give some margin to the 170 mV
- V_{IHA} is set to 70% of VCCA to be consistent with standard CMOS levels

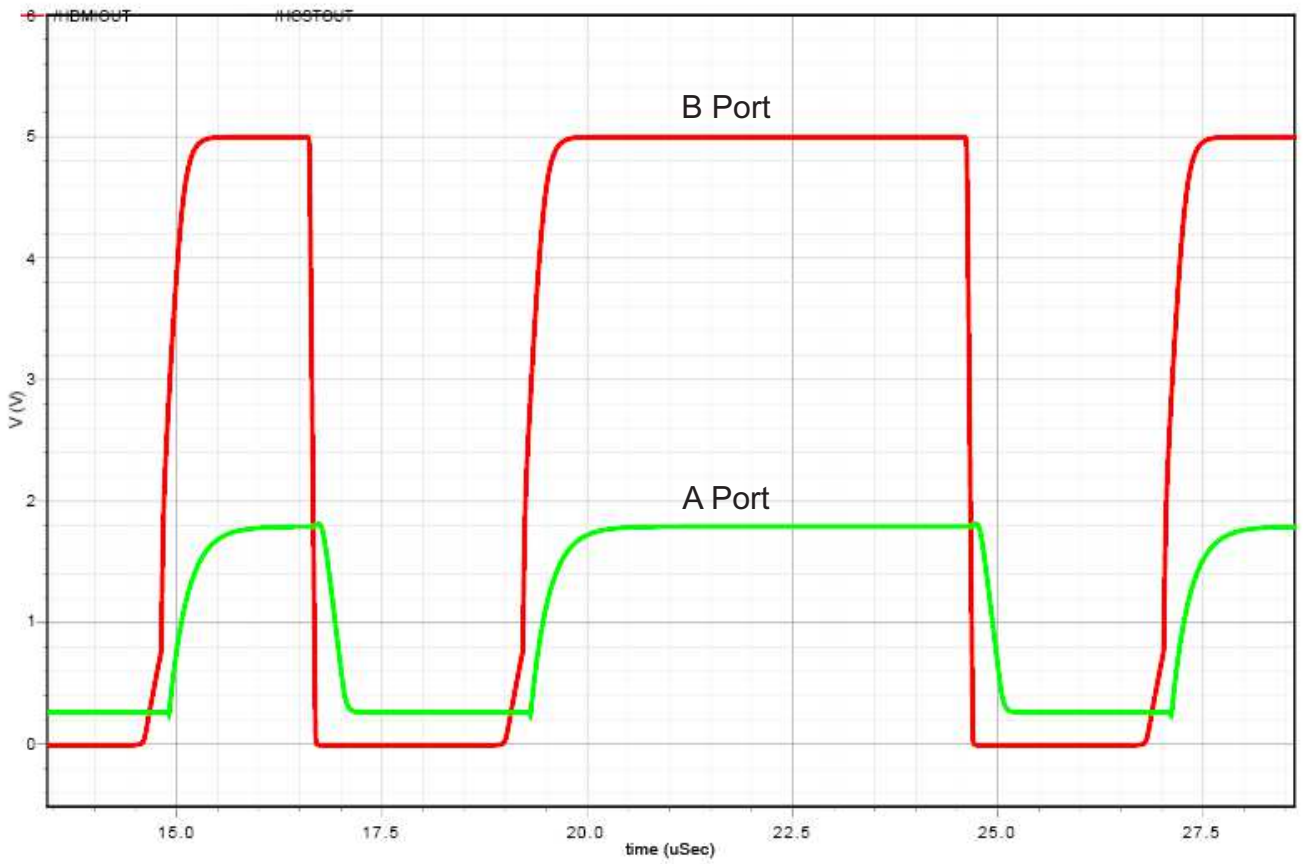


Figure 15. DDC Level Shifter Operation (B to A Direction)

Rise-Time Accelerators

The HDMI cable side of the DDC lines incorporates rise-time accelerators to support the high capacitive load on the HDMI cable side. The rise time accelerator boosts the cable side DDC signal independent of which side of the bus is releasing the signal.

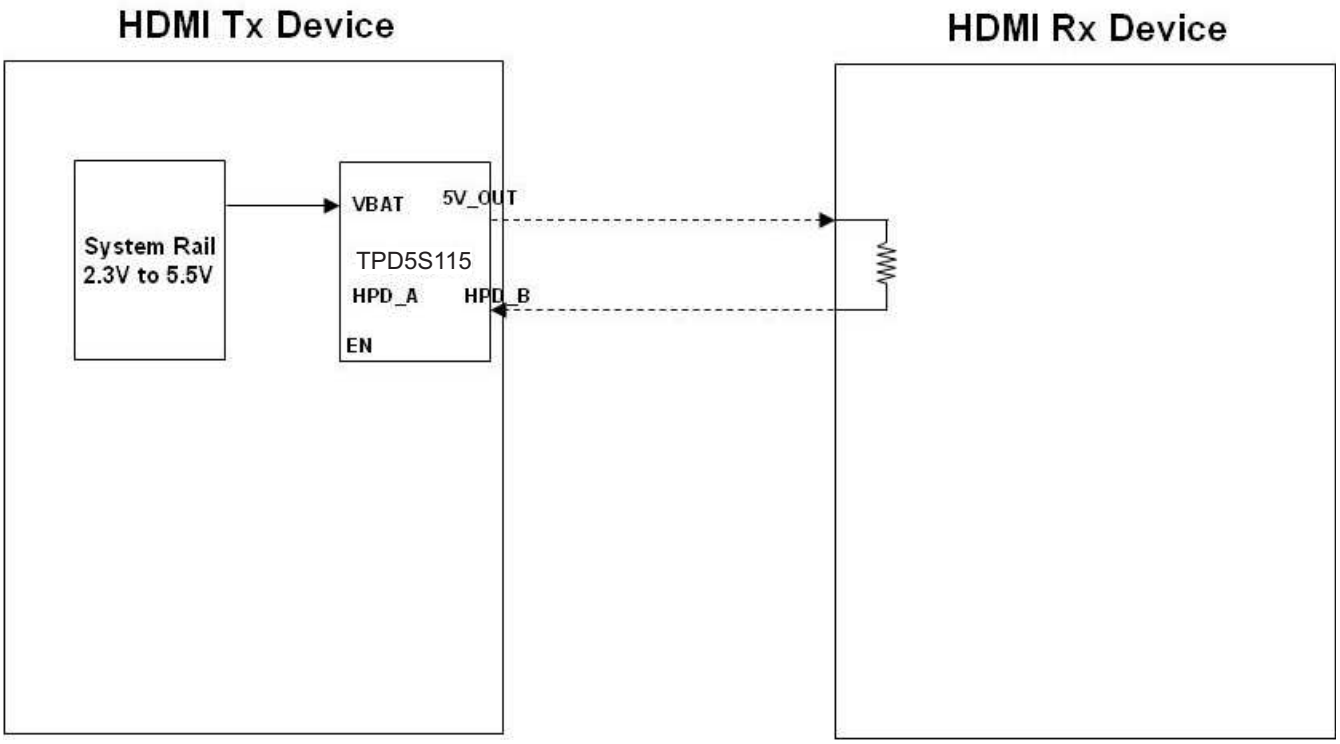


Figure 16. Receiving and transmitting interaction

Hot Plug Detect

Once TPD5S115's DCDC converter and HPD block are enabled through the EN pin, it is ready for continual HDMI receiver detection. Once a HDMI cable connects receiving and transmitting device together, the 5V signal from the DCDC output flows through the receiving device's internal resistor and into HPD's input. The HPD buffer's output then goes high, indicating to the transmitter that a receiving device is connected. To save power, periodic detection can be done by turning on and off the DCDC converter before a receiving device is connected.

Remark: Ground offset between the TPD5S115 ground and the ground of devices on port A of the TPD5S115 must be avoided. The reason for this cautionary remark is that a CMOS/NMOS open-drain capable of sinking 3 mA of current at 0.4 V will have an output resistance of 133 Ω or less (R = E / I). Such a driver will share enough current with the port A output pull-down of the TPD5S115 to be seen as a LOW as long as the ground offset is zero. If the ground offset is greater than 0V, then the driver resistance must be less. Since V_{ILC} can be as low as 90 mV at cold temperatures and the low end of the current distribution, the maximum ground offset should not exceed 50 mV. Bus repeaters that use an output offset are not interoperable with the port A of the TPD5S115 as their output LOW levels will not be recognized by the TPD5S115 as a LOW. If the TPD5S115 is placed in an application where the VIL of port A of the TPD5S115 does not go below its V_{ILC} it will pull port B LOW initially when port A input transitions LOW but the port B will return HIGH, so it will not reproduce the port A input on port B. Such applications should be avoided. Port B is interoperable with all I2C-bus slaves, masters and repeaters.

CEC Level Shift Operation

The CEC level shift function operates in the same manner as the DDC lines except that the CEC line does not need the rise time accelerator function.

Resistor Pull-Up Value Selection

The system is designed to work properly with no external pull-up resistors on the DDC, CEC, and HPD lines.

Power-Save Mode

The TPD5S115 integrates a power save mode to improve efficiency at light load. In power save mode the converter only operates when the output voltage trips below a set threshold voltage. It ramps up the output voltage with several pulses and goes into power save mode once the output voltage exceeds the set threshold voltage. The PFM mode is left and PWM mode entered in case the output current can not longer be supported in PFM mode.

Under-Voltage Lockout

The under voltage lockout circuit prevents the dc/dc converter from malfunctioning at low input voltages and from excessive discharge of the battery. It disables the output stage of the converter once the falling VIN trips the under-voltage lockout threshold VBATUV. The under-voltage lockout threshold V_{BATUV} for falling VIN is typically 2.0 V. The device starts operation once the rising VIN trips under-voltage lockout threshold V_{BATUV} again at typ. 2.1 V.

Enable

The dc/dc converter is enabled when the EN is set to high. At first, the internal reference is activated and the internal analog circuits are settled. Afterwards, the soft start is activated and the output voltage is ramped up. The output voltage reaches its nominal value in typically 250 µs after the device has been enabled. The EN input can be used to control power sequencing in a system with various DC/DC converters. The EN pin can be connected to the output of another converter, to drive the EN pin high and getting a sequencing of supply rails. With EN = GND, the dc/dc enters shutdown mode.

Soft Start

The DC/DC converter has an internal soft start circuit that controls the ramp up of the output voltage. The output voltage reaches its nominal value within t_{Start} of typically 250 µs after EN pin has been pulled to high level. The output voltage ramps up from 5% to its nominal value within t_{Ramp} of typ. 300 µs. This limits the inrush current in the converter during start up and prevents possible input voltage drops when a battery or high impedance power source is used. During soft start, the switch current limit is reduced to 300 mA until the output voltage reaches VIN. Once the output voltage trips this threshold, the device operates with its nominal current limit ILIMF.

Input Capacitor

Due to the nature of the boost converter having a pulsating input current, a low ESR input capacitor is required to prevent large voltage transients that can cause misbehavior of the device or interferences with other circuits in the system. At least 1.2 µF input capacitor is recommended to improve transient behavior of the regulator and EMI behavior of the total power supply circuit. It is recommended to place a ceramic capacitor as close as possible to the VIN and GND pins and better to use a 4.7 µF capacitor, in order to improve the input noise filtering.

Output Capacitor

For the output capacitor, it is recommended to use small ceramic capacitors placed as close as possible to the VOUT and GND pins of the IC. If, for any reason, the application requires the use of large capacitors which can not be placed close to the IC, using a smaller ceramic capacitor in parallel to the large one is recommended. This small capacitor should be placed as close as possible to the VOUT and GND pins of the IC. To get an estimate of the recommended minimum output capacitance, Equation 1 can be used.

$$C_{min} = \frac{I_{OUT} \times (V_{OUT} - V_{IN})}{f \times \Delta V \times V_{OUT}} \quad (1)$$

Parameter f is the switching frequency and ΔV is the maximum allowed ripple. With a chosen ripple voltage of 10 mV, a minimum effective capacitance of 2.7 µF is needed. The total ripple is larger due to the ESR of the output capacitor. This additional component of the ripple can be calculated using:

$$\Delta V_{ESR} = I_{OUT} \times R_{ESR}$$

A capacitor with a value in the range of the calculated minimum should be used. This is required to maintain control loop stability. There are no additional requirements regarding minimum ESR. There is no upper limit for the output capacitance value. Larger capacitors cause lower output voltage ripple as well as lower output voltage drop during load transients.

Note that ceramic capacitors have a DC Bias effect, which will have a strong influence on the final effective capacitance needed. Therefore the right capacitor value has to be chosen very carefully. Package size and voltage rating in combination with material are responsible for differences between the rated capacitor value and the effective capacitance. The minimum effective capacitance value should be 1.2 µF but preferred value is about 4.7 µF

Table 1. Passive Components: Recommended Minimum Effective Values

Component	Min	Target	Max	Units
CIN	1.2	4.7	6.5	µF
COUT	1.2	4.7	10	µF
LIN	0.7	1.0	1.3	µH

TPD5S115 Board layout

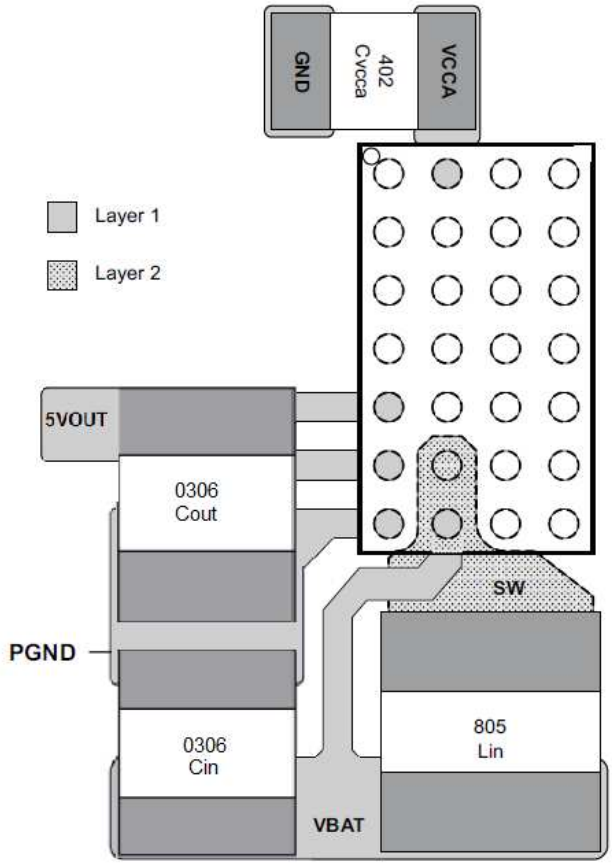


Figure 17. Board Layout (DC-DC Components) (Top View)

List of components:

- L_{IN} = MURATA LQM21PN1R0MC0 (1.0 µH, 800 mA, 0805, Shielded)
- C_{IN} = C_{OUT} = MURATA LLL31MR70J475MA01 (4.7 µF, Low ESL type, 6.3 V, 0306, X7R)
- C_{VCCA} = MURATA GRM155R60J475ME87D (0.1 µF, 6.3 V, 0402, X5R)

REVISION HISTORY

Changes from Revision A (February 2013) to Revision B	Page
• Changed Board Layout section	19

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPD5S115YFFR	ACTIVE	DSBGA	YFF	16	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	RE115	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

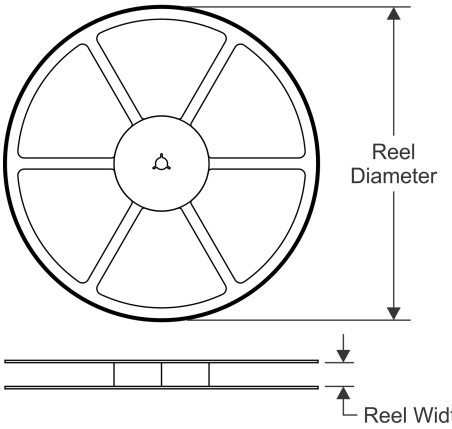
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

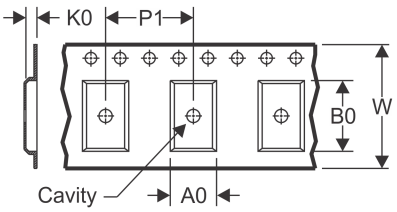
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

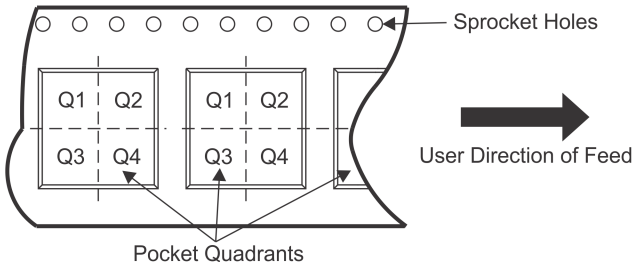


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

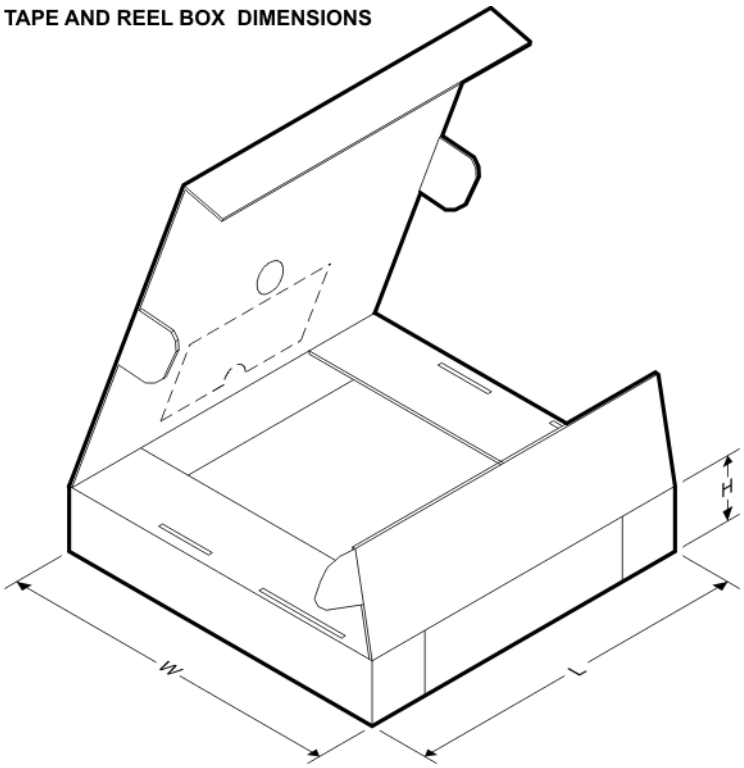
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD5S115YFFR	DSBGA	YFF	16	3000	180.0	8.4	1.84	1.84	0.69	4.0	8.0	Q1

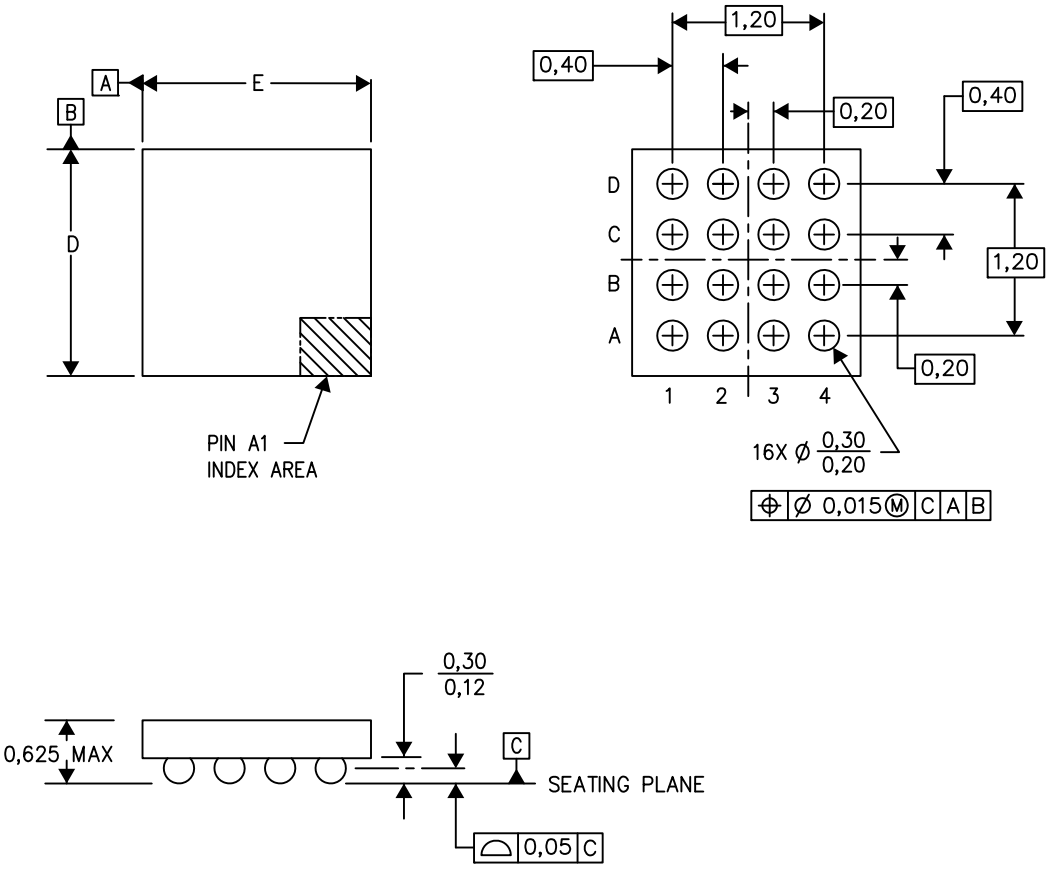
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD5S115YFFR	DSBGA	YFF	16	3000	210.0	185.0	35.0

YFF (S–XBGA–N16) DIE–SIZE BALL GRID ARRAY



D: Max = 1.768 mm, Min =1.708 mm

E: Max = 1.768 mm, Min =1.708 mm

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NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

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