

## SINGLE DIFFERENTIAL COMPARATOR

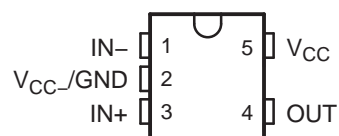
 Check for Samples: [TL331-EP](#)

### FEATURES

- Single Supply or Dual Supplies
- Wide Range of Supply Voltage: 2 V to 36 V
- Low Supply-Current Drain Independent of Supply Voltage: 0.4 mA Typ.
- Low Input Bias Current: 25 nA Typ.
- Low Input Offset Voltage: 2 mV Typ.
- Common-Mode Input Voltage Range Includes Ground
- Differential Input Voltage Range Equal to Maximum-Rated Supply Voltage:  $\pm 36$  V
- Low Output Saturation Voltage
- Output Compatible With TTL, MOS, and CMOS

### SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- Controlled Baseline
- One Assembly and Test Site
- One Fabrication Site
- Available in Military ( $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ) Temperature Range
- Extended Product Life Cycle
- Extended Product-Change Notification
- Product Traceability

 DBV PACKAGE  
(TOP VIEW)


### DESCRIPTION/ORDERING INFORMATION

This device consists of a single voltage comparator designed to operate from a single power supply over a wide range of voltages. Operation from dual supplies also is possible if the difference between the two supplies is 2 V to 36 V and  $V_{CC}$  is at least 1.5 V more positive than the input common-mode voltage. Current drain is independent of the supply voltage. To achieve wired-AND relationships, one can connect the output to other open-collector outputs.

#### ORDERING INFORMATION<sup>(1)</sup>

| $T_A$  | $V_{IO(MAX)}$ at $25^{\circ}\text{C}$ | PACKAGE      | ORDERABLE PART NUMBER | TOP-SIDE MARKING | VID NUMBER |                |
|--|---------------------------------------|--------------|-----------------------|------------------|------------|----------------|
| $-55^{\circ}\text{C}$ to $125^{\circ}\text{C}$ | 5 mV                                  | SOT-23 (DBV) | Reel of 3000          | TL331MDBVREP     | TEPU       | V62/13611-01XE |
|  |                                       |              | Reel of 250           | TL331MDBVTEP     |            |                |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).

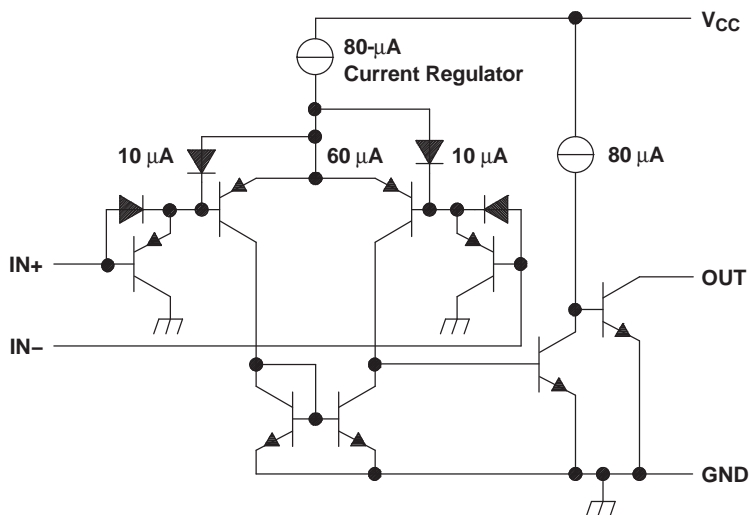


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LOGIC DIAGRAM



SCHEMATIC



| COMPONENT COUNT |    |
|-----------------|----|
| Epi-FET         | 1  |
| Diodes          | 2  |
| Resistors       | 1  |
| Transistors     | 20 |

Note: Current values shown are nominal.

ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

|           |   |                |
|-----------|---|----------------|
| $V_{CC}$  | Supply voltage <sup>(2)</sup>                             | 36 V           |
| $V_{ID}$  | Differential input voltage <sup>(3)</sup>                 | $\pm 36$ V     |
| $V_I$     | Input voltage range (either input)                        | -0.3 V to 36 V |
| $V_O$     | Output voltage  | 36 V           |
| $I_O$     | Output current  | 20 mA          |
|           | Duration of output short-circuit to ground <sup>(4)</sup> | Unlimited      |
| $T_J$     | Operating virtual junction temperature                    | 150°C          |
| $T_{stg}$ | Storage temperature range                                 | -65°C to 150°C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential voltages, are with respect to the network ground.
- (3) Differential voltages are at IN+ with respect to IN-.
- (4) Short circuits from outputs to  $V_{CC}$  can cause excessive heating and eventual destruction.

## THERMAL INFORMATION

| THERMAL METRIC <sup>(1)</sup> |   | TL331-EP |  | UNITS |
|-------------------------------|---|----------|--|-------|
|                               |   | DBV      |  |       |
|                               |   | 5 PINS   |  |       |
| $\theta_{JA}$                 | Junction-to-ambient thermal resistance <sup>(2)</sup>       | 299      |  | °C/W  |
| $\theta_{JCTop}$              | Junction-to-case (top) thermal resistance <sup>(3)</sup>    | 65.4     |  |       |
| $\theta_{JB}$                 | Junction-to-board thermal resistance <sup>(4)</sup>         | 97.1     |  |       |
| $\psi_{JT}$                   | Junction-to-top characterization parameter <sup>(5)</sup>   | 0.8      |  |       |
| $\psi_{JB}$                   | Junction-to-board characterization parameter <sup>(6)</sup> | 95.5     |  |       |
| $\theta_{JCbott}$             | Junction-to-case (bottom) thermal resistance <sup>(7)</sup> | N/A      |  |       |

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
- (5) The junction-to-top characterization parameter,  $\psi_{JT}$ , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining  $\theta_{JA}$ , using a procedure described in JESD51-2a (sections 6 and 7).
- (6) The junction-to-board characterization parameter,  $\psi_{JB}$ , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining  $\theta_{JA}$ , using a procedure described in JESD51-2a (sections 6 and 7).
- (7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

## ELECTRICAL CHARACTERISTICS

at specified free-air temperature,  $V_{CC} = 5\text{ V}$  (unless otherwise noted)

| PARAMETER |   | TEST CONDITIONS <sup>(1)</sup>   | $T_A$          | MIN | TYP                    | MAX  | UNIT          |
|-----------|---|--|----------------|-----|------------------------|------|---------------|
| $V_{IO}$  | Input offset voltage                            | $V_{CC} = 5\text{ V}$ to $30\text{ V}$ , $V_O = 1.4\text{ V}$ ,<br>$V_{IC} = V_{IC(min)}$                      | 25°C           |     | 2                      | 5    | mV            |
|           |   |  | –55°C to 125°C |     |                        | 9    |               |
| $I_{IO}$  | Input offset current                            | $V_O = 1.4\text{ V}$   | 25°C           |     | 5                      | 50   | nA            |
|           |   |  | –55°C to 125°C |     |                        | 250  |               |
| $I_{IB}$  | Input bias current                              | $V_O = 1.4\text{ V}$   | 25°C           |     | –25                    | –250 | nA            |
|           |   |  | –55°C to 125°C |     |                        | –400 |               |
| $V_{ICR}$ | Common-mode input voltage range <sup>(2)</sup>  |  | 25°C           |     | 0 to<br>$V_{CC} - 1.5$ |      | V             |
|           |   |  | –55°C to 125°C |     | 0 to<br>$V_{CC} - 2$   |      |               |
| $A_{VD}$  | Large-signal differential-voltage amplification | $V_{CC} = 15\text{ V}$ , $V_O = 1.4\text{ V}$ to $11.4\text{ V}$ ,<br>$R_L \geq 15\text{ k}\Omega$ to $V_{CC}$ | 25°C           |     | 50                     | 200  | V/mV          |
| $I_{OH}$  | High-level output current                       | $V_{OH} = 5\text{ V}$ , $V_{ID} = 1\text{ V}$  | 25°C           |     | 0.1                    | 50   | nA            |
|           |   | $V_{OH} = 30\text{ V}$ , $V_{ID} = 1\text{ V}$   | –55°C to 125°C |     |                        | 1    | $\mu\text{A}$ |
| $V_{OL}$  | Low-level output voltage                        | $I_{OL} = 4\text{ mA}$ , $V_{ID} = -1\text{ V}$  | 25°C           |     | 150                    | 400  | mV            |
|           |   |  | –55°C to 125°C |     |                        | 700  |               |
| $I_{OL}$  | Low-level output current                        | $V_{OL} = 1.5\text{ V}$ , $V_{ID} = -1\text{ V}$   | 25°C           |     | 6                      |      | mA            |
| $I_{CC}$  | Supply current                                  | $R_L = \infty$ , $V_{CC} = 5\text{ V}$   | 25°C           |     | 0.4                    | 0.7  | mA            |

- (1) All characteristics are measured with zero common-mode input voltage, unless otherwise specified.
- (2) The voltage at either input or common-mode should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is  $V_{CC+} - 1.5\text{ V}$ , but either or both inputs can go to 30 V without damage.

**SWITCHING CHARACTERISTICS** $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ 

| PARAMETER     | TEST CONDITIONS  | TYP                                   | UNIT |
|---------------|--|---------------------------------------|------|
| Response time | $R_L$ connected to 5 V through 5.1 k $\Omega$ , $C_L = 15\text{ pF}^{(1) (2)}$ | 100-mV input step with 5-mV overdrive | 1.3  |
|               |  | TTL-level input step                  | 0.3  |

(1)  $C_L$  includes probe and jig capacitance.

(2) The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)         | Lead/Ball Finish | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|------------------|----------------------|--------------|-------------------------|---------|
| TL331MDBVREP     | PREVIEW       | SOT-23       | DBV             | 5    | 3000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -55 to 125   | TEPU                    |         |
| TL331MDBVTEP     | PREVIEW       | SOT-23       | DBV             | 5    | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -55 to 125   | TEPU                    |         |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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**OTHER QUALIFIED VERSIONS OF TL331-EP :**

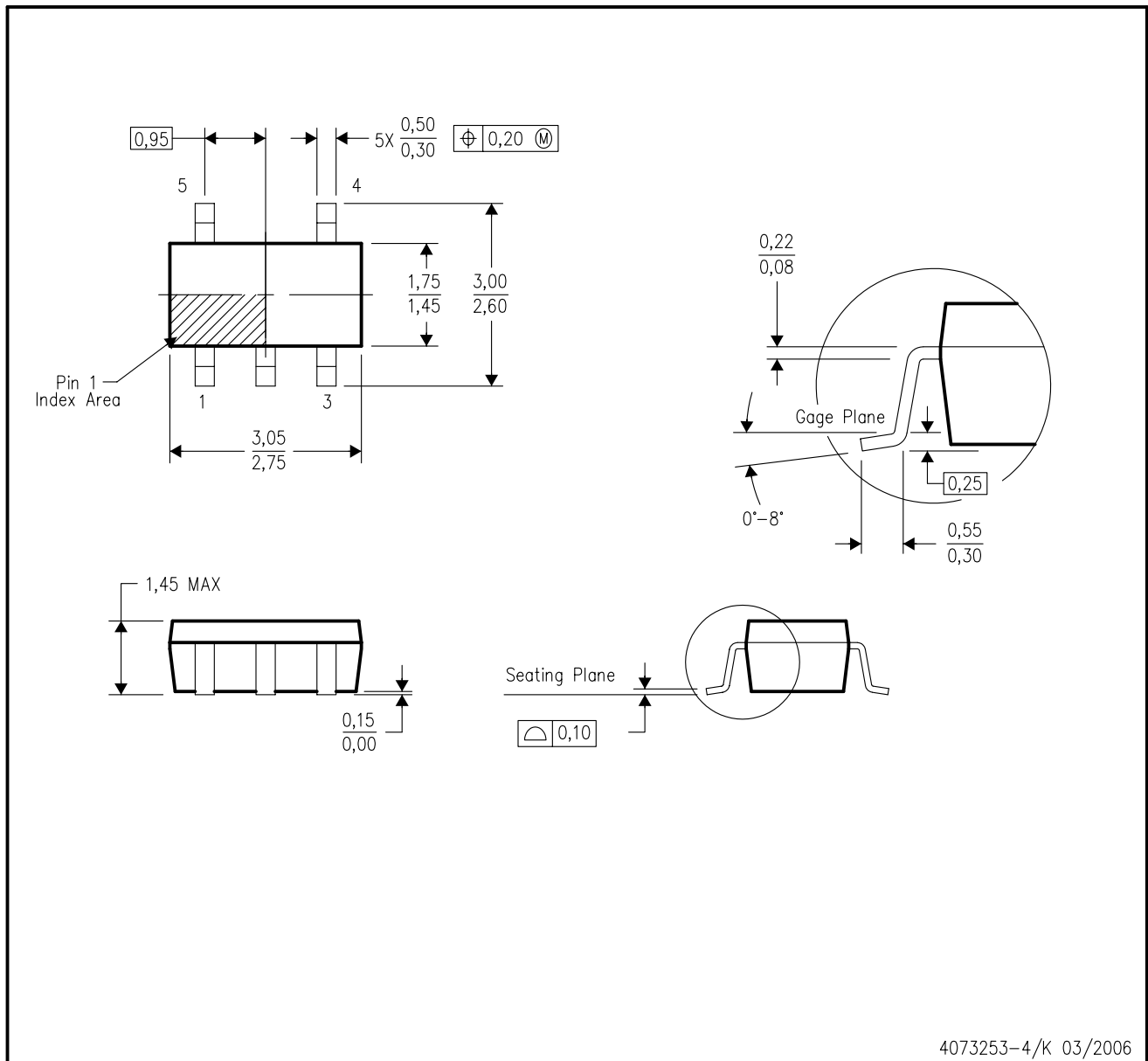
- Catalog: [TL331](#)
- Automotive: [TL331-Q1](#)

## NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



4073253-4/K 03/2006

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



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|                               |  |
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