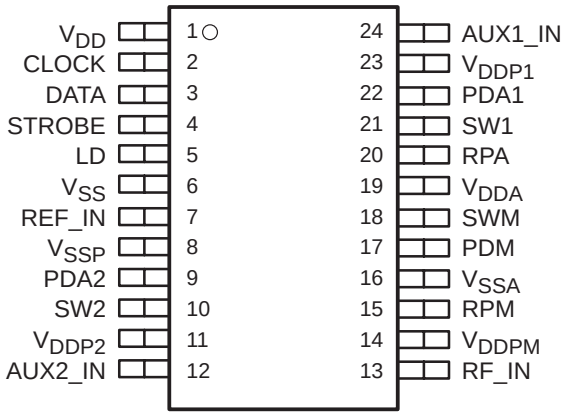
- **Three Separate Loops: 1 UHF and 2 VHF**
- **Operation to 1.2-GHz for Main Synthesizer**
- **Operation to 250 MHz for Auxiliary Synthesizers**
- **Fast Lock-up Time**
- **High-Speed Serial Data Bus**
- **Low Power Consumption**
- **Ideal for Global Systems for Mobile Communications (GSM) Applications**

PW PACKAGE
(TOP VIEW)



description

The Texas Instruments (TI™) TRF2020 is an integrated high performance frequency synthesizer device. The TRF2020 consists of one main 1.2-GHz synthesizer and two auxiliary 250-MHz synthesizers. Each synthesizer has an independent dual-modulus prescaler and separate powerdown modes. These features provide maximum flexibility for the design of 900-MHz wireless systems.

The main synthesizer consists of a 32/33-modulus prescaler with an 11-bit counter, a phase-frequency detector, and a charge pump. The phase-frequency detector is referenced to an internal reference frequency that is derived from an external TCXO signal. The phase-frequency detector is also provided with a dead-zone compensation circuit that reduces synthesizer phase noise during locked conditions.

Each auxiliary synthesizer consists of an independent 8/9-modulus prescaler with an 11-bit counter, a phase-frequency detector, and a charge pump. Similar to the main synthesizer, each auxiliary synthesizer's phase-frequency detector is referenced to an internal reference frequency that is derived from an external TCXO signal.

The external TCXO signal is prescaled by an 11-bit counter and then distributed to three independent postscalers. Each postscaler provides a selectable, divide-by-1, -2, -4, or -8 function before the reference signal is distributed to the associated synthesizer phase detector. The reference frequency prescaler and independent postscalers are software programmable.

To achieve minimum lock-up time, each synthesizer contains a speed-up mode charge pump capable of providing 2 mA output current and an analog switch that can change the loop-filter time constant. The duration of the speed-up mode operations can be independently controlled with software.

The states of the three internal lock detectors are provided on a programmable, combinational logic output; each synthesizer can be selected independently or ANDed together.

The device is programmed over a three-wire, synchronous, serial data bus (clock, data, strobe) with achievable bit rates as high as 20 Mbits/sec. The data is partitioned into words in such a manner that static parameters may be sent once during initialization, and dynamic parameters, such as frequency, may be sent as often as needed.

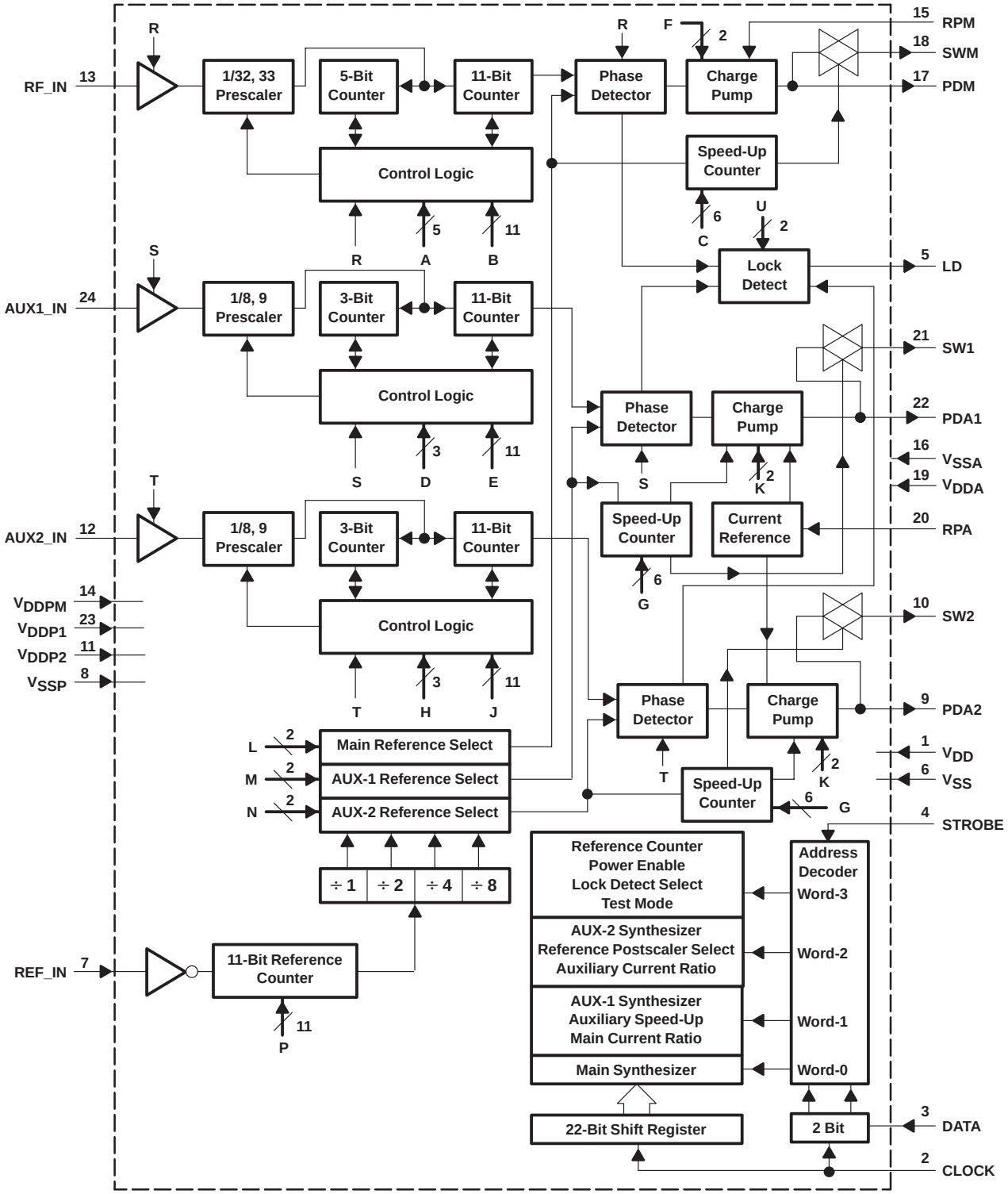
The TRF2020 is offered in a 24-pin plastic thin-shrink small-outline package (TSSOP) and is characterized for free-air operation from –40°C to 85°C.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TI is a trademark of Texas Instruments Incorporated.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AUX1_IN	24	I	RF input auxiliary-1 synthesizer
AUX2_IN	12	I	RF input auxiliary-2 synthesizer
CLOCK	2	I	Clock input
DATA	3	I	Data input
LD	5	O	Lock detect output
PDA1	22	O	Auxiliary-1 synthesizer phase detector output
PDA2	9	O	Auxiliary-2 synthesizer phase detector output
PDM	17	O	Main synthesizer phase detector output
REF_IN	7	I	Reference input
RF_IN	13	I	Main synthesizer RF input
RPA	20	I	Reference current input for AUX-1 and AUX-2 charge pumps
RPM	15	I	Reference current input for main charge pump
STROBE	4	I	Strobe input
SWM	18	O	Main analog switch output
SW1	21	O	Auxiliary-1 analog switch output
SW2	10	O	Auxiliary-2 analog switch output
V_{DD}	1		Digital supply voltage
V_{DDA}	19		Analog supply voltage
V_{DDPM}	14		Main prescaler supply voltage
V_{DDP1}	23		Auxiliary-1 prescaler supply voltage
V_{DDP2}	11		Auxiliary-2 prescaler supply voltage
V_{SS}	6		Digital ground
V_{SSA}	16		Analog ground
V_{SSP}	8		Prescaler ground

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage V_{DDP} . . . . . –0.3 V to 4.6 V
Supply voltage V_{DD}, V_{DDA} . . . . . –0.3 V to 6 V
Voltage applied to any other pin, V_{IN} . . . . . –0.3 V to V_{DD} + 0.3 V
Power dissipation at or below T_A = 25°C . . . . . 300 mW
Junction temperature, T_J . . . . . 150°C
Ambient operating temperature, T_A . . . . . –40°C to 85°C
Storage temperature, T_{STG} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{DDA}	Analog supply voltage	2.75	3	4.5	V
V_{DD}, V_{DDP}	Digital supply voltage	2.75	3	3.6	V
T_A	Operating free-air temperature	–40	25	85	°C
T_J	Junction temperature	–30		105	°C

electrical characteristics with V_{DDA} = 4.5 V, V_{DDP} = V_{DD} = 3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OPER}	Operational supply current	R = S = T = 1 (see Note 1)		11	13	mA
I_{STDBY}	Maximum standby current	R = S = T = 0			10	µA
I_{DDPM}	Main synthesizer operational supply current	R = 1, S = T = 0 (see Note 1)		6	8	mA
I_{DDP1}	Auxiliary-1 synthesizer operational supply current	R = 0, S = 1, T = 0 (see Note 1)		3.3	4.5	mA
I_{DDP2}	Auxiliary-2 synthesizer operational supply current	R = 0, S = 0, T = 1 (see Note 1)		3.3	4.5	mA

NOTES: 1. Operational supply currents measured with RF_IN = 1200 MHz, AUX1_IN = 250 MHz, AUX2_IN = 250 MHz, f_{REF_IN} = 39.6 MHz. All loops are in lock condition and normal mode. Operational supply current = $I_{OPER} = I_{DDA} + I_{DDP1} + I_{DDP2} + I_{DDPM} + I_{DD}$

digital interface characteristics

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage	Clock		0.7 V_{DD}		V_{DD}	V
		Data					
		Strobe					
V_{IL}	Low-level input voltage	Clock		0		0.3 V_{DD}	V
		Data					
		Strobe					
$\|I_{IH}\|$	High-level input current	Clock		0		1	µA
		Data					
		Strobe					
$\|I_{IL}\|$	Low-level input current	Clock		0		1	µA
		Data					
		Strobe					
V_{OH}	High-level output voltage	LD	I_{OH} = 1 mA	V_{DD} – 0.4			V
V_{OL}	Low-level output voltage	LD	I_{OH} = –2 mA			0.4	V

ac electrical characteristics with V_{DDA} = 4.5 V, V_{DDP} = V_{DD} = 3 V, T_A = 25°C (unless otherwise noted)

main loop, RF_IN

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{RF_IN}	Input signal frequency	2.75 ≤ V_{DDP} ≤ 3.5 V			1200	MHz
P_{RF_IN}	Input sensitivity	2.75 ≤ V_{DDP} ≤ 3.5 V, R_{source} = 50 Ω	–20		0	dBm
f_{COMP}	Phase detector comparison	2.75 ≤ V_{DD} ≤ 3.5 V	0		2	MHz

auxiliary loops, AUX1_IN and AUX2_IN

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{AUX_IN}	Input signal frequency	2.75 ≤ V_{DDP} ≤ 3.5 V			250	MHz
P_{AUX_IN}	Input sensitivity	2.75 ≤ V_{DDP} ≤ 3.5 V, R_{source} = 50 Ω	–20		0	dBm
f_{AUX_COMP}	Phase detector comparison	2.75 ≤ V_{DD} ≤ 3.5 V	0		2	MHz

reference divider, REF_IN

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{REF_IN}	Input signal frequency		$2.75 \le V_{DDP} \le 3.5$ V			40	MHz
V_{REF_IN}	Input sensitivity			0.3		$V_{DDP} - 0.8$	V_{p-p}
Z_{REF_IN}	Input impedance	Resistive				100	kΩ
		Capacitive				3	pF

charge pump characteristics

main charge pump output

PARAMETER			TEST CONDITIONS†	MIN	TYP	MAX	UNIT
$\lvert I_{PDM}\rvert$	Output current PDM	normal mode	$V_{PDM} = 0.5\ V_{DDA}$	400	500	600	µA
		speed-up mode		1.5	2	2.5	mA
$\frac{\Delta I_{PDM}}{\lvert I_{PDM}\rvert}$	Relative output current variation PDM (see Figure 1)		RPM 5% tolerance, $V_{SSA} + 0.5 \le V_{PDM} \le V_{DDA} - 0.5$			15	%
ΔI_{PDM}	Output current matching (see Figure 1)		$V_{PDM} = 0.5\ V_{DDA}$			8	%
$\lvert I_{SWM}\rvert$	Analog switch output current SWM, speed-up mode		$V_{SWM} = 0.5\ V_{DDA}$	1.5	2	2.5	mA

† RPM = RPA = 27 kΩ to V_{SSA}, F = K = 10.

auxiliary-1 charge pump output

PARAMETER			TEST CONDITIONS†	MIN	TYP	MAX	UNIT
$\lvert I_{PDA1}\rvert$	Output current PDA1	normal mode	$V_{PDA1} = 0.5\ V_{DDA}$	400	500	600	µA
		speed-up mode		1.5	2	2.5	mA
$\frac{\Delta I_{PDA1}}{\lvert I_{PDA1}\rvert}$	Relative output current variation PDA1 (see Figure 1)		RPA 5% tolerance $V_{SSA} + 0.5 \le V_{PDA1} \le V_{DDA} - 0.5$			15	%
ΔI_{PDA1}	Output current matching (see Figure 1)		$V_{PDA1} = 0.5\ V_{DDA}$			8	%
$\lvert I_{SW1}\rvert$	Analog switch output current SW1, speed-up mode		$V_{SW1} = 0.5\ V_{DDA}$	1.5	2	2.5	mA

† RPM = RPA = 27 kΩ to V_{SSA}, F = K = 10.

auxiliary-2 charge pump output

PARAMETER			TEST CONDITIONS†	MIN	TYP	MAX	UNIT
$\lvert I_{PDA2}\rvert$	Output current PDA2	normal mode	$V_{PDA2} = 0.5\ V_{DDA}$	400	500	600	µA
		speed-up mode		1.5	2	2.5	mA
$\frac{\Delta I_{PDA2}}{\lvert I_{PDA2}\rvert}$	Relative output current variation PDA2 (see Figure 1)		RPA 5% tolerance $V_{SSA} + 0.5 \le V_{PDA2} \le V_{DDA} - 0.5$			15	%
ΔI_{PDA2}	Output current matching (see Figure 1)		$V_{PDA2} = 0.5\ V_{DDA}$			8	%
$\lvert I_{SW2}\rvert$	Analog switch output current SW2, speed-up mode		$V_{SW2} = 0.5\ V_{DDA}$	1.5	2	2.5	mA

† RPM = RPA = 27 kΩ to V_{SSA}, F = K = 10.

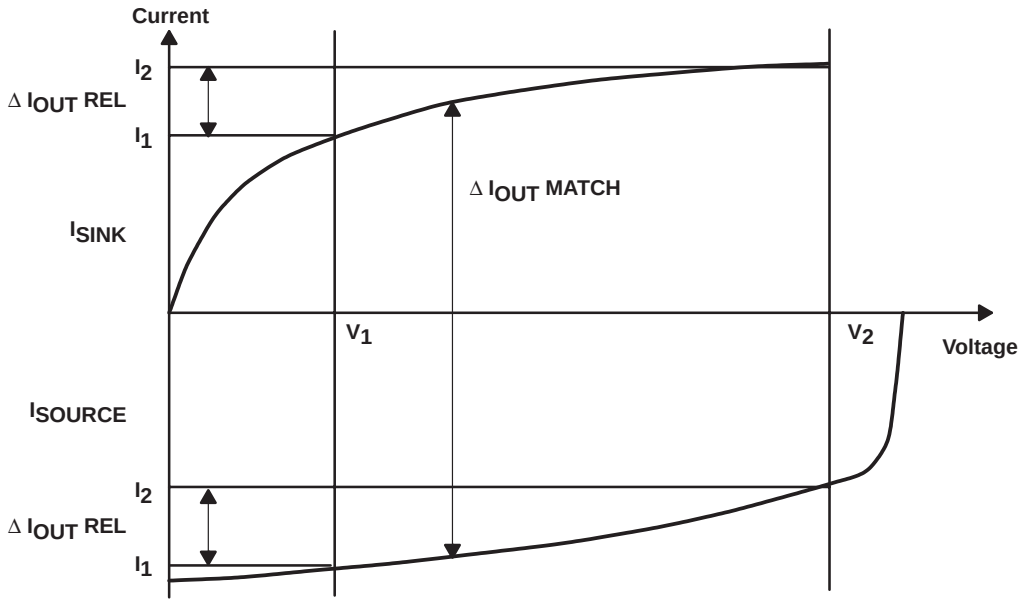


Figure 1. Charge-Pump Output Current Definitions

The relative output current variation is defined as the percent difference between charge-pump current output at two charge-pump output voltages and the mean charge-pump current output:

$$\frac{\Delta I_{OUT\ REL}}{|I_{OUT\ MEAN}|} = 2 \times \frac{(I_2 - I_1)}{|(I_2 + I_1)|} \text{ x } 100\%; \text{ with } V_1 = 0.5\ V,\ V_2 = V_{DDA} - 0.5\ V.$$

Output current matching is defined as the difference in charge-pump sinking current output and charge-pump sourcing current output at a given charge-pump output (see Figure 1).

$\Delta I_{OUT\ MATCH} = I_{SINK} - I_{SOURCE}$; with $V_1 \le$ Voltage $\le V_2$.

charge-pump leakage currents, charge pumps not active

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OZ}	Disabled output current	PDM	$V_O = 0.5V_{DDA}$, RPM = RPA = V_{DDA}, Normal and speed-up modes		10		nA
		PDA1					
		PDA2					
		SWM					
		SW1					
		SW2					

serial interface timing requirements with V_{DDA} = 4.5 V, V_{DDP} = V_{DD} = 3.0 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_I	Input capacitance				10	pF
R_I	Input resistance		10 k			Ω
f_{clock}	CLOCK frequency			13	20	MHz
t_r, t_f	CLOCK input rise and fall time				8	ns
t_w(High)	Pulse duration, CLOCK high		20			ns
t_w(Low)	Pulse duration, CLOCK low		20			ns
t_{su}	Data before CLOCK high		15			ns
	Strobe before CLOCK high	Under continuous operation	15			ns
		First power on or programmed from standby mode	10 × $C_{ext\_coupling}$ × 60 kΩ			µs
t_h	Data after CLOCK high		15			ns
	Strobe after CLOCK high		15			ns
$t_{w(pulse)}$	Strobe pulse width		$\frac{2}{REF\_IN}$			s

PARAMETER MEASUREMENT INFORMATION

The timing relationship between the TRF2020 Data, Clock, and Strobe registers is shown in Figure 2.

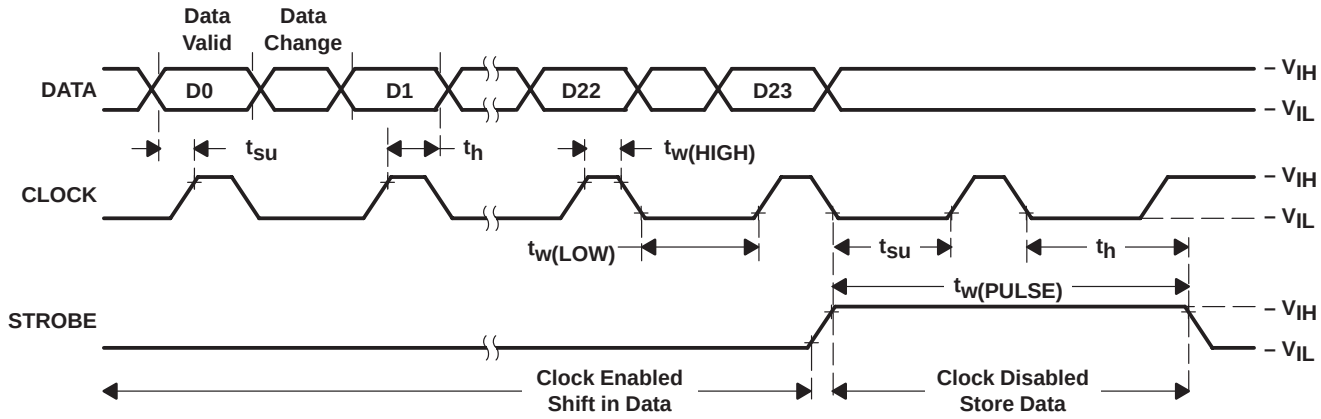


Figure 2. Serial Data Interface Timing

TYPICAL CHARACTERISTICS

MAIN DIVIDER INPUT POWER vs. FREQUENCY AND SUPPLY VOLTAGE

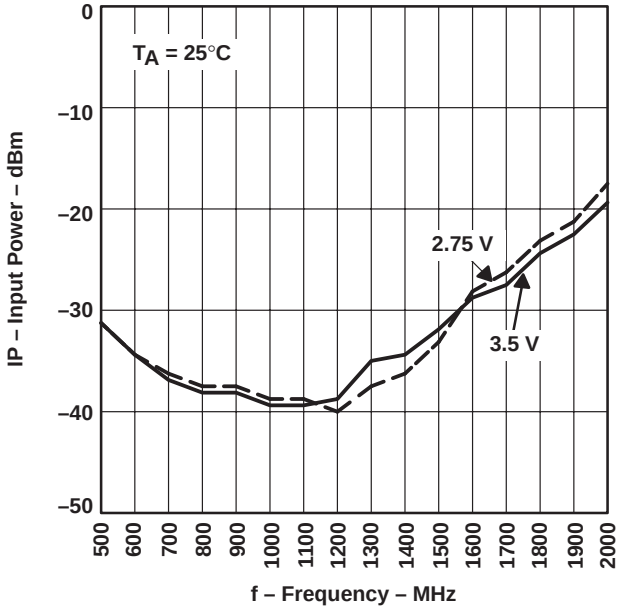


Figure 3

MAIN DIVIDER MINIMUM INPUT POWER vs. FREQUENCY AND TEMPERATURE

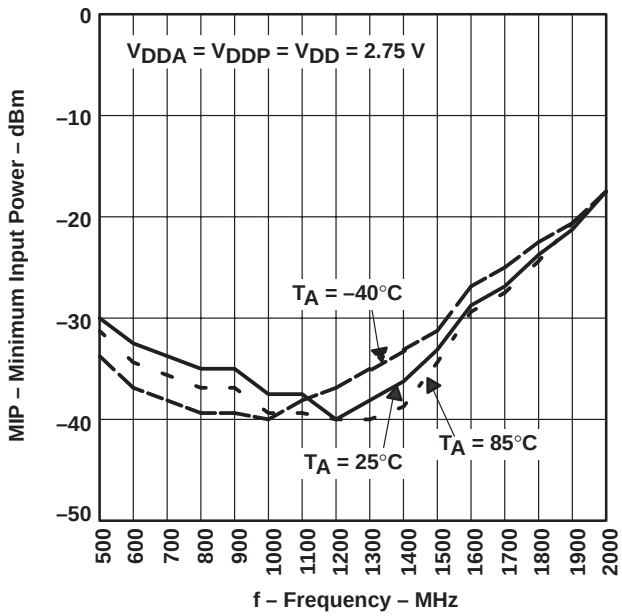


Figure 4

REFERENCE DIVIDER MINIMUM INPUT VOLTAGE vs. FREQUENCY AND SUPPLY VOLTAGE

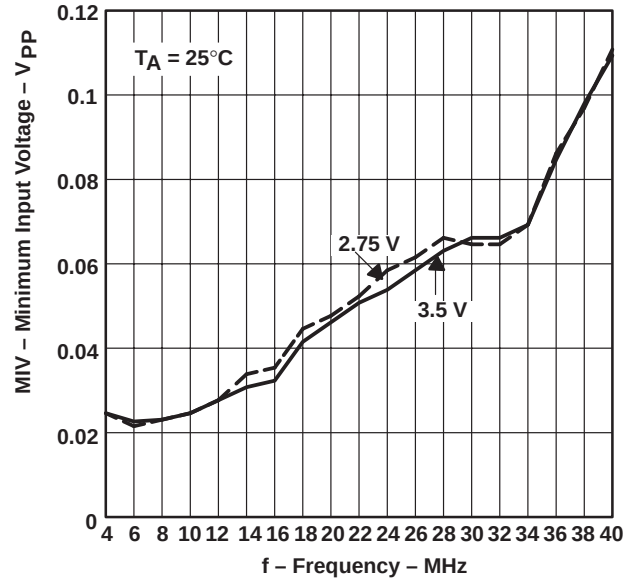


Figure 5

REFERENCE DIVIDER MINIMUM INPUT VOLTAGE vs. FREQUENCY AND TEMPERATURE

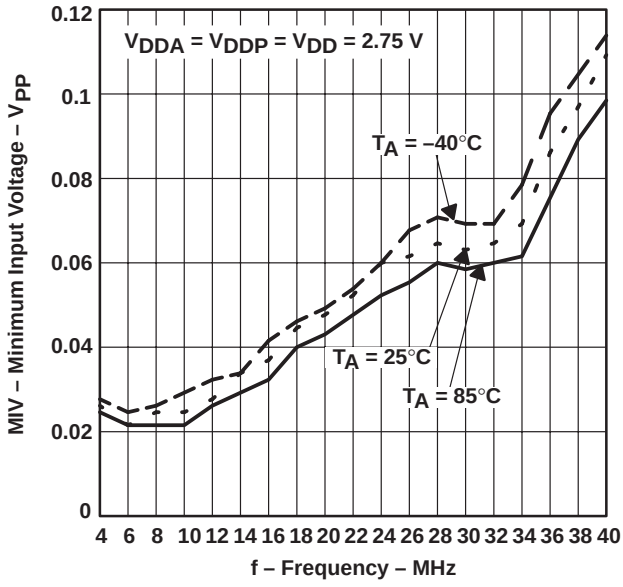


Figure 6

TYPICAL CHARACTERISTICS

AUXILIARY-1 DIVIDER MINIMUM INPUT POWER vs. FREQUENCY AND SUPPLY VOLTAGE

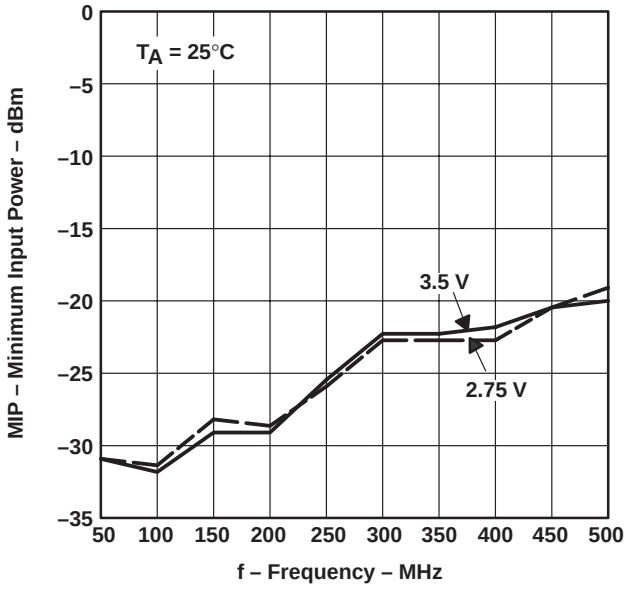


Figure 7

AUXILIARY-1 DIVIDER MINIMUM INPUT POWER vs. FREQUENCY AND TEMPERATURE

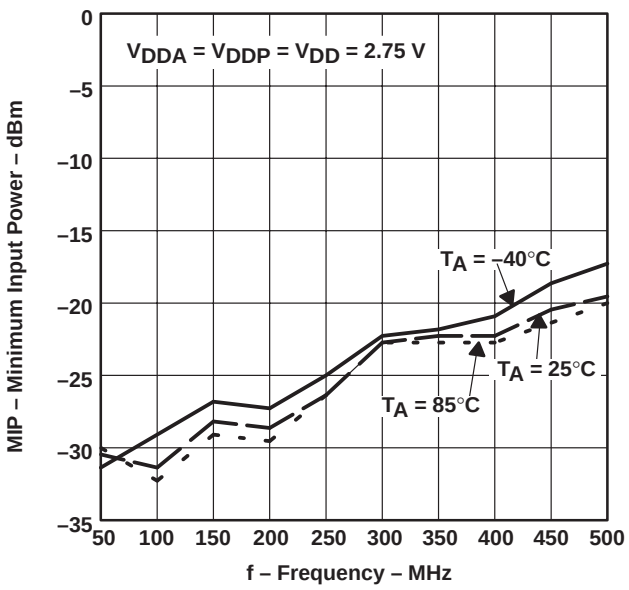


Figure 8

AUXILIARY-2 DIVIDER MINIMUM INPUT POWER vs. FREQUENCY AND SUPPLY VOLTAGE

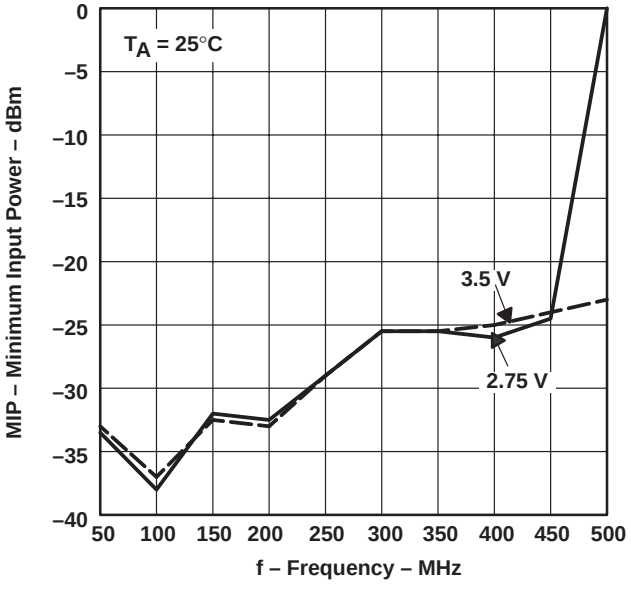


Figure 9

AUXILIARY-2 DIVIDER MINIMUM INPUT POWER vs. FREQUENCY AND SUPPLY VOLTAGE

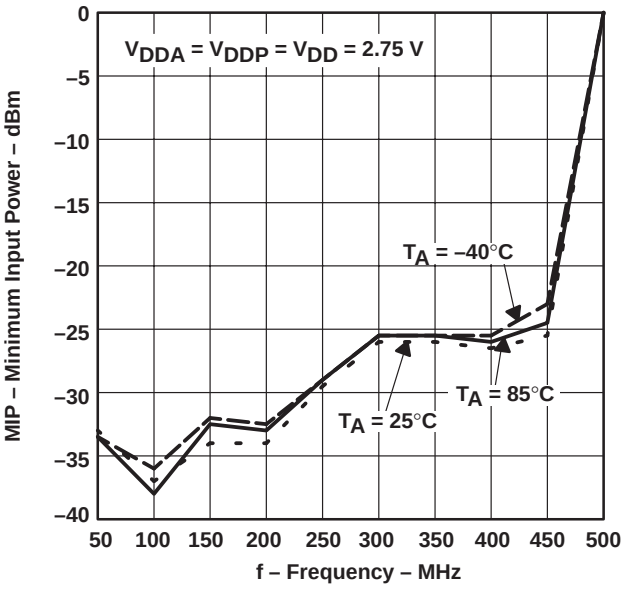


Figure 10

TYPICAL CHARACTERISTICS

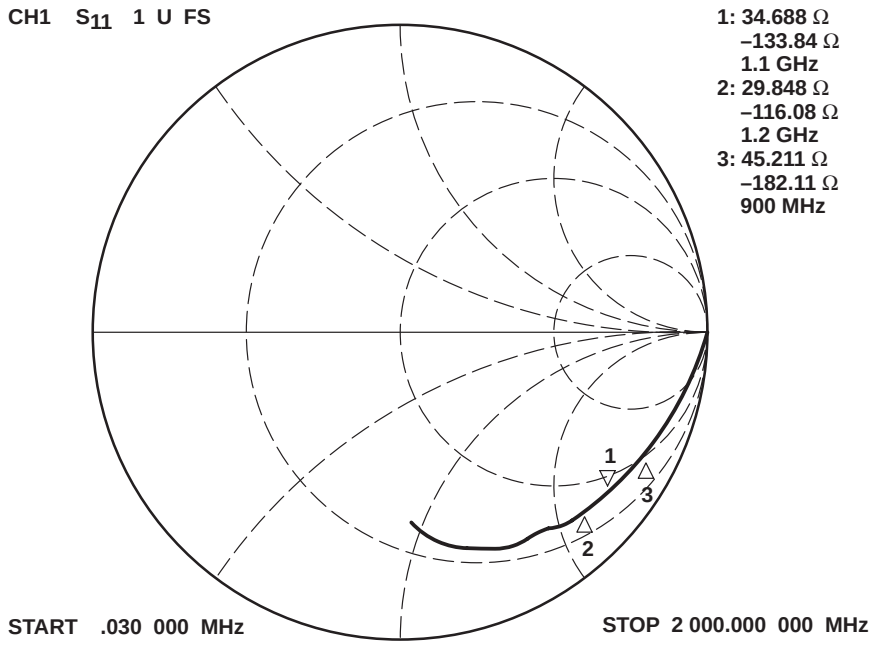


Figure 11. Typical RF_IN Input Impedance (S_{11})

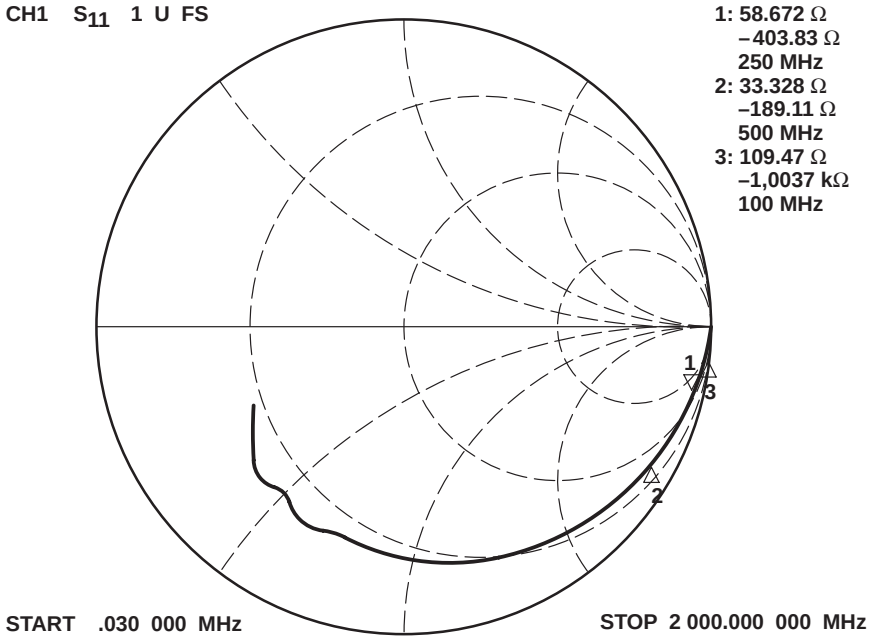


Figure 12. Typical AUX1_IN Input Impedance (S_{11})

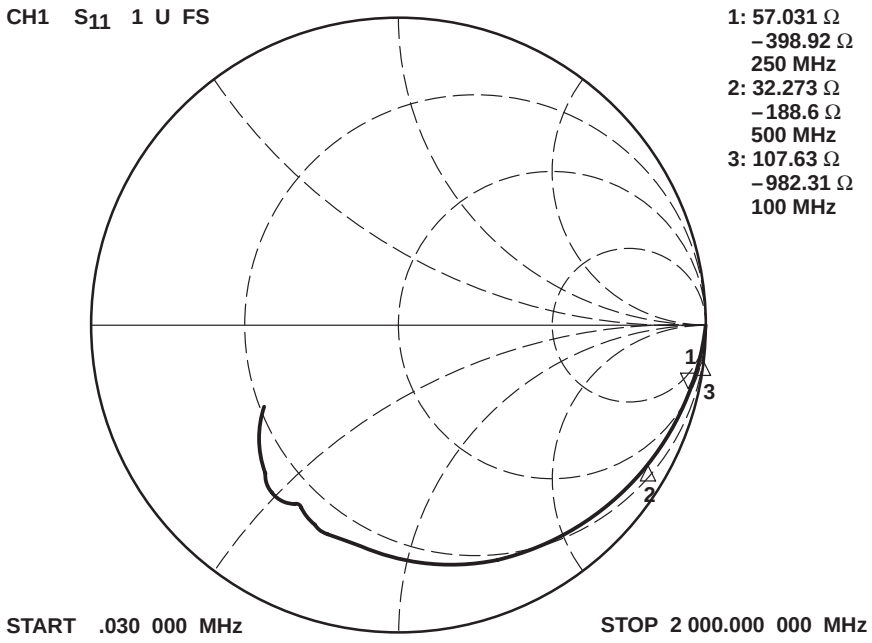


Figure 13. Typical AUX2_IN Input Impedance (S_{11})

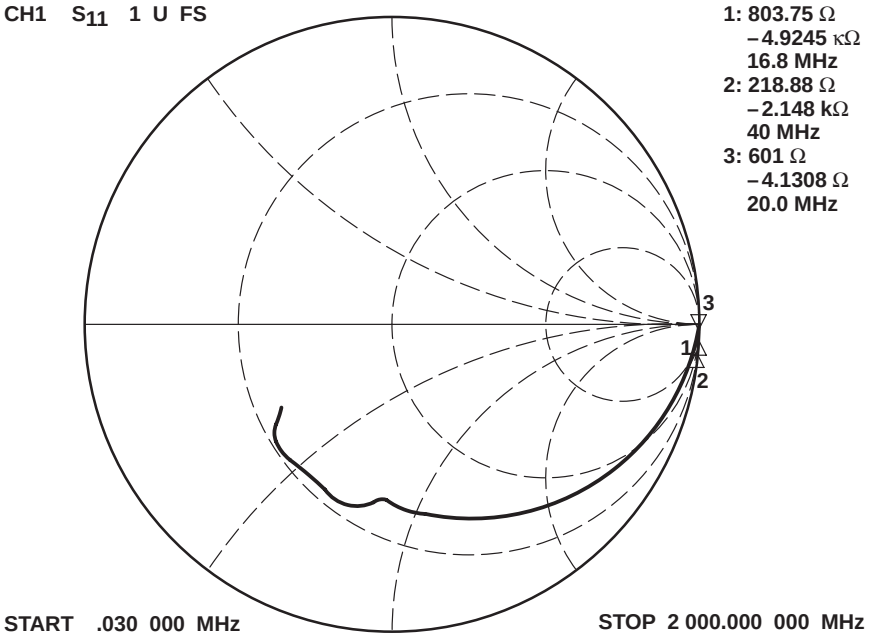


Figure 14. Typical REF_IN Input Impedance (S_{11})

APPLICATION INFORMATION

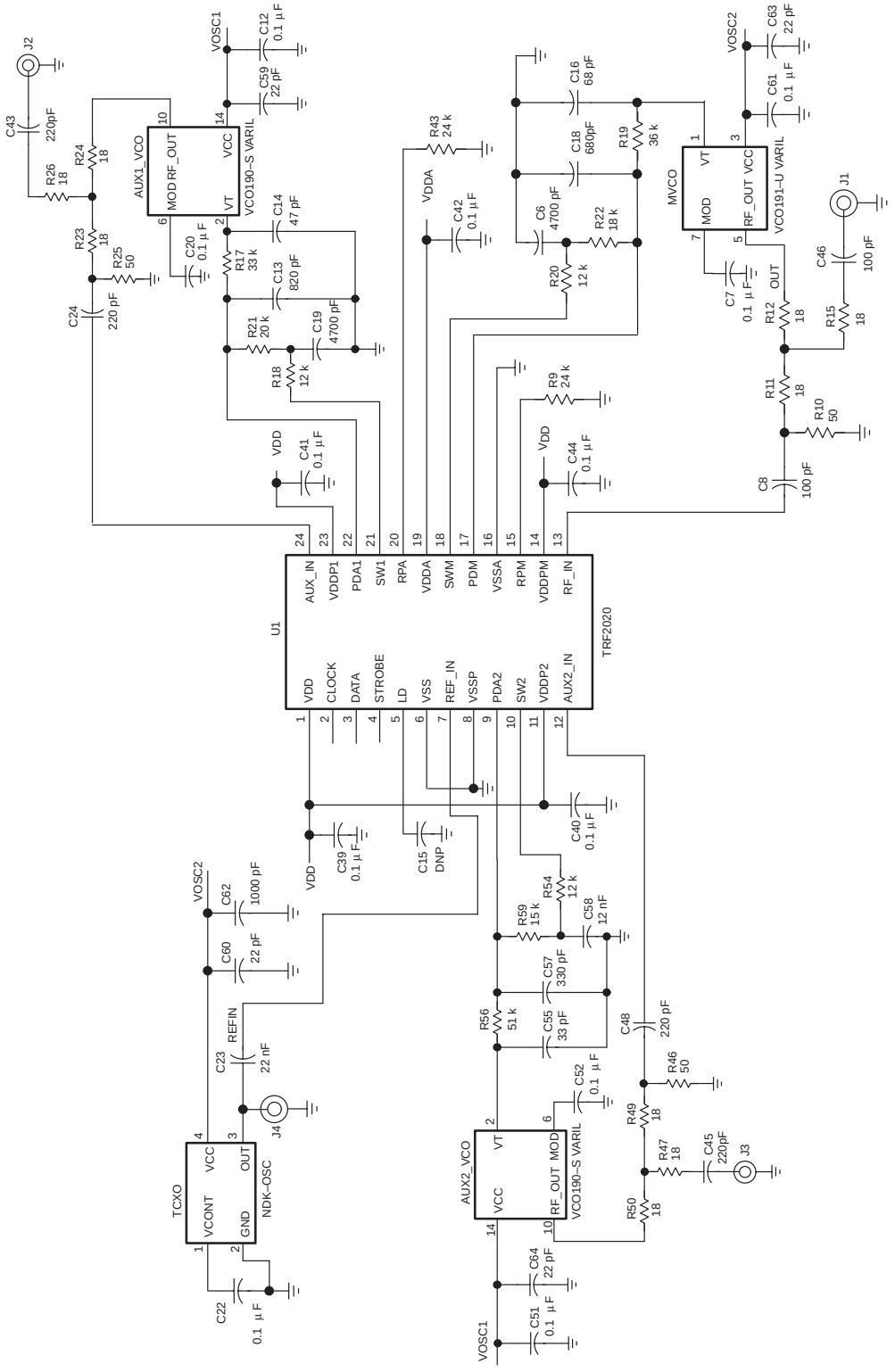


Figure 15. Evaluation Board Schematic (Part 1 of 2)

APPLICATION INFORMATION

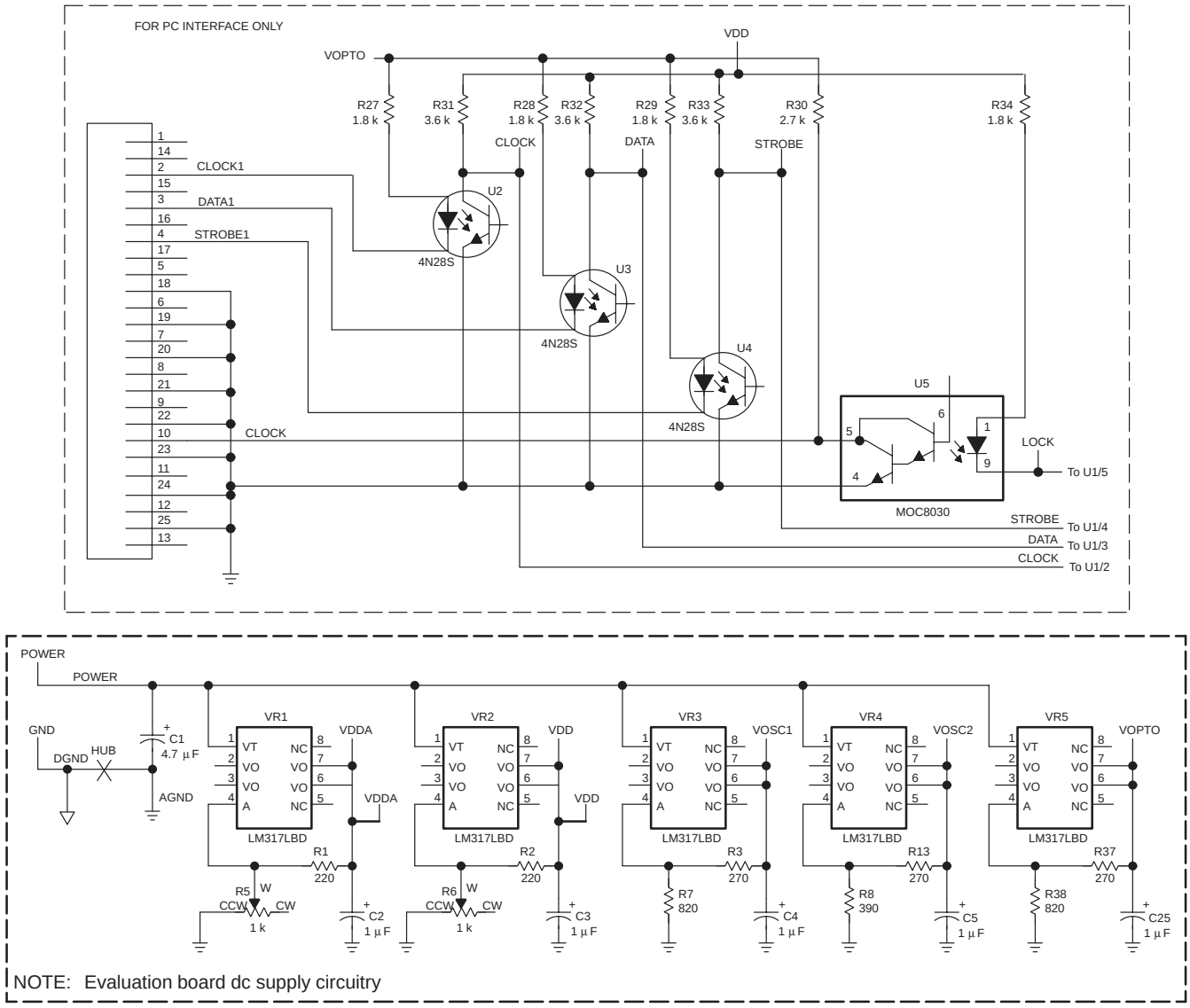


Figure 15. Evaluation Board Schematic (Part 2 of 2)

APPLICATION INFORMATION

Table 1. TRF2020 Evaluation Board Parts List

DESIGNATORS	DESCRIPTION	VALUE	QTY	SIZE (mm)	MANUFACTURER	MANUFACTURER P/N
C1	Capacitor	4.7 uF	1	“A” 3.2x1.6	Venkel	TA025TCM series
C2, 3, 4, 5, 25	Capacitor	1 uF	5	“A” 3.2x1.6	Venkel	TA025TCM series
C6, 19	Capacitor	4700 pF	2	0603 1.6x.08	Murata	GRM39X7R series
C7, 12, 20, 22, 39, 40, 41, 42, 44, 51, 52, 61	Capacitor	0.1 uF	12	0603 1.6x.08	Murata	GRM39X7R series
C8, 46	Capacitor	100 pF	2	0603 1.6x.08	Murata	GRM39X7R series
C13	Capacitor	820 pF	1	0603 1.6x.08	Murata	GRM39X7R series
C14	Capacitor	47 pF	1	0603 1.6x.08	Murata	GRM39X7R series
C15	Capacitor	DNP	1	0603 1.6x.08		
C16	Capacitor	68 pF	1	0603 1.6x.08	Murata	GRM39X7R series
C18	Capacitor	680 pF	1	0603 1.6x.08	Murata	GRM39X7R series
C23	Capacitor	22 nF	1	0603 1.6x.08	Murata	GRM39X7R series
C24, 43, 45, 48	Capacitor	220 pF	4	0603 1.6x.08	Murata	GRM39X7R series
C55	Capacitor	33 pF	1	0603 1.6x.08	Murata	GRM39X7R series
C57	Capacitor	330 pF	1	0603 1.6x.08	Murata	GRM39X7R series
C58	Capacitor	12 nF	1	0603 1.6x.08	Murata	GRM39X7R series
C59, 60, 63, 64	Capacitor	22 pF	4	0603 1.6x.08	Murata	GRM39X7R series
C62	Capacitor	1000 pF	1	0603 1.6x.08	Murata	GRM39X7R series
R1, 2	Resistor	220	2	0603 1.6x.08	Panasonic	ERJ–3GSYJ series
R3, 13, 37	Resistor	270	3	0603 1.6x.08	Panasonic	ERJ–3GSYJ series
R5, 6	Resistor	1K	2	.25” square	Bourns	3269W001 series
R7, 38	Resistor	820	2	0603 1.6x.08	Panasonic	ERJ–3GSYJ series
R8	Resistor	390	1	0603 1.6x.08	Panasonic	ERJ–3GSYJ series
R9, 43	Resistor	24K	2	0603 1.6x.08	Panasonic	ERJ–3GSYJ series
R10, 25, 46	Resistor	50	3	0603 1.6x.08	Panasonic	ERJ–3GSYJ series
R11, 12, 15, 23, 24, 26, 47, 49, 50	Resistor	18	9	0603 1.6x.08	Panasonic	ERJ–3GSYJ series
R17	Resistor	33K	1	0603 1.6x.08	Panasonic	ERJ–3GSYJ series
R18, 20, 54	Resistor	12K	3	0603 1.6x.08	Panasonic	ERJ–3GSYJ series
R19	Resistor	36K	1	0603 1.6x.08	Panasonic	ERJ–3GSYJ series
R21	Resistor	20K	1	0603 1.6x.08	Panasonic	ERJ–3GSYJ series
R22	Resistor	18K	1	0603 1.6x.08	Panasonic	ERJ–3GSYJ series
R27, 28, 29, 34	Resistor	1.8K	4	0603 1.6x.08	Panasonic	ERJ–3GSYJ series
R30	Resistor	2.7K	1	0603 1.6x.08	Panasonic	ERJ–3GSYJ series
R31, 32, 33	Resistor	3.6K	3	0603 1.6x.08	Panasonic	ERJ–3GSYJ series
R56	Resistor	51K	1	0603 1.6x.08	Panasonic	ERJ–3GSYJ series
R59	Resistor	15K	1	0603 1.6x.08	Panasonic	ERJ–3GSYJ series
U1	Integrated Circuit		1		TI	TRF2020
U2, 3, 4	Optoelectronics		3	730C–04	Motorola	4N28S

APPLICATION INFORMATION

Table 1. TRF2020 Evaluation Board Parts List (Continued)

DESIGNATORS	DESCRIPTION	VALUE	QTY	SIZE (mm)	MANUFACTURER	MANUFACTURER P/N
U5	Optoelectronics		1	730C–04	Motorola	MOC8030S
VR1, 2, 3, 4, 5	Voltage regulator		5	SO–8	National Semiconductor	LM317LBD
P1	Para. connector		1		AMP	747238–4
J1, 2, 3, 4	SMA connector		4		EF Johnson	142–0701–831
MVCO	Voltage-controlled oscillator		1		Vari-L Comp.	VCO190–U
TCXO	Temp.-compensated crystal oscillator		1		Toyocom	TCO–980 series
AUX 1_VCO	Voltage-controlled oscillator		1		Vari-L Comp.	VCO190–S
AUX 2_VCO	Voltage-controlled oscillator		1		Vari-L Comp.	VCO190–S
DATA, VDDA, VDD, LOCK, POWER, CLOCK, GND, STROBE	Test point		8		Components Corp.	TP–105–01 series

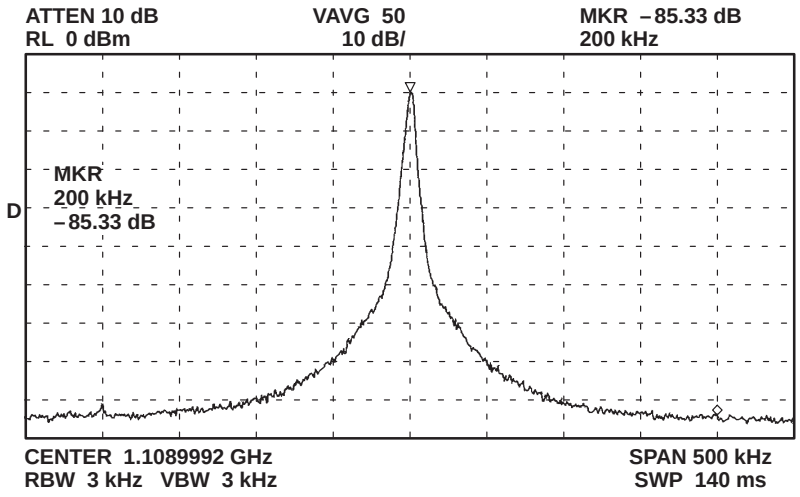


Figure 16. Typical Main Synthesizer Reference Spurs

APPLICATION INFORMATION

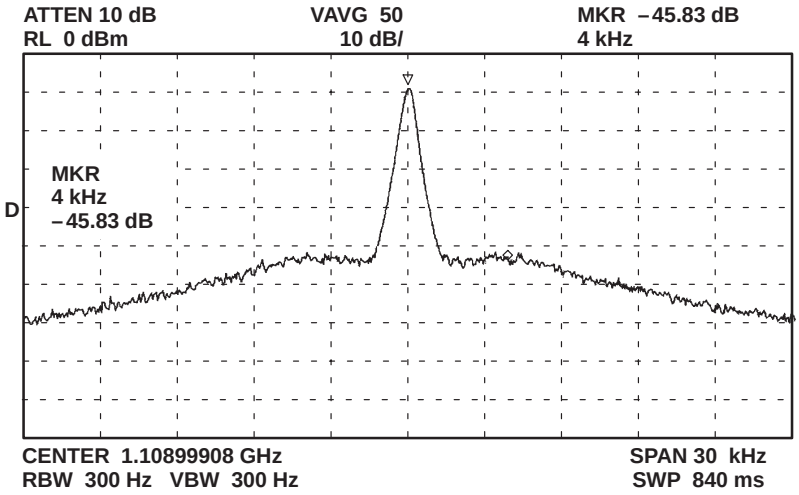


Figure 17. Typical Main Synthesizer Close-in Noise at 4 kHz Offset

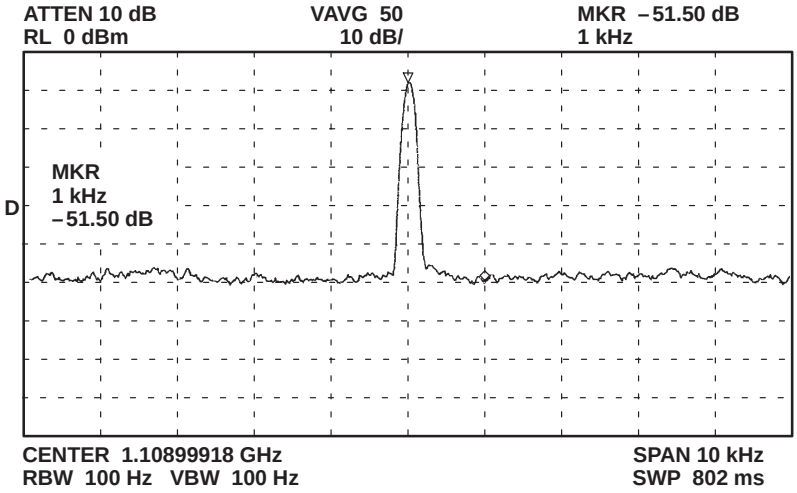


Figure 18. Typical Main Synthesizer Close-in Noise at 1 kHz Offset

APPLICATION INFORMATION

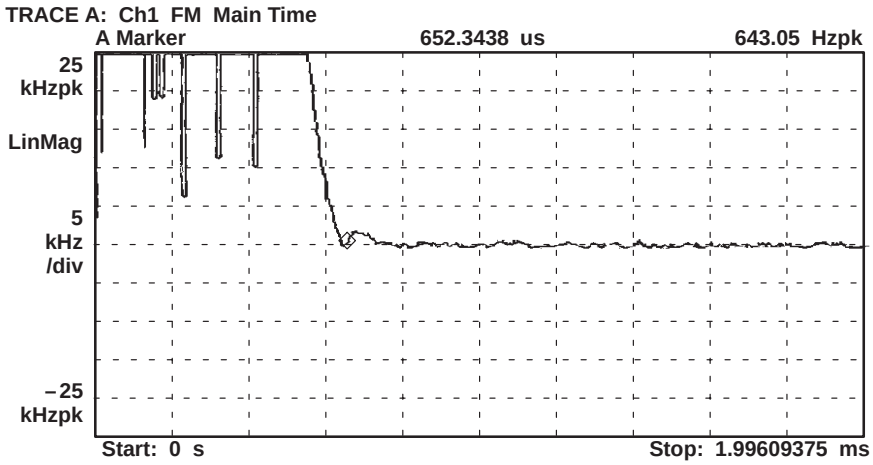


Figure 19. Typical Main Synthesizer Transient Response For 35-MHz Jump From 1074 MHz to 1109 MHz

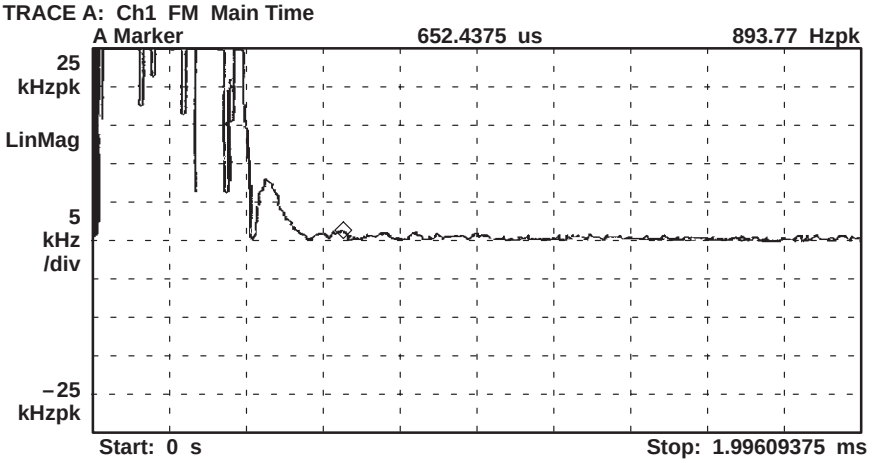


Figure 20. Typical Main Synthesizer Transient Response For 35-MHz Jump From 1109 MHz to 1074 MHz

APPLICATION INFORMATION

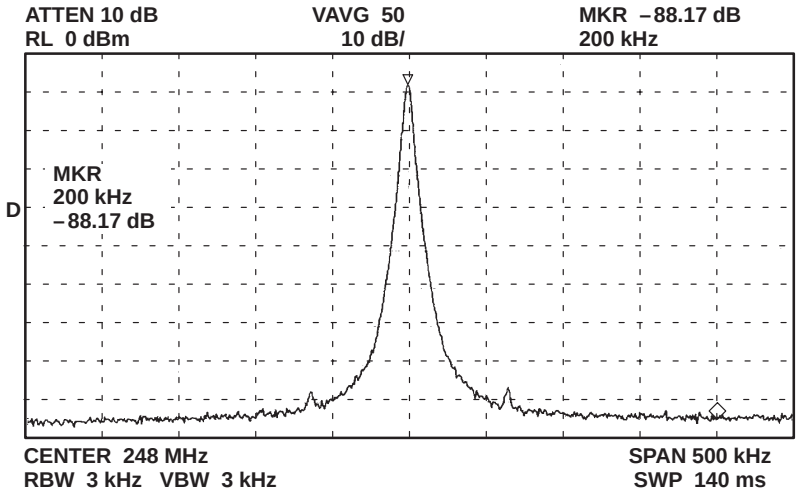


Figure 21. Typical Auxiliary-1 Synthesizer Reference Spurs

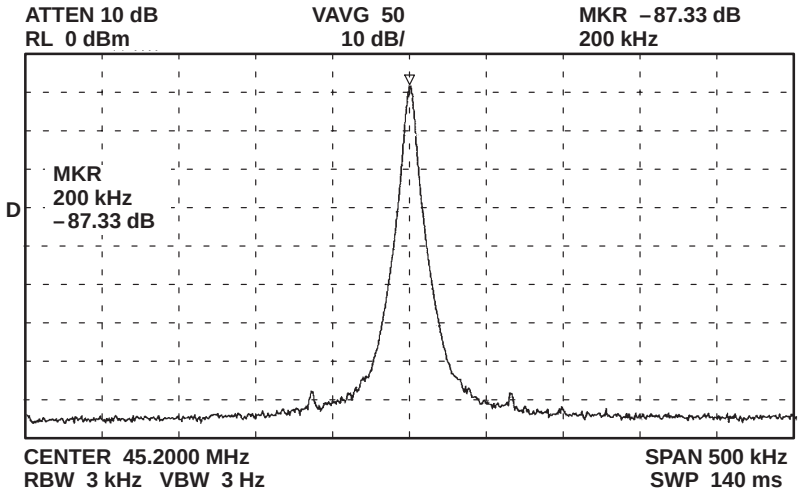


Figure 22. Typical Auxiliary-2 Synthesizer Reference Spurs

PRINCIPLES OF OPERATION

serial port operation

The TRF2020 device registers are manipulated via a synchronous serial data port. The timing relationships are defined in Figure 2, in the parameter measurement information section. Four 24-bit words are clocked into temporary holding registers with the least significant bit clocked first. The operation registers are loaded with the new data residing in the temporary registers with the rising edge of the strobe input.

Each word can be written to the device independently. In this manner, only the words containing the information required to change the current state of the device need to be written. To fully program the device, the words are written in the following order:

Word-1	Auxiliary-1 synthesizer
Word-2	Auxiliary-2 synthesizer
Word-3	Device
Word-0	Main synthesizer

Word-3 follows Word-1 and Word-2 because the frequency information for the auxiliary synthesizers is stored in the operational registers with Word-1 and Word-2. It is necessary to load this frequency information before the speed-up mode is activated by the auxiliary synthesizers' power enable bits in Word-3.

Word-0 is written last because the speed-up mode for the main synthesizers is activated by the writing of Word-0. If the main synthesizer is to be enabled, the power enable bit is written to the device in the preceding Word-3.

The two most significant bits of each word contain the unique address of the word; the balance of the 22 bits contains the data fields.

serial word format

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR		DATA																					
0	0	C						B											A				
0	1	G						F		E											D		
1	0	N		M		L		K		J											H		
1	1	V						U		T	S	R	P										

serial word format function

A: 5-bit NM2 data for main divider coefficient

B: 11-bit NM1 data for main divider coefficient

C: 6-bit data to control speed-up mode time of main synthesizer analog switch

D: 3-bit NM2 data for auxiliary-1 divider coefficient

E: 11-bit NM1 data for auxiliary-1 divider coefficient

F: 2-bit data to select main synthesizer speed-up/normal mode current ratio

G: 6-bit data to control speed-up mode time of auxiliary synthesizers

H: 3-bit NM2 data for auxiliary-2 divider coefficient

PRINCIPLES OF OPERATION

serial word format function (continued)

J: 11-bit NM1 data for auxiliary-2 divider coefficient

K: 2-bit data to select auxiliary synthesizers speed-up/normal mode current ratio

L: 2-bit data to select reference postscaler for main synthesizer

M: 2-bit data to select reference postscaler for auxiliary-1

N: 2-bit data to select reference postscaler for auxiliary-2

P: 11-bit data for reference divider coefficient

R: 1-bit data to enable main synthesizer power. When 1, power is enabled

S: 1-bit data to enable auxiliary-1 synthesizer power. When 1, power is enabled

T: 1-bit data to enable auxiliary-2 synthesizer power. When 1, power is enabled

U: 2-bit data to select lock detect for main, auxiliary-1, and auxiliary-2 synthesizers

V: 6-bit data reserved for test purposes

main prescaler

Main prescaler and speed-up mode coefficients are defined by Word-0 at address 00.

The total division of the main synthesizer prescaler is defined as follows:

$TOTAL_{MAIN} = 32 \times B + A$,

where $31 \leq B < 2^{11}$†, and $0 \leq A < 2^5$.

† The above equation defines a synthesizer operation where contiguous channels exist for all combinations of A and B. If B < 31, the synthesizer no longer provides contiguous channels. In either case, it is important that the value assigned to A is never greater than the value assigned to B.

The speed-up mode total-time duration of the main synthesizer analog switch is defined by field C in Word-0 as follows:

$$TIME_{MAIN-SP} = 2 \times C \times \frac{1}{f_{ref}},$$

where $1 \leq C < 2^6$, and f_{ref} is the corresponding phase detector reference frequency.

auxiliary-1 prescaler

Auxiliary-1 prescaler coefficients are defined by Word-1 at address 01. The total division of the auxiliary-1 synthesizer prescaler is defined as follows:

$TOTAL_{AUX-1} = 8 \times E + D$,

where $7 \leq E < 2^{11}$‡, and $0 \leq D < 2^3$.

‡ The above equation defines a synthesizer operation where contiguous channels exist for all combinations of D and E. If E < 7, the synthesizer no longer provides contiguous channels. In either case, it is important that the value assigned to D is never greater than the value assigned to E.

PRINCIPLES OF OPERATION

auxiliary-1 prescaler (continued)

The speed-up total-time duration of the auxiliary synthesizer boost charge pumps is defined as follows:

$$TIME_{AUX-SP} = 2 \times G \times \frac{1}{f_{ref}},$$

where $1 \le G < 2^6$, and f_{ref} is the corresponding phase detector reference frequency.

The speed-up mode of both auxiliary synthesizers is controlled by field G in Word-1, although each auxiliary synthesizer has its own independent speed-up mode counter.

auxiliary-2 prescaler

Auxiliary-2 prescaler coefficients are defined by Word-2 at address 10.

The total division of the auxiliary-2 synthesizer prescaler is defined as follows:

$TOTAL_{AUX-2} = 8 \times J + H,$

where $7 \le J < 2^{11}$†, and $0 \le H < 2^3$.

† The above equation defines a synthesizer operation where contiguous channels exist for all combinations of H and J. If J < 7, the synthesizer no longer provides contiguous channels. In either case, it is important that the value assigned to H is never greater than the value assigned to J.

reference divider postscalers

Each synthesizer section is referenced to the main reference divider through a selectable divide-by-1, -2, -4, or -8 postscaler (see the reference divider section below). Selection of the additional 1, 2, 4, or 8 division is determined by the state of bits L, M, and N, as depicted in Word-2 as follows:

Additional Postscaler Division

N1, M1, OR L1	N0, M0, OR L0	ADDITIONAL DIVISION
0	0	1
0	1	2
1	0	4
1	1	8

reference divider

The reference divider coefficients are defined by Word-3 at address 11. The total division of the 11-bit reference counter is defined as follows:

$$TOTAL_{REF} = \frac{1}{P},$$

where $1 \le P < 2^{11}$.

power enable

Each synthesizer section can be enabled/disabled by manipulation of fields R, S, and T of Word-3. The appropriate synthesizer section is enabled if a logic one (1) is written to the appropriate field.

PRINCIPLES OF OPERATION

lock detect (LD) selection

The phase-locked state of each synthesizer section is indicated by the logic state of the LD terminal. Each synthesizer section can be selected individually or as an ANDed function by the manipulation of field U in Word-3 as follows:

Additional Postscaler Division

U1	U0	LOCK DETECT
0	0	MAIN
0	1	AUX-1
1	0	AUX-2
1	1	ANDed

The terms in the ANDed function are dependent on the power enable bit state of each synthesizer section. Only if the synthesizer section is enabled is its term significant in the ANDed term of the lock detect output. This is depicted in the following logic equation:

$LD_{U1 = U0 = 1} = (MAIN + \overline{R}) \bullet (AUX1 + \overline{S}) \bullet (AUX2 + \overline{T}) \bullet (R + S + T)$

where R, S, and T are the power enable bits of Word-3.

test mode selection

Internal signals can be routed to the LD terminal by manipulating the test mode field V in Word-3 as shown in Table 2.

Table 2. Test Mode Selection

V4	V3	V2	V1	V0	ROUTING TO LD TERMINAL
0	0	1	0	1	Main prescaler output
0	0	1	1	0	Main 11-bit counter output
0	0	1	1	1	Main 5-bit counter output
1	1	0	0	1	Main phase comparator down pulse output
1	1	0	1	0	Main phase comparator up pulse output
1	1	0	1	1	Main timer output
1	0	1	0	1	Auxiliary-1 prescaler output
1	0	1	1	0	Auxiliary-1 11-bit counter output
1	0	1	1	1	Auxiliary-1 3-bit counter output
0	1	1	0	1	Auxiliary-1 phase comparator down pulse output
0	1	1	1	0	Auxiliary-1 phase comparator up pulse output
0	1	1	1	1	Auxiliary-1 timer output
1	1	1	0	1	Auxiliary-2 prescaler output
1	1	1	1	0	Auxiliary-2 11-bit counter output
1	1	1	1	1	Auxiliary-2 3-bit counter output
1	0	0	0	1	Auxiliary-2 phase comparator down pulse output
1	0	0	1	0	Auxiliary-2 phase comparator up pulse output
1	0	0	1	1	Auxiliary-2 timer output
0	1	0	0	1	Main reference clock

PRINCIPLES OF OPERATION

test mode selection (continued)

Table 2. Test Mode Selection (continued)

V4	V3	V2	V1	V0	ROUTING TO LD TERMINAL
0	1	0	1	0	Auxiliary-1 reference clock
0	1	0	1	1	Auxiliary-2 clock reference clock

NOTE: All other binary combinations of the test mode field V not shown above are reserved for future use.

Bit 5 in the V-word is used to select an external pulse mode. In the external pulse mode, the CMOS main and subcounters are fed externally sourced clock pulses through pin 18 instead of from the prescaler inputs as normally operated. This mode makes testing of the internal CMOS counters easy.

speed-up switching time

main synthesizer

When the main frequency synthesizer is changed in frequency, it may be desirable to increase the loop bandwidth for a short time in order to achieve a faster lock time. An analog switch is provided that can vary the topography of the loop filter in order to achieve a faster loop gain. When the frequency is changed (and speed-up operation is desired), the following actions occur:

1. The new frequency coefficients for the main synthesizer are sent to the device over the serial bus.
2. After the data is clocked in, the strobe is toggled to high.
3. The positive edge of the strobe loads the new frequency into the main synthesizer prescaler (using the next reference frequency pulse to synchronize).
4. With loading of the main synthesizer prescaler, the speed-up mode analog switch is activated to a low-impedance state and the speed-up mode charge-pump boost circuit is activated.
5. The speed-up mode is maintained until the main synthesizer speed-up counter, previously loaded with field C of Word-0, counts down to zero (0). The speed-up counter is clocked with the main synthesizer phase detector reference frequency.
6. With the speed-up counter reaching a terminal count of zero (0), the speed-up analog switch reverts to the normal mode high-impedance state, and the speed-up mode charge pump boost circuit is deactivated.

auxiliary synthesizer

Because the frequency of the auxiliary synthesizers is rarely changed during normal operation, speed-up mode occurs during the independent power enable of the auxiliary synthesizer sections as controlled by fields S and T in Word-3. Upon the transition of these 1-bit fields from a logic zero (0) to a logic one (1), the following actions occur:

1. It is assumed that the proper frequency coefficients were written to the corresponding auxiliary synthesizer prescaler field.
2. The power enable bit for the corresponding auxiliary synthesizer is changed from a zero (0) to a one (1).
3. The positive edge of the strobe loads Word-3, which contains the power enable bit fields (using the next reference frequency pulse to synchronize).
4. With the loading of Word-3, the speed-up mode charge-pump boost circuit is activated and the analog switch is activated to a low-impedance state.

PRINCIPLES OF OPERATION

auxiliary synthesizer (continued)

5. The speed-up mode is maintained until the corresponding speed-up mode counter counts down to a terminal count of zero. The speed-up counter is clocked with the corresponding auxiliary synthesizer phase detector reference frequency.
6. With the corresponding speed-up counter reaching terminal count, the speed-up mode charge-pump boost circuit and the analog switch for the corresponding auxiliary synthesizer revert to the normal mode, high-impedance, off state.

using the speed-up mode

By changing the loop filter frequency response or the charge-pump output current, the overall closed-loop response of the synthesizer system is altered. Without careful consideration, synthesizer lock-up times may degrade rather than improve using the speed-up mode.

selecting current ratios

The normal mode and speed-up mode charge-pump current ratios for the main synthesizer and the auxiliary synthesizers are selected using field F of Word-1 and field K of Word-2, respectively, as shown in Table 3.

Table 3. Charge-Pump Current Ratio Selection

F AND K FIELDS	SPEED-UP/NORMAL MODE RATIO
11	8 (2 mA/0.25 mA)
10	4 (2 mA/0.5 mA)
01	2 (2 mA/ 1 mA)
00	1 (2 mA/2 mA)

external charge-pump scaling resistors

Two external scaling resistors are connected between RPM, RPA, and V_{SSA} (analog ground) in order to scale the speed-up mode charge-pump output current for the main synthesizer and the two auxiliary synthesizers as defined in the following equations. The external scaling resistors in conjunction with the programmable charge-pump current ratios determine speed-up and normal mode currents.

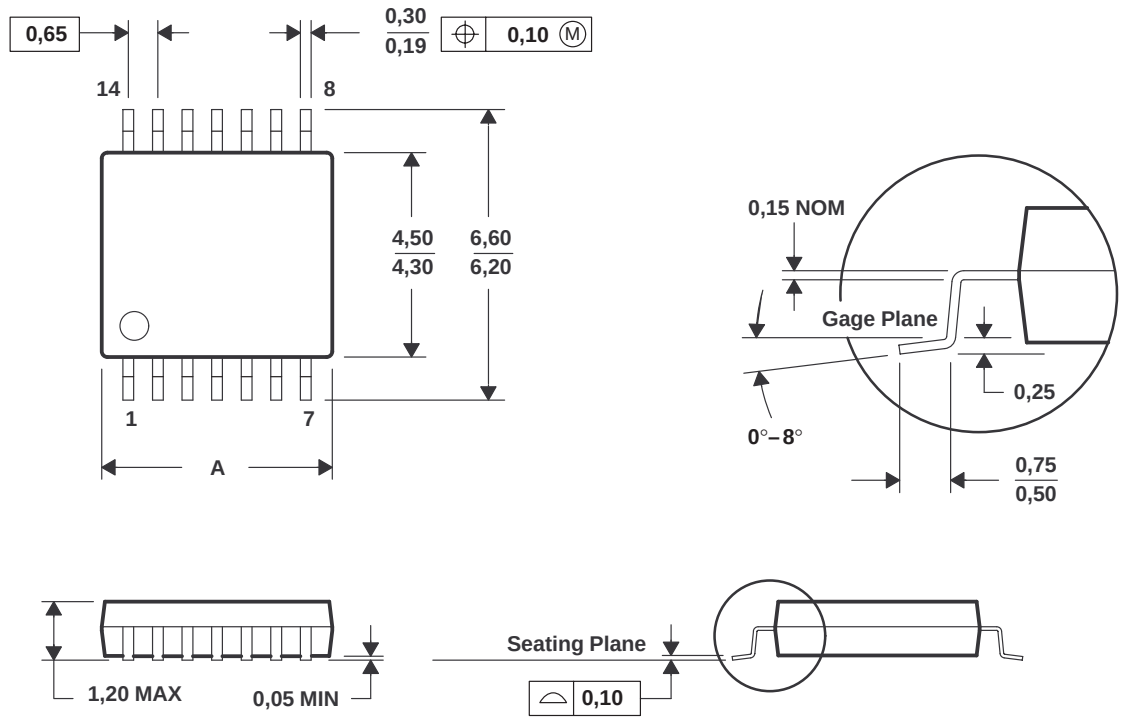
Main charge-pump speed-up mode current = $\frac{1}{\text{RPM}} \times 2\ \text{mA} \times 27\ \text{k}\Omega\ (5\ \text{k}\Omega \leq \text{RPM} \leq \infty)$,

Auxiliary charge-pump speed-up mode current = $\frac{1}{\text{RPA}} \times 2\ \text{mA} \times 27\ \text{k}\Omega\ (5\ \text{k}\Omega \leq \text{RPM} \leq \infty)$,

MECHANICAL DATA

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/E 08/96

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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