SLWS028B – MAY 1998 – REVISED SEPTEMBER 1998

- **Operates from 2.75 V to 3.5 V Supply**
- **Low Current Consumption**
- **Low Profile Package: 48-pin Plastic Quad Flat Package (PQFP)**
- **Global System for Mobile Communications (GSM), Class 3, 4, or 5 Mobile Station (MS) Portable Cellular Telephone Applications**
- **Conversion from Radio Frequency (RF) to I and Q Baseband on a Single Chip**
- **Independent Powerdown of Low Noise Amplifiers (LNA), Mixers, Intermediate Frequency (IF) Amplifiers, and Voltage-Controlled Oscillator (VCO)**
- **Digital Gain Control for LNA and IF Amplifiers**
- **Two IF Amplifiers for Dual Conversion if Required**
- **Cascaded Operation of IF Amplifiers for Single-Conversion Configurations**
- **DC Compensation of I and Q Outputs**

description

The TRF1020 is a single-chip radio frequency (RF) downconverter suitable for 900-MHz GSM applications. It combines in one small package an LNA, an RF mixer, an IF mixer, two IF amplifiers, an I and Q mixer, and one buffered VCO. The TRF1020 requires few external components.

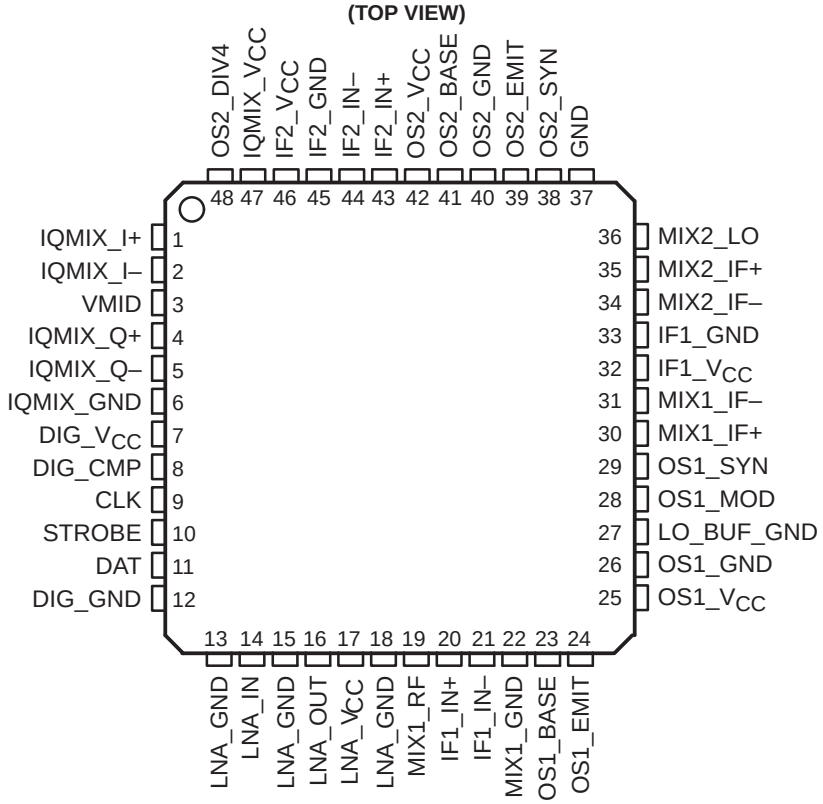
The LNA has a nominal gain of 12.4 dB and noise figure of 2.1 dB. The first RF mixer has a conversion gain of 13.4 dB and a single-sideband (SSB) noise figure of 8.3 dB. The IF amplifiers have combined variable gain from 0 to 84 dB in approximately 3-dB steps. The IF amplifier frequency range is 40 to 180 MHz for the first IF amplifier and 10 to 180 MHz for the second IF amplifier. The local oscillator of the I and Q mixer operates at four times the last frequency of the IF mixer.

Power consumption is kept to a minimum and can be further reduced by dynamically placing selected functions in standby power-down mode when not required. Power-down control is provided through the three-line digital serial interface.

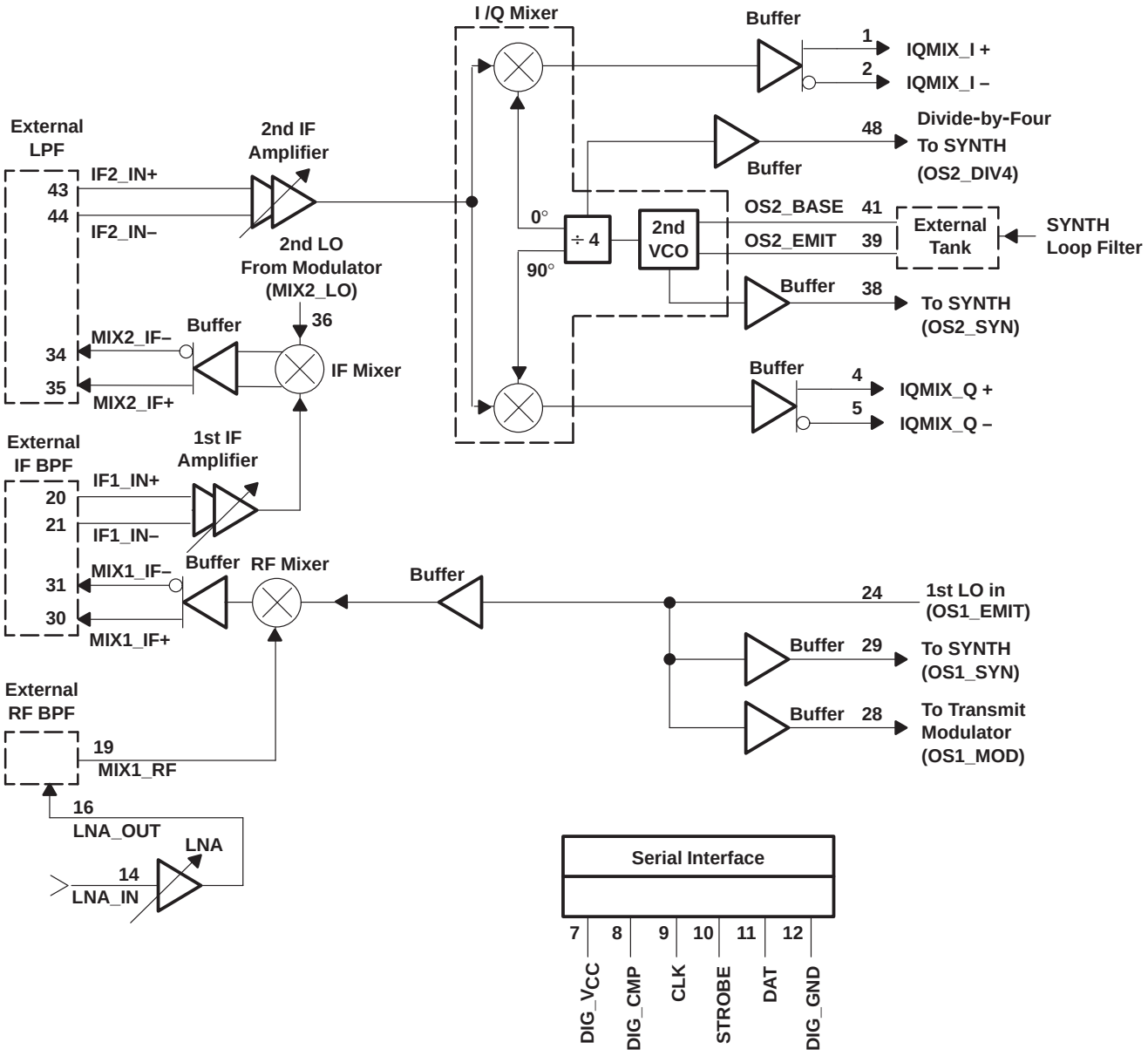
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the gates.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PFB PACKAGE
(TOP VIEW)



functional block diagram



serial port operation

The TRF1020 device register is manipulated through a synchronous serial data port. The timing relationships are defined in Figure 1. One 24-bit word is clocked into a temporary holding register in little endian fashion (LSB clocked in first). New data, residing in the temporary registers, is loaded into the operation registers on the rising edge of the STROBE line. The control data-bit functions are detailed in Tables 1, 2, 3, 4, 5, 6, and 7 in the following sections.

Table 1. Control Data BIT/Signal Name Map

CONTROL DATA BIT†	SIGNAL NAME
D0	LNAP
D1	LNAG
D2	MX1STBY
D3	MX1P
D4	MX2P
D5	MX2BYP
D6	IF1AGC1
D7	IF1AGC2
D8	IF1AGC3
D9	IF1AGC4
D10	IF1AGC5
D11	IF1AGC6
D12	DMODP
D13	DMODSTBY
D14	IF2AGC1
D15	IF2AGC2
D16	IF2AGC3
D17	IF2AGC4
D18	IF2AGC5
D19	IF2AGC6
D20	DMDISABLE
D21	<Not Used>
D22	<Not Used>
D23	<Not Used>

† D0 is the first bit sent in the 24-bit serial data word, D23 is the last bit sent.

low noise amplifier (LNA)

The LNA gain is controlled as described in Table 2.

Table 2. LNA Gain Control (see Note 1)

LNAP	LNAG	NOMINAL GAIN (dB)
0	0	–30†
1	0	12.4‡
0	1	–6
1	1	Not Allowed

† Low gain state
‡ High gain state
NOTE 1: See Table 1, Control Data BIT/Signal Name Map.

RF mixer

The RF mixer section is controlled as described in Table 3.

Table 3. RF Mixer Control (see Note 1)

SIGNAL	DESCRIPTION	OPERATION
MX1STBY	RF mixer standby	1: Entire section on 0: Don't care
MX1P	RF mixer power	1: Section powered up 0: Power shut down

NOTE 1: See Table 1, Control Data BIT/Signal Name Map.

first IF amplifier and IF mixer

The second downconverter group consists of the first IF amplifier whose output feeds the IF mixer function. Because the first IF amplifier output is not brought out to device terminals, the two functions are specified together. In order to provide for cascaded operation of the first and second IF amplifiers, it is possible to bypass the IF mixer function. The first IF amplifier gain is controlled according to Table 4. The first IF amplifier and IF mixer power-down control are described in Table 5.

first IF amplifier and IF mixer (continued)

Table 4. First IF Amplifier Gain Control (see Note 1)

IF1AGC6	IF1AGC5	IF1AGC4	IF1AGC3	IF1AGC2	IF1AGC1	GAIN (dB)
0	0	0	0	0	0	0
0	0	0	0	0	1	3
0	0	0	0	1	1	6
0	0	0	1	1	1	9
0	0	1	0	0	0	12
0	0	1	0	0	1	14.5
0	0	1	0	1	1	17.5
0	0	1	1	1	1	20.5
0	1	1	0	0	0	23
0	1	1	0	0	1	26
0	1	1	0	1	1	29
0	1	1	1	1	1	32
1	1	1	0	0	0	34.5
1	1	1	0	0	1	37
1	1	1	0	1	1	39.5
1	1	1	1	1	1	42

NOTE 1: See Table 1, Control Data BIT/Signal Name Map.

Table 5. IF Mixer Bias Control (see Note 1)

SIGNAL	DESCRIPTION	OPERATION
MX2BYP (see Note 2)	IF mixer bypass	1: Mixer bypassed 0: Normal operation
MX2P	IF mixer power control	1: Operational 0: Nonoperational

NOTES: 1. See Table 1, Control Data BIT/Signal Name Map.
2. Using the mixer-bypass function disables the LO input to the mixer (at the buffer) and unbalances the mixer to allow the signal to pass through the mixer.

second IF amplifier and I/Q mixer

The second IF amplifier gain is controlled as described in Table 6, while the second IF amplifier, I/Q mixer and second VCO power-down controls are described in Table 7.

Table 6. Second IF Amplifier Gain Control (see Note 1)

IF2AGC6	IF2AGC5	IF2AGC4	IF2AGC3	IF2AGC2	IF2AGC1	GAIN (dB)
0	0	0	0	0	0	0
0	0	0	0	0	1	3
0	0	0	0	1	1	6
0	0	0	1	1	1	8.5
0	0	1	0	0	0	12
0	0	1	0	0	1	15
0	0	1	0	1	1	18
0	0	1	1	1	1	21
0	1	1	0	0	0	24
0	1	1	0	0	1	27
0	1	1	0	1	1	30
0	1	1	1	1	1	33
1	1	1	0	0	0	36
1	1	1	0	0	1	39
1	1	1	0	1	1	40
1	1	1	1	1	1	42.5

NOTE 1: See Table 1, Control Data BIT/Signal Name Map.

Table 7. I/Q Mixer and Second VCO Control (see Note 1)

SIGNAL	DESCRIPTION	OPERATION
DMODSTBY	DEMOD standby	1: Entire section on 0: Only second VCO/synth buffer on
DMODP	Power control	1: Normal operation 0: Power shut down
DMDISABLE	DC correction	1: Internal dc correction off 0: Internal dc correction on

NOTE 1: See Table 1, Control Data BIT/Signal Name Map.

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CLK	9	I	Serial data timing control signal.
DAT	11	I	Serial data input.
DIG_CMP	8	I	Control signal for I and Q DC compensation circuitry.
DIG_GND	12		Ground connection for digital control circuitry.
DIG_V_{CC}	7		Voltage supply connection for digital control circuitry.
GND	37		Ground
IF1_GND	33		Ground connection for first IF amplifier and IF mixer circuitry.
IF2_GND	45		Ground connection for second IF amplifier.
IF1_IN+	20	I	Noninverting RF mixer output.
IF2_IN+	43	I	Noninverting second IF amplifier input signal.
IF1_IN–	21	I	Inverting RF mixer output.
IF2_IN–	44	I	Inverting second IF amplifier input signal.
IF1_V_{CC}	32		Voltage supply connection for first IF amplifier.
IF2_V_{CC}	46		Voltage supply connection for second IF amplifier.
IQMIX_GND	6		Ground connection for the I and Q mixer.
IQMIX_I+	1	O	Noninverting in-phase output.
IQMIX_I –	2	O	Inverting in-phase output.
IQMIX_Q+	4	O	Noninverting quadrature-phase output.
IQMIX_Q–	5	O	Inverting quadrature-phase output.
IQMIX_V_{CC}	47		Voltage supply connection for the I and Q mixer circuitry.
LNA_GND	13, 15, 18		Ground connection for the LNA circuitry.
LNA_IN	14	I	Low-noise amplifier input.
LNA_OUT	16	O	Low-noise amplifier output.
LNA_V_{CC}	17		Bias supply for the LNA circuitry.
LO_BUF_GND	27		Ground connection for OS1 LO buffer.
MIX1_GND	22		Ground connection for RF mixer circuitry.
MIX1_IF+	30	O	Noninverting first IF amplifier input signal.
MIX1_IF–	31	O	Inverting first IF amplifier input signal.
MIX1_RF	19	I	RF mixer input.
MIX2_IF+	35	O	Noninverting first IF amplifier and IF mixer input.
MIX2_IF–	34	O	Inverting first IF amplifier and IF mixer input.
MIX2_LO	36	I	IF mixer LO input.
OS1_BASE	23	I	Base of OS1 transistor.
OS2_BASE	41	I	Base of the OS2 transistor.
OS2_DIV4	48	O	Oscillator frequency divided by 4.
OS1_EMIT	24		External RF mixer LO input.
OS2_EMIT	39		Emitter of OS2 transistor.
OS1_GND	26		Ground connection for the OS1 circuitry.
OS2_GND	40		Ground connection for OS2 circuitry.
OS1_MOD	28	O	OS1 buffered output.
OS1_SYN	29	O	OS1 buffered output.
OS2_SYN	38	O	OS2 buffered output.

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
OS1_V_{CC}	25		Bias supply for OS1 circuitry.
OS2_V_{CC}	42		Bias supply for the OS2 circuitry.
STROBE	10	I	Data strobe.
VMID	3	I	Bias supply reference voltage for A/D converters (VDD/2).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.3 V to +5.5 V
Input voltage to any other pin, V_{IN} . . . . . –0.3 V to (V_{CC} +0.3) V
Power dissipation, PD . . . . . 300 mW
Maximum operating junction temperature, T_{Jmax} . . . . . 150°C
Operating ambient temperature range, T_A . . . . . –40 °C to +85°C
Storage temperature range, T_{stg} . . . . . –65°C to +150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Logic 1 level, V_{IH}	2		V_{CC}	V
Logic 0 level, V_{IL}	–0.3		0.8	V
Supply voltage, V_{CC}	2.75		3.5	V
Operating free-air temperature, T_A	–40		85	°C
Operating junction temperature, T_J	–30		105	°C

typical power consumption, V_{CC} = 3 V

MODULE	OPERATING CURRENT (mA)	STANDBY CURRENT (μA)	OPERATING POWER (mW)	STANDBY POWER (μW)
LNA	11	5	33	15
RF mixer	18	5	54	15
Main VCO and buffers	6	5	18	15
First IF amplifier and IF mixer	22	15	66	45
Second IF amplifier and I/Q mixer	30	20	90	60
Second VCO and buffers	6	5	18	15
Total	93	55	279	165

electrical characteristics over recommended free-air temperature range (unless otherwise noted)

low noise amplifier (LNA), V_{CC} = 3 V (typical values)

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
RF frequency range		915		970	MHz
Power gain	High gain		12.4		dB
	Low gain		–5.8		dB
Noise figure	High gain		2.1		dB
	Low gain		N/A	N/A	
Gain/temperature sensitivity			0.003		dB/°C
Gain/frequency sensitivity			0.012		dB/MHz
Reverse isolation			20		dB
Input 1-dB compression	High gain		–12		dBm
	Low gain		> 5		
Input third-order intercept (IP3)	High gain		3.9		dBm
	Low gain		7.3		

RF mixer (MIX1), V_{CC} = 3 V (typical values)

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
RF frequency range		915		970	MHz
LO frequency range		975		1220	MHz
IF frequency range		40	149	180	MHz
Power conversion gain (see Note 3)			13.4		dB
SSB noise figure			8.3		dB
RF input resistance	Single ended		50		Ω
LO input impedance	Single ended		50		Ω
LO Power level	Into OS1-base, pin 23 (for external VCO applications)		–5		dBm
IF output load impedance	Open-collector output, 149 MHz differential		500		Ω
RF input 1-dB compression (see Note 3)			–9.1		dBm
RF input third-order intercept (see Note 3)	$\lvert f_2 - f_1 \rvert$ = 200 kHz, $f_{desired} = 2f_1 - f_2$		4.7		dBm
Input second-order intercept	$2 f_{LO} - 2 f_{RF}$, $f_{desired}$ = 925.2 MHz, f_{LO} = 1074.2 MHz, f_{RF} = 999.7 MHz		15		dBm
RF feedthrough to IF (see Note 3)	915 MHz to 970 MHz		–15.6		dBc
LO feedthrough to IF (see Note 3)	970 MHz to 1220 MHz		–35		dBm
LO feedthrough to RF (see Note 4)	975 MHz to 1220 MHz		–35		dBm

NOTES: 3. Into 500-Ω differential load
4. Into 50-Ω load

electrical characteristics over recommended free-air temperature range (unless otherwise noted) (continued)

first IF amplifier (IF1) and IF mixer (MIX2), V_{CC} = 3 V, T_A = 25°C, $f_{I(IF)}$ = 149 MHz, $f_{(LO)}$ = 97 MHz, $f_{O(IF)}$ = 52 MHz

PARAMETERS	TEST CONDITIONS		MIN	TYP	MAX	UNIT
IF frequency range			40		180	MHz
LO port frequency range			60		180	MHz
Second mixer output frequency range	Mixer on		10		80	MHz
	Mixer bypassed		40		180	
Power conversion gain at max IF gain setting (see Note 5)			39	42.5	46	dB
Dynamic range				39.5		dB
Gain error (see Note 6)	See Table 4			±1		dB
DSB noise figure at max IF gain				9.4	15	dB
IF input impedance	Differential			2		kΩ
LO input impedance	Single-ended			50		Ω
LO input level				–10		dBm
Output impedance	52 MHz, differential, open collector			2500		Ω
Input 1-dB compression (see Note 5)	Maximum IF gain			–61.6		dBm
	Minimum IF gain			–19.7		
Input third-order intercept (see Note 5)	$\lvert f_2 - f_1 \rvert$ = 200 kHz, $f_{desired} = 2f_1 - f_2$	Maximum IF gain		–52.5		dBm
		Minimum IF gain		–9.6		

NOTES: 5. For 500 Ω differential load.
6. Error at any gain step relative to gain state per Table 4 at a single frequency.

electrical characteristics over recommended free-air temperature range (unless otherwise noted) (continued)

second IF amplifier (IF2) and I/Q mixer ((IQMIX) and second VCO (OS2)), V_{CC} = 3 V, Vmid = V_{CC}/2, T_A = 25°C, $f_{I(IF)}$ = 52 MHz

PARAMETERS	TEST CONDITIONS		MIN	TYP	MAX	UNIT
IF frequency range			10		180	MHz
Power gain at max IF gain setting (see Note 7)			37	42	47	dB
Dynamic range				40		dB
Gain error (see Notes 7 and 8)	See Table 6			±1		dB
SSB noise figure	Maximum IF gain			12		dB
IF input impedance	Differential			2		kΩ
Input 1-dB compression (see Note 7)	Maximum IF gain			–55		dBm
	Minimum IF gain			–19		
Input third-order intercept (see Note 7)	$\|f_2 - f_1\|$ = 200 kHz, $f_{desired} = 2f_1 - f_2$	Maximum IF gain		–45		dBm
		Minimum IF gain		–9		
I and Q output impedance	Differential open collector			1100		Ω
I and Q output voltage swing (see Note 7)	Each differential line			1.7		Vpp
I and Q output dc level (see Note 7)	Each differential line			Vmid±10 mV (see Note 9)		V
I and Q baseband bandwidth (see Note 7)				200		kHz
I to Q output gain balance (see Note 7)	Between I or Q outputs			±0.5		dB
I or Q amplitude balance (see Note 7)				±0.69		dB
I or Q phase accuracy (see Note 7)				±1		deg

NOTES: 7. For 10-kΩ differential load at I and Q outputs
8. Error at any gain step is relative to gain setting per Table 6 at a single frequency.
9. DC compensation operating

second VCO (OS2), V_{CC} = 3 V (typical values)

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency range		180		720	MHz
Auxiliary LO output power	Into 100 Ω		–14.5		dBm
Phase noise	Offset = 200 kHz		–120		dBc/Hz

second VCO (OS2) divide-by-four output (OS2_DIV4), V_{CC} = 3 V

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency range		45		180	MHz
Output voltage level			250		mV_{p-p}

electrical characteristics over recommended free-air temperature range (unless otherwise noted) (continued)

serial interface timing requirements with $V_{DDP} = V_{DDA} \geq 2.75$ V and ≤ 3.5 V, $T_A = 25°C$ (see Figure 1)

PARAMETER		MIN	TYP	MAX	UNIT
C_i	CLOCK, DATA and STROBE input capacitance			10	pF
R_i	CLOCK, DATA and STROBE input resistance	10			kΩ
f_{clock}	CLOCK frequency	0		20	MHz
$t_{(r)}$, $t_{(f)}$	CLOCK input rise and fall time			8	ns
t_w(High)	Pulse duration, CLOCK high	20			ns
t_w(Low)	Pulse duration, CLOCK low	20			ns
t_{su}	Data setup time before CLOCK high	20			ns
	Strobe setup time before CLOCK high	20			ns
t_h	Data hold timeafter CLOCK high	20			ns
	Strobe hold time after CLOCK high	20			ns
$t_{w(pulse)}$	Strobe pulse width duration	$\frac{2}{REF\_IN}$			ns

cascaded performance $V_{CC} = 3$ V, LNA through Mixer1, $T_A = 25°C$

PARAMETER			MIN	TYP	MAX	UNIT
RF = 940 MHz, LO = 1089 MHz, IF = 149 MHz (measurements include filter loss)						
Cascaded gain		Max LNA gain setting	25	27	29	dB
		Min LNA gain setting		6.8		dB
Cascaded SSB NF		Max LNA gain setting		3.8	4.5	dB
Input, third order intercept	$\lvert f_2 - f_1 \rvert$ = 200 kHz	Max LNA gain setting		–8.9		dBm
		Min LNA gain setting		9.1		dBm
RF input return loss				8.4		dB
LO input return loss				13.5		dB
IF input return loss				10.6		dB

PARAMETER MEASUREMENT INFORMATION

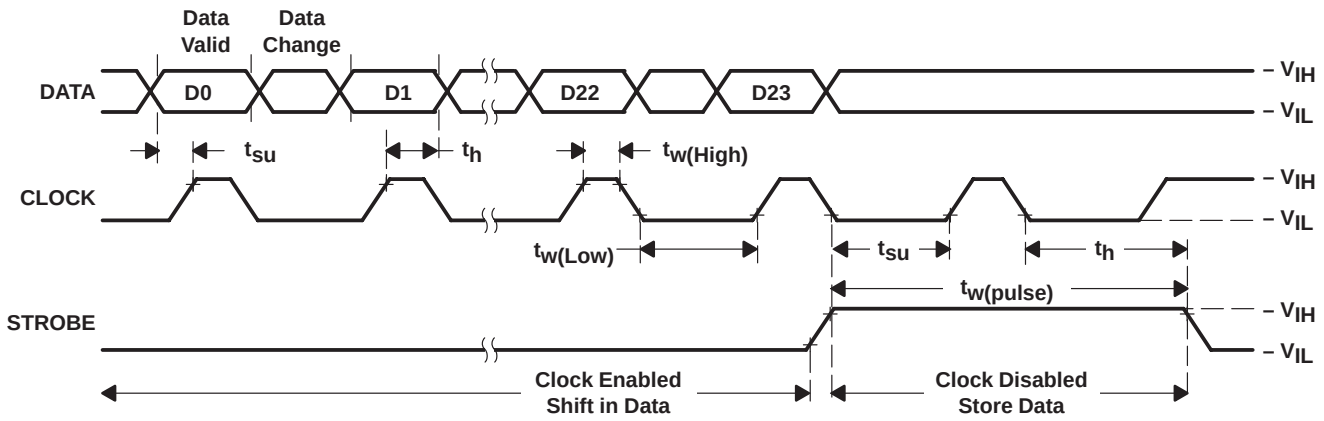


Figure 1. TRF1020 Timing Relationships

APPLICATION INFORMATION

Table 8. TRF1020 Evaluation Board Parts List

DESIGNATORS	DESCRIPTION	VALUE	SIZE (mm)	MANUFACTURER	MANUFACTURER P/N
C1, 2, 3, 4	Capacitor	100 pF	0402	Murata	GRM36COG101J50
C5,	Capacitor	9 pF	0402	Murata	GRM36COG090D50
C6	Capacitor	100 pF	0402	Murata	GRM36COG101J50
C7	Capacitor	10000 pF	0402	Murata	GRM36COG103K50
C10, 11	Capacitor	56 pF	0402	Murata	GRM36COG560J50
C14, 16	Capacitor	1 μF	3258B	Venkel	TA025TCM105KAR
C15	Capacitor	39 pF	0402	Murata	GRM36COG390J50
C19	Capacitor	56 pF	0402	Murata	GRM36COG560J50
C20	Capacitor	5 pF	0402	Murata	GRM36COG050D50
C21	Capacitor	5 pF	0402	Murata	GRM36COG050C50
C22	Capacitor	330 pF	1206	Murata	GRM42–6COG331J50
C23	Capacitor	1000 pF	0402	Murata	GRM36COG102Z50
C24	Capacitor	100 pF	0402	Murata	GRM36COG101J50
C25	Capacitor	4 pF	0402	Murata	GRM36COG040C50
C26	Capacitor	56 pF	0402	Murata	GRM36COG560K50
C27	Capacitor	100 pF	0402	Murata	GRM36COG101J50
C28	Capacitor	2.7 pF	0402	Murata	GRM36COG2R7J50
C29	Capacitor	100 pF	0402	Murata	GRM36COG101J50
C31	Capacitor	330 pF	1206	Murata	GRM42–6COG331J50
C32	Capacitor	100 pF	0402	Murata	GRM36COG101J50
C34	Capacitor	100 pF	0402	Murata	GRM36COG101J50
C35	Capacitor	220 pF	1206	Murata	GRM42-6COG221J50
C37	Capacitor	2 pF	0402	Murata	GRM36COG020C50

APPLICATION INFORMATION

Table 8. TRF1020 Evaluation Board Parts List (Continued)

DESIGNATORS	DESCRIPTION	VALUE	SIZE (mm)	MANUFACTURER	MANUFACTURER P/N
C38	Capacitor	33 pF	0402	Murata	GRM36COG330J50
C41, 42, 43, 44	Capacitor	10 pF	0402	Murata	GRM36COG100D50
C45, 46, 47	Capacitor	100 pF	0402	Murata	GRM36COG101J50
C48	Capacitor	220 pF	1206	Murata	GRM42-6COG221J50
C49	Capacitor	10000 pF	0402	Murata	GRM36COG103K50
C50, 51	Capacitor	100000 pF	0402	Murata	GRM36COG1042016
C52	Capacitor	10000 pF	0402	Murata	GRM36COG103K50
C53	Capacitor	56 pF	0402	Murata	GRM36COG056J50
C54	Capacitor	1 pF	0402	Murata	GRM36COG010C50
C55	Capacitor	1000 pF	0402	Murata	GRM36X7R102K50
C56	Capacitor	39pF	1206	Murata	GRM42–6COG390J50
C57	Capacitor	1 pF	0402	Murata	GRM36COG010C50
C58	Capacitor	3.3 pF	0402	Murata	GRM36COG3R3050
C59	Capacitor	18 pF	1206	Murata	GRM42–6COG180J50
C60	Capacitor	100 pF	0402	Murata	GRM36COG101J50
C61	Capacitor	10000 pF	0402	Murata	GRM36X7R103K16
C62	Capacitor	1000000 pF	3258B	Venkel	TA025TCM105KAR
C63	Capacitor	1000000 pF	1206	Murata	GRM42-6Y5V105
C64	Capacitor	100 pF	0402	Murata	GRM36COG101J50
C65	Capacitor	2 pF	0402	Murata	GRM36COG020C50
C66	Capacitor	6 pF	0402	Murata	GRM36COG060J50
C72	Capacitor	1000 pF	0402	Murata	GRM36Y5V102Z50
C73	Capacitor	33 pF	0402	Murata	GRM36COG330O50
C74, 75, 76	Capacitor	1000 pF	0402	Murata	GRM36Y5V102Z50
C77	Capacitor	82 pF	0402	Murata	GRM36COG820J50
C80	Capacitor	12 pF	0402	Murata	GRM36COG120O50
C81	Capacitor	5 pF	0402	Murata	GRM36COG050C50
C82	Capacitor	12 pF	0402	Murata	GRM36X7R120K16
C83	Capacitor	5 pF	0402	Murata	GRM36COG050C50
C84	Capacitor	9 pF	0402	Murata	GRM36COG090J50
C85	Capacitor	10000 pF	0402	Murata	GRM36COG103K50
C86	Capacitor	22 pF	0402	Murata	GRM36COG220J50
C87	Capacitor	5.6 pF	0603	Murata	GRM39COG5R6C50
L1	Inductor	150 nH	1008	Coilcraft	1008CS-151XKBC
L2	Inductor	470 nH	0603	Toko	LL2012-FR47K
L3	Inductor	180 nH	0805	Coilcraft	0805HS–181TKBC
L4	Inductor	6.8 nH	0603	Coilcraft	0603HS–6N8TKBC
L5	Inductor	15 nH	0603	Coilcraft	0603HS–15NTJBC

APPLICATION INFORMATION

Table 8. TRF1020 Evaluation Board Parts List (Continued)

DESIGNATORS	DESCRIPTION	VALUE	SIZE (mm)	MANUFACTURER	MANUFACTURER P/N
L6	Inductor	15 nH	0603	Coilcraft	0603HS-15NTJBC
L7	Inductor	6.8 nH	0603	Coilcraft	0603HS–6N8TJBC
L8, 9	Inductor	120 nH	0603	Coilcraft	0603HS-R12TJBC
L10	Inductor	180 nH	0805	Coilcraft	0805HS–180TKBC
L11	Inductor	150 nH	1008	Coilcraft	1008CS-151XKBC
L12	Inductor	56 nH	0603	Coilcraft	0603HS-56NTJBC
L13, 14	Inductor	3.9 nH	0603	Coilcraft	0603HS-3N9TKBC
L15, 16	Inductor	390 nH	1008	Coilcraft	1008CS–391XKBC
L17	Inductor	39 nH	0603	Coilcraft	0603HS–39NTJBC
L18	Inductor	390 nH	1008	Coilcraft	1008CS–391XKBC
L19	Inductor	120 nH	1008	Coilcraft	1008CS–121XKBC
L21	Inductor	39 nH	0805	Coilcraft	0805HS-390TMBC
L22	Inductor	6.8 nH	0402	Toko	LL1005–F6N8K
L23	Inductor	180 nH	0805	Coilcraft	0805HS–181TKBC
L25, 26	Inductor	47 nH	0603	Coilcraft	0603HS–47NTJBC
L27	Inductor	39 nH	0805	Coilcraft	0805HS-390TMBC
L28	Inductor	150 nH	0805	Coilcraft	0805HS–151TKBC
L29	Inductor	120 nH	0603	Coilcraft	0603HS–R12TJBC
R1, 2	Resistor	0 Ω	0402	Panasonic	ERJ–2GEJ0R00
R3	Resistor	10 kΩ	0402	Panasonic	ERJ-2GEJ103
R4	Resistor	1.5 kΩ	0402	Panasonic	ERJ-2GEJ152
R5, 6	Resistor	1 kΩ	0402	Panasonic	ERJ-2GEJ102
R7	Resistor	1.5kΩ	0402	Panasonic	ERJ-2GEJ152
R8	Resistor	1 kΩ	0402	Panasonic	ERJ-2GEJ102
R9	Resistor	1.5 kΩ	0402	Panasonic	ERJ-2GEJ152
R10	Resistor	1 kΩ	0402	Panasonic	ERJ-2GEJ102
R11	Resistor	1.5 kΩ	0402	Panasonic	ERJ-2GEJ152
R12	Resistor	10 kΩ	Trimpot	Bourns	3214W–1–103ECT
R13	Resistor	10 kΩ	0402	Panasonic	ERJ-2GEJ103
R14	Resistor	9.1 kΩ	0402	Panasonic	ERJ-2GEJ912
R15	Resistor	10 kΩ	0402	Panasonic	ERJ-2GEJ103
R16	Resistor	10 kΩ	0402	Panasonic	ERJ-2GEJ103
R17	Resistor	2 kΩ	Trimpot	Bourns	3214W–1–202ECT
R18, 21	Resistor	22 kΩ	0402	Panasonic	ERJ-2GEJ223
R19	Resistor	10 kΩ	Trimpot	Bourns	3214W–1–103ECT
R20, 22, 23	Resistor	10 kΩ	0402	Panasonic	ERJ-2GEJ103
R24	Resistor	9.1 kΩ	0402	Panasonic	ERJ-2GEJ912
R25	Resistor	10 kΩ	0402	Panasonic	ERJ-2GEJ103
R26	Resistor	2 kΩ	Trimpot	Bourns	3214W–1–202ECT
R29	Resistor	10 kΩ	0402	Panasonic	ERJ-2GEJ103
R30	Resistor	5.1kΩ	0402	Panasonic	ERJ–2GEJ512

APPLICATION INFORMATION

Table 8. TRF1020 Evaluation Board Parts List (Continued)

DESIGNATORS	DESCRIPTION	VALUE	SIZE (mm)	MANUFACTURER	MANUFACTURER P/N
R31, 32, 33	Resistor	0 Ω	0402	Panasonic	ERJ-2GEJ0R00
R36	Resistor	10 kΩ	Trimpot	Bourns	3214W-103ECT
R39	Resistor	200 Ω	0402	Panasonic	ERJ-2GEJ201
R40, 41	Resistor	50 Ω	0402	Panasonic	ERK-2GEJ201
R42	Resistor	47 kΩ	0402	Panasonic	ERJ-2GEJ473
R43	Resistor	0 Ω	0402	Panasonic	ERJ-2GEJ0R00
R44	Adj. Resistor	10 kΩ		Bourns	3296–Y–1–103
R50, 51	Resistor	0 Ω	0402	Panasonic	ERJ-2GEJ0R00
P1	Connector, 9-pin serial			Amp	745990-4
J1, 2, 4, 5, 6, 8, 10, 11, 12, 13, 14, 15	SMA board connector			EF Johnson	142-0701-801
J20, 21	DC voltage connector			Amp	4-103239-0
U1	Voltage regulator (3 V)			Toko	TK11230CT-ND
U10	GSM receiver			TI	TRF1020
U11, 12	Operational amplifiers			Motorola	MC34071D
CR1	Varactor diode			Motorola	MMBV2109
F1	Differential SAW filter			RF Monolithics	RFM_SF 1076A
F2	Bandpass filter			Murata	SAFC942.5MA7ON
T1, 2	Balun transformer			Toko	617PT1026
T3, 4	Balun transformer			MA/COM	ETC1–1–13

APPLICATION INFORMATION

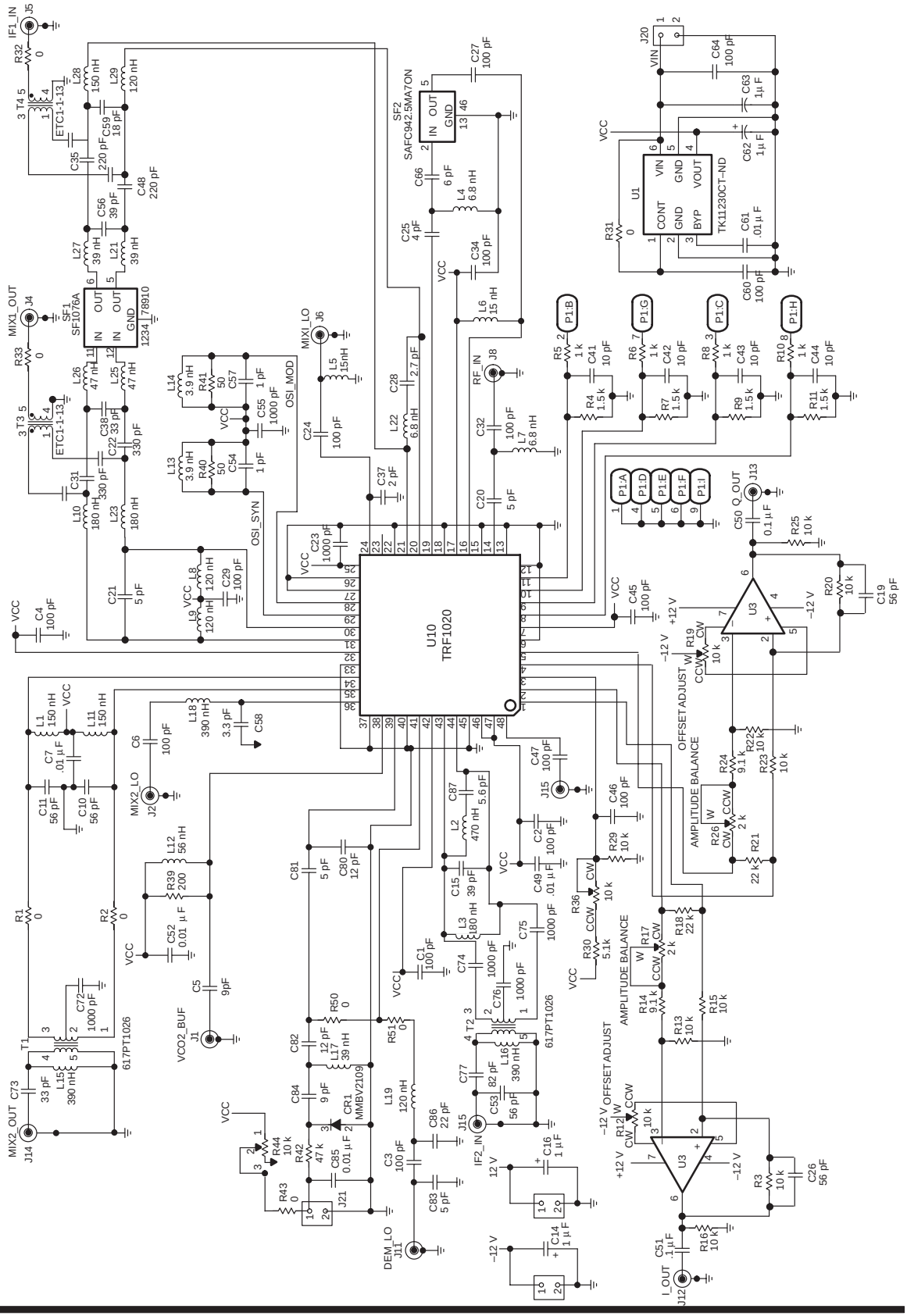


Figure 2. Evaluation Board Schematic

TYPICAL CHARACTERISTICS

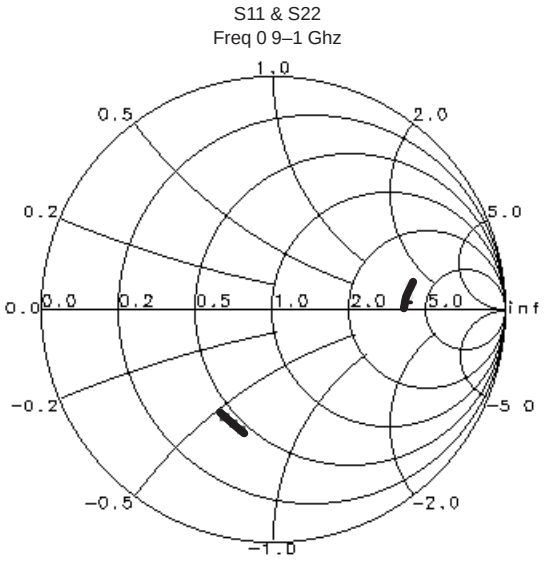


Figure 3. LNA S-Parameters

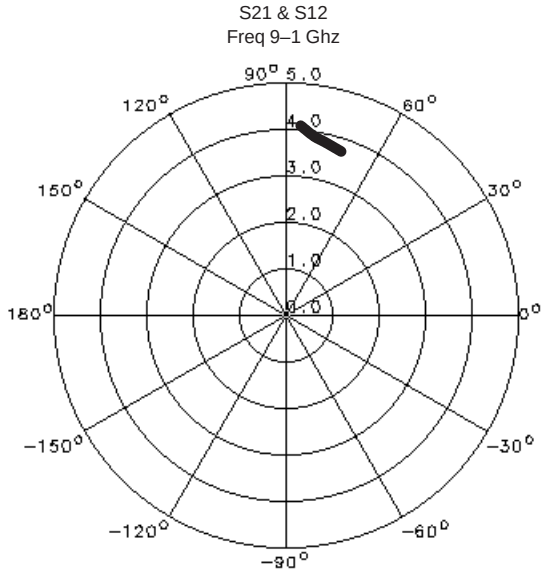


Figure 4. LNA Gain

Table 9. Listing of LNA S-Parameters (see Note 10)

FREQ (MHz)	S11 (MAG)	S11 (ANG)	S21 (MAG)	S21 (ANG)	S12 (MAG)	S12 (ANG)	S22 (MAG)	S22 (ANG)
920	0.528	–106.9	3.941	81.85	0.016	89.3	0.596	7.7
930	0.523	–108.0	3.906	80.50	0.016	88.4	0.590	6.5
940	0.520	–109.1	3.873	79.44	0.016	87.3	0.586	5.4
950	0.515	–110.2	3.854	78.36	0.017	86.3	0.582	4.2
960	0.512	–111.3	3.827	77.19	0.017	86.6	0.577	3.2
970	0.509	–112.7	3.813	76.05	0.017	85.7	0.571	2.2

NOTE 10: The numbers in Table 9 were taken using a 50-Ω setup with no I/O gain or noise-figure matching.

TYPICAL CHARACTERISTICS

LNA HIGH GAIN vs FREQUENCY

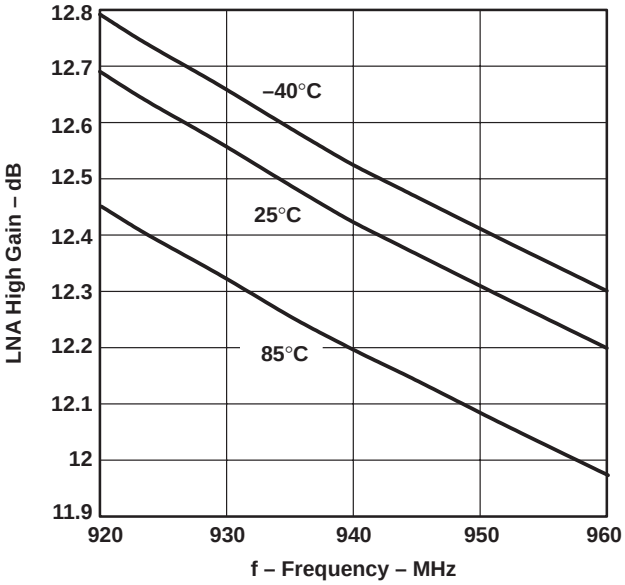


Figure 5

LNA HIGH-GAIN NOISE FIGURE vs FREQUENCY

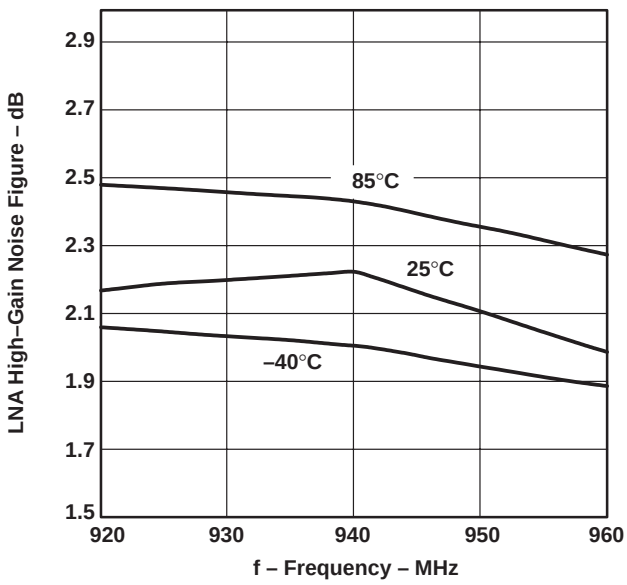


Figure 6

LNA HIGH-GAIN IP3 vs FREQUENCY

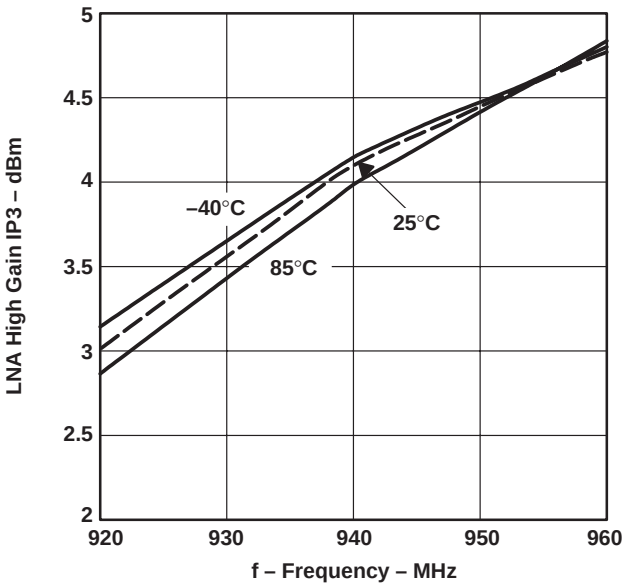


Figure 7

LNA HIGH-GAIN 1-dB COMPRESSION POINT vs FREQUENCY

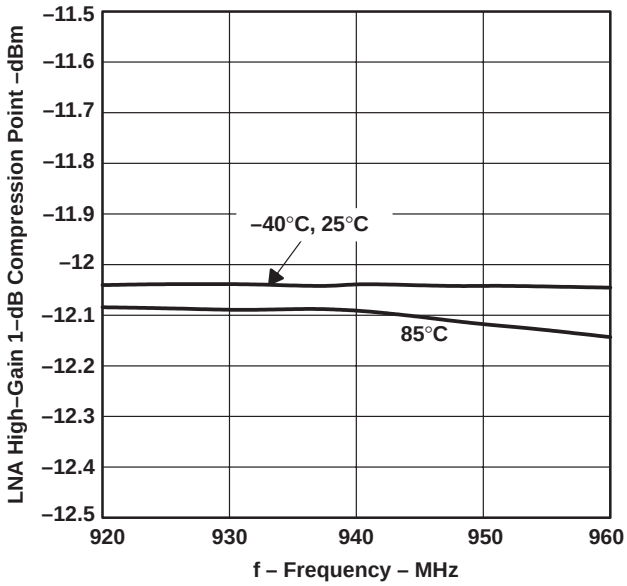


Figure 8

TYPICAL CHARACTERISTICS

LNA HIGH GAIN AT 25°C
vs
VOLTAGE

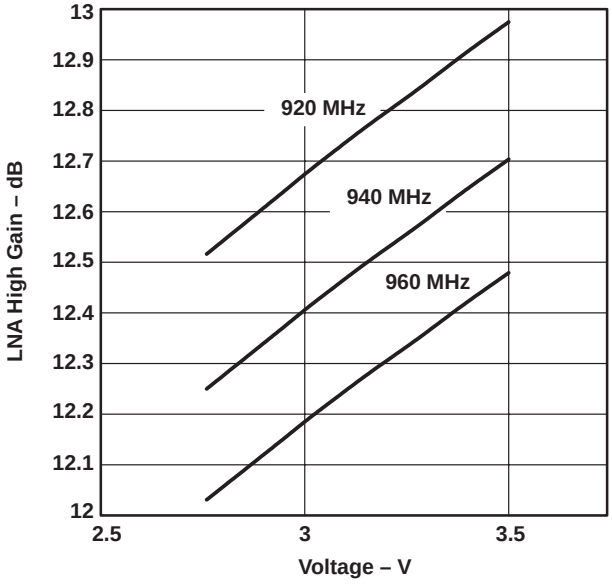


Figure 9

LNA HIGH-GAIN NOISE FIGURE AT 25°C
vs
VOLTAGE

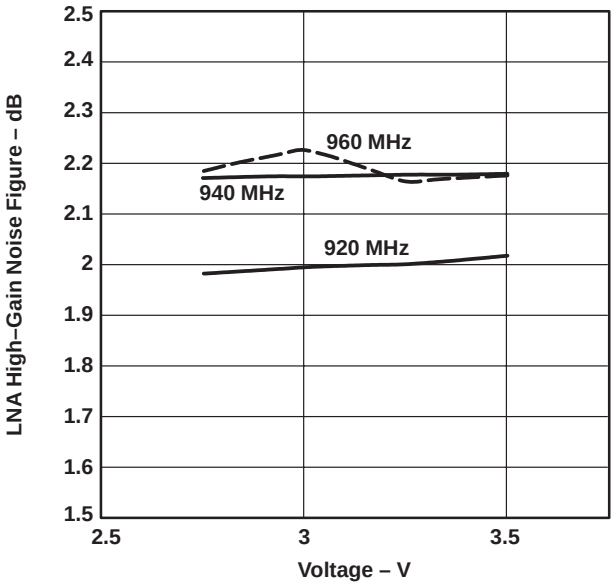


Figure 10

LNA HIGH-GAIN IP3 AT 25°C
vs
VOLTAGE

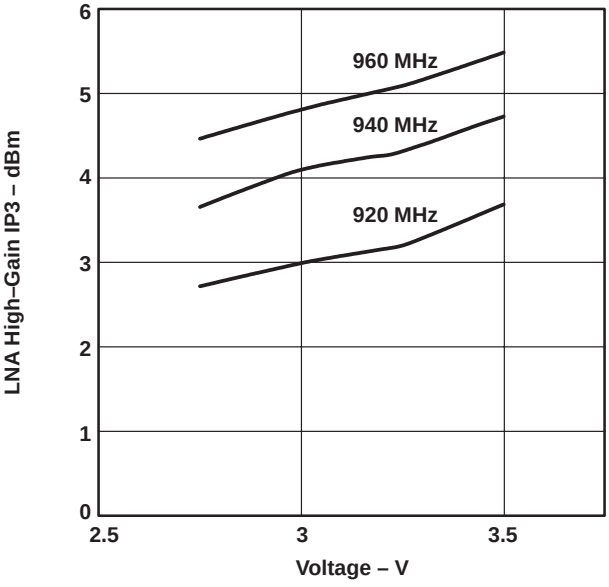


Figure 11

LNA HIGH-GAIN CURRENT AT 25°C
vs
VOLTAGE

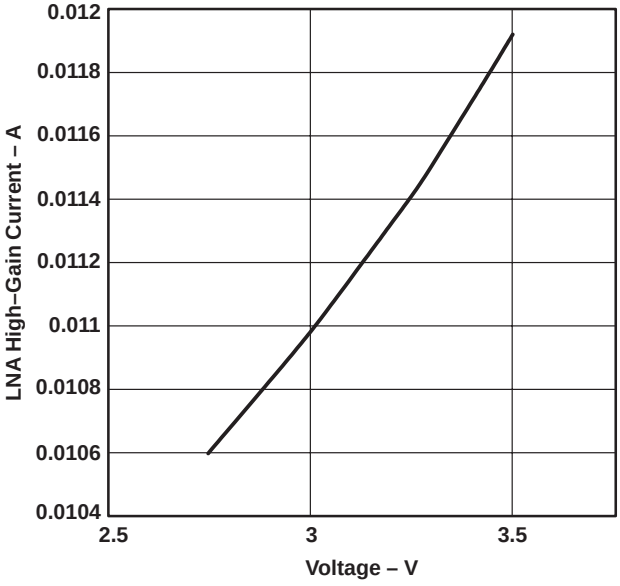


Figure 12

TYPICAL CHARACTERISTICS

MIX1 GAIN
vs
FREQUENCY

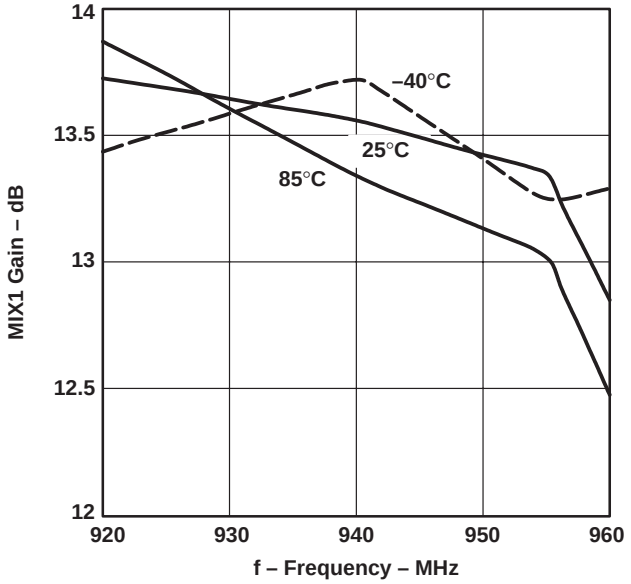


Figure 13

MIX1 SSB NOISE FIGURE
vs
FREQUENCY

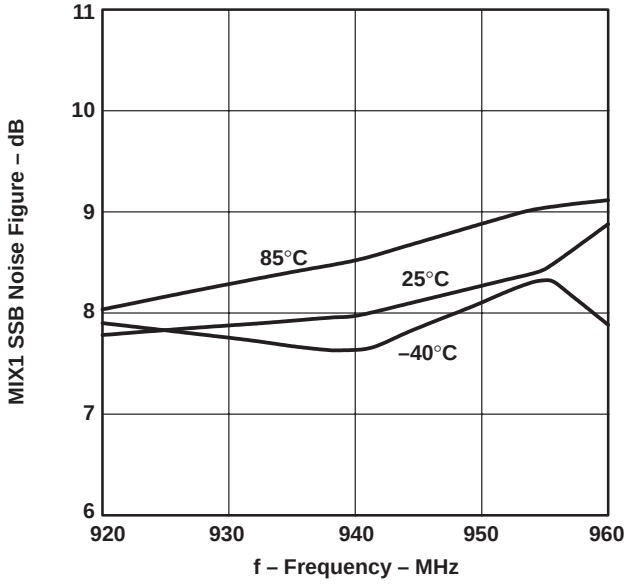


Figure 14

MIX1 IP3
vs
FREQUENCY

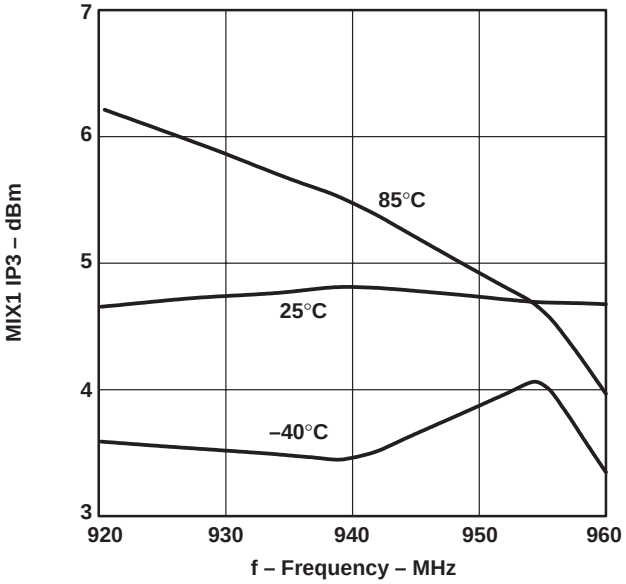


Figure 15

MIX1 1-dB COMPRESSION POINT
vs
FREQUENCY

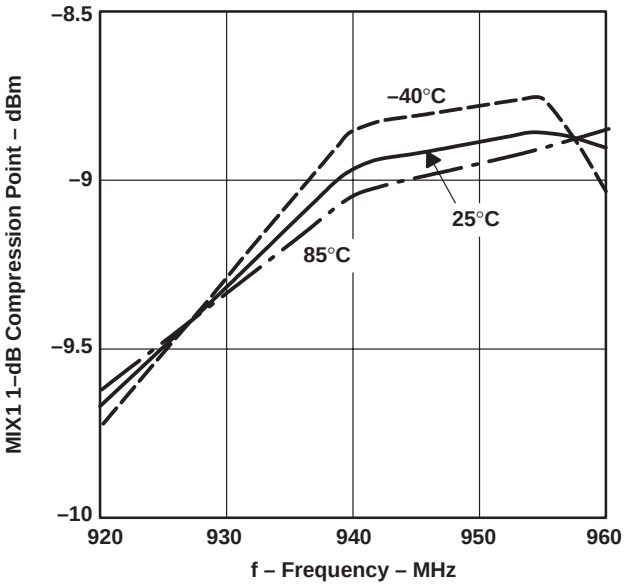


Figure 16

TYPICAL CHARACTERISTICS

MIX1 GAIN AT 25°C
vs
VOLTAGE

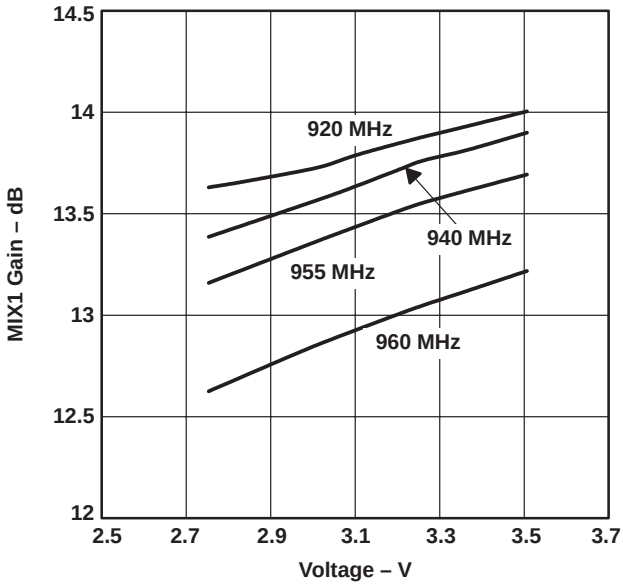


Figure 17

MIX1 NOISE FIGURE AT 25°C
vs
VOLTAGE

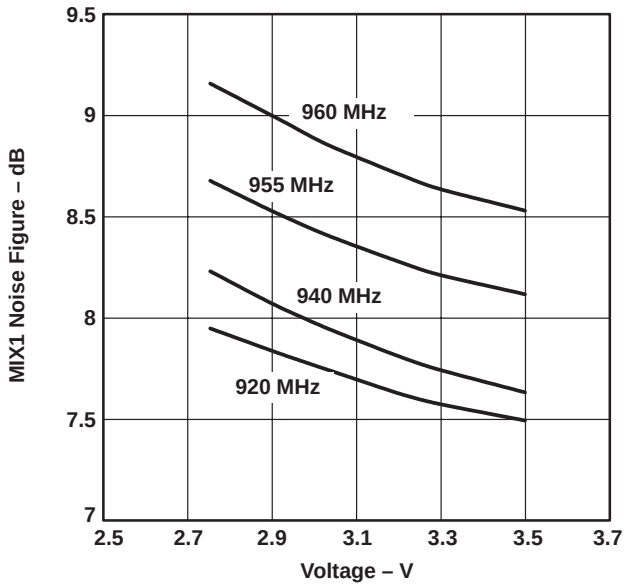


Figure 18

MIX1 IP3 AT 25°C
vs
VOLTAGE

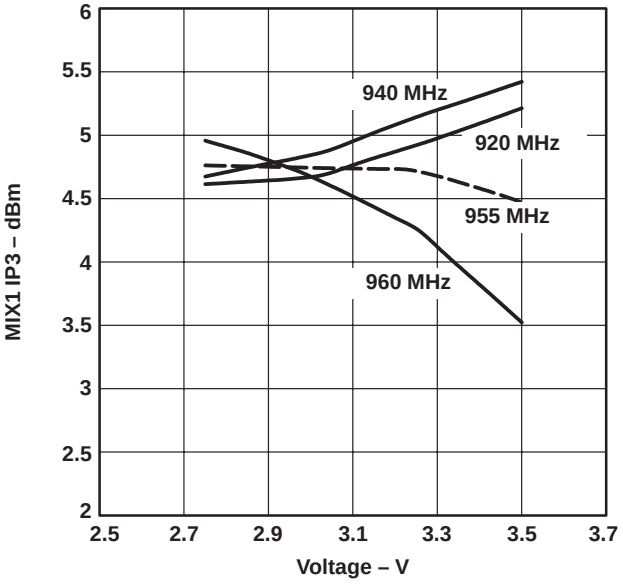


Figure 19

MIX1 CURRENT AT 25°C
vs
VOLTAGE

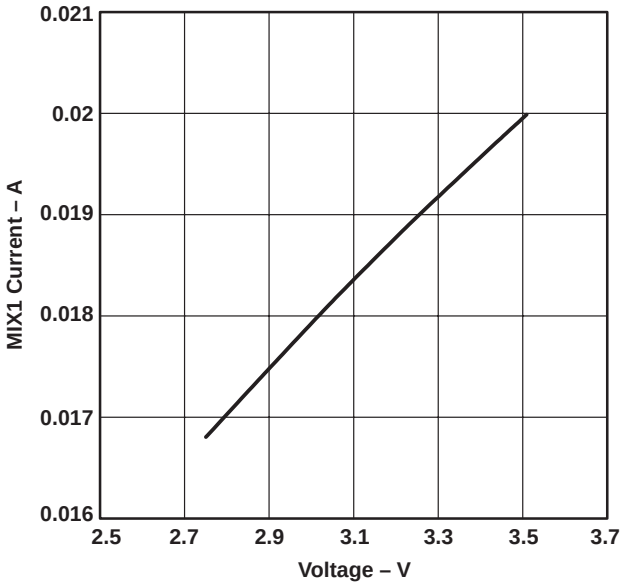


Figure 20

TYPICAL CHARACTERISTICS

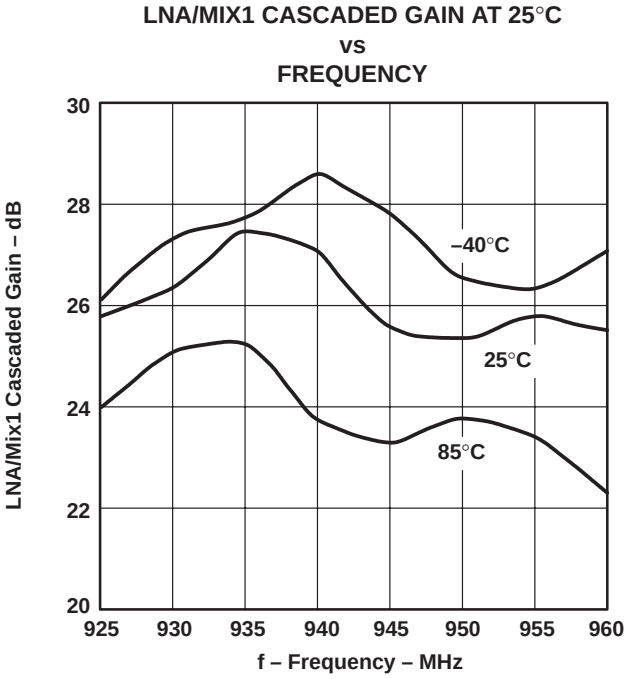


Figure 21

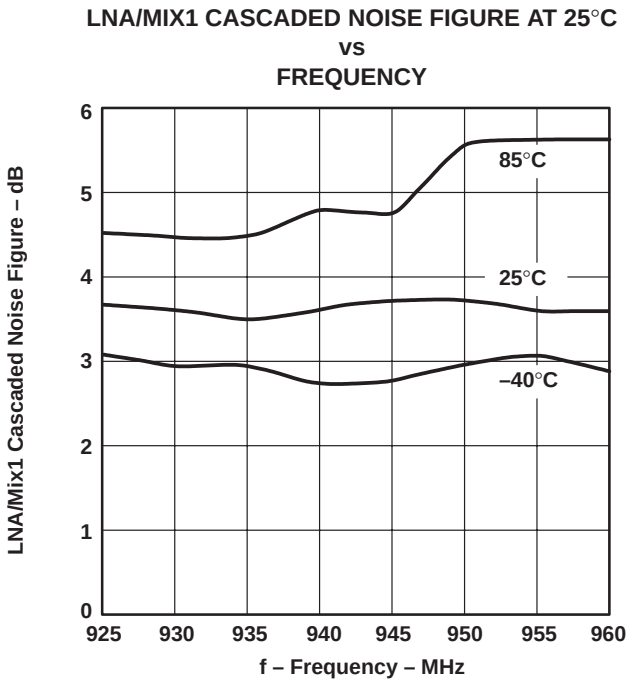


Figure 22

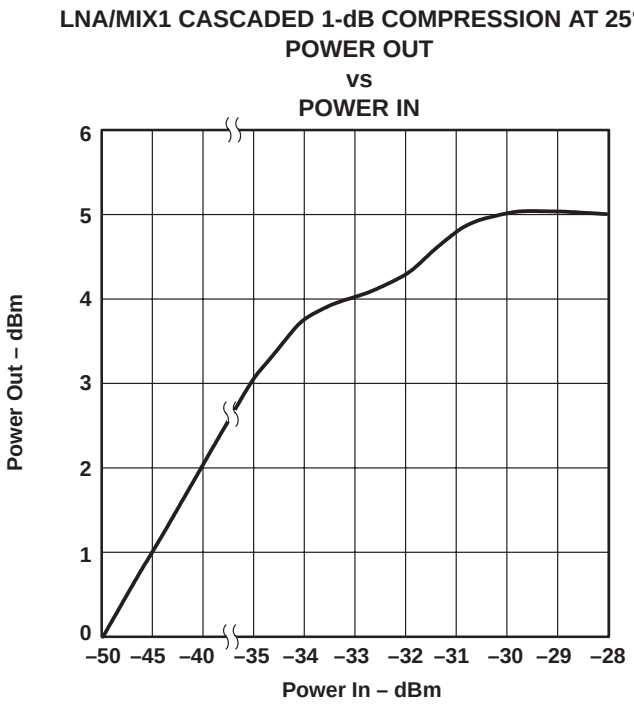
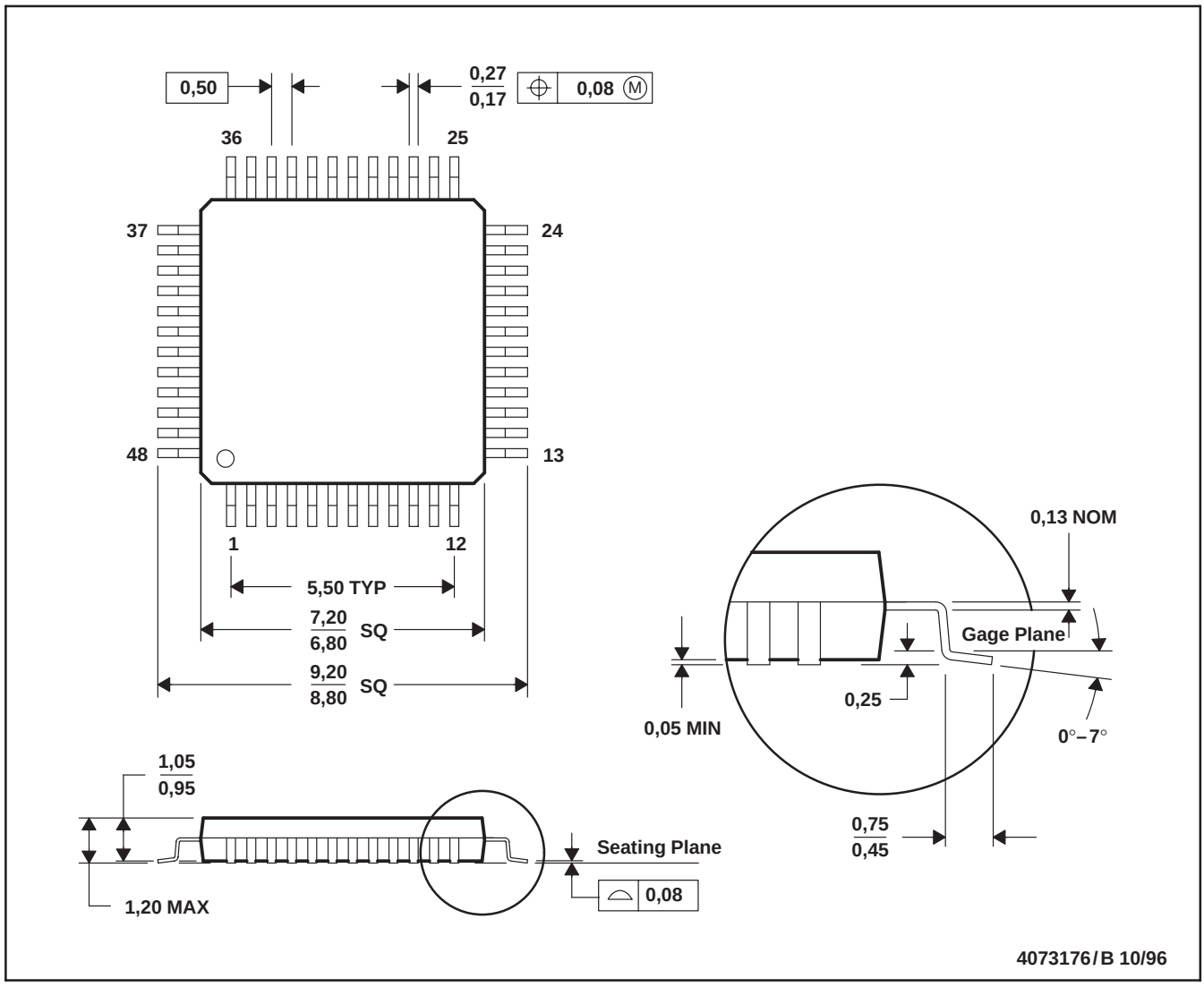


Figure 23

MECHANICAL DATA

PFB (S-PQFP-G48) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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