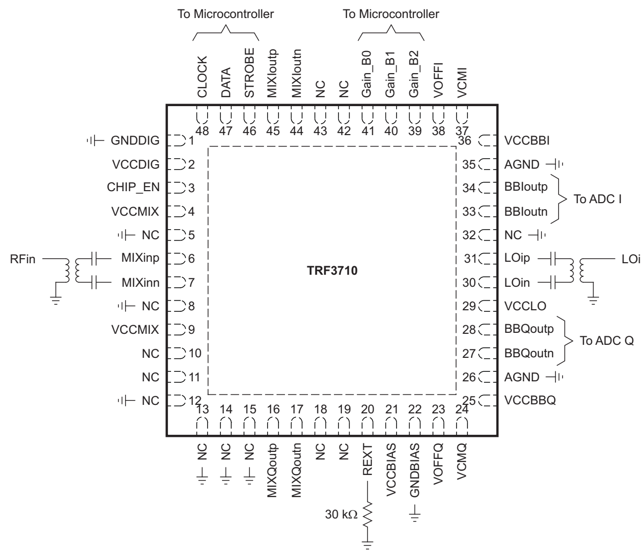
IQ DEMODULATOR

FEATURES

- **Frequency Range: 1.7 GHz to 2 GHz**
- **Integrated Baseband Programmable-Gain Amplifier**
- **On-Chip Programmable Baseband Filter**
- **High Cascaded IP3: 21 dBm at 1.9 GHz**
- **High IP2: 60 dBm at 1.9 GHz**
- **Hardware and Software Power Down**
- **3-Wire Serial Programmable Interface**
- **Single Supply: 4.5-V to 5.5-V Operation**



APPLICATIONS

- **Wireless Infrastructure:**
  - **WCDMA**
  - **CDMA**
- **Wireless Local Loop**
- **High-Linearity Direct Downconversion Receiver**

DESCRIPTION

The TRF3710 is a highly linear and integrated direct-conversion quadrature demodulator optimized for third-generation (3G) wireless infrastructure. The TRF3710 integrates balanced I and Q mixers, LO buffers, and phase splitters to convert an RF signal directly to I and Q baseband. The on-chip programmable-gain amplifiers allow adjustment of the output signal level without the need for external variable-gain (attenuator) devices. The TRF3710 integrates programmable baseband low-pass filters that attenuate nearby interference, eliminating the need for an external baseband filter.

Housed in a 7-mm × 7-mm QFN package, the TRF3710 provides the smallest and most integrated receiver solution available for high-performance equipment.

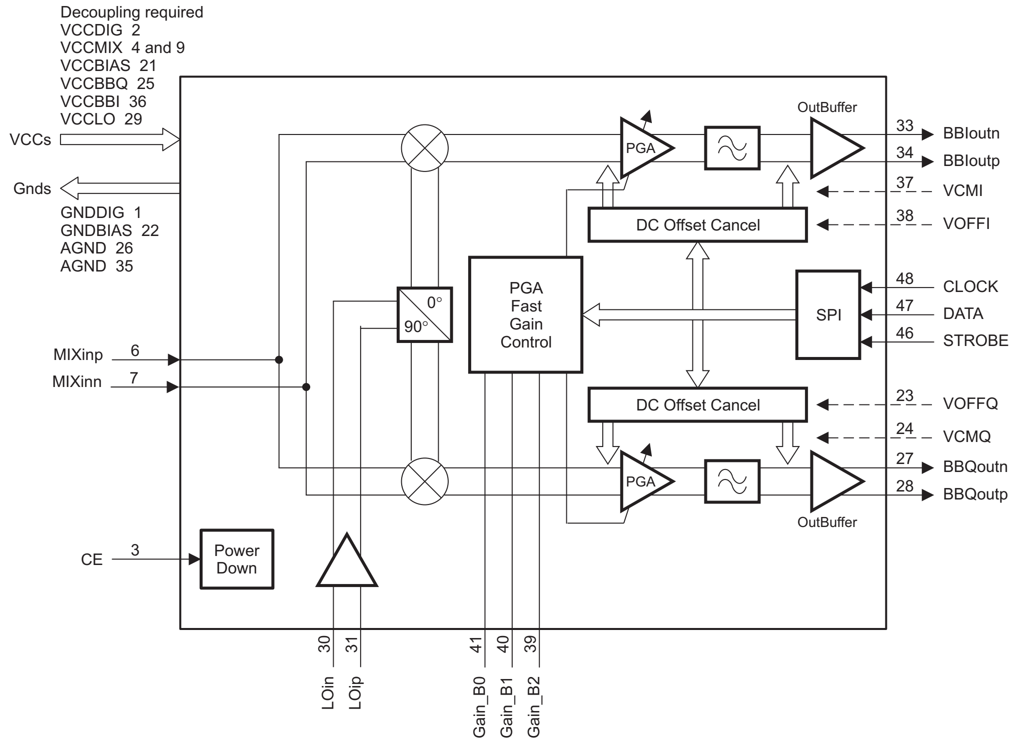
AVAILABLE DEVICE OPTIONS(1)

PRODUCT	PACKAGE LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKINGS	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
TRF3710	QFN-48	RGZ	–40°C to 85°C	TRF3710	TRF3710IRGZR	Tape and reel, 2500
					TRF3710IRGZT	Tape and reel, 500

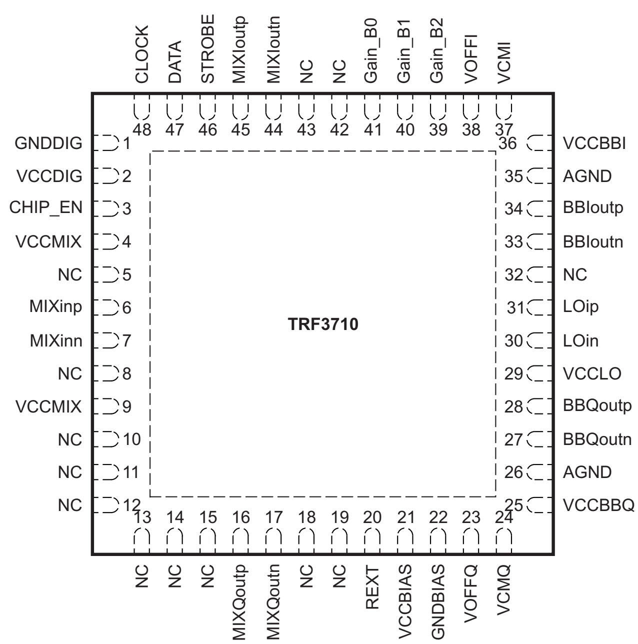
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

FUNCTIONAL BLOCK DIAGRAM



RGZ Package
(Top View)



TERMINAL FUNCTIONS

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AGND	26, 35		Analog ground; grounds can be tied together.
BBIoutn	33	O	Baseband I output: negative terminal
BBIoutp	34	O	Baseband I output: positive terminal
BBQoutn	27	O	Baseband Q output: negative terminal
BBQoutp	28	O	Baseband Q output: positive terminal
CHIP_EN	3	I	Chip enable; enabled = logic level 1, disabled = logic level 0
CLOCK	48	I	SPI clock input
DATA	47	I	SPI data input (programming data for baseband filter frequency setting, PGA gain settings, and dc offset calibration).
Gain_B0	41	I	PGA fast-gain control bit 0
Gain_B1	40	I	PGA fast-gain control bit 1
Gain_B2	39	I	PGA fast-gain control bit 2
GNDBIAS	22		Bias-block ground. Grounds can be tied together.
GNDDIG	1		Digital ground. Grounds can be tied together.
LOin	30	I	Local oscillator input: negative terminal
LOip	31	I	Local oscillator input: positive terminal
MIXinn	7	I	Mixer input: negative terminal, connected to external balanced-to-unbalanced (balun) transformer; balun type is frequency-specific.
MIXIoutn	44	O	Mixer I output: negative terminal (test pin). NC for normal operation
MIXIoutp	45	O	Mixer I output: positive terminal (test pin). NC for normal operation
MIXinp	6	I	Mixer input: positive terminal, connected to external balun; balun type is frequency-specific.
MIXQoutn	17	O	Mixer Q output: negative terminal (test pin). NC for normal operation
MIXQoutp	16	O	Mixer Q output: positive terminal (test pin). NC for normal operation
REXT	20	O	Reference-bias external resistor: 30 kΩ; used to set the bias of internal circuits of chip
STROBE	46	I	SPI enable (latches data into SPI after final clock pulse. Logic level = 1.
VCCBBQ	25		Baseband Q-chain power supply, 4.5 V to 5.5 V. Decoupled from other sources
VCCBIAS	21		Bias-block power supply, 4.5 V to 5.5 V. Decoupled from other sources
VCCDIG	2		Digital power supply, 4.5 V to 5.5 V. Decoupled from other sources
VCCLO	29		Local oscillator power supply, 4.5 V to 5.5 V. Decoupled from other sources
VCCMIX	4, 9		Mixer power supply, 4.5 V to 5.5 V. Decoupled from other sources
VCMQ	24	I	Baseband Q-chain input common mode, nominally 1.5 V
VOFFQ	23	I	Q-chain analog-offset correction input, 0 V to 3 V.
VCCBBI	36		Baseband I power supply, 4.5 V to 5.5 V. Decoupled from other sources
VCMI	37	I	Baseband I chain input common mode, nominally 1.5 V
VOFFI	38	I	I-chain analog-offset correction input, 0 V to 3 V

THERMAL CHARACTERISTICS

Over operating free-air temperature range (unless otherwise noted)

PARAMETER(1)		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Thermal derating, junction-to-ambient	Soldered slug, no airflow		26		°C/W
		Soldered slug, 200-LFM (1,016 m/s) airflow		20.1		
		Soldered slug, 400-LFM (2,032 m/s) airflow		17.4		
$R_{\theta JA}$(2)		7-mm × 7-mm, 48-pin PDFP		25		
$R_{\theta JB}$	Thermal derating, junction-to-board	7-mm × 7-mm, 48-pin PDFP		12		°C/W

(1) Determined using JEDEC standard JESD-51 with high-K board
(2) 16 layers, high-K board

ABSOLUTE MAXIMUM RATINGS[1]

Over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
	Supply voltage range[2]	–0.3 to 5.5	V
	Digital I/O voltage range	–0.3 to V_{CC} + 0.5	V
T_J	Operating virtual junction temperature range	–40 to 150	°C
T_A	Operating ambient temperature range	–40 to 85	°C
T_{stg}	Storage temperature range	–65 to 150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Power supply voltage	4.5	5	5.5	V
	Power supply voltage ripple			940	μV_{pp}
T_A	Operating ambient temperature range	–40		85	°C
T_J	Operating virtual junction temperature range	–40		150	°C

ELECTRICAL CHARACTERISTICS

Power supply = 5 V, LO = 0 dBm at 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]	MIN	TYP	MAX	UNIT
DC PARAMETERS						
I_{CC}	Total supply current			360		mA
	Power-down current			5		mA
IQ DEMODULATOR AND BASEBAND SECTION						
f_{RF}	Frequency range		1700		2000	MHz
G_{minBB}	Minimum gain				20	dB
G_{maxBB}	Maximum gain			43	45	dB
	Gain range		22	24		dB
	Gain step			1[2]		dB
NF_{BB}	Noise figure	Gain setting = 15		13.5	14.5	dB
$IIP3_{BB}$	Third-order input intercept point	Gain setting = 15 [3] [4]		21		dBm
$OIP3_{BB}$	Output third intercept point	Gain setting = 15; two tones, 1 V_{PP} each [5]		32		dBVrms
$OIP1_{BB}$	Output compression point	One tone[6]		3		dBVrms
$IIP2_{BB}$	Second-order input intercept point	Gain setting = 15[7]		60		dBm
f_{LPF}	Baseband low-pass filter cutoff frequency	1-dB point[8]	0.615		1.92	MHz

(1) Balun used for measurements: Band 1: 1700-MHz balun = Murata LDB211G8005C-001; Band 2: 1800- to 1900-MHz balun = Murata LDB211G9005C-001
(2) Between two consecutive gain settings
(3) Two CW tones of –30 dBm at ±900-kHz and ±1.7-MHz offset (baseband filter 1-dB cutoff frequency of minimum LPF).
(4) Two CW tones of –30 dBm at ±2.7-MHz and ±5.9-MHz offset (baseband filter 1-dB cutoff frequency of maximum LPF).
(5) Two CW tones at an offset from LO frequency smaller than the baseband filter cutoff frequency.
(6) Single CW tone at an offset from LO smaller than the baseband filter cutoff frequency.
(7) Two tones at $f_{RF1} = f_{LO} \pm 900$ kHz and $f_{RF2} = f_{LO} \pm 1$ MHz; IM_2 product measured at 100-kHz output frequency (for minimum baseband filter 1-dB cutoff frequency). The two tones are at $f_{RF1} = f_{LO} \pm 2.7$ MHz and $f_{RF2} = f_{LO} \pm 2.8$ MHz, and the IM_2 product measured at 100-kHz output frequency (for maximum baseband filter 1-dB cutoff frequency).
(8) Baseband low-pass filter 1-dB cutoff frequency is programmable through SPI between minimum and maximum values.

ELECTRICAL CHARACTERISTICS (continued)

Power supply = 5 V, LO = 0 dBm at 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]	MIN	TYP	MAX	UNIT
	Baseband relative attenuation at minimum LPF cutoff frequency[9]	615 kHz			1	dB
		900 kHz		10		
		1.7 MHz		50		
		5 MHz	60			
		20 MHz		100		
	Baseband relative attenuation at maximum LPF cutoff frequency[9]	1.92 MHz			1	dB
		2.7 MHz		10		
		5 MHz		50		
		20 MHz		100		
	Baseband filter phase linearity	RMS phase deviation from linear phase[10]		1.8		Degrees
	Baseband filter amplitude ripple	See [10]		0.5		dB
	Sideband suppression		35			dB
	Output load impedance	Parallel resistance		1		kΩ
		Parallel capacitance		20		pF
V_{CM}	Output common mode	Measured at I and Q channel baseband outputs	0.7	1.5	4	V
LOCAL OSCILLATOR PARAMETERS						
	Local oscillator frequency		1700		2000	MHz
	LO input level			0		dBm
	LO leakage	At MIXinn/p			–58	dBm
DIGITAL INTERFACE						
V_{IH}	High-level input voltage		2	5	V_{CC}	V
V_{IL}	Low-level input voltage		0		0.8	V
V_{OH}	High-level output voltage		0.8 V_{CC}			V
V_{OL}	Low-level output voltage				0.2 V_{CC}	V

(9) Attenuation relative to passband gain
(10) Across-filter passband: 615 kHz (minimum baseband filter cutoff frequency) and 1.92 MHz (maximum baseband filter cutoff frequency).

TIMING REQUIREMENTS

Power supply = 5 V, LO = 0 dBm at 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(CLK)}$	Clock period		50			ns
t_{su1}	Setup time, data		10			ns
t_h	Hold time, data		10			ns
t_w	Pulse width, STROBE		20			ns
t_{su2}	Setup time, STROBE		10			ns

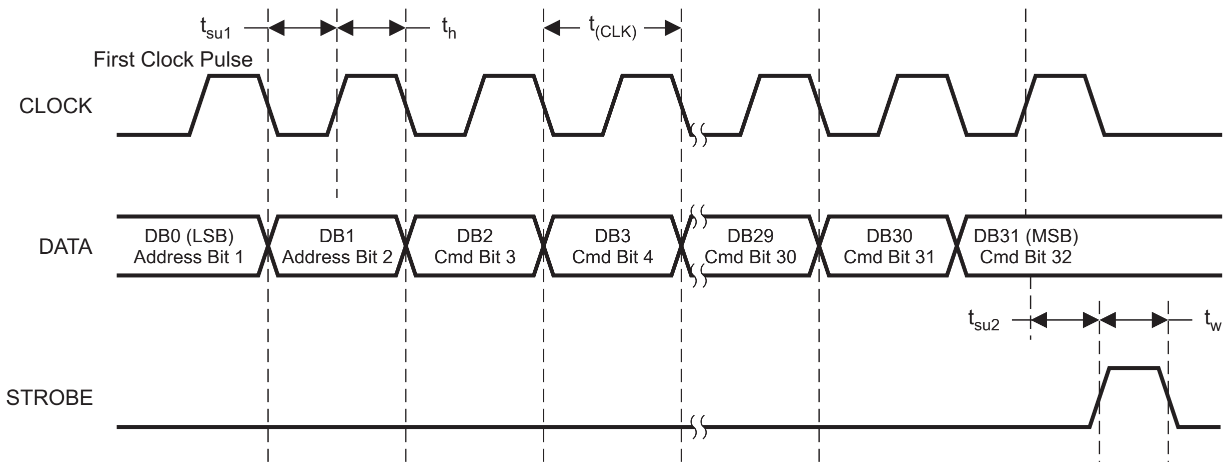


Figure 1. Serial Programming Timing

TYPICAL CHARACTERISTICS

V_{CC} = 5 V, T_A = 25°C, 1950 MHz, gain setting = 24 (unless otherwise stated).
(CDMA = *BBFREQ* = 90, WCDMA = *BBFREQ* = 7)

GAIN vs FREQUENCY

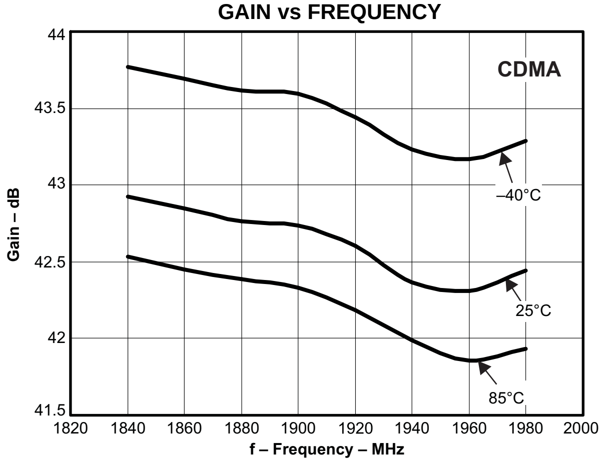


Figure 2.

GAIN vs GAIN STATE

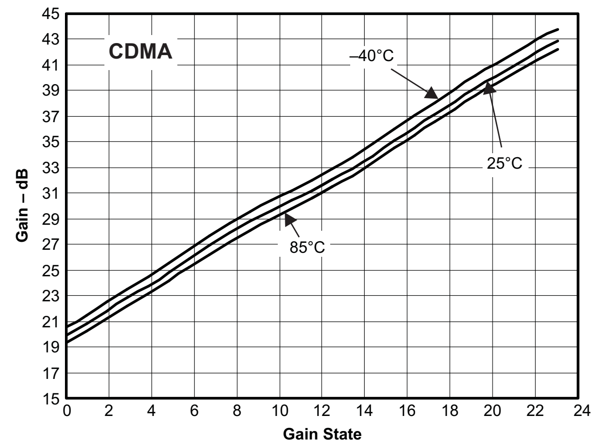


Figure 3.

IIP_3 vs FREQUENCY

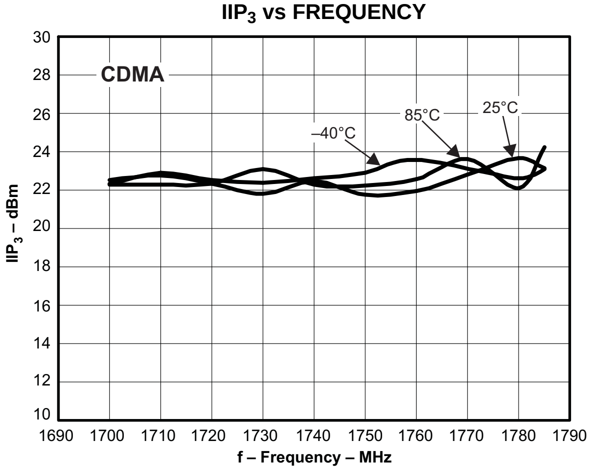


Figure 4.

IIP_3 vs FREQUENCY

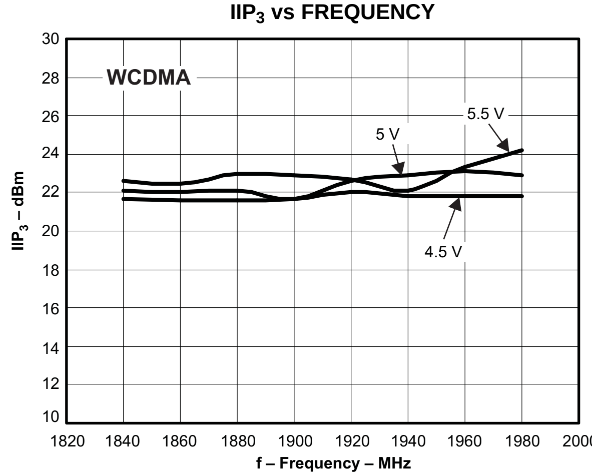


Figure 5.

IIP_3 vs FREQUENCY

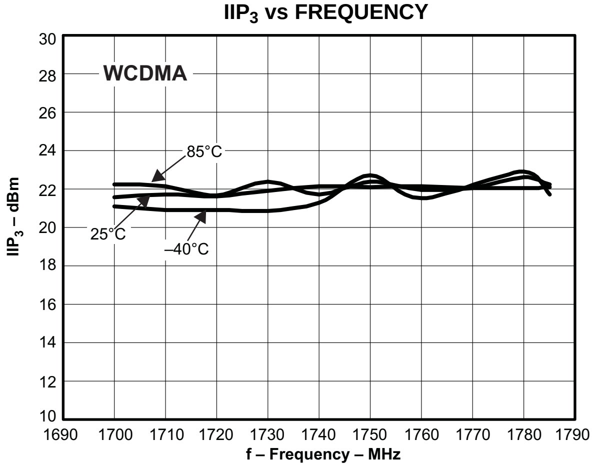


Figure 6.

IIP_3 vs FREQUENCY

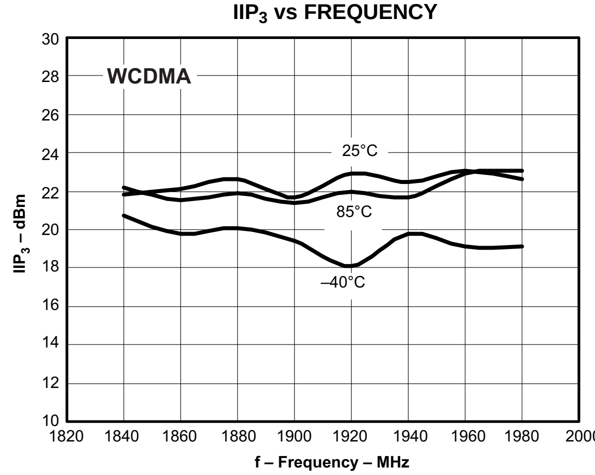


Figure 7.

TYPICAL CHARACTERISTICS (continued)

V_{CC} = 5 V, T_A = 25°C, 1950 MHz, gain setting = 24 (unless otherwise stated).
(CDMA = *BBFREQ* = 90, WCDMA = *BBFREQ* = 7)

IIP_2 vs FREQUENCY

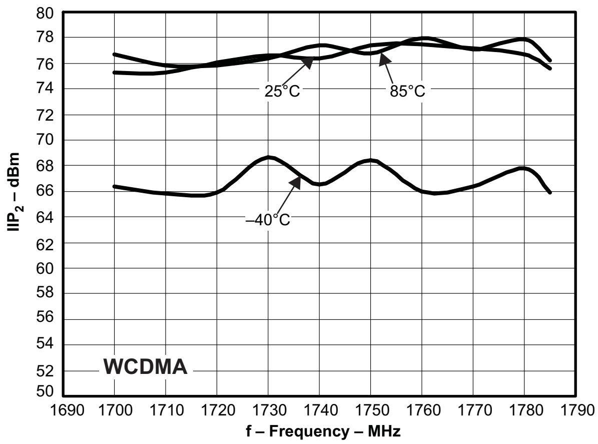


Figure 8.

IIP_2 vs FREQUENCY

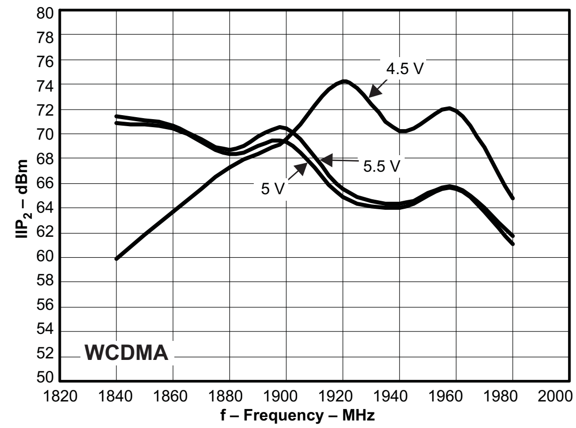


Figure 9.

IIP_2 vs FREQUENCY

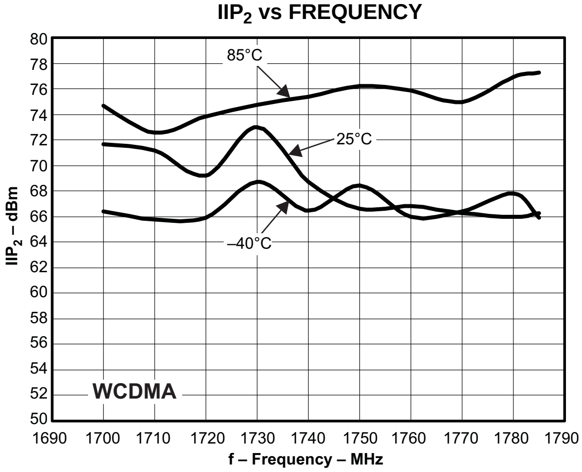


Figure 10.

IIP_2 vs FREQUENCY

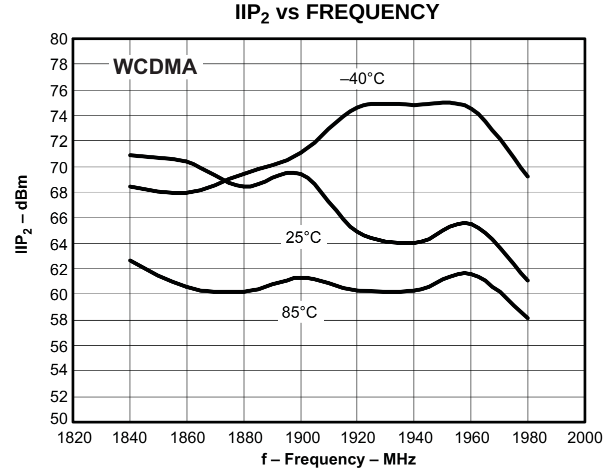


Figure 11.

OIP_3 vs FREQUENCY

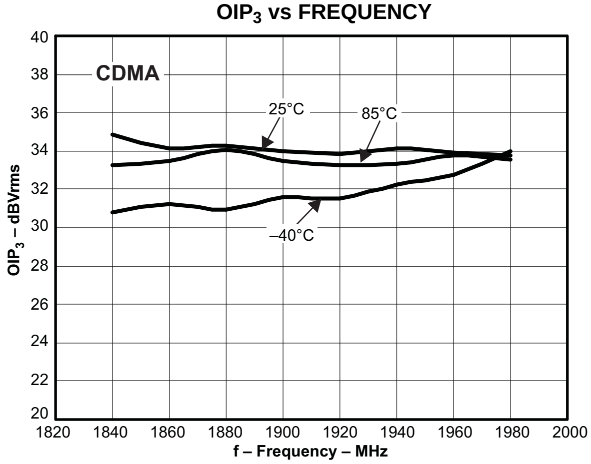


Figure 12.

OIP_3 vs FREQUENCY

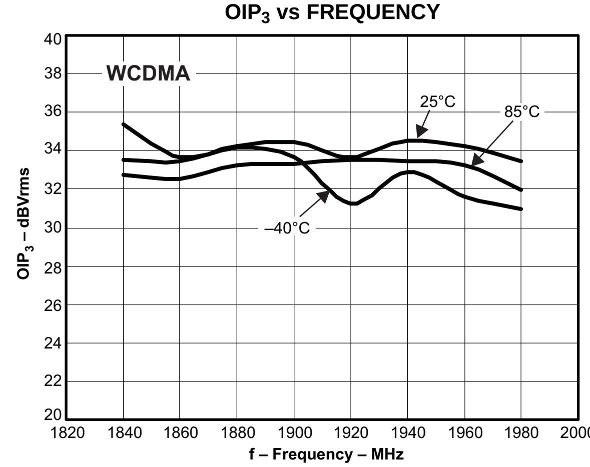


Figure 13.

TYPICAL CHARACTERISTICS (continued)

V_{CC} = 5 V, T_A = 25°C, 1950 MHz, gain setting = 24 (unless otherwise stated).
(CDMA = *BBFREQ* = 90, WCDMA = *BBFREQ* = 7)

OIP_3 vs GAIN STATE

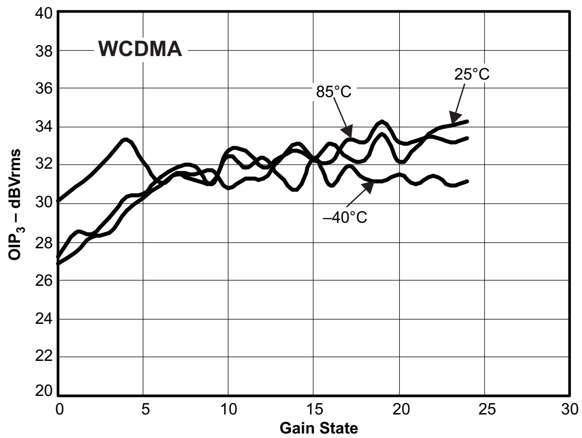


Figure 14.

OIP_3 vs GAIN STATE

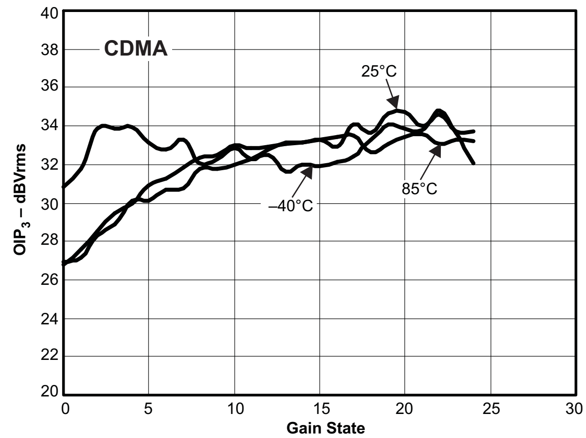


Figure 15.

OIP_3 vs LO POWER

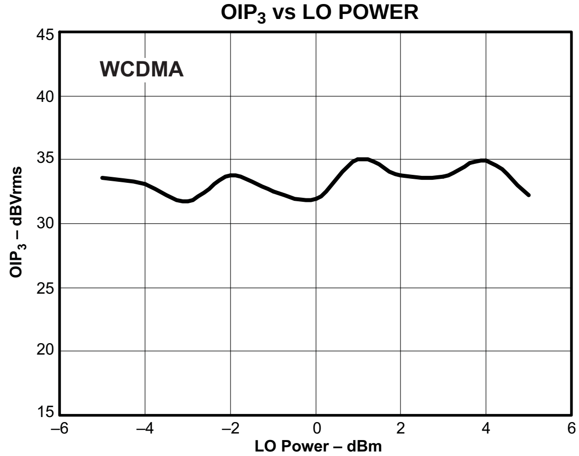


Figure 16.

IIP_3 vs LO POWER

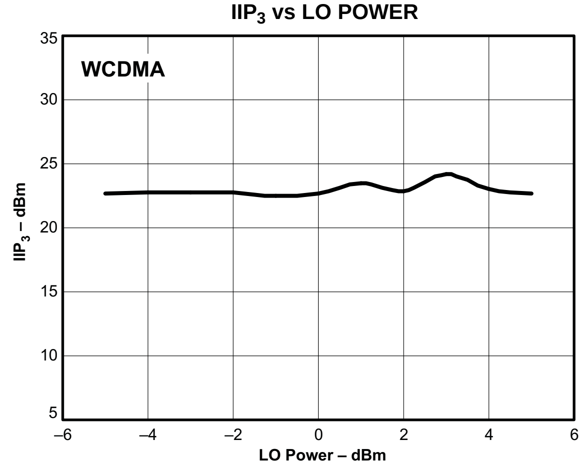


Figure 17.

IIP_2 vs LO POWER

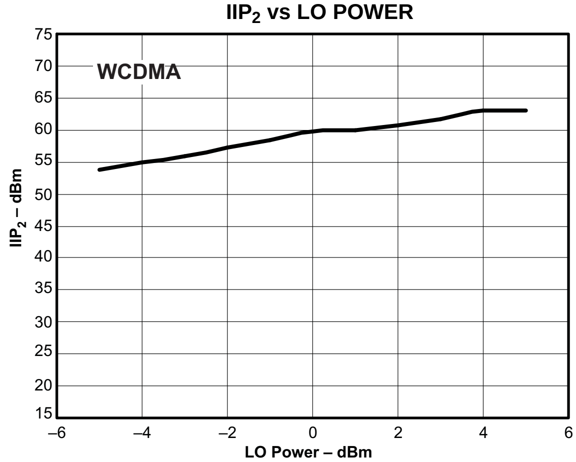


Figure 18.

GAIN ERROR vs GAIN STATE

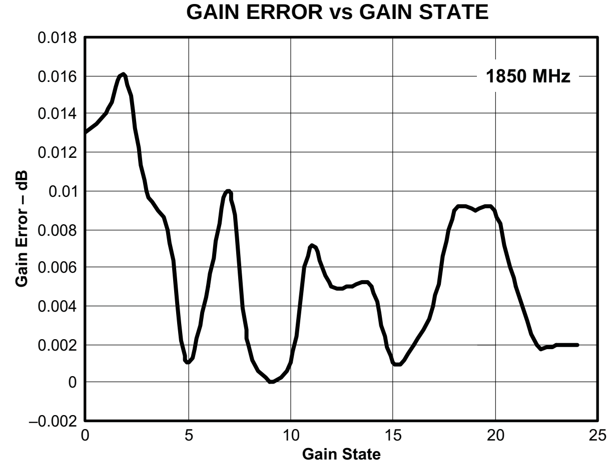


Figure 19.

TYPICAL CHARACTERISTICS (continued)

V_{CC} = 5 V, T_A = 25°C, 1950 MHz, gain setting = 24 (unless otherwise stated).
(CDMA = *BBFREQ* = 90, WCDMA = *BBFREQ* = 7)

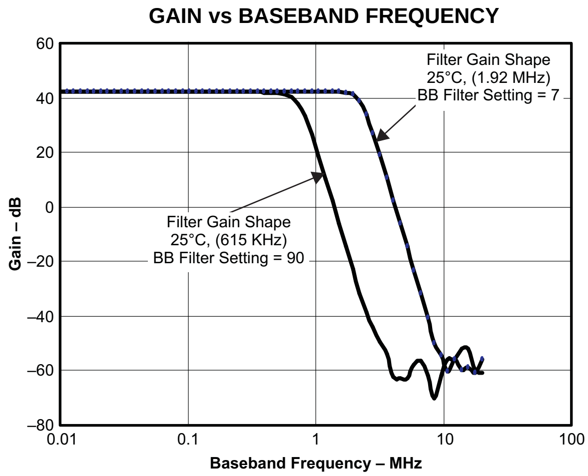


Figure 20.

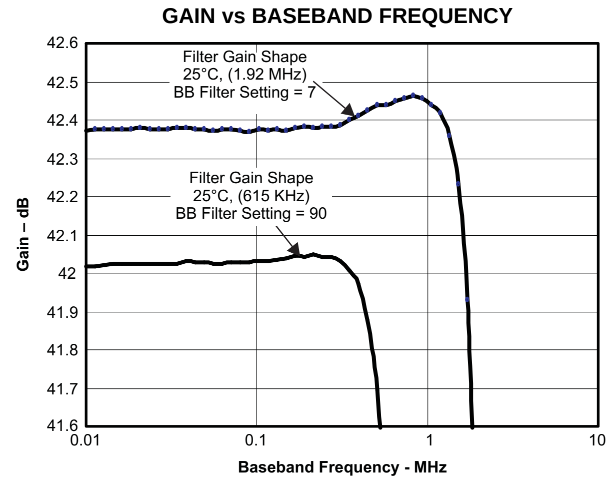


Figure 21.

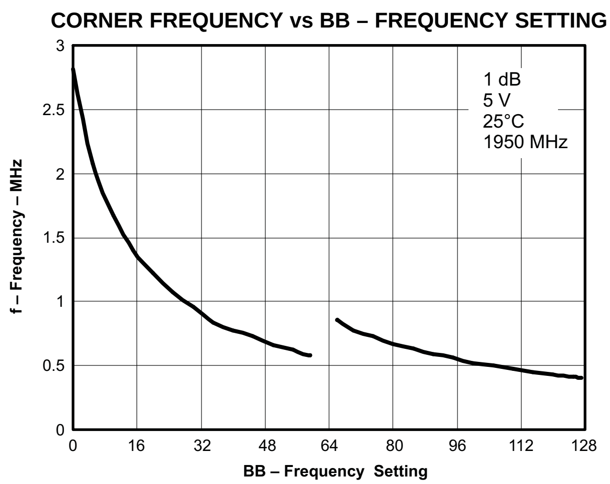


Figure 22.

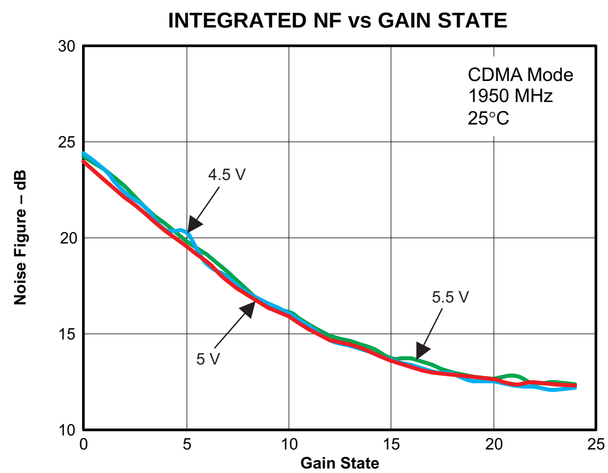


Figure 23.

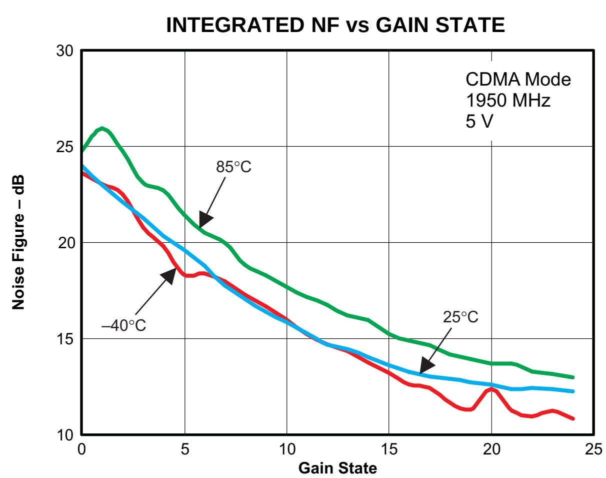


Figure 24.

TYPICAL CHARACTERISTICS

HISTOGRAM PLOTS

CONVERSION GAIN DISTRIBUTION

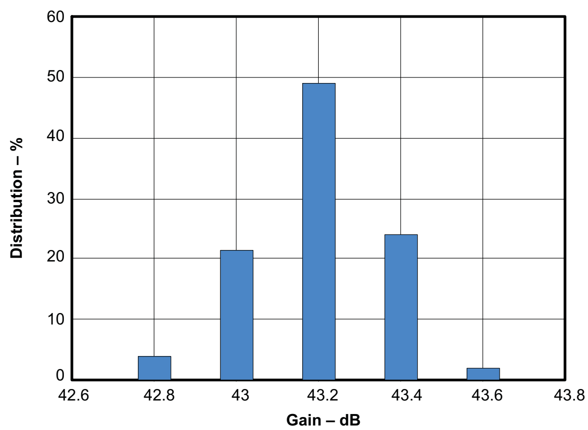


Figure 25.

IIP_3 DISTRIBUTION

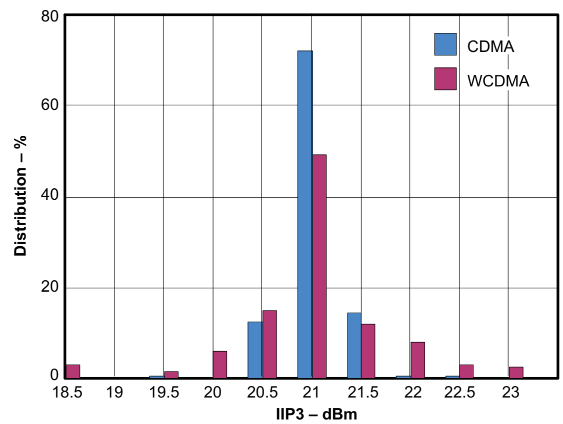


Figure 26.

IIP_2 DISTRIBUTION

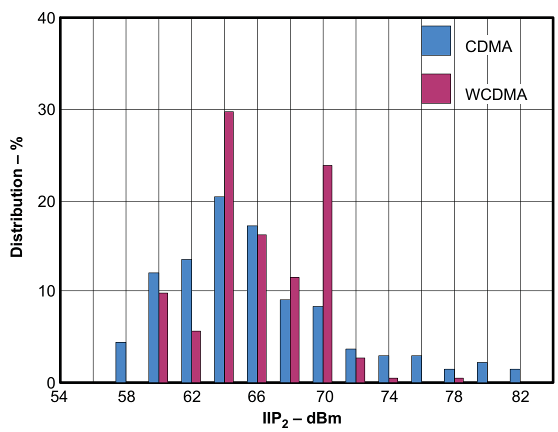


Figure 27.

OIP_3 DISTRIBUTION

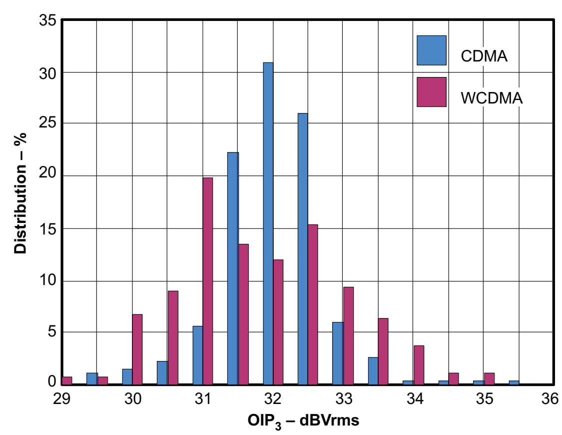


Figure 28.

NF DISTRIBUTION

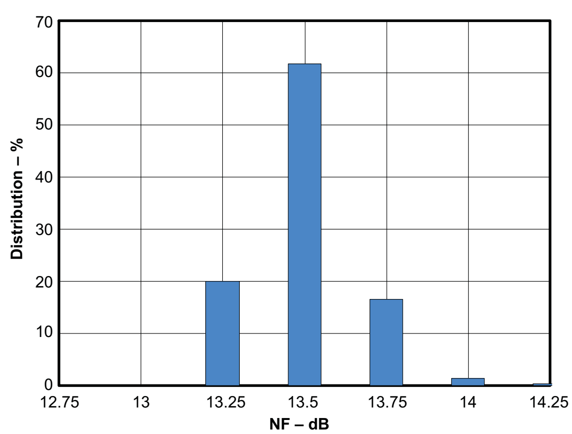
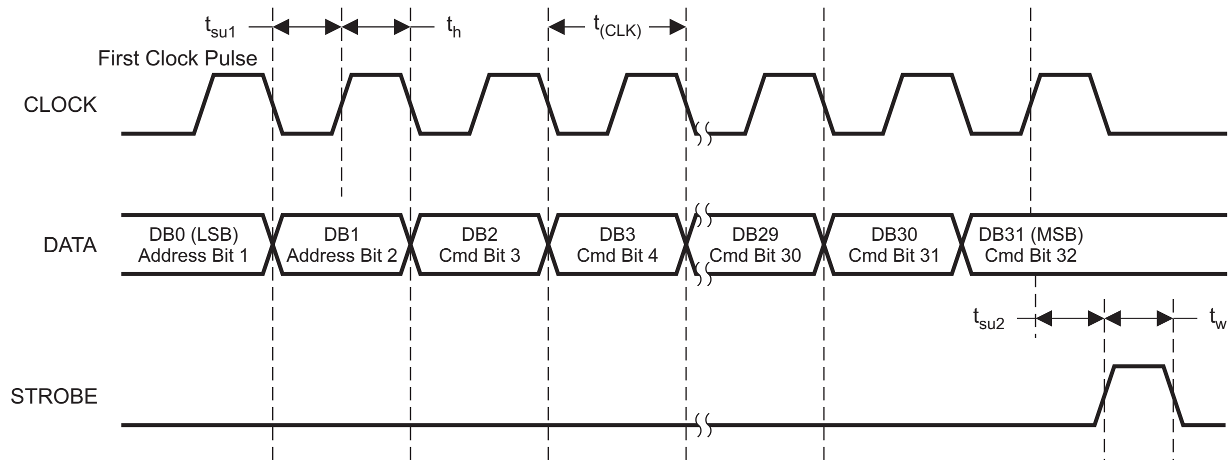


Figure 29.

SERIAL INTERFACE PROGRAMMING REGISTERS DEFINITION

The TRF3710 features a 3-wire serial programming interface (SPI) that controls an internal 32-bit shift register. There are a total of three signals that must be applied: CLOCK (pin 48), serial DATA (pin 47), and STROBE (pin 46). DATA (DB0–DB31) is loaded LSB-first and is read on the rising edge of the CLOCK. STROBE is asynchronous to CLOCK, and at its rising edge, the data in the shift register are loaded onto the selected internal register. The first two bits (DB0–DB1) are the address to select the available internal registers. Figure 30 shows the serial interface timing for the TRF3710.



PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(CLK)}$	Clock period		50			ns
t_{su1}	Setup time, data		10			ns
t_h	Hold time, data		10			ns
t_w	Pulse width, STROBE		20			ns
t_{su2}	Setup time, STROBE		10			ns

Figure 30. Serial Interface Timing

Register 0

Register Address		PWD Mixer	PWD LO Buff	PWD Test Buff	PWD Filter	PWD Output Buff	RSVD	PWD Dig Cal Block	PWD Ana Cal Block	Baseband Gain Setting					BB Freq Cutoff Set
Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7	Bit8	Bit9	Bit10	Bit11	Bit12	Bit13	Bit14	Bit15

Baseband Freq Cutoff Settings Cont.						RSVD		DC Detector Bandwidth		RSVD			Cal Reset	Spare	Spare
Bit16	Bit17	Bit18	Bit19	Bit20	Bit21	Bit22	Bit23	Bit24	Bit25	Bit26	Bit27	Bit28	Bit29	Bit30	Bit31

Figure 31. Register 0 Map

Table 1. Register 0: Device Setup

REGISTER 0	NAME	RESET VALUE	WORKING DESCRIPTION
Bit0	ADDR_0	0	Address bits
Bit1	ADDR_1	0	
Bit2	PWD_MIX	0	Mixer power down (off = 1)
Bit3	PWD_LO	0	LO buffer power down (off = 1)
Bit4	PWD_BUF1	1	Test buffer power down (off = 1)
Bit5	PWD_FILT	0	Baseband filter power down (off = 1)
Bit6	PWD_BUF2	0	Output buffer power down (off = 1)
Bit7	Reserved	0	
Bit8	PWD_DC_OFF_DIG	1	Digital calibration blocks power down (off = 1)
Bit9	PWD_DC_OFF_ANA	1	Analog calibration blocks power down (off = 1)
Bit10	BBGAIN_0	1	Sets baseband gain: the default power-on *BBGAIN* setting = 15 (corresponding to a typical gain of 34 dB). There are 25 gain settings (0 to 24) in 1-dB increments. For a desired device gain, the *BBGAIN* setting is determined by the following equation: *BBGAIN* setting = 24 – [(typical device gain at *BBGAIN* = 24) – (desired device gain)]. For example, for a desired device gain of 27 dB, the *BBGAIN* setting would be 24 – (43 – 27) = 8, which is bits 14–10 <0 1000>.
Bit11	BBGAIN_1	1	
Bit12	BBGAIN_2	1	
Bit13	BBGAIN_3	1	
Bit14	BBGAIN_4	0	
Bit15	BBFREQ_0	1	Sets BB frequency cutoff; default = 85. Example: For CDMA, the corner frequency is 615 kHz. See the 1-dB corner frequency vs. frequency setting plot Figure 22 to determine the setting, which is 90. Then set bit 15 through bit 21 to <101 1010>, which corresponds to 90.
Bit16	BBFREQ_1	0	
Bit17	BBFREQ_2	1	
Bit18	BBFREQ_3	0	
Bit19	BBFREQ_4	1	
Bit20	BBFREQ_5	0	
Bit21	BBFREQ_6	1	
Bit22	Reserved	1	
Bit23	Reserved	0	
Bit24	EN_FLT_B0	0	DC detector bandwidth
Bit25	EN_FLT_B1	0	
Bit26	Reserved	0	
Bit27	Internal use only	0	
Bit28	Internal use only	0	
Bit29	CAL_RESET	0	Reset the internal calibration logic when = 1.
Bit30	Spare0	0	
Bit31	Spare1	0	

- **Baseband PGA gain:** *BBGAIN*_[4:0] (B[14:10]) sets the gain of the baseband programmable gain amplifier. The acceptable values are from <0 0000> to <1 1000>. (See the *Gain Control* section for more information.)
- **Baseband filter cutoff frequency:** *BBFREQ*_[6:0] (B[21:15]) controls the baseband 1-dB cutoff frequency. An all-0s word sets the filter to its maximum cutoff frequency, whereas an all-1s word corresponds to minimum filter bandwidth.
- ***EN_FLT_B*[0:1]:** These bits control the bandwidth of the detector used to measure the dc offset during the automatic calibration. There is an RC filter in front of the detector that can be fully bypassed. *EN_FLT_B0* controls the resistor (bypass = 1), while *EN_FLT_B1* controls the capacitor (bypass = 1). The typical 3-dB cutoff frequencies of the detector bandwidth are summarized in Table 2 (see the *Application Information* section for more detail on the dc offset calibration and the detector bandwidth).

Table 2. Typical Cutoff Frequencies

EN_FLT_B1	*EN_FLT_B0*	Typical 3-dB Cutoff Frequency	Notes
X	0	10 MHz	Maximum bandwidth; bypass R, C
0	1	10 kHz	Enable R
1	1	1 kHz	Minimum bandwidth; enable R, C

Register 1

Register Address		Autocal	Enable Autocal	DAC Bits to Be Set During Manual Cal I/Q											
Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7	Bit8	Bit9	Bit10	Bit11	Bit12	Bit13	Bit14	Bit15

DAC Bits CONT				DC Offset Digital Cal. Resolution for I Channel		DC Offset Digital Cal. Resolution for Q Channel		Bin Search	Division Ratio for Clock Divider			Cal Clk Select	Internal Osc Freq Trimming		
Bit16	Bit17	Bit18	Bit19	Bit20	Bit21	Bit22	Bit23	Bit24	Bit25	Bit26	Bit27	Bit28	Bit29	Bit30	Bit31

Figure 32. Register 1 Map

Table 3. Register 1: Device Setup

REGISTER 1	NAME	RESET VALUE	WORKING DESCRIPTION
Bit0	ADDR_0	1	Address bits
Bit1	ADDR_1	0	
Bit2	AUTO_CAL	1	Auto dc offset correction when = 1; otherwise manual
Bit3	EN_AUTOCAL	0	Autocalibration begins when bit = 1. This bit is reset after calibration completes.
Bit4	IDAC_BIT0	0	DAC bits to be set during manual cal I/Q
Bit5	IDAC_BIT1	0	
Bit6	IDAC_BIT2	0	
Bit7	IDAC_BIT3	0	
Bit8	IDAC_BIT4	0	
Bit9	IDAC_BIT5	0	
Bit10	IDAC_BIT6	0	
Bit11	IDAC_BIT7	1	
Bit12	QDAC_BIT0	0	
Bit13	QDAC_BIT1	0	
Bit14	QDAC_BIT2	0	
Bit15	QDAC_BIT3	0	
Bit16	QDAC_BIT4	0	
Bit17	QDAC_BIT5	0	
Bit18	QDAC_BIT6	0	
Bit19	QDAC_BIT7	1	
Bit20	IDET_B0	1	Set the dc offset digital calibration resolution for I channel.
Bit21	IDET_B1	1	
Bit22	QDET_B0	1	Set the dc offset digital calibration resolution for Q channel.
Bit23	QDET_B1	1	
Bit24	Bin Search	1	Set to 1 for autocalibration; set to 0 for manual control.
Bit25	CLK_DIV_RATIO0	0	DC offset autocalibration clock divider: division ratios = 1, 8, 16, 128, 256, 1024, 2048, 16,684
Bit26	CLK_DIV_RATIO1	0	
Bit27	CLK_DIV_RATIO2	0	
Bit28	CAL_CLK_SEL	1	Select internal oscillator when 1; select SPI clock when 0.
Bit29	OSC_TRIM0	1	Internal oscillator frequency trimming 000 → 300 kHz 111 → 1.8 MHz
Bit30	OSC_TRIM1	1	
Bit31	OSC_TRIM2	0	

- ***AUTO_CAL* (Bit2):** When 1, the dc offset autocalibration is selected.
- ***EN_AUTOCAL* (Bit3):** Setting this bit to 1 starts the dc offset autocalibration. At the end of the calibration, the bit is reset to 0 (see the *Application Information* section for more details on dc offset correction).
- ***IDET_B*[1:0], *QDET_B*[1:0]:** These bits control the maximum output dc voltage of the dc-offset correction DAC (I and Q channels).
- ***CLK_DIV_RATIO*[2:0]:** Frequency divider for the calibration clock. The incoming clock (either the serial interface clock or the internal oscillator) divided by the divider ratio set by bits 25–27, generates the reference clock used during the autocalibration.
- ***CAL_CLK_SEL*:** Selects the internal oscillator or the external SPI clock as calibration clock
- ***OSC_TRIM*[2:0]:** Bits 29–31 control the internal oscillator frequency.

APPLICATION INFORMATION

GAIN CONTROL

The TRF3710 integrates a baseband programmable-gain amplifier (PGA) that provides 24 dB of gain range with 1-dB steps. The PGA gain is controlled through SPI by a 5-bit word (register 0, bits 10–14). Alternatively, the PGA can be programmed by a combination of 5 bits programmed through the SPI and three parallel external bits (pins Gain_B2, Gain_B1, Gain_B0). The parallel bits allow a fast gain change (0 db to 7 dB by 1-dB steps) without the need to reprogram the SPI registers.

The PGA gain control word (*BBGAIN*[0:4]) can be programmed to a setting between 0 and 24. This word is the sum of the SPI programmed gain (register 0, bits 10–14) and the parallel external 3 bits as shown in Figure 33. Setting the PGA gain setting above 24 is not valid. Typical applications set the PGA gain to 15, which allows room to adjust the PGA gain up or down to maintain desired output signal to the analog-to-digital converter over all conditions.

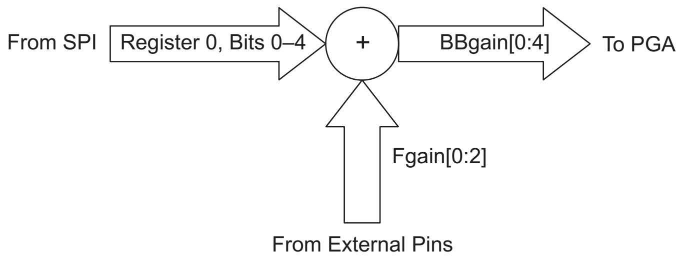


Figure 33. PGA Gain Control Word

For example, if a PGA gain setting of 20 dB is desired, then the SPI can be programmed directly to 20. Alternatively, the SPI gain register can be programmed to 15 and the parallel external bits set to 101 (binary), corresponding to an additional 5 dB.

AUTOMATED DC OFFSET CALIBRATION

The TRF3710 provides an automatic calibration procedure for adjusting the dc offset in the baseband I/Q paths. The digital dc offset correction is engaged by setting the *PWD_DC_OFF_DIG* (register 0, bit 8) to 0 and the *PWD_DC_OFF_ANA* (register 0, bit 9) to 1. The internal calibration requires a clock in order to function. TRF3710 can use the internal relaxation oscillator or the external SPI clock. Using the internal oscillator is the preferred method. Selecte the internal oscillator by setting the Cal_Sel_Clk (register 1, bit 28) to 1. The internal oscillator frequency is set through the *OSC_TRIM* bits (register 1, bits 29–31). The frequency of the oscillator is detailed in Table 4.

Table 4. Internal Oscillator Frequency Control

OSC_TRIM2	*OSC_TRIM1*	*OSC_TRIM0*	Frequency
0	0	0	300 kHz
0	0	1	500 kHz
0	1	0	700 kHz
0	1	1	900 kHz
1	0	0	1.1 MHz
1	0	1	1.3 MHz
1	1	0	1.5 MHz
1	1	1	1.8 MHz

The default setting of these registers corresponds to 900-kHz oscillator frequency; this setting is sufficient for autocalibration and does not need to be modified.

The internal dc offset correction DACs output full scale range is programmable (*IDET_B*[0:1] and *QDET_B*[0:1], register 1, bits 20–23). The range is shown in Table 5.

Table 5. DC Offset Correction DAC Programmable Range

I(Q)DET_B1	I(Q)DET_B0	Full Scale
0	0	10 mV
0	1	20 mV
1	0	30 mV
1	1	40 mV

The maximum dc offset correction range can be calculating by multiplying the values in Table 5 by the baseband PGA gain. The LSB of the digital correction depends on the programmed maximum correction range. For optimum resolution and best correction, the dc offset DAC range should be set to 10 mV for both the I and Q channels with the PGA gain set for the nominal condition. The output of the dc-offset-correction DAC is affected by a change in the PGA gain, but if the initial calibration yields optimum results, then the adjustment of the PGA gain during normal operation does not significantly impair the dc offset balance. For example, if the optimized calibration yields a dc offset balance of 2 mV at a gain setting of 17, then the dc offset maintains less than 10-mV balance as the gain is adjusted ±7 dB.

The dc offset correction DACs are programmed from the internal registers when the *AUTO_CAL* bit (register 1, bit 2) is set to 1. At start-up, the internal registers are loaded at half-scale, corresponding to a decimal value of 128. When an autocalibration is desired, verify that the *Bin_Search* bit (register 1, bit 24) is set to 1. Initiate the autocalibration process by toggling the *EN_AUTOCAL* bit (register 1, bit 3) to 1. When the calibration is over, this bit is automatically reset to 0. During calibration, the RF local oscillator must be applied.

At each clock cycle during an autocalibration sequence, the internal circuitry senses the output dc offset and calculates the new dc current for the DAC. After the ninth clock cycle, the calibration is complete and the *AUTO_CAL* bit is reset to 0. The dc offset DAC state is stored in the internal registers and maintained as long as the power supply is kept on, or until the *Cal Reset* (register 1, bit 29) is toggled to 1 or a new calibration is started.

The required clock speed for the optimum calibration is determined by the internal detector behavior (integration bandwidth, gain, sensitivity). The input bandwidth of the detector can be adjusted by changing the cutoff frequency of the RC low-pass filter in front of the detector (register 0, bits 24–25), corresponding to 3-dB corner-frequency steps of 10 MHz, 10 kHz, and 1 kHz. The speed of the clock can be slowed down by selecting a clock divider ratio (register 1, bits 25–27).

The detector has more averaging time the slower the clock; therefore, it can be desirable to slow down the clock speed for a given condition to achieve optimum results. For example, if there is no RF present on the RF input port, the detection filter can be left wide (10 MHz) and the clock divider can be left at div-by-1. The autocalibration yields a dc offset balance between the differential baseband output ports (I and Q) that is less than 15 mV. Some minor improvement may be obtained by increasing the averaging of the detector by increasing the clock divider up to 256.

However, if there is a modulated RF signal present at the input port, it is desirable to reduce the detector bandwidth to filter out most of the modulated signal. The detector bandwidth can be set to a 1-kHz corner frequency. With the modulated signal present, and with the detection bandwidth reduced, additional averaging is required to get optimum results. A clock divider setting of 1024 yields optimum results.

An increase in the averaging is possible by increasing the clock divider at the expense of longer converging time. The convergence time can be calculated by the following:

$$\tau_C = \frac{(\text{Auto\_Cal\_Clk\_Cycles}) \times (\text{Clk\_Divider})}{\text{Osc\_Freq}} \quad (1)$$

With a clock divider of 1024 and with the nominal oscillator frequency of 900 kHz, the convergence time is:

$$\tau_C = \frac{(9) \times (1024)}{900\ \text{kHz}} = 10.24\ \text{ms} \tag{2}$$

ALTERNATE METHOD FOR ADJUSTING DC OFFSET

The internal registers controlling the internal dc current DAC are accessible through the SPI, providing a user-programmable method for implementing the dc offset calibration. To employ this option, the *Auto Cal* bit must be set to 0 and the *Bin_Search* set to 0. During this calibration, an external instrument monitors the output dc offset between the I/Q differential outputs and programs the internal registers (*IDAC_BIT*[0:7] and *QDAC_BIT*[0:7] bits, register 1, bits 4–19) to cancel the dc offset.

The TRF3710 also offers a third dc offset calibration option to control the output dc offset by an external voltage (0–3 V) injected at the VOFFI and VOFFQ pins. Set *PWD_DC_OFF_DIG* (register 0, bit 8) to 1 (Off) and set *PWD_DC_OFF_ANA* (register 0, bit 9) to 0 to engage the external analog voltage control of the output dc offset. The analog voltage at the VOFFI and VOFFQ pins can be adjusted to provide the proper dc offset balance.

PCB LAYOUT GUIDELINES

The TRF3710 device is designed with a ground slug on the back of the package that must be soldered to the printed-circuit board (PCB) ground with adequate ground vias to ensure a good thermal and electrical connection. The recommended via pattern and ground pad dimensions are shown in Figure 34. The recommended via diameter is 8 mils (0.203 mm). The ground pins of the device can be directly tied to the ground slug pad for a low-inductance path to ground. Additional ground vias may be added if space allows. The NC (no connect) pins can also be tied to the ground plane.

Decoupling capacitors at each of the supply pins is recommended. The high-frequency decoupling capacitors for the RF mixers (VCCMIX) should be placed close to the respective pins. The value of the capacitor should be chosen to provide a low impedance RF path to ground at the frequency of operation. Typically, this value is around 10 pF or lower. The other decoupling capacitors at the other supply pins should be kept as close to the respective pins as possible.

The device exhibits symmetry with respect to the quadrature output paths. It is recommended that the PCB layout maintain that symmetry in order to ensure the quadrature balance of the device is not impaired. The I/Q output traces should be routed as differential pairs and the lengths all kept equal to each other. Decoupling capacitors for the supply pins should be kept symmetrical where possible. The RF differential input lines related to the RF input and the LO input should also be routed as differential lines with the respective lengths kept equal. If an RF balun is used to convert a single-ended input to a differential input, then the RF balun should be placed close to the device. Implement the RF balun layout according to the manufacturer's guidelines to provide best gain and phase balance to the differential outputs. On the RF traces, maintain proper trace widths to keep the characteristic impedance of the RF traces at a nominal 50 Ω.

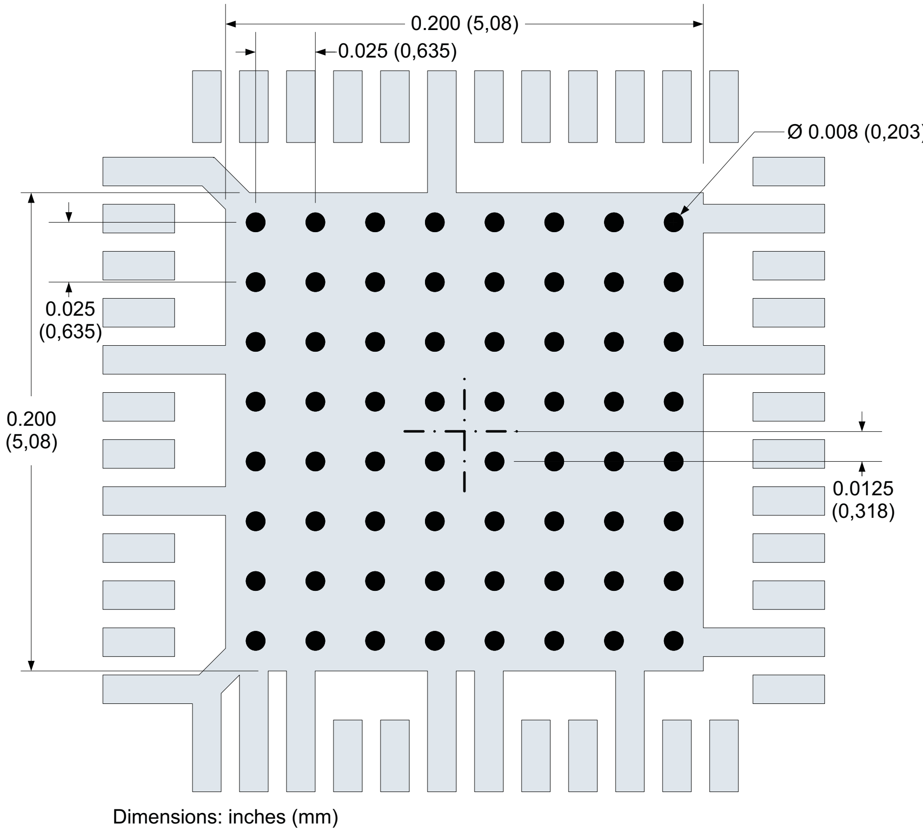


Figure 34. PCB Layout Guidelines

APPLICATION SCHEMATICS

The typical application schematic is shown in Figure 35. The RF bypass capacitors and coupling capacitors are depicted with 10-pF capacitors. These values can be adjusted to provide the best high-frequency bypass based on the frequency of operation.

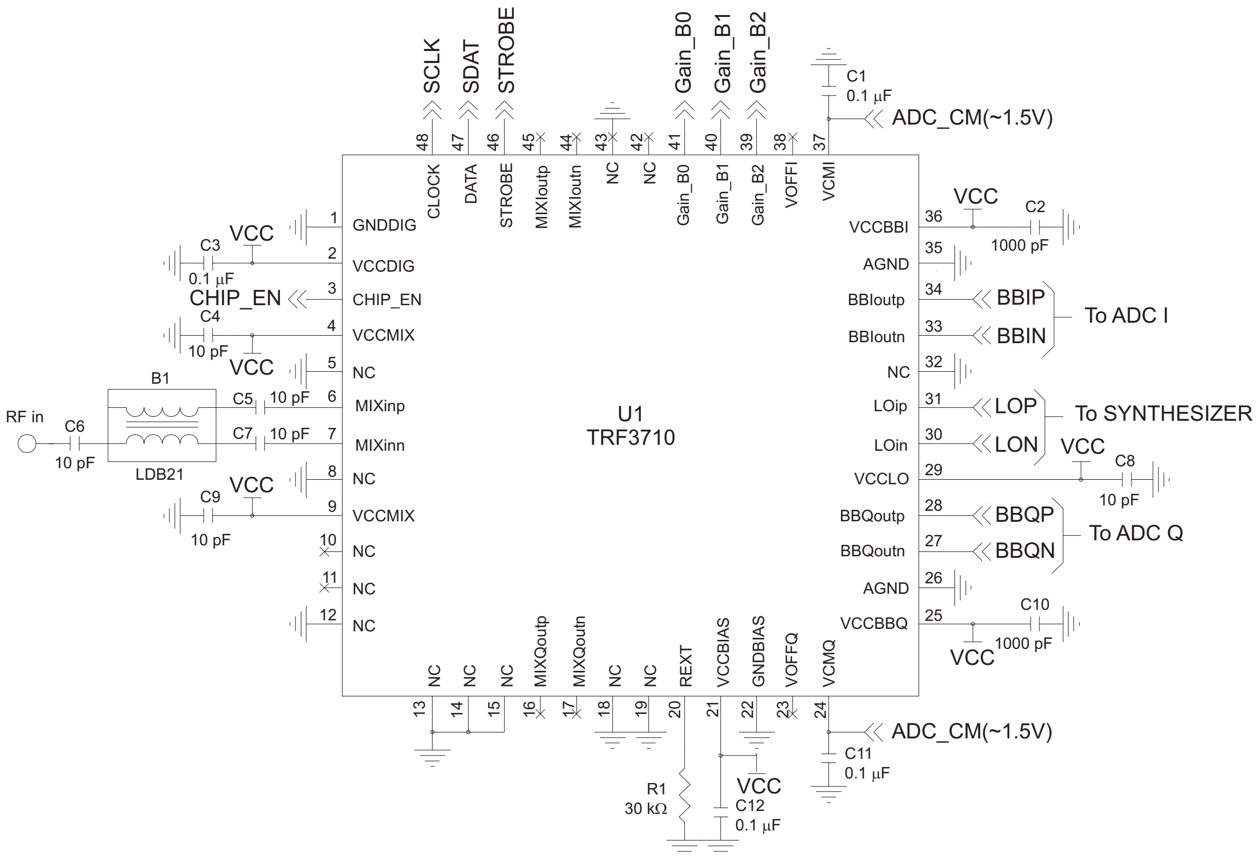


Figure 35. TRF3710 Application Schematic

The RF input port and the RF LO port require differential input paths. Single-ended RF inputs to these ports can be converted with an RF balun that is centered on the band of interest. Linearity performance of the TRF3710 depends on the amplitude and phase balance of the RF balun; therefore, care should be taken with the selection of the balun device and with the RF layout of the device. The recommended RF balun devices are listed in Table 6.

Table 6. Recommended RF Balun Devices

MANUFACTURER	PART NUMBER	FREQUENCY RANGE (MHz)	UNBALANCE IMPEDANCE	BALANCE IMPEDANCE
Murata	LDB211G8005C-001	1800 ±100 MHz	50 Ω	50 Ω
Murata	LDB211G9005C-001	1900 ±100 MHz	50 Ω	50 Ω

ADC INTERFACE

The TRF3710 has an integrated ADC driver buffer that allows direct connection to an analog-to-digital converter (ADC) without additional active circuitry. The common-mode voltage generated by the ADC can be directly supplied to the TRF3710 through the VCMI/Q pins (pins 24, 37). Otherwise, a nominal common-mode voltage of 1.5 V should be applied to those pins. The TRF3710 device can operate with a common-mode voltage from 1.5 V to 2.8 V without any impairment to the output performance. Figure 36 illustrates the degradation of the output compression point as the common mode voltage exceeds those values.

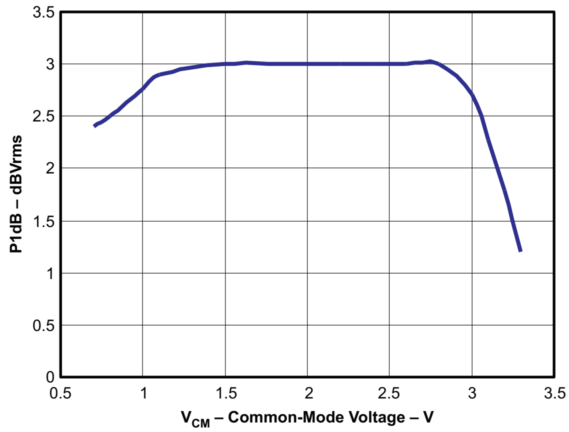


Figure 36. P1dB Performance vs Common-Mode Voltage

APPLICATION FOR A HIGH-PERFORMANCE RF RECEIVER SIGNAL CHAIN

The TRF3710 is the centerpiece component in a high-performance direct downconverting receiver. The device is a highly integrated direct downconverting demodulator that requires minimal additional devices to complete the signal chain. A signal chain block diagram example is shown in Figure 37.

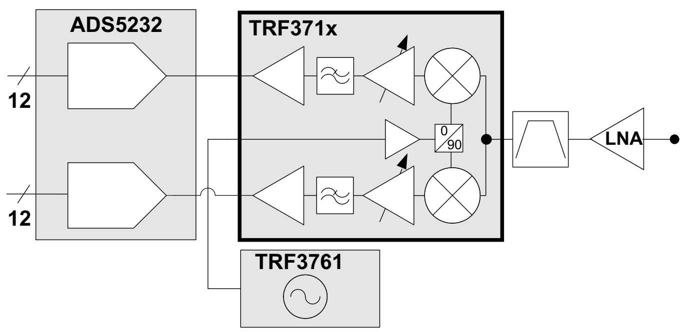


Figure 37. Block Diagram of Direct Downconverting Receiver

The lineup requires a low-noise amplifier (LNA) that operates at the frequency of interest with typical 1-db to 2-dB noise-figure (NF) performance. An RF band-pass filter (BPF) is selected at the frequency band of interest to eliminate unwanted signals and images outside the band from reaching the demodulator. The TRF3710 incorporates the direct downconverter demodulation, baseband filtering, and baseband gain control functions. An external synthesizer, such as the TRF3761, provides the local oscillator (LO) source to the TRF3710. The differential outputs of the TRF3761 directly mate with the LO inputs of the TRF3710. The quadrature outputs (I/Q) of the TRF3710 directly drive the input to the ADC. A dual ADC such as the ADS5232 12-bit, 65-MSPS ADC mates perfectly with the differential I/Q output of the TRF3710. In addition, the common-mode output voltage generated by the ADS5232 is fed directly into the common-mode ports (pins 24, 37) to ensure the optimum dynamic range of the ADC is maintained.

The cascaded performance of the TRF3710 with the ADS5232 and the TRF3761 was measured with WCDMA modulated signals. A single channel WCDMA receive signal was injected into the TRF3710 at –100 dBm. This power roughly corresponds to typical levels this device would see at sensitivity when an appropriate LNA and filter are used. The error-vector magnitude (EVM) of the RX channel was measured as a gauge of the system performance. The EVM percentage at –100 dBm is approximately 27.6% at 60 ksym/s. This result correlates with the required signal-to-noise ratio (SNR) for the device with an appropriate LNA to meet or exceed the bit error rate (BER) specification of 0.1% according to the standards at the input sensitivity level.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TRF3710IRGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TRF 3710	Samples
TRF3710IRGZRG4	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TRF 3710	Samples
TRF3710IRGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TRF 3710	Samples
TRF3710IRGZTG4	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TRF 3710	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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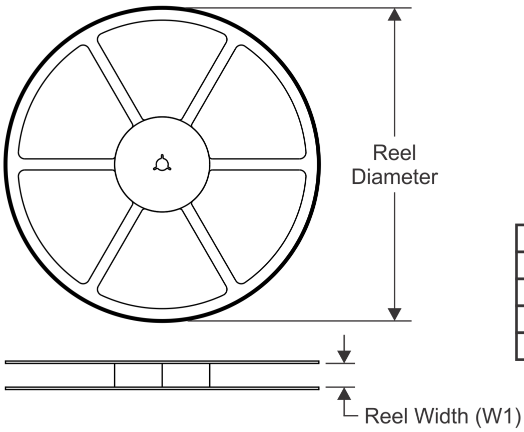
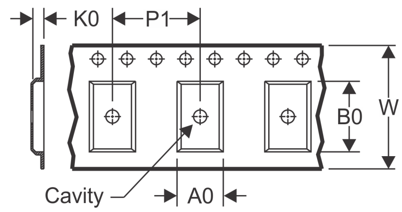
TAPE AND REEL INFORMATION

REEL DIMENSIONS

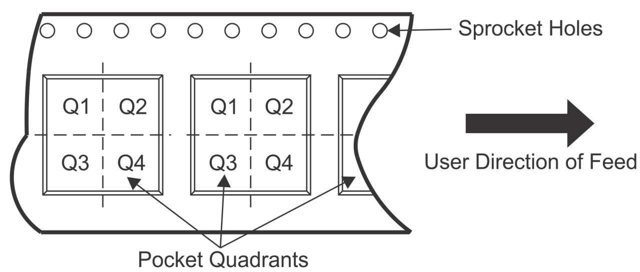


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

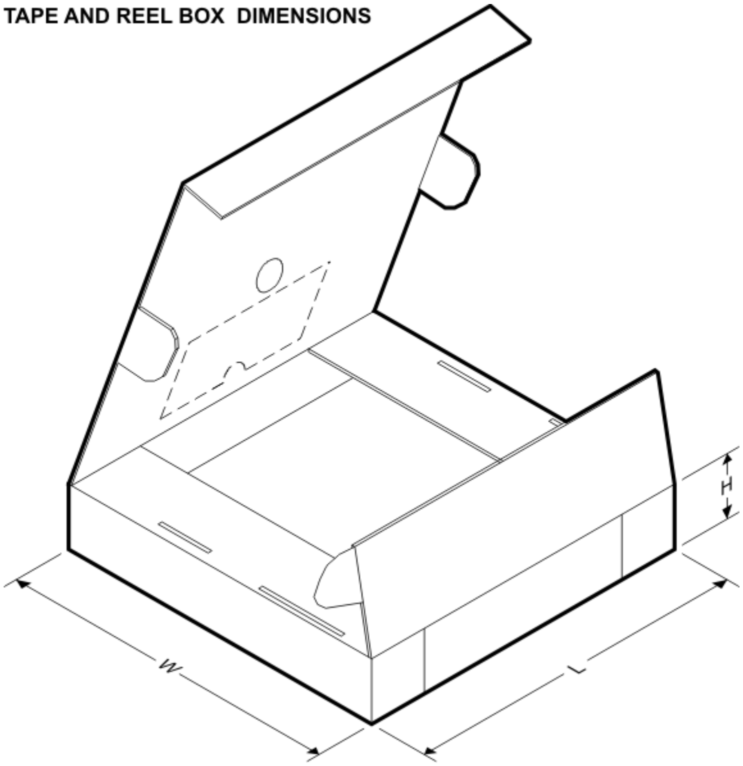
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRF3710IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
TRF3710IRGZT	VQFN	RGZ	48	250	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2

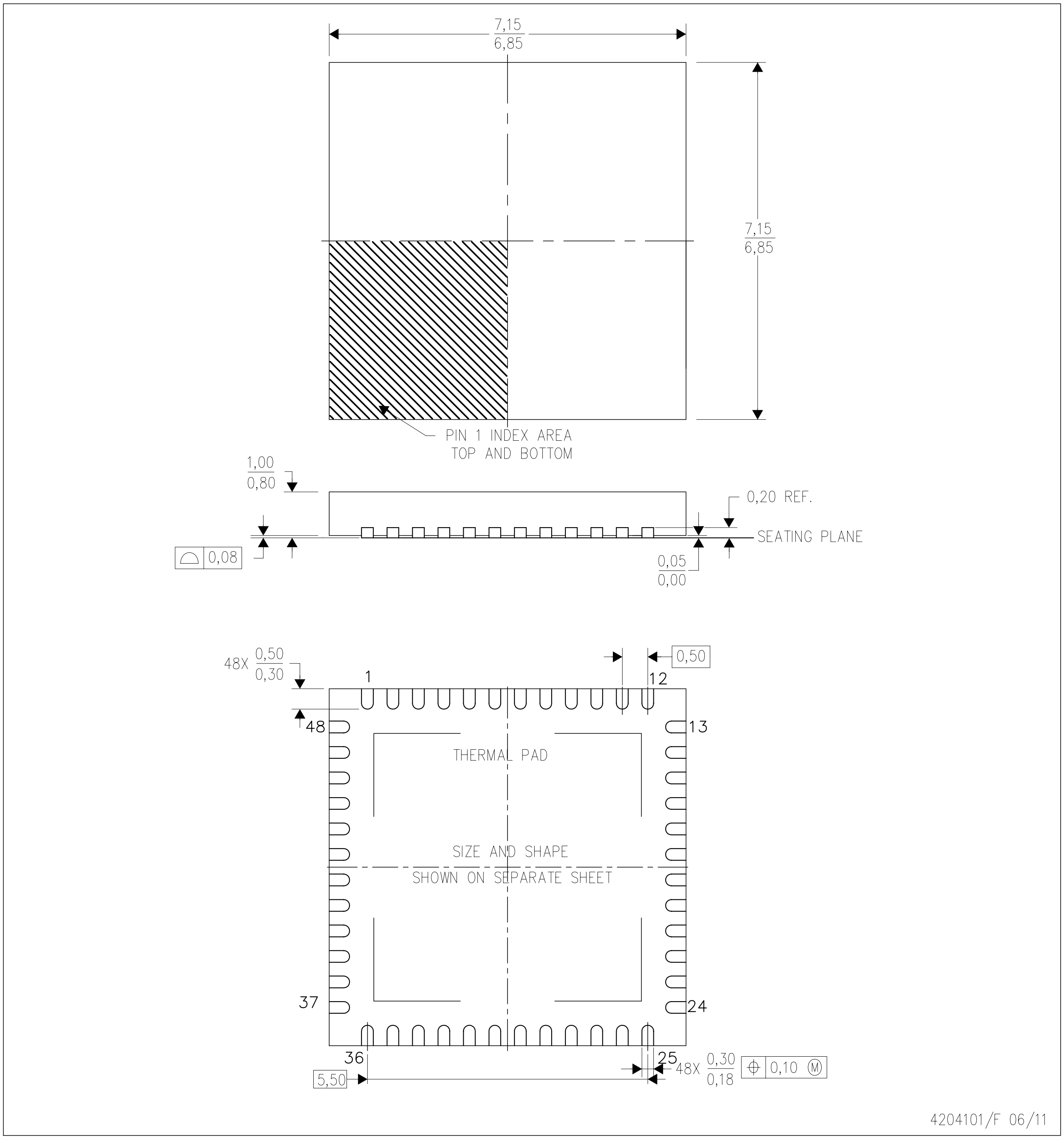
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRF3710IRGZR	VQFN	RGZ	48	2500	336.6	336.6	28.6
TRF3710IRGZT	VQFN	RGZ	48	250	336.6	336.6	28.6

RGZ (S-PVQFN-N48) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- B. This drawing is subject to change without notice.
- C. Quad Flatpack, No-leads (QFN) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Falls within JEDEC MO-220.

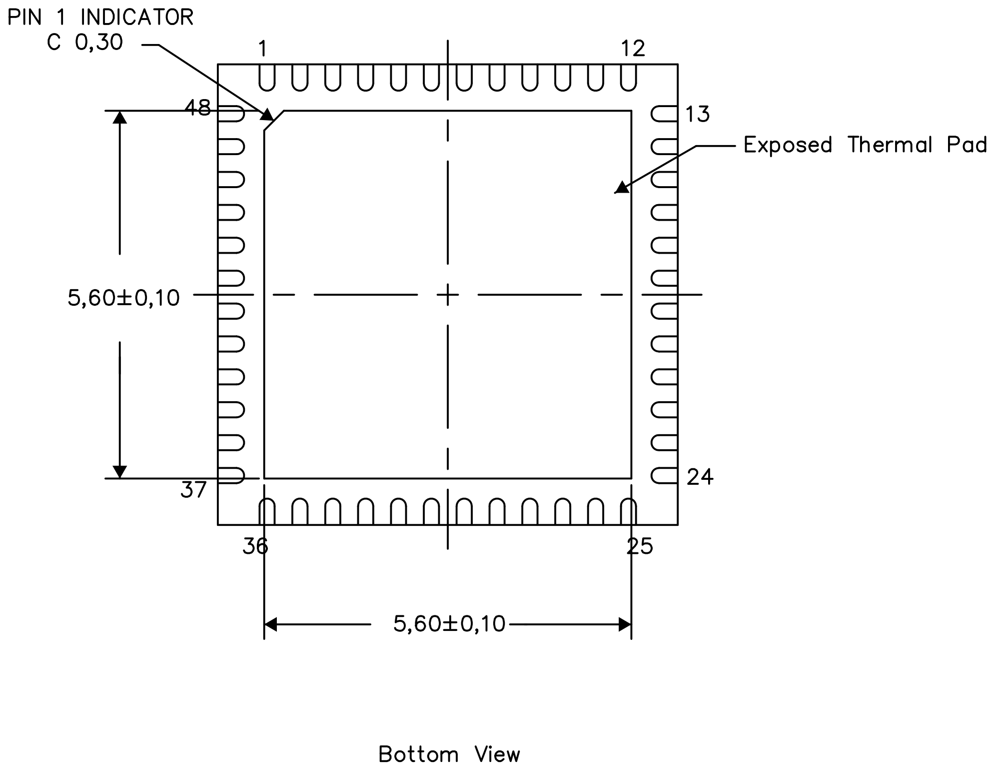
RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

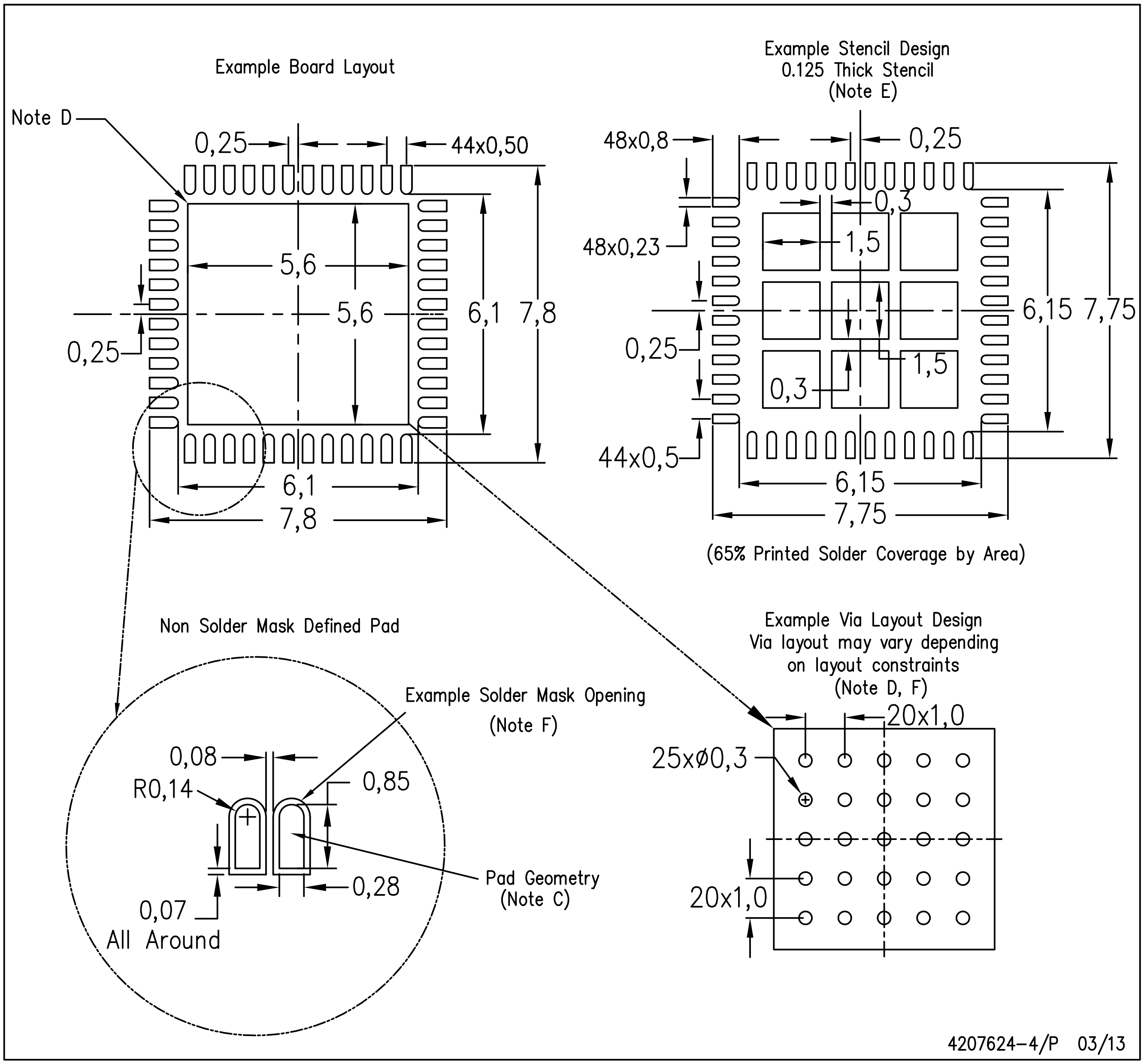


Exposed Thermal Pad Dimensions

4206354-5/T 03/13

NOTE: All linear dimensions are in millimeters

RGZ (S-PVQFN-N48) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:

A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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