TM2EJ64DPN, TM2FJ64DPN 2097152 BY 64-BIT
TM2EJ64EPN, TM2FJ64EPN 2097152 BY 64-BIT
EXTENDED-DATA-OUT DYNAMIC RAM MODULES — SODIMM

SMMS685 − AUGUST 1997

- **Organization**
  - **TM2xJ64xPN-xx . . . 2097152 × 64 Bits**
- **Single 3.3-V Power Supply (±10% Tolerance)**
- **JEDEC 144-Pin Small Outline Dual-In-Line Memory Module (SODIMM) Without Buffer for Use With Socket**
- **TM2xJ64xPN-xx — Utilizes Eight 16M-Bit (2M×8-Bit) Dynamic RAMs in TSOPs**
- **Performance ranges**

	ACCESS TIME t_{RAC} MAX	ACCESS TIME t_{CAC} MAX	ACCESS TIME t_{AA} MAX	EDO CYCLE t_{HPC} MIN
'2xJ64xPN-50	50 ns	13 ns	25 ns	20 ns
'2xJ64xPN-60	60 ns	15 ns	30 ns	25 ns
'2xJ64xPN-70	70 ns	18 ns	35 ns	30 ns

- **High-Speed, Low-Noise LVTTL Interface**
- **Long Refresh Period:**
  - **TM2EJ64DPN: 32 ms (2048 cycles)**
  - **TM2EJ64EPN: 64 ms (4096 cycles)**
- **Low-Power, Battery-Backup Refresh Available:**
  - **TM2FJ64DPN: 128 ms (2048 cycles)**
  - **TM2FJ64EPN: 128 ms (4096 cycles)**
- **3-State Output**
- **Extended-Data-Out (EDO) Operation With $\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ (CBR), $\overline{\text{RAS}}$-Only, and Hidden Refresh**
- **Serial Presence-Detect (SPD) Using EEPROM**
- **Ambient Temperature Range 0°C to 70°C**
- **Gold-Plated Contacts**

description

The TM2EJ64DPN is a 16M-byte, 144-pin, small outline dual-in-line memory module (SODIMM). The SODIMM is composed of eight TMS427809A, 2097152 × 8-bit 2K-refresh EDO dynamic random-access memories (DRAMs), each in a 400-mil, 28-pin plastic thin small-outline package (TSOP) (DGC suffix) mounted on a substrate with decoupling capacitors. See the TMS427809A data sheet (literature number SMKS894).

The TM2EJ64EPN is an 16M-byte, 144-pin SODIMM. The SODIMM is composed of eight TMS426809A, 2097152 × 8-bit 4K-refresh EDO DRAMs, each in a 400-mil, 28-pin plastic TSOP (DGC suffix) mounted on a substrate with decoupling capacitors. See the TMS426809A data sheet (literature number SMKS894).

The TM2FJ64DPN is a 16M-byte, 144-pin SODIMM. The SODIMM is composed of eight TMS427809AP, 2097152 × 8-bit 2K low-power battery-backup refresh EDO DRAMs, each in a 400-mil, 28-pin plastic TSOP (DGC suffix) mounted on a substrate with decoupling capacitors. See the TMS427809AP data sheet (literature number SMKS894).

The TM2FJ64EPN is a 16M-byte, 144-pin SODIMM. The SODIMM is composed of eight TMS426809AP, 2097152 × 8-bit 4K low-power battery-backup refresh EDO DRAMs, each in a 400-mil, 28-pin plastic TSOP (DGC suffix) mounted on a substrate with decoupling capacitors. See the TMS426809AP data sheet (literature number SMKS894).

operation

The TM2xJ64xPN operates as eight TMS42x809A/Ps, connected as shown in the functional block diagram.

PRODUCT PREVIEW

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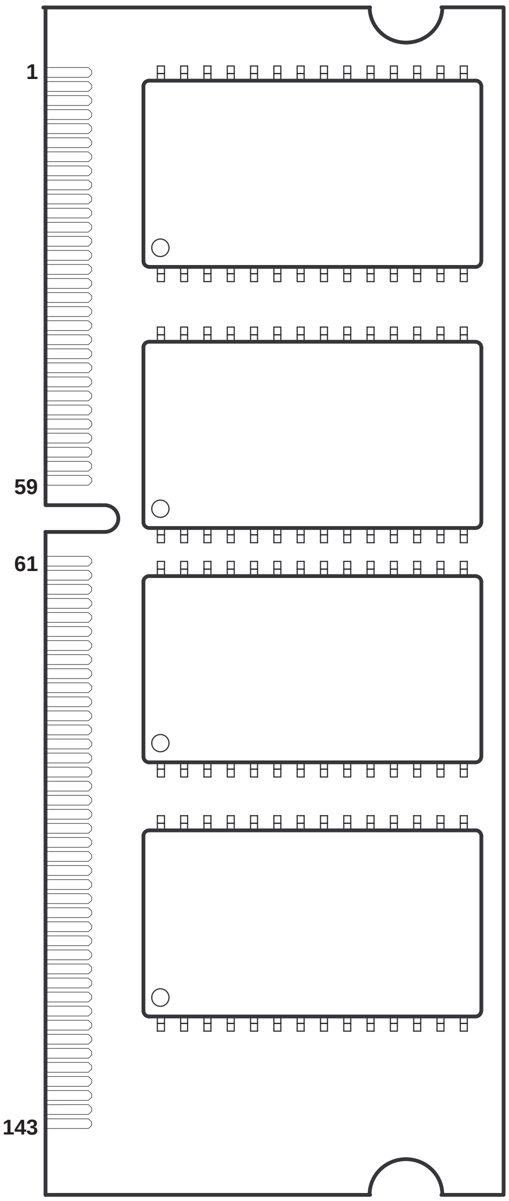
TEXAS INSTRUMENTS

PRODUCT PREVIEW

DUAL-IN-LINE MEMORY MODULE
(TOP VIEW)



TM2xJ64xPN
(SIDE VIEW)

PIN NOMENCLATURE

A[0:11][†]	Row Address Inputs
A[0:9]	Column Address Inputs
DQ[0:63]	Data In / Data Out
$\overline{\text{CAS}}$[0:7]	Column-Address Strobe
$\overline{\text{RAS0}}$	Row-Address Strobe
$\overline{\text{WE0}}$	Write Enable
$\overline{\text{OE0}}$	Output Enable
SDA	Serial PD Address / Data
SCL	Serial PD Clock
NC	No-Connect Pin
V_{DD}	3.3-V Supply
V_{SS}	Ground

[†] A11 is NC for TM2xJ64DPN

Pin Assignments

PIN		PIN		PIN		PIN	
NO.	**NAME**	**NO.**	**NAME**	**NO.**	**NAME**	**NO.**	**NAME**
1	V_{SS}	37	DQ8	73	$\overline{\mathrm{OE}}$	109	A9
2	V_{SS}	38	DQ40	74	NC	110	NC
3	DQ0	39	DQ9	75	V_{SS}	111	A10
4	DQ32	40	DQ41	76	V_{SS}	112	NC
5	DQ1	41	DQ10	77	NC	113	V_{DD}
6	DQ33	42	DQ42	78	NC	114	V_{DD}
7	DQ2	43	DQ11	79	NC	115	$\overline{\mathrm{CAS2}}$
8	DQ34	44	DQ43	80	NC	116	$\overline{\mathrm{CAS6}}$
9	DQ3	45	V_{DD}	81	V_{DD}	117	$\overline{\mathrm{CAS3}}$
10	DQ35	46	V_{DD}	82	V_{DD}	118	$\overline{\mathrm{CAS7}}$
11	V_{DD}	47	DQ12	83	DQ16	119	V_{SS}
12	V_{DD}	48	DQ44	84	DQ48	120	V_{SS}
13	DQ4	49	DQ13	85	DQ17	121	DQ24
14	DQ36	50	DQ45	86	DQ49	122	DQ56
15	DQ5	51	DQ14	87	DQ18	123	DQ25
16	DQ37	52	DQ46	88	DQ50	124	DQ57
17	DQ6	53	DQ15	89	DQ19	125	DQ26
18	DQ38	54	DQ47	90	DQ51	126	DQ58
19	DQ7	55	V_{SS}	91	V_{SS}	127	DQ27
20	DQ39	56	V_{SS}	92	V_{SS}	128	DQ59
21	V_{SS}	57	NC	93	DQ20	129	V_{DD}
22	V_{SS}	58	NC	94	DQ52	130	V_{DD}
23	$\overline{\mathrm{CAS0}}$	59	NC	95	DQ21	131	DQ28
24	$\overline{\mathrm{CAS4}}$	60	NC	96	DQ53	132	DQ60
25	$\overline{\mathrm{CAS1}}$	61	NC	97	DQ22	133	DQ29
26	$\overline{\mathrm{CAS5}}$	62	NC	98	DQ54	134	DQ61
27	V_{DD}	63	V_{DD}	99	DQ23	135	DQ30
28	V_{DD}	64	V_{DD}	100	DQ55	136	DQ62
29	A0	65	NC	101	V_{DD}	137	DQ31
30	A3	66	NC	102	V_{DD}	138	DQ63
31	A1	67	$\overline{\mathrm{WE0}}$	103	A6	139	V_{SS}
32	A4	68	NC	104	A7	140	V_{SS}
33	A2	69	$\overline{\mathrm{RAS0}}$	105	A8	141	SDA
34	A5	70	NC	106	A11	142	SCL
35	V_{SS}	71	NC	107	V_{SS}	143	V_{DD}
36	V_{SS}	72	NC	108	V_{SS}	144	V_{DD}

PRODUCT PREVIEW

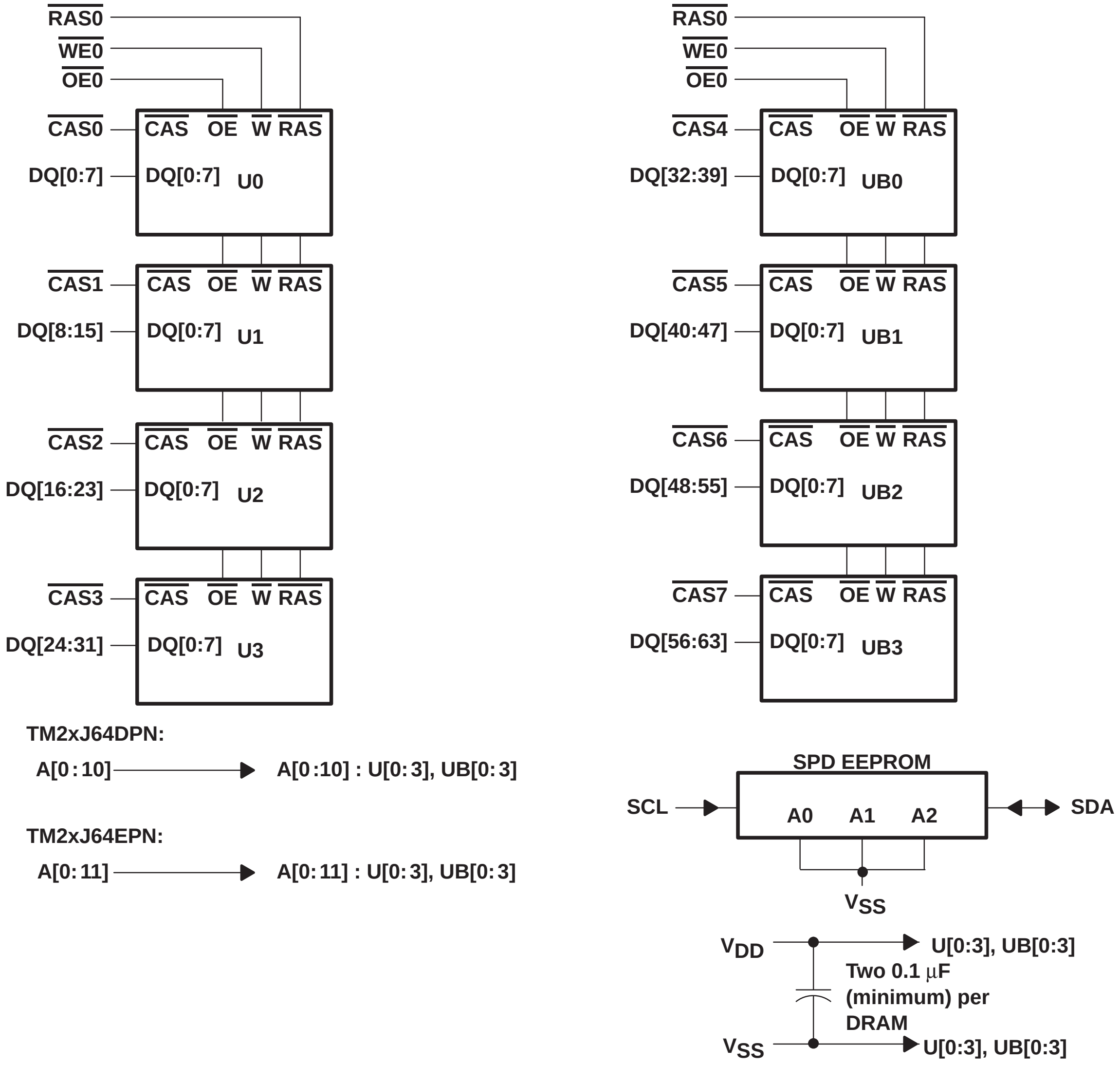
PRODUCT PREVIEW

small outline dual-in-line memory module and components

The small−outline dual-in-line memory module and components include:

- PC substrate: 1,10 ± 0,1 mm (0.04 inch) nominal thickness
- Bypass capacitors: Multilayer ceramic
- Contact area: Nickel plate and gold plate over copper

functional block diagram for the TM2xJ64xPN


RAS0
WE0
OE0
CAS0
DQ[0:7]
CAS OE W RAS
DQ[0:7] U0
CAS1
DQ[8:15]
CAS OE W RAS
DQ[0:7] U1
CAS2
DQ[16:23]
CAS OE W RAS
DQ[0:7] U2
CAS3
DQ[24:31]
CAS OE W RAS
DQ[0:7] U3
RAS0
WE0
OE0
CAS4
DQ[32:39]
CAS OE W RAS
DQ[0:7] UB0
CAS5
DQ[40:47]
CAS OE W RAS
DQ[0:7] UB1
CAS6
DQ[48:55]
CAS OE W RAS
DQ[0:7] UB2
CAS7
DQ[56:63]
CAS OE W RAS
DQ[0:7] UB3
TM2xJ64DPN:
A[0:10]
A[0:10] : U[0:3], UB[0:3]
TM2xJ64EPN:
A[0:11]
A[0:11] : U[0:3], UB[0:3]
SPD EEPROM
SCL
A0 A1 A2
SDA
VSS
VDD
U[0:3], UB[0:3]
Two 0.1 µF (minimum) per DRAM
VSS
U[0:3], UB[0:3]

absolute maximum ratings over ambient temperature range (unless otherwise noted)†

Supply voltage range, V_{DD}	−0.5 V to 4.6 V
Voltage range on any pin (see Note 1)	− 0.5 V to 4.6 V
Short-circuit output current	50 mA
Power dissipation: TM2xP64DPN	8 W
TM2xP64EPN	8 W
Ambient temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	− 55°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	3	3.3	3.6	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2		V_{DD} + 0.3	V
$V_{IH\text{-}SPD}$	High-level input voltage for the SPD device	2		5.5	V
V_{IL}	Low-level input voltage	−0.3		0.8	V
T_A	Ambient temperature	0		70	°C

capacitance over recommended ranges of supply voltage and ambient temperature, f = 1 MHz (see Note 2)

PARAMETER		’2xJ64xPN		UNIT
		MIN	MAX	
$C_{i(A)}$	Input capacitance, A0−A10		42	pF
$C_{i(OE)}$	Input capacitance, $\overline{\text{OE0}}$		58	pF
$C_{i(CAS)}$	Input capacitance, $\overline{\text{CASx}}$		9	pF
$C_{i(RAS)}$	Input capacitance, $\overline{\text{RAS0}}$		58	pF
$C_{i(W)}$	Input capacitance, $\overline{\text{WE0}}$		58	pF
C_o	Output capacitance		9	pF
$C_{i/o(SDA)}$	Input/output capacitance, SDA input		9	pF
$C_{i(SPD)}$	Input capacitance, SA0, SA1, SA2, SCL inputs		7	pF

NOTE 2: V_{DD} = NOM supply voltage ±10%, and the bias on pins under test is 0 V.

PRODUCT PREVIEW

electrical characteristics over recommended ranges of supply voltage and ambient temperature (unless otherwise noted)

TM2EJ64DPN

PARAMETER		TEST CONDITIONS†		’2EJ64DPN-50		’2EJ64DPN-60		’2EJ64DPN-70		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = − 2 mA	LVTTL	2.4		2.4		2.4		V
		I_{OH} = − 100 µA	LVCMOS	V_{DD} − 0.2		V_{DD} − 0.2		V_{DD} − 0.2		
V_{OL}	Low-level output voltage	I_{OL} = 2 mA	LVTTL		0.4		0.4		0.4	V
		I_{OL} = 100 µA	LVCMOS		0.2		0.2		0.2	
I_I	Input current (leakage)	V_{DD} = 3.6 V, V_I = 0 V to 3.9 V, All others = 0 V to V_{DD}			± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{DD} = 3.6 V, V_O = 0 V to V_{DD}, $\overline{\text{CASx}}$ high			± 10		± 10		± 10	µA
I_{CC1}‡§	Read- or write-cycle current	V_{DD} = 3.6 V, Minimum cycle			960		800		720	mA
I_{CC2}	Standby current	V_{IH} = 2 V (LVTTL), After one memory cycle, $\overline{\text{RAS0}}$ and $\overline{\text{CASx}}$ high			16		16		16	mA
		V_{IH} = V_{DD} − 0.2 V (LVCMOS), After one memory cycle, $\overline{\text{RAS0}}$ and $\overline{\text{CASx}}$ high			8		8		8	mA
I_{CC3}‡§	Average refresh current ($\overline{\text{RAS}}$-only refresh or CBR)	V_{DD}= 3.6 V, Minimum cycle, $\overline{\text{RAS0}}$ cycling, $\overline{\text{CASx}}$ high ($\overline{\text{RAS}}$-only refresh), $\overline{\text{RAS0}}$ low after $\overline{\text{CASx}}$ low (CBR)			960		800		720	mA
I_{CC4}‡¶	Average EDO current	V_{DD} = 3.6 V, t_{HPC} = MIN, $\overline{\text{RAS0}}$ low, $\overline{\text{CASx}}$ cycling			880		720		640	mA

† For conditions shown as MIN / MAX, use the appropriate value specified in the timing requirements.
‡ Measured with outputs open
§ Measured with a maximum of one address change while $\overline{\text{RAS0}}$ = V_{IL}
¶ Measured with a maximum of one address change during each EDO cycle, t_{HPC}

PRODUCT PREVIEW

electrical characteristics over recommended ranges of supply voltage and ambient temperature (unless otherwise noted)

TM2EJ64EPN

PARAMETER		TEST CONDITIONS[†]		’2EJ64EPN-50		’2EJ64EPN-60		’2EJ64EPN-70		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = − 2 mA	LVTTL	2.4		2.4		2.4		V
		I_{OH} = − 100 µA	LVCMOS	V_{DD} − 0.2		V_{DD} − 0.2		V_{DD} − 0.2		
V_{OL}	Low-level output voltage	I_{OL} = 2 mA	LVTTL		0.4		0.4		0.4	V
		I_{OL} = 100 µA	LVCMOS		0.2		0.2		0.2	
I_I	Input current (leakage)	V_{DD} = 3.6 V, All others = 0 V to V_{DD}	V_I = 0 V to 3.9 V,		± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{DD} = 3.6 V, $\overline{\text{CASx}}$ high	V_O = 0 V to V_{DD},		± 10		± 10		± 10	µA
I_{CC1}[‡§]	Read- or write-cycle current	V_{DD} = 3.6 V,	Minimum cycle		720		560		480	mA
I_{CC2}	Standby current	V_{IH} = 2 V (LVTTL), After one memory cycle, $\overline{\text{RAS0}}$ and $\overline{\text{CASx}}$ high			16		16		16	mA
		V_{IH} = V_{DD} − 0.2 V (LVCMOS), After one memory cycle, $\overline{\text{RAS0}}$ and $\overline{\text{CASx}}$ high			8		8		8	mA
I_{CC3}[‡§]	Average refresh current ($\overline{\text{RAS}}$-only refresh or CBR)	V_{DD} = 3.6 V, $\overline{\text{RASx}}$ cycling, $\overline{\text{CASx}}$ high ($\overline{\text{RAS}}$-only refresh), $\overline{\text{RAS0}}$ low after $\overline{\text{CASx}}$ low (CBR)	Minimum cycle,		720		560		480	mA
I_{CC4}[‡¶]	Average EDO current	V_{DD} = 3.6 V, $\overline{\text{RAS0}}$ low,	t_{HPC} = MIN, $\overline{\text{CASx}}$ cycling		800		720		640	mA

[†] For conditions shown as MIN / MAX, use the appropriate value specified in the timing requirements.
[‡] Measured with outputs open
[§] Measured with a maximum of one address change while $\overline{\text{RAS0}}$ = V_{IL}
[¶] Measured with a maximum of one address change during each EDO cycle, t_{HPC}

PRODUCT PREVIEW

PRODUCT PREVIEW

electrical characteristics over recommended ranges of supply voltage and ambient temperture (unless otherwise noted) (continued)

TM2FJ64DPN

PARAMETER		TEST CONDITIONS†		’2FJ64DPN-50		’2FJ64DPN-60		’2FJ64DPN-70		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = − 2 mA	LVTTL	2.4		2.4		2.4		V
		I_{OH} = − 100 µA	LVCMOS	V_{DD} − 0.2		V_{DD} − 0.2		V_{DD} − 0.2		
V_{OL}	Low-level output voltage	I_{OL} = 2 mA	LVTTL		0.4		0.4		0.4	V
		I_{OL} = 100 µA	LVCMOS		0.2		0.2		0.2	
I_I	Input current (leakage)	V_{DD} = 3.6 V, V_I = 0 V to 3.9 V, All others = 0 V to V_{DD}			± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{DD} = 3.6 V, V_O = 0 V to V_{DD}, $\overline{\text{CASx}}$ high			± 10		± 10		± 10	µA
I_{CC1}‡§	Read- or write-cycle current	V_{DD} = 3.6 V, Minimum cycle			960		800		720	mA
I_{CC2}	Standby current	V_{IH} = 2 V (LVTTL), After one memory cycle, $\overline{\text{RAS0}}$ and $\overline{\text{CASx}}$ high			8		8		8	mA
		V_{IH} = V_{DD} − 0.2 V (LVCMOS), After one memory cycle, $\overline{\text{RAS0}}$ and $\overline{\text{CASx}}$ high			1.2		1.2		1.2	mA
I_{CC3}‡§	Average refresh current ($\overline{\text{RAS}}$-only refresh or CBR)	V_{DD}= 3.6 V, Minimum cycle, $\overline{\text{RAS0}}$ cycling, $\overline{\text{CASx}}$ high ($\overline{\text{RAS}}$-only refresh), $\overline{\text{RAS0}}$ low after $\overline{\text{CASx}}$ low (CBR)			960		800		720	mA
I_{CC4}‡¶	Average EDO current	V_{DD} = 3.6 V, t_{HPC} = MIN, $\overline{\text{RAS0}}$ low, $\overline{\text{CASx}}$ cycling			880		720		640	mA
I_{CC6}	Average self-refresh current	$\overline{\text{CASx}}$ < 0.2 V, $\overline{\text{RAS0}}$ < 0.2 V, Measured after t_{RASS} min			1.6		1.6		1.6	mA
I_{CC10}	Average battery back-up operating current (equivalent refresh time is 128 ms), CBR only	t_{RC} = 31.25 µs, $t_{RAS} \leq$ 300 ns, $V_{DD} - 0.2\ V \leq V_{IH} \leq 3.9\ V$, $0\ V \leq V_{IL} \leq 0.2\ V$, $\overline{\text{WE0}}$ and $\overline{\text{OE0}}$ = V_{IH}, Address and data stable			2.8		2.8		2.8	mA

† For conditions shown as MIN / MAX, use the appropriate value specified in the timing requirements.
‡ Measured with outputs open
§ Measured with a maximum of one address change while $\overline{\text{RAS0}}$ = V_{IL}
¶ Measured with a maximum of one address change during each EDO cycle, t_{HPC}

electrical characteristics over recommended ranges of supply voltage and ambient temperature (unless otherwise noted) (continued)

TM2FJ64EPN

PARAMETER		TEST CONDITIONS†		’2FJ64EPN-50		’2FJ64EPN-60		’2FJ64EPN-70		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	$I_{OH} = -2$ mA	LVTTL	2.4		2.4		2.4		V
		$I_{OH} = -100$ µA	LVCMOS	$V_{DD} - 0.2$		$V_{DD} - 0.2$		$V_{DD} - 0.2$		
V_{OL}	Low-level output voltage	$I_{OL} = 2$ mA	LVTTL		0.4		0.4		0.4	V
		$I_{OL} = 100$ µA	LVCMOS		0.2		0.2		0.2	
I_I	Input current (leakage)	$V_{DD} = 3.6$ V, $V_I = 0$ V to 3.9 V, All others = 0 V to V_{DD}			± 10		± 10		± 10	µA
I_O	Output current (leakage)	$V_{DD} = 3.6$ V, $V_O = 0$ V to V_{DD}, $\overline{\text{CASx}}$ high			± 10		± 10		± 10	µA
I_{CC1}‡§	Read- or write-cycle current	$V_{DD} = 3.6$ V, Minimum cycle			720		560		480	mA
I_{CC2}	Standby current	$V_{IH} = 2$ V (LVTTL), After one memory cycle, $\overline{\text{RAS0}}$ and $\overline{\text{CASx}}$ high			8		8		8	mA
		$V_{IH} = V_{DD} - 0.2$ V (LVCMOS), After one memory cycle, $\overline{\text{RAS0}}$ and $\overline{\text{CASx}}$ high			1.2		1.2		1.2	mA
I_{CC3}‡§	Average refresh current ($\overline{\text{RAS}}$-only refresh or CBR)	$V_{DD} = 3.6$ V, Minimum cycle, $\overline{\text{RAS0}}$ cycling, $\overline{\text{CASx}}$ high ($\overline{\text{RAS}}$-only refresh), $\overline{\text{RAS0}}$ low after $\overline{\text{CASx}}$ low (CBR)			720		560		480	mA
I_{CC4}‡¶	Average EDO current	$V_{DD} = 3.6$ V, t_{HPC} = MIN, $\overline{\text{RAS0}}$ low, $\overline{\text{CASx}}$ cycling			800		720		640	mA
I_{CC6}	Average self-refresh current	$\overline{\text{CASx}} < 0.2$ V, $\overline{\text{RAS0}} < 0.2$ V, Measured after t_{RASS} min			2		2		2	mA
I_{CC10}	Average battery back-up operating current (equivalent refresh time is 128 ms), CBR only	$t_{RC} = 31.25$ µs, $t_{RAS} \le 300$ ns, $V_{DD} - 0.2\text{ V} \le V_{IH} \le 3.9$ V, $0\text{ V} \le V_{IL} \le 0.2$ V, $\overline{\text{WE0}}$ and $\overline{\text{OE0}}$ = V_{IH}, Address and data stable			2.8		2.8		2.8	mA

† For conditions shown as MIN / MAX, use the appropriate value specified in the timing requirements.
‡ Measured with outputs open
§ Measured with a maximum of one address change while $\overline{\text{RAS0}} = V_{IL}$
¶ Measured with a maximum of one address change during each EDO cycle, t_{HPC}

PRODUCT PREVIEW

PRODUCT PREVIEW

switching characteristics over recommended ranges of supply voltage and ambient temperature (see Note 3)

PARAMETER		’2XJ64xPN-50		’2XJ64xPN-60		’2XJ64xPN-70		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column address (see Note 4)		25		30		35	ns
t_{CAC}	Access time from $\overline{\text{CAS}}$x (see Note 4)		13		15		18	ns
t_{CPA}	Access time from $\overline{\text{CAS}}$x precharge (see Note 4)		28		35		40	ns
t_{RAC}	Access time from $\overline{\text{RAS0}}$ (see Note 4)		50		60		70	ns
t_{OEA}	Access time from $\overline{\text{OE0}}$ (see Note 4)		13		15		18	ns
t_{CLZ}	Delay time, $\overline{\text{CAS}}$x to output in low impedance	0		0		0		ns
t_{REZ}	Output buffer turn off delay from $\overline{\text{RAS0}}$ (see Note 5)	3	13	3	15	3	18	ns
t_{CEZ}	Output buffer turn off delay from $\overline{\text{CAS}}$x (see Note 5)	3	13	3	15	3	18	ns
t_{OEZ}	Output buffer turn off delay from $\overline{\text{OE0}}$ (see Note 5)	3	13	3	15	3	18	ns
t_{WEZ}	Output buffer turn off delay from $\overline{\text{WE0}}$ (see Note 5)	3	13	3	15	3	18	ns

NOTES: 3. With ac parameters, it is assumed that t_T = 2 ns.
4. Access times are measured with output reference levels of V_{OH} = 2 V and V_{OL} = 0.8 V.
5. The maximum values of t_{REZ}, t_{CEZ}, t_{OEZ}, and t_{WEZ} are specified when the outputs are no longer driven. Data-in should not be driven until one of the applicable maximum values is satisfied.

EDO timing requirements (see Note 3)

		’2XJ64xPN-50		’2XJ64xPN-60		’2XJ64xPN-70		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{HPC}	Cycle time, EDO page mode, read-write	20		25		30		ns
t_{PRWC}	Cycle time, EDO read-write	57		68		78		ns
t_{CSH}	Delay time, $\overline{\text{RAS0}}$ active to $\overline{\text{CAS}}$x precharge	40		48		58		ns
t_{CHO}	Hold time, $\overline{\text{OE0}}$ from $\overline{\text{CAS}}$x	7		10		10		ns
t_{DOH}	Hold time, output from $\overline{\text{CAS}}$x	5		5		5		ns
t_{CAS}	Pulse duration, $\overline{\text{CAS}}$x active	8	10 000	10	10 000	12	10 000	ns
t_{WPE}	Pulse duration, $\overline{\text{WE0}}$ active (output disable only)	7		7		7		ns
t_{CP}	Pulse duration, $\overline{\text{CAS}}$x precharge	8		10		10		ns
t_{OCH}	Setup time, $\overline{\text{OE0}}$ before $\overline{\text{CAS}}$x	8		10		10		ns
t_{OEP}	Precharge time, $\overline{\text{OE0}}$	5		5		5		ns

NOTE 3: With ac parameters, it is assumed that t_T = 2 ns.

ac timing requirements (see Note 3)

		’2xJ64xPN-50		’2xJ64xPN-60		’2xJ64xPN-70		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Cycle time, random read or write	84		104		124		ns
t_{RWC}	Cycle time, read-write	111		135		160		ns
t_{RASP}	Pulse duration, $\overline{\text{RAS0}}$ active, fast page mode (see Note 6)	50	100 000	60	100 000	70	100 000	ns
t_{RAS}	Pulse duration, $\overline{\text{RAS0}}$ active, non-page mode (see Note 6)	50	10 000	60	10 000	70	10 000	ns
t_{RP}	Pulse duration, $\overline{\text{RAS0}}$ precharge	30		40		50		ns
t_{WP}	Pulse duration, write command	8		10		10		ns
t_{RASS}	Pulse duration, $\overline{\text{RAS0}}$ active, self refresh (see Note 7)	100		100		100		µs
t_{RPS}	Pulse duration, $\overline{\text{RAS0}}$ precharge after self refresh	90		110		130		ns
t_{ASC}	Setup time, column address	0		0		0		ns
t_{ASR}	Setup time, row address	0		0		0		ns
t_{DS}	Setup time, data in (see Note 8)	0		0		0		ns
t_{RCS}	Setup time, read command	0		0		0		ns
t_{CWL}	Setup time, write command before $\overline{\text{CASx}}$ precharge	8		10		12		ns
t_{RWL}	Setup time, write command before $\overline{\text{RAS0}}$ precharge	8		10		12		ns
t_{WCS}	Setup time, write command before $\overline{\text{CASx}}$ active (early-write only)	0		0		0		ns
t_{WRP}	Setup time, $\overline{\text{WE0}}$ high before $\overline{\text{RAS0}}$ low (CBR refresh only)	10		10		10		ns
t_{CSR}	Setup time, $\overline{\text{CASx}}$ referenced to $\overline{\text{RAS0}}$ (CBR refresh only)	5		5		5		ns
t_{CAH}	Hold time, column address	8		10		12		ns
t_{DH}	Hold time, data in (see Note 8)	8		10		12		ns
t_{RAH}	Hold time, row address	8		10		10		ns
t_{RCH}	Hold time, read command referenced to $\overline{\text{CASx}}$ (see Note 9)	0		0		0		ns
t_{RRH}	Hold time, read command referenced to $\overline{\text{RAS0}}$ (see Note 9)	0		0		0		ns
t_{WCH}	Hold time, write command during $\overline{\text{CASx}}$ active (early-write only)	8		10		12		ns
t_{ROH}	Hold time, $\overline{\text{RAS0}}$ referenced to $\overline{\text{OE0}}$	8		10		10		ns
t_{WRH}	Hold time, $\overline{\text{WE0}}$ high after $\overline{\text{RAS0}}$ low (CBR refresh only)	10		10		10		ns
t_{CHR}	Hold time, $\overline{\text{CASx}}$ referenced to $\overline{\text{RAS0}}$ (CBR refresh only)	10		10		10		ns
t_{OEH}	Hold time, $\overline{\text{OE0}}$ command	13		15		18		ns
t_{RHCP}	Hold time, $\overline{\text{RAS0}}$ active from $\overline{\text{CASx}}$ precharge	28		35		40		ns
t_{CHS}	Hold time, $\overline{\text{CASx}}$ referenced to $\overline{\text{RAS0}}$ (self refresh only)	− 50		− 50		− 50		ns
t_{AWD}	Delay time, column address to write command (read-write only)	42		49		57		ns
t_{CRP}	Delay time, $\overline{\text{CASx}}$ precharge to $\overline{\text{RAS0}}$	5		5		5		ns

NOTES:
3. With ac parameters, it is assumed that t_T = 2 ns.
6. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
7. During the period of 10 µs ≤ t_{RASS} ≤100 µs, the device is in a transition state from normal-operation mode to self-refresh mode.
8. Referenced to the later of $\overline{\text{CASx}}$ or $\overline{\text{WE0}}$ in write operations
9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

PRODUCT PREVIEW

ac timing requirements (see Note 3) (continued)

			’2xJ64xPN-50		’2xJ64xPN-60		’2xJ64xPN-70		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{CWD}	Delay time, $\overline{\text{CASx}}$ to write command (read-write only)		0		0		0		ns
t_{OED}	Delay time, $\overline{\text{OE0}}$ to data in		0		0		0		ns
t_{RAD}	Delay time, $\overline{\text{RAS0}}$ to column address (see Note 10)		8		10		12		ns
t_{RAL}	Delay time, column address to $\overline{\text{RAS0}}$ precharge		8		10		12		ns
t_{CAL}	Delay time, column address to $\overline{\text{CASx}}$ precharge		0		0		0		ns
t_{RCD}	Delay time, $\overline{\text{RAS0}}$ to $\overline{\text{CASx}}$ (see Note 10)		5		5		5		ns
t_{RPC}	Delay time, $\overline{\text{RAS0}}$ precharge to $\overline{\text{CASx}}$		5		5		5		ns
t_{RSH}	Delay time, $\overline{\text{CASx}}$ active to $\overline{\text{RAS0}}$ precharge		8		10		12		ns
t_{RWD}	Delay time, $\overline{\text{RAS0}}$ to write command (read−write only)		67		79		92		ns
t_{CPW}	Delay time, $\overline{\text{CASx}}$ precharge to write command (read-write only)		45		54		62		ns
t_{REF}	Refresh time interval	’2EJ64DPN		32		32		32	ms
		’2EJ64EPN		64		64		64	
		’2FJ64xPN		128		128		128	
t_T	Transition time		2	30	2	30	2	30	ns

NOTES: 3. With ac parameters, it is assumed that t_T = 2 ns.

10. The maximum value is specified only to ensure access time.

PRODUCT PREVIEW

serial presence detect

The serial presence detect (SPD) is contained in a 2K-bit serial EEPROM located on the module. The SPD nonvolatile EEPROM contains various data such as module configuration, DRAM organization, and timing parameters (see tables below). Only the first 128 bytes are programmed by Texas Instruments, while the remaining 128 bytes are available for customer use. Programming is done through an IIC bus using the clock (SCL) and data (SDA) signals. All Texas Instruments modules comply with the current JEDEC SPD Standard. See the *Texas Instruments Serial Presence Detect Technical Reference* (literature number SMMU001) for further details.

Tables in this section list the SPD contents as follows:

Table 1−TM2EJ64DPN	Table 2−TM2EJ64EPN
Table 3−TM2FJ64DPN	Table 4−TM2FJ64EPN

PRODUCT PREVIEW

serial presence detect (continued)

Table 1. Serial Presence-Detect Data for the TM2EJ64DPN

BYTE NO.	FUNCTION DESCRIBED	’2EJ64DPN-50		’2EJ64DPN-60		’2EJ64DPN-70	
		ITEM	DATA	ITEM	DATA	ITEM	DATA
0	Defines number of bytes written into serial memory during module manufacturing	128 bytes	80h	128 bytes	80h	128 bytes	80h
1	Total number of bytes of SPD memory device	256 bytes	08h	256 bytes	08h	256 bytes	08h
2	Fundamental memory type (FPM, EDO, SDRAM)	EDO	02h	EDO	02h	EDO	02h
3	Number of row addresses on this assembly	11	0Bh	11	0Bh	11	0Bh
4	Number of column addresses on this assembly	10	0Ah	10	0Ah	10	0Ah
5	Number of module banks on this assembly	1 bank	01h	1 bank	01h	1 bank	01h
6	Data width of this assembly	64 bits	40h	64 bits	40h	64 bits	40h
7	Data width continuation		00h		00h		00h
8	Voltage interface standard of this assembly	LVTTL	01h	LVTTL	01h	LVTTL	01h
9	$\overline{\text{RAS0}}$ access time of module	t_{RAC} = 50 ns	32h	t_{RAC} = 60 ns	3Ch	t_{RAC} = 70 ns	46h
10	$\overline{\text{CASx}}$ access time of module	t_{CAC} = 13 ns	0Dh	t_{CAC} = 15 ns	0Fh	t_{CAC} = 18 ns	12h
11	SODIMM configuration type (non-parity, parity, ECC)	Non-parity	00h	Non-parity	00h	Non-parity	00h
12	Refresh rate / type	15.6 µs	00h	15.6 µs	00h	15.6 µs	00h
13	DRAM width, primary DRAM	x8	08h	x8	08h	x8	08h
14	Error-checking SDRAM data width	N / A	00h	N / A	00h	N / A	00h
62	SPD revision	Rev. 1	01h	Rev. 1	01h	Rev. 1	01h
63	Checksum for bytes 0 − 62	41	29h	53	35h	66	42h
64−71	Manufacturer’s JEDEC ID code per JEP-106E	97h	9700...00h	97h	9700...00h	97h	9700...00h
72	Manufacturing location†	TBD		TBD		TBD	
73−90	Manufacturer’s part number†	TBD		TBD		TBD	
91	Die revision code†	TBD		TBD		TBD	
92	PCB revision code†	TBD		TBD		TBD	
93−94	Manufacturing date†	TBD		TBD		TBD	
95−98	Assembly serial number†	TBD		TBD		TBD	
99−125	Manufacturer specific data†	TBD		TBD		TBD	
126−127	Vendor specific data†	TBD		TBD		TBD	
128−166	System integrator’s specific data‡	TBD		TBD		TBD	
167−255	Open						

† TBD indicates values are determined at manufacturing time and are module dependent.
‡ These TBD values are determined and programmed by the customer (optional).

serial presence detect (continued)

Table 2. Serial Presence-Detect Data for the TM2EJ64EPN

BYTE NO.	FUNCTION DESCRIBED	’2EJ64EPN-50		’2EJ64EPN-60		’2EJ64EPN-70	
		ITEM	DATA	ITEM	DATA	ITEM	DATA
0	Defines number of bytes written into serial memory during module manufacturing	128 bytes	80h	128 bytes	80h	128 bytes	80h
1	Total number of bytes of SPD memory device	256 bytes	08h	256 bytes	08h	256 bytes	08h
2	Fundamental memory type (FPM, EDO, SDRAM)	EDO	02h	EDO	02h	EDO	02h
3	Number of row addresses on this assembly	12	0Ch	12	0Ch	12	0Ch
4	Number of column addresses on this assembly	9	09h	9	09h	9	09h
5	Number of module banks on this assembly	1 bank	01h	1 bank	01h	1 bank	01h
6	Data width of this assembly	64 bits	40h	64 bits	40h	64 bits	40h
7	Data width continuation		00h		00h		00h
8	Voltage interface standard of this assembly	LVTTL	01h	LVTTL	01h	LVTTL	01h
9	$\overline{\text{RAS0}}$ access time of module	t_{RAC} = 50 ns	32h	t_{RAC} = 60 ns	3Ch	t_{RAC} = 70 ns	46h
10	$\overline{\text{CASx}}$ access time of module	t_{CAC} = 13 ns	0Dh	t_{CAC} = 15 ns	0Fh	t_{CAC} = 18 ns	12h
11	SODIMM configuration type (non-parity, parity, ECC)	Non-parity	00h	Non-parity	00h	Non-parity	00h
12	Refresh rate / type	15.6 µs	00h	15.6 µs	00h	15.6 µs	00h
13	DRAM width, primary DRAM	x8	08h	x8	08h	08h	08h
14	Error-checking SDRAM data width	N / A	00h	N / A	00h	N / A	00h
62	SPD revision	Rev. 1	01h	Rev. 1	01h	Rev. 1	01h
63	Checksum for bytes 0 − 62	41	29h	53	35h	66	42h
64−71	Manufacturer’s JEDEC ID code per JEP-106E	97h	9700...00h	97h	9700...00h	97h	9700...00h
72	Manufacturing location†	TBD		TBD		TBD	
73−90	Manufacturer’s part number†	TBD		TBD		TBD	
91	Die revision code†	TBD		TBD		TBD	
92	PCB revision code†	TBD		TBD		TBD	
93−94	Manufacturing date†	TBD		TBD		TBD	
95−98	Assembly serial number†	TBD		TBD		TBD	
99−125	Manufacturer specific data†	TBD		TBD		TBD	
126−127	Vendor specific data†	TBD		TBD		TBD	
128−166	System integrator’s specific data‡	TBD		TBD		TBD	
167−255	Open						

† TBD indicates values are determined at manufacturing time and are module dependent.
‡ These TBD values are determined and programmed by the customer (optional).

PRODUCT PREVIEW

PRODUCT PREVIEW

serial presence detect (continued)

Table 3. Serial Presence-Detect Data for the TM2FJ64DPN

BYTE NO.	FUNCTION DESCRIBED	’2FJ64DPN-50		’2FJ64DPN-60		’2FJ64DPN-70	
		ITEM	DATA	ITEM	DATA	ITEM	DATA
0	Defines number of bytes written into serial memory during module manufacturing	128 bytes	80h	128 bytes	80h	128 bytes	80h
1	Total number of bytes of SPD memory device	256 bytes	08h	256 bytes	08h	256 bytes	08h
2	Fundamental memory type (FPM, EDO, SDRAM)	EDO	02h	EDO	02h	EDO	02h
3	Number of row addresses on this assembly	11	0Bh	11	0Bh	11	0Bh
4	Number of column addresses on this assembly	10	0Ah	10	0Ah	10	0Ah
5	Number of module banks on this assembly	1 bank	01h	1 bank	01h	1 bank	01h
6	Data width of this assembly	64 bits	40h	64 bits	40h	64 bits	40h
7	Data width continuation		00h		00h		00h
8	Voltage interface standard of this assembly	LVTTL	01h	LVTTL	01h	LVTTL	01h
9	$\overline{\text{RAS0}}$ access time of module	t_{RAC} = 50 ns	32h	t_{RAC} = 60 ns	3Ch	t_{RAC} = 70 ns	46h
10	$\overline{\text{CASx}}$ access time of module	t_{CAC} = 13 ns	0Dh	t_{CAC} = 15 ns	0Fh	t_{CAC} = 18 ns	12h
11	SODIMM configuration type (non-parity, parity, ECC)	Non-parity	00h	Non-parity	00h	Non-parity	00h
12	Refresh rate / type	15.6 µs / self-refresh	80h	15.6 µs / self-refresh	80h	15.6 µs / self-refresh	80h
13	DRAM width, primary DRAM	x8	08h	x8	08h	x8	08h
14	Error-checking SDRAM data width	N / A	00h	N / A	00h	N / A	00h
62	SPD revision	Rev. 1	01h	Rev. 1	01h	Rev. 1	01h
63	Checksum for bytes 0 − 62	169	A9h	181	B5h	194	C2h
64−71	Manufacturer’s JEDEC ID code per JEP-106E	97h	9700...00h	97h	9700...00h	97h	9700...00h
72	Manufacturing location†	TBD		TBD		TBD	
73−90	Manufacturer’s part number†	TBD		TBD		TBD	
91	Die revision code†	TBD		TBD		TBD	
92	PCB revision code†	TBD		TBD		TBD	
93−94	Manufacturing date†	TBD		TBD		TBD	
95−98	Assembly serial number†	TBD		TBD		TBD	
99−125	Manufacturer specific data†	TBD		TBD		TBD	
126−127	Vendor specific data†	TBD		TBD		TBD	
128−166	System integrator’s specific data‡	TBD		TBD		TBD	
167−255	Open						

† TBD indicates values are determined at manufacturing time and are module dependent.
‡ These TBD values are determined and programmed by the customer (optional).

serial presence detect (continued)

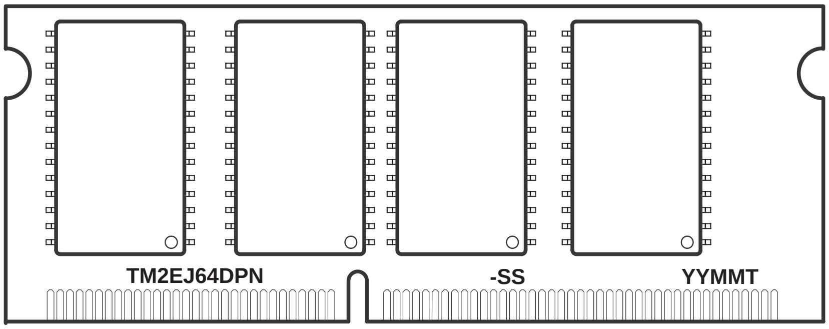
Table 4. Serial Presence-Detect Data for the TM2FJ64EPN

BYTE NO.	FUNCTION DESCRIBED	’2FJ64EPN-50		’2FJ64EPN-60		’2FJ64EPN-70	
		ITEM	DATA	ITEM	DATA	ITEM	DATA
0	Defines number of bytes written into serial memory during module manufacturing	128 bytes	80h	128 bytes	80h	128 bytes	80h
1	Total number of bytes of SPD memory device	256 bytes	08h	256 bytes	08h	256 bytes	08h
2	Fundamental memory type (FPM, EDO, SDRAM)	EDO	02h	EDO	02h	EDO	02h
3	Number of row addresses on this assembly	12	0Ch	12	0Ch	12	0Ch
4	Number of column addresses on this assembly	9	09h	9	09h	9	09h
5	Number of module banks on this assembly	1 bank	02h	1 bank	02h	1 bank	02h
6	Data width of this assembly	64 bits	40h	64 bits	40h	64 bits	40h
7	Data width continuation		00h		00h		00h
8	Voltage interface standard of this assembly	LVTTL	01h	LVTTL	01h	LVTTL	01h
9	$\overline{\text{RAS0}}$ access time of module	t_{RAC} = 50 ns	32h	t_{RAC} = 60 ns	3Ch	t_{RAC} = 70 ns	46h
10	$\overline{\text{CAS}}$x access time of module	t_{CAC} = 13 ns	0Dh	t_{CAC} = 15 ns	0Fh	t_{CAC} = 18 ns	12h
11	SODIMM configuration type (non-parity, parity, ECC)	Non-parity	00h	Non-parity	00h	Non-parity	00h
12	Refresh rate / type	15.6 µs / self-refresh	80h	15.6 µs / self-refresh	80h	15.6 µs / self-refresh	80h
13	DRAM width, primary DRAM	x8	08h	x8	08h	x8	08h
14	Error-checking SDRAM data width	N / A	00h	N / A	00h	N / A	00h
62	SPD revision	Rev. 1	01h	Rev. 1	01h	Rev. 1	01h
63	Checksum for bytes 0 − 62	169	A9h	181	B5h	194	C2h
64−71	Manufacturer’s JEDEC ID code per JEP-106E	97h	9700...00h	97h	9700...00h	97h	9700...00h
72	Manufacturing location†	TBD		TBD		TBD	
73−90	Manufacturer’s part number†	TBD		TBD		TBD	
91	Die revision code†	TBD		TBD		TBD	
92	PCB revision code†	TBD		TBD		TBD	
93−94	Manufacturing date†	TBD		TBD		TBD	
95−98	Assembly serial number†	TBD		TBD		TBD	
99−125	Manufacturer specific data†	TBD		TBD		TBD	
126−127	Vendor specific data†	TBD		TBD		TBD	
128−166	System integrator’s specific data‡	TBD		TBD		TBD	
167−255	Open						

† TBD indicates values are determined at manufacturing time and are module dependent.
‡ These TBD values are determined and programmed by the customer (optional).

PRODUCT PREVIEW

device symbolization (TM2EJ64DPN illustrated)



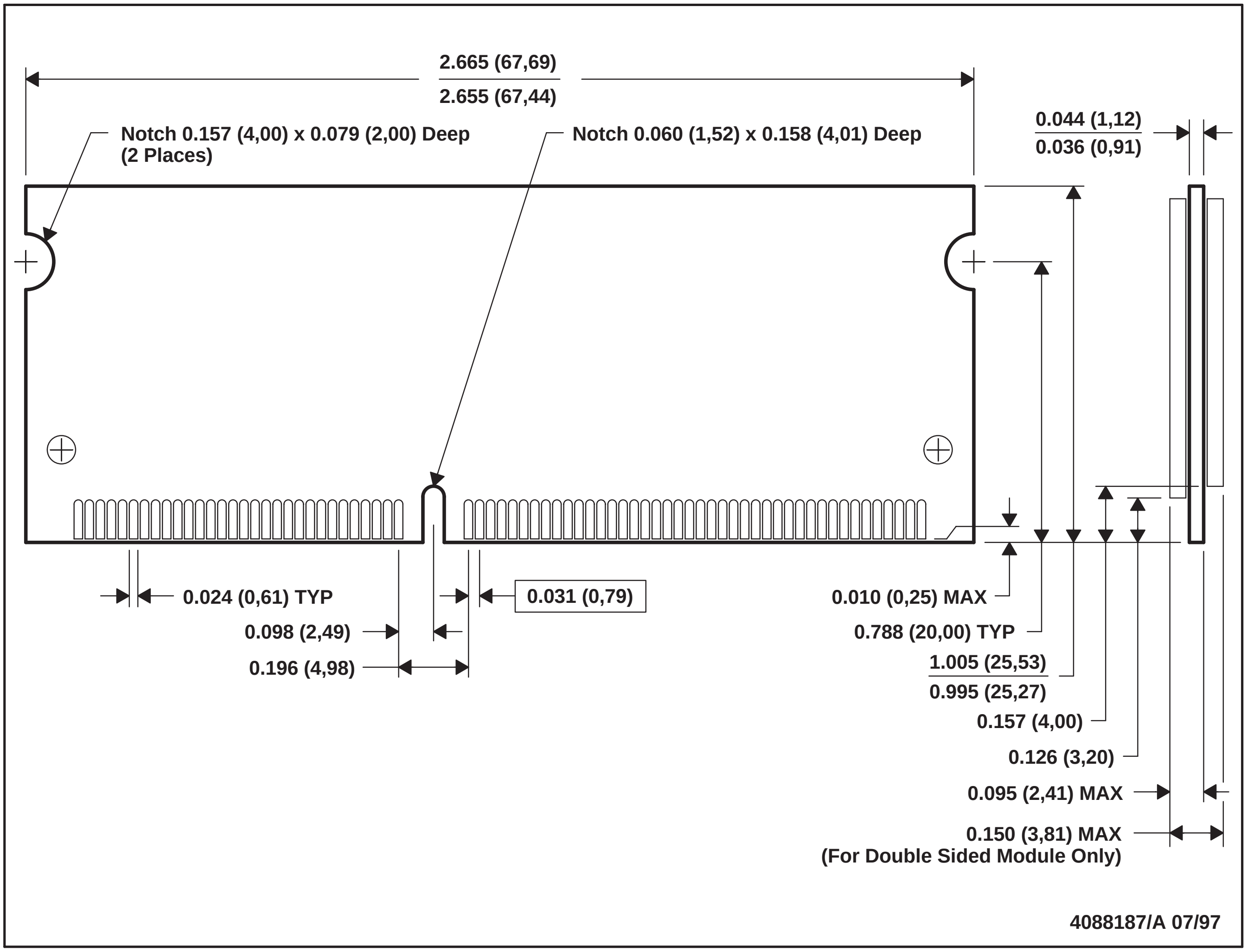
YY = Year Code
MM = Month Code
T = Assembly Site Code
-SS = Speed Code

NOTE A: Location of symbolization may vary.

PRODUCT PREVIEW

MECHANICAL DATA

BDM (R-SODIMM-N144) **SMALL OUTLINE DUAL IN-LINE MEMORY MODULE**


2.665 (67,69)
2.655 (67,44)
Notch 0.157 (4,00) x 0.079 (2,00) Deep (2 Places)
Notch 0.060 (1,52) x 0.158 (4,01) Deep
0.044 (1,12)
0.036 (0,91)
0.024 (0,61) TYP
0.031 (0,79)
0.098 (2,49)
0.196 (4,98)
0.010 (0,25) MAX
0.788 (20,00) TYP
1.005 (25,53)
0.995 (25,27)
0.157 (4,00)
0.126 (3,20)
0.095 (2,41) MAX
0.150 (3,81) MAX
(For Double Sided Module Only)
4088187/A 07/97

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-190

PRODUCT PREVIEW

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Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
RFID	www.ti-rfid.com	Telephony	www.ti.com/telephony
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Video & Imaging	www.ti.com/video
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