- **Organization . . . 4194304 × 72 Bits**
- **Single 3.3-V Power Supply (±10% Tolerance)**
- **JEDEC 168-Pin Dual-In-Line Memory Module (DIMM) With Buffer for Use With Socket**
- **TM4EP72xxB-xx — Uses Eighteen 16M-Bit High-Speed (4M×4-Bit) Dynamic Random Access Memories (DRAMs)**
- **High-Speed, Low-Noise LVTTL Interface**
- **High-Reliability Plastic 26-Lead 300-Mil-Wide Surface-Mount Small-Outline J-Lead (SOJ) Package (DJ Suffix) and 26-Lead 300-Mil-Wide Surface-Mount Thin Small-Outline Package (TSOP) (DGA Suffix)**
- **Intended for Workstation/Server Applications**
- **Long Refresh Periods:**
  - **TM4EP72CxB: 64 ms (4096 Cycles)**
  - **TM4EP72BxB: 32 ms (2048 Cycles)**
- **3-State Output**
- **Extended-Data-Out (EDO) Operation With CAS-Before-RAS (CBR), RAS-Only, and Hidden Refresh**
- **Ambient Temperature Range 0°C to 70°C**
- **Gold-Plated Contacts**
- **Performance Ranges**

	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{CAC} (MAX)	ACCESS TIME t_{AA} (MAX)	EDO CYCLE t_{HPC} (MIN)
’4EP72xxB-50	50 ns	13 ns	25 ns	20 ns
’4EP72xxB-60	60 ns	15 ns	30 ns	25 ns
’4EP72xxB-70	70 ns	18 ns	35 ns	30 ns

description

The TM4EP72BxB is a 32M-byte, 168-pin, buffered, dual-in-line memory module (DIMM). The DIMM is composed of eighteen TMS427409A, 4194304 × 4-bit 2K refresh EDO DRAMs, each in a 300-mil, 26-lead plastic TSOP (DGA suffix) or SOJ package (DJ suffix), and two SN74LVT162244 16-bit buffers, each in a 48-lead plastic TSOP mounted on a substrate with decoupling capacitors. See the TMS427409A data sheet (literature number SMKS893).

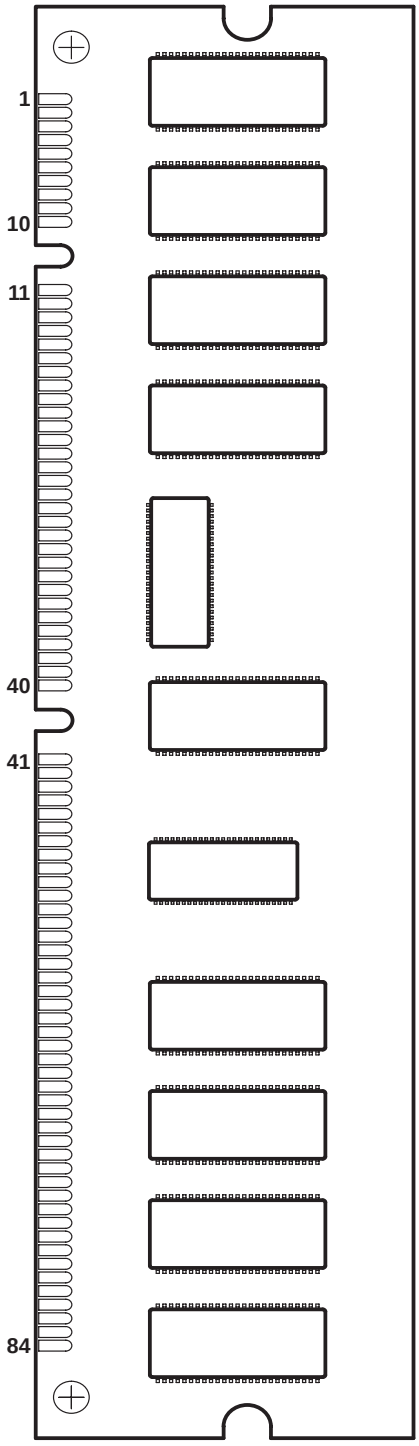
The TM4EP72CxB is a 32M-byte, 168-pin, buffered DIMM. The DIMM is composed of eighteen TMS426409A, 4194304 × 4-bit 4K refresh EDO DRAMs, each in a 300-mil, 26-lead plastic TSOP (DGA suffix) or SOJ package (DJ suffix), and two 16-bit buffers mounted on a substrate with decoupling capacitors. See the TMS427409A data sheet (literature number SMKS893).

These modules are intended for multimodule workstation/server applications where buffering is needed for address and control signals. Two copies of address 0 (A0 and B0) are defined to allow maximum performance for 4-byte applications which interleave between two 4-byte banks. A0 is common to the DRAMs used for DQ0−DQ31, while B0 is common to the DRAMs used for DQ32−DQ63.

operation

The TM4EP72xxB operates as eighteen TMS42x409As that are connected as shown in the TM4EP72xxB functional block diagram.

DUAL-IN-LINE MEMORY MODULE (TOP VIEW)



TM4EP72xPB (SIDE VIEW)

PIN NOMENCLATURE − TM4EP72BxB	
A[0:10]	Row-Address Inputs
A[0:10]	Column-Address Inputs
B0	Addr0 for Bank 2 Devices
DQ[0:63]	Data In/Data Out
CB[0:7]	Check Bit In/Check Bit Out
ID[0:1]	ID Pins
$\overline{CAS0}$ and $\overline{CAS4}$	Column-Address Strobe
$\overline{RAS0}$ and $\overline{RAS2}$	Row-Address Strobe
$\overline{WE0}$ and $\overline{WE2}$	Write Enable
$\overline{OE0}$ and $\overline{OE2}$	Output Enable
PD[1:8]	Presence Detect
PDE	Presence Detect Enable
NC	No-Connect Pin
V_{DD}	3.3-V Supply
V_{SS}	Ground

PIN NOMENCLATURE − TM4EP72CxB	
A[0:11]	Row-Address Inputs
A[0:9]	Column-Address Inputs
B0	Addr0 for Bank 2 Devices
DQ[0:63]	Data In/Data Out
CB[0:7]	Check Bit In/Check Bit Out
ID[0:1]	ID Pins
$\overline{CAS0}$ and $\overline{CAS4}$	Column-Address Strobe
$\overline{RAS0}$ and $\overline{RAS2}$	Row-Address Strobe
$\overline{WE0}$ and $\overline{WE2}$	Write Enable
$\overline{OE0}$ and $\overline{OE2}$	Output Enable
PD[1:8]	Presence Detect
PDE	Presence Detect Enable
NC	No-Connect Pin
V_{DD}	3.3-V Supply
V_{SS}	Ground

PRESENCE DETECT			
PIN	**− 50**	**− 60**	**− 70**
PD1	1	1	1
PD2	1	1	1
PD3	0	0	0
PD4	1	1	1
PD5	1	1	1
PD6	0	1	0
PD7	0	1	1
PD8	0	0	0
ID0	0	0	0
ID1	0	0	0

Pin Assignments

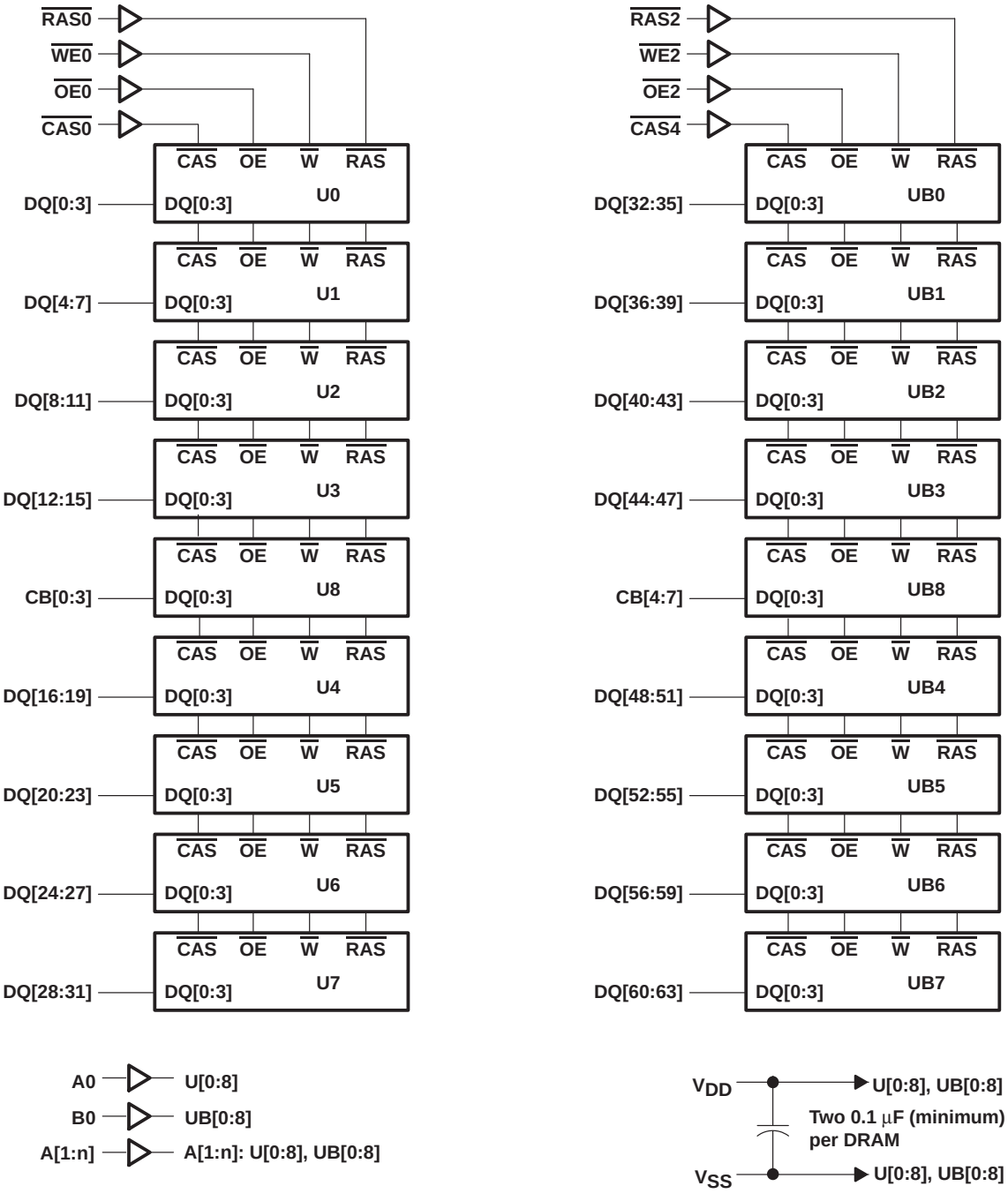
PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME
1	V_{SS}	43	V_{SS}	85	V_{SS}	127	V_{SS}
2	DQ0	44	$\overline{OE2}$	86	DQ32	128	NC
3	DQ1	45	$\overline{RAS2}$	87	DQ33	129	NC
4	DQ2	46	$\overline{CAS4}$	88	DQ34	130	NC
5	DQ3	47	NC	89	DQ35	131	NC
6	V_{DD}	48	$\overline{WE2}$	90	V_{DD}	132	PDE
7	DQ4	49	V_{DD}	91	DQ36	133	V_{DD}
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	CB2	94	DQ39	136	CB6
11	DQ8	53	CB3	95	DQ40	137	CB7
12	V_{SS}	54	V_{SS}	96	V_{SS}	138	V_{SS}
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	V_{DD}	101	DQ45	143	V_{DD}
18	V_{DD}	60	DQ20	102	V_{DD}	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	NC	104	DQ47	146	NC
21	CB0	63	NC	105	CB4	147	NC
22	CB1	64	NC	106	CB5	148	NC
23	V_{SS}	65	DQ21	107	V_{SS}	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	V_{DD}	68	V_{SS}	110	V_{DD}	152	V_{SS}
27	$\overline{WE0}$	69	DQ24	111	NC	153	DQ56
28	$\overline{CAS0}$	70	DQ25	112	NC	154	DQ57
29	NC	71	DQ26	113	NC	155	DQ58
30	$\overline{RAS0}$	72	DQ27	114	NC	156	DQ59
31	$\overline{OE0}$	73	V_{DD}	115	NC	157	V_{DD}
32	V_{SS}	74	DQ28	116	V_{SS}	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	V_{SS}	120	A7	162	V_{SS}
37	A8	79	PD1	121	A9	163	PD2
38	A10	80	PD3	122	A11	164	PD4
39	NC	81	PD5	123	NC	165	PD6
40	V_{DD}	82	PD7	124	V_{DD}	166	PD8
41	NC	83	ID0	125	NC	167	ID1
42	NC	84	V_{DD}	126	B0	168	V_{DD}

buffered dual-in-line memory module and components

The buffered dual-in-line memory module and components include:

- PC substrate: 1,27 ± 0,1 mm (0.05 inch) nominal thickness; 0.005 inch/inch maximum warpage
- Bypass capacitors: Multilayer ceramic
- Contact area: Nickel plate and gold plate over copper

functional block diagram for the TM4EP72xxB



absolute maximum ratings over ambient temperature range (unless otherwise noted)†

Supply voltage range, V_{DD} . . . . . −0.5 V to 4.6 V
Voltage range on any pin (see Note 1) . . . . . − 0.5 V to 4.6 V
Short-circuit output current . . . . . 50 mA
Power dissipation: TM4EP72xxB . . . . . 20 W
Ambient temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . − 55°C to 125°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	3	3.3	3.6	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2		V_{DD} + 0.3	V
V_{IL}	Low-level input voltage	−0.3		0.8	V
T_A	Ambient temperature	0		70	°C

electrical characteristics over recommended ranges of supply voltage and ambient temperature (unless otherwise noted)

TM4EP72BxB

PARAMETER		TEST CONDITIONS†		'4EP72BxB-50		'4EP72BxB-60		'4EP72BxB-70		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = − 2 mA	LVTTL	2.4		2.4		2.4		V
		I_{OH} = − 100 µA	LVCMOS	V_{DD}−0.2		V_{DD}−0.2		V_{DD}−0.2		
V_{OL}	Low-level output voltage	I_{OL} = 2 mA	LVTTL		0.4		0.4		0.4	V
		I_{OL} = 100 µA	LVCMOS		0.2		0.2		0.2	
I_I	Input current (leakage)	V_{DD} = 3.6 V, V_I = 0 V to 3.9 V, All others = 0 V to V_{DD}			± 20		± 20		± 20	µA
I_O	Output current (leakage)	V_{DD} = 3.6 V, V_O = 0 V to V_{DD}, CASx high			± 20		± 20		± 20	µA
I_{CC1}‡§	Average read- or write-cycle current	V_{DD} = 3.6 V, Minimum cycle			2160		1800		1620	mA
I_{CC2}	Average standby current	V_{IH} = 2 V (LVTTL), After one memory cycle, RASx and CASx high			36		36		36	mA
		V_{IH} = V_{DD} − 0.2 V (LVCMOS), After one memory cycle, RASx and CASx high			18		18		18	mA
I_{CC3}‡§	Average refresh current (RAS-only refresh or CBR)	V_{DD} = 3.6 V, Minimum cycle, RASx cycling, CASx high (RASx-only refresh), RASx low after CASx low (CBR)			2160		1800		1620	mA
I_{CC4}‡¶	Average EDO current	V_{DD} = 3.6 V, t_{HPC} = MIN, RASx low, CASx cycling			1980		1620		1440	mA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.
‡ Measured with outputs open
§ Measured with a maximum of one address change while $\overline{RASx}$ = V_{IL}
¶ Measured with a maximum of one address change during each EDO cycle, t_{HPC}

electrical characteristics over recommended ranges of supply voltage and ambient temperature (unless otherwise noted) (continued)

TM4EP72CxB

PARAMETER		TEST CONDITIONS†		'4EP72CxB-50		'4EP72CxB-60		'4EP72CxB-70		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = − 2 mA	LVTTL	2.4		2.4		2.4		V
		I_{OH} = − 100 µA	LVCMOS	V_{DD}−0.2		V_{DD}−0.2		V_{DD}−0.2		
V_{OL}	Low-level output voltage	I_{OL} = 2 mA	LVTTL		0.4		0.4		0.4	V
		I_{OL} = 100 µA	LVCMOS		0.2		0.2		0.2	
I_I	Input current (leakage)	V_{DD} = 3.6 V, V_I = 0 V to 3.9 V, All others = 0 V to V_{DD}			± 20		± 20		± 20	µA
I_O	Output current (leakage)	$\overline{V_{DD}}$ = 3.6 V, V_O = 0 V to V_{DD}, $\overline{CAS}$x high			± 20		± 20		± 20	µA
I_{CC1}‡§	Average read- or write-cycle current	V_{DD} = 3.6 V, Minimum cycle			1620		1260		1080	mA
I_{CC2}	Average standby current	V_{IH} = 2 V (LVTTL), After one memory cycle, $\overline{RAS}$x and $\overline{CAS}$x high			36		36		36	mA
		V_{IH} = V_{DD} − 0.2 V (LVCMOS), After one memory cycle, $\overline{RAS}$x and $\overline{CAS}$x high			18		18		18	mA
I_{CC3}‡§	Average refresh current ($\overline{RAS}$-only refresh or CBR)	$\overline{V_{DD}}$ = 3.6 V, Minimum cycle, $\overline{RAS}$x cycling, $\overline{CAS}$x high ($\overline{RAS}$x-only refresh), $\overline{RAS}$x low after $\overline{CAS}$x low (CBR)			1620		1260		1080	mA
I_{CC4}‡¶	Average EDO current	$\overline{V_{DD}}$ = 3.6 V, $\overline{RAS}$x low, t_{HPC} = MIN, $\overline{CAS}$x cycling			1800		1620		1440	mA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.
‡ Measured with outputs open
§ Measured with a maximum of one address change while $\overline{RAS}$x = V_{IL}
¶ Measured with a maximum of one address change during each EDO cycle, t_{HPC}

capacitance over recommended ranges of supply voltage and ambient temperature, f = 1 MHz (see Note 2)

PARAMETER		’4EP72xxB		UNIT
		MIN	MAX	
$C_{i(A)}$	Input capacitance, A0 − A10		6	pF
$C_{i(OE)}$	Input capacitance, $\overline{OEx}$		6	pF
$C_{i(CAS)}$	Input capacitance, $\overline{CASx}$		6	pF
$C_{i(RAS)}$	Input capacitance, $\overline{RASx}$		65	pF
$C_{i(W)}$	Input capacitance, $\overline{WEx}$		6	pF
C_o	Output capacitance		9	pF

NOTE 2: V_{DD}= NOM supply voltage ±10%, and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and ambient temperature (see Note 3)

PARAMETER		’4EP72xxB-50		’4EP72xxB-60		’4EP72xxB-70		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column address (see Note 4)		30		35		40	ns
t_{CAC}	Access time from $\overline{CASx}$ (see Note 4)		18		20		23	ns
t_{CPA}	Access time from $\overline{CASx}$ precharge (see Note 4)		33		40		45	ns
t_{RAC}	Access time from $\overline{RASx}$ (see Note 4)		50		60		70	ns
t_{OEA}	Access time from $\overline{OEx}$ (see Note 4)		18		20		23	ns
t_{CLZ}	Delay time, $\overline{CASx}$ to output in low impedance	2		2		2		ns
t_{REZ}	Output buffer turn off delay from $\overline{RASx}$ (see Note 5)	3	13	3	15	3	18	ns
t_{CEZ}	Output buffer turn off delay from $\overline{CASx}$ (see Note 5)	5	18	5	20	5	23	ns
t_{OEZ}	Output buffer turn off delay from $\overline{OEx}$ (see Note 5)	5	18	5	20	5	23	ns
t_{WEZ}	Output buffer turn off delay from $\overline{WEx}$ (see Note 5)	3	13	3	15	3	18	ns

NOTES: 3. With ac parameters, it is assumed that t_T = 2 ns.
4. Access times are measured with output reference levels of V_{OH} = 2 V and V_{OL} = 0.8 V.
5. The maximum values of t_{REZ}, t_{CEZ}, t_{OEZ}, and t_{WEZ} are specified when the outputs are no longer driven. Data in must not be driven until one of the applicable maximum values is satisfied.

EDO timing requirements (see Note 3)

		’4EP72xxB-50		’4EP72xxB-60		’4EP72xxB-70		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{HPC}	Cycle time, EDO page mode, read-write	20		25		30		ns
t_{PRWC}	Cycle time, EDO read-write	55		64		71		ns
t_{CSH}	Delay time, $\overline{RASx}$ active to $\overline{CASx}$ precharge	38		46		56		ns
t_{CHO}	Hold time, $\overline{OEx}$ from $\overline{CASx}$	7		10		10		ns
t_{DOH}	Hold time, output from $\overline{CASx}$	5		5		5		ns
t_{CAS}	Pulse duration, $\overline{CASx}$ active	8	10000	10	10000	12	10000	ns
t_{WPE}	Pulse duration, $\overline{WEx}$ active (output disable only)	7		7		7		ns
t_{OCH}	Setup time, $\overline{OEx}$ before $\overline{CASx}$	8		10		10		ns
t_{CP}	Pulse duration, $\overline{CASx}$ precharge	8		10		10		ns
t_{OEP}	Precharge time, $\overline{OEx}$	5		5		5		ns

NOTE 3: With ac parameters, it is assumed that t_T = 2 ns.

ac timing requirements (see Note 3)

		'4EP72xxB-50		'4EP72xxB-60		'4EP72xxB-70		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Cycle time, random read or write	84		104		124		ns
t_{RWC}	Cycle time, read-write	116		140		165		ns
t_{RASP}	Pulse duration, $\overline{RAS}x$ active, fast page mode (see Note 6)	50	100 000	60	100 000	70	100 000	ns
t_{RAS}	Pulse duration, $\overline{RAS}x$ active, non-page mode (see Note 6)	50	10 000	60	10 000	70	10 000	ns
t_{RP}	Pulse duration, $\overline{RAS}x$ precharge	30		40		50		ns
t_{WP}	Pulse duration, write command	9		11		11		ns
t_{ASC}	Setup time, column address	0		0		0		ns
t_{ASR}	Setup time, row address	5		5		5		ns
t_{DS}	Setup time, data in (see Note 7)	5		5		5		ns
t_{RCS}	Setup time, read command	0		0		0		ns
t_{CWL}	Setup time, write command before $\overline{CAS}x$ precharge	9		11		13		ns
t_{RWL}	Setup time, write command before $\overline{RAS}x$ precharge	10		12		14		ns
t_{WCS}	Setup time, write command before $\overline{CAS}x$ active (early-write only)	0		0		0		ns
t_{WRP}	Setup time, $\overline{WE}x$ high before RAS low (CBR refresh only)	12		12		12		ns
t_{WTS}	Setup time, $\overline{WE}x$ low before RAS low (test mode only)	12		12		12		ns
t_{CSR}	Setup time, $\overline{CAS}x$ referenced to $\overline{RAS}x$ (CBR refresh only)	3		3		3		ns
t_{CAH}	Hold time, column address	8		10		12		ns
t_{DH}	Hold time, data in (see Note 7)	13		15		17		ns
t_{RAH}	Hold time, row address	6		8		8		ns
t_{RCH}	Hold time, read command referenced to $\overline{CAS}x$ (see Note 8)	0		0		0		ns
t_{RRH}	Hold time, read command referenced to $\overline{RAS}x$ (see Note 8)	− 2		− 2		− 2		ns
t_{WCH}	Hold time, write command during $\overline{CAS}x$ active (early-write only)	9		11		13		ns
t_{ROH}	Hold time, $\overline{RAS}x$ referenced to $\overline{OE}x$	8		10		10		ns
t_{WRH}	Hold time, $\overline{WE}x$ high after RAS low (CBR refresh)	12		12		12		ns
t_{WTH}	Hold time, $\overline{WE}x$ low after RAS low (test mode only)	12		12		12		ns
t_{CHR}	Hold time, $\overline{CAS}x$ referenced to $\overline{RAS}x$ (CBR refresh only)	8		8		8		ns
t_{OEH}	Hold time, $\overline{OE}x$ command	14		16		19		ns
t_{RHCP}	Hold time, $\overline{RAS}x$ active from $\overline{CAS}x$ precharge	33		40		45		ns
t_{AWD}	Delay time, column address to write command (read-write only)	47		54		62		ns
t_{CPW}	Delay time, $\overline{WE}x$ low after $\overline{CAS}x$ precharge (read-write only)	45		54		62		ns
t_{CRP}	Delay time, $\overline{CAS}x$ precharge to $\overline{RAS}x$	3		3		3		ns
t_{CWD}	Delay time, $\overline{CAS}x$ to write command (read-write only)	35		39		45		ns
t_{OED}	Delay time, $\overline{OE}x$ to data in	15		17		20		ns
t_{RAD}	Delay time, $\overline{RAS}x$ to column address (see Note 9)	8	20	10	25	10	30	ns
t_{RAL}	Delay time, column address to $\overline{RAS}x$ precharge	30		35		40		ns
t_{CAL}	Delay time, column address to $\overline{CAS}x$ precharge	20		23		28		ns

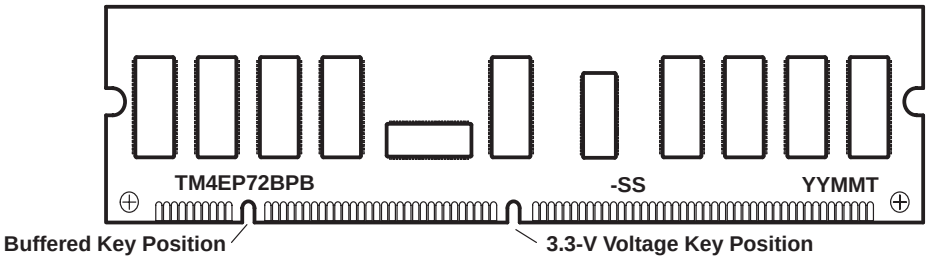
NOTES: 3. With ac parameters, it is assumed that t_T = 2 ns.
6. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
7. Referenced to the later of $\overline{CAS}x$ or $\overline{WE}x$ in write operations
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. The maximum value is specified only to ensure access time.

ac timing requirements (see Note 3) (continued)

		’4EP72xxB-50		’4EP72xxB-60		’4EP72xxB-70		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RCD}	Delay time, $\overline{RAS}$x to $\overline{CAS}$x (see Note 9)	10	32	12	40	12	47	ns
t_{RPC}	Delay time, $\overline{RAS}$x precharge to $\overline{CAS}$x	3		3		3		ns
t_{RSH}	Delay time, $\overline{CAS}$x active to $\overline{RAS}$x precharge	18		20		23		ns
t_{RWD}	Delay time, $\overline{RAS}$x to write command (read-write only)	67		79		92		ns
t_{TAA}	Access time from address (test mode)	30		35		40		ns
t_{TCPA}	Access time from column precharge (test mode)	40		45		50		ns
t_{TRAC}	Access time from $\overline{RAS}$x (test mode)	50		60		70		ns
t_{REF}	Refresh time interval		32		32		32	ms
t_T	Transition time	2	30	2	30	2	30	ns

NOTES: 3. With ac parameters, it is assumed that t_T = 2 ns.
9. The maximum value is specified only to ensure access time.

device symbolization (TM4EP72BPB illustrated)

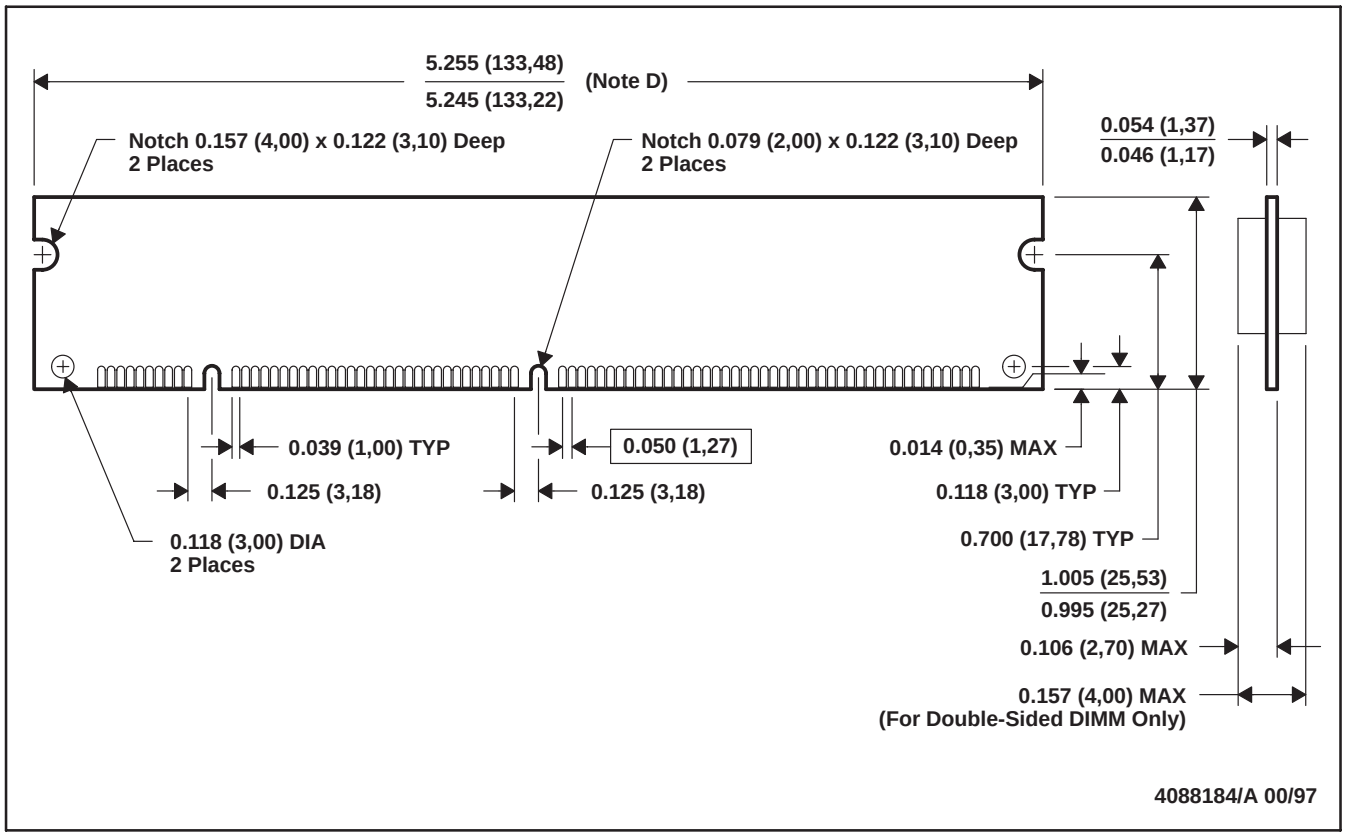


YY = Year Code
MM = Month Code
T = Assembly Site Code
-SS = Speed Code

NOTE A: Location of symbolization may vary.

MECHANICAL DATA

BRW (R-PDIM-N168) **DUAL IN-LINE MEMORY MODULE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-161
D. Dimension includes De−panelization variations; applies between notch and tab edge.
E. Outline may vary above notches to allow router/panelization irregularities.

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