LM81

LM81 Serial Interface ACPI-Compatible Microprocessor System Hardware Monitor

Literature Number: SNAS011D

National Semiconductor

February 2002

LM81
Serial Interface ACPI-Compatible Microprocessor System Hardware Monitor

General Description

The LM81 is a highly integrated data acquisition system for hardware monitoring of servers, Personal Computers, or virtually any microprocessor-based system. In a PC, the LM81 can be used to monitor power supply voltages, temperatures, and fan speeds. Actual values for these inputs can be read at any time. Programmable WATCHDOG limits in the LM81 activate a fully programmable and maskable interrupt system with two outputs ($\overline{INT}$ and $\overline{T\_CRIT\_}$).

The LM81 has an on-chip digital output temperature sensor with 9-bit or 12-bit resolution, a 6 analog input ADC with 8-bit resolution and an 8-bit DAC. Two fan tachometer outputs can be measured with the LM81's FAN1 and FAN2 inputs. The DAC, with a 0 to 1.25V output voltage range, can be used for fan speed control. Additional inputs are provided for Chassis Intrusion detection circuits, and VID monitor inputs. The LM81 has a Serial Bus interface that is compatible with SMBus™.

Features

- Temperature sensing
- 6 positive voltage inputs with scaling resistors to monitor +5V, +12V, +3.3V, +2.5V, Vccp power supplies directly
- 8-bit DAC output for controlling fan speed
- 2 fan speed monitoring inputs
- Chassis Intrusion detector input
- WATCHDOG comparison of all monitored values
- SMBus 1.0 (LM81C) and 1.1 (LM81B) Serial Bus interface compatibility
- LM81B has improved voltage monitoring accuracy
- VID0-VID4 monitoring inputs

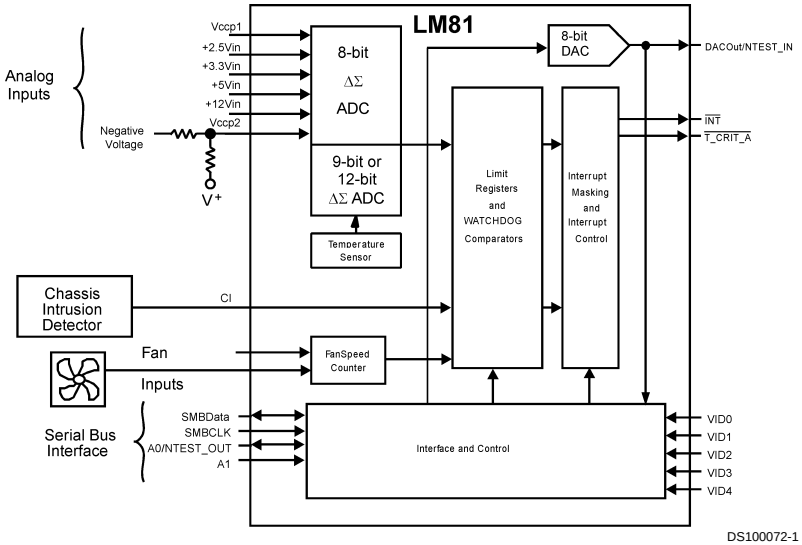
Key Specifications

■ Voltage Monitoring Error	+2% or ±1.2% (max)
■ Temperature Error −40˚C to +125˚C	± 3˚C (max)
■ Supply Voltage Range	2.8V to 3.8V
■ Supply Current	0.4 mA (typ)
■ ADC and DAC Resolution	8 Bits
■ Temperature Resolution	0.5˚C

Applications

- System Thermal and Hardware Monitoring for Servers and PCs
- Office Electronics
- Electronic Test Equipment and Instrumentation

Typical Application



# Indicates Active Low ("Not")

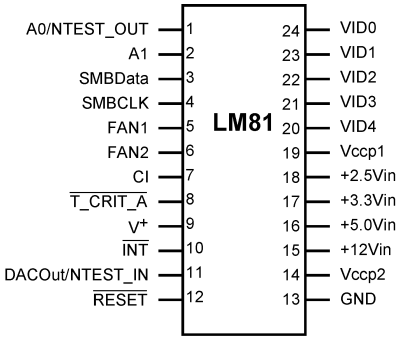
Ordering Information

Temperature Range $-40^{\circ}C \leq T_A \leq +125^{\circ}C$		NS Package Number	SMBus Revision Level	Voltage Monitoring Error
Order Number	Device Marking			
LM81BIMT-3[1]	LM81BIMT-3	MTC24B	1.1	±1.2%
LM81BIMTX-3[2]	LM81BIMT-3	MTC24B	1.1	±1.2%
LM81CIMT-3[1]	LM81CIMT-3	MTC24B	1.0	+2%
LM81CIMTX-3[2]	LM81CIMT-3	MTC24B	1.0	+2%

Note: [1]-Rail transport media, 62 parts per rail

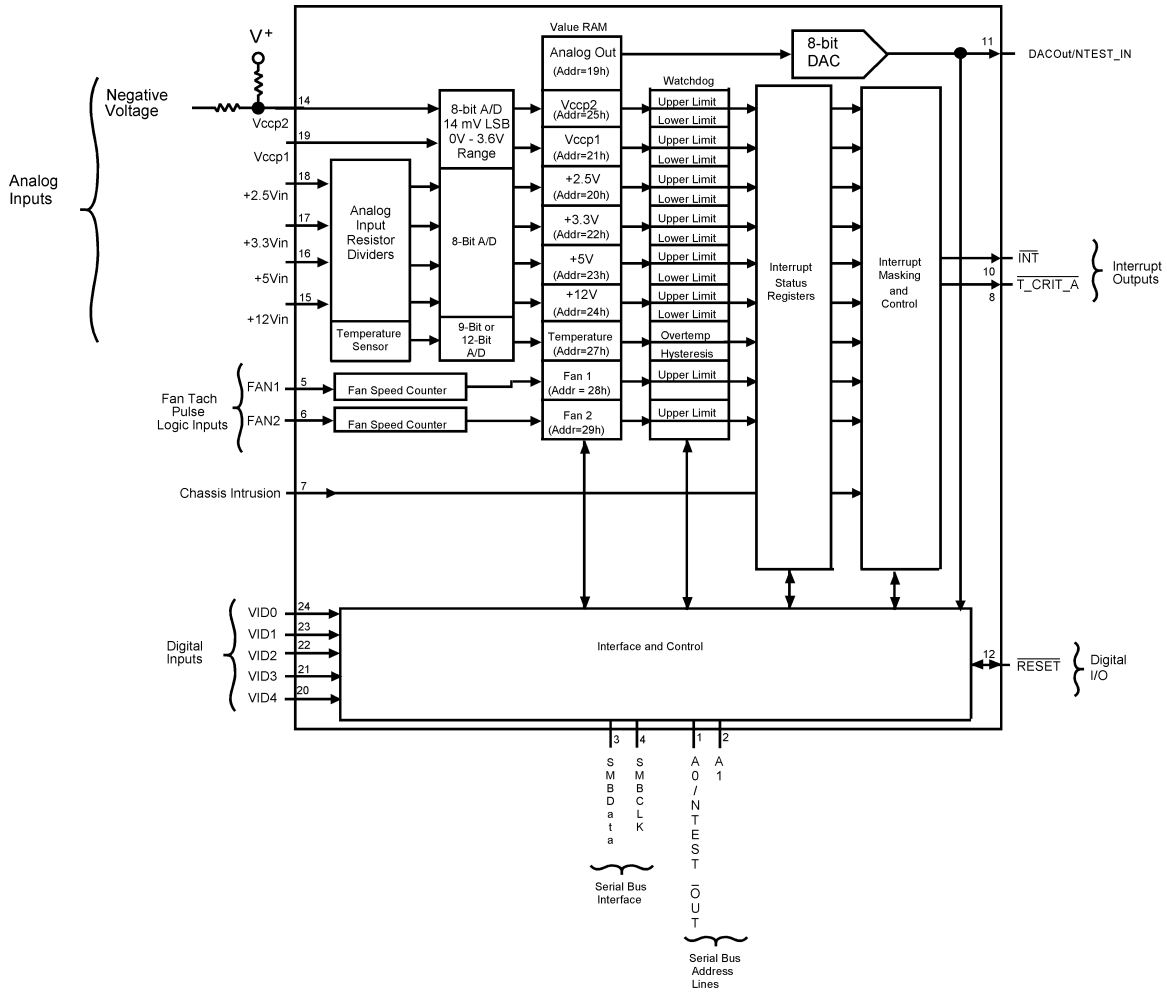
[2]-Tape and reel transport media, 3400 parts per reel

Connection Diagram



DS100072-3

Block Diagram



DS100072-2

Pin Description

Pin Name(s)	Pin Number	Number of Pins	Type	Description
A0/NTEST_OUT	1	1	Digital I/0	The lowest order programmable bit of the serial bus address. This pin functions as an output during NAND Tree tests (board-level connectivity testing). Refer to *SECTION 11* on NAND Tree testing.
A1	2	1	Digital Input	The highest order programmable bit of the serial bus address.
SMBData	3	1	Digital I/O	Serial Bus bidirectional Data. Open-drain output.
SMBCLK	4	1	Digital Input	Serial Bus Clock.
FAN1-FAN2	5-6	2	Digital Inputs	Schmitt Trigger fan tachometer inputs.
CI	7	1	Digital I/O	An active high input from an external circuit which latches a Chassis Intrusion event. This line can go high without any clamping action regardless of the powered state of the LM81. There is also an internal open-drain output on this line, controlled by Bit 6 of the Configuration Register (40h) or Bit 7 CI Clear Register (46h), to provide a minimum 20 ms reset pulse. See *Section 3.3* and *Section 9.0*.
$\overline{\text{T\_CRIT\_A}}$	8	1	Digital Output	Critical Temperature Alarm active low open-drain output. This pin can be grounded when not used.
V^+ (+2.8V to +3.8V)	9	1	POWER	+3.3V V^+ power. Bypass with the parallel combination of 10 µF (electrolytic or tantalum) and 0.1 µF (ceramic) bypass capacitors.

Pin Description (Continued)

Pin Name(s)	Pin Number	Number of Pins	Type	Description
$\overline{\text{INT}}$	10	1	Digital Output	Interrupt active low open-drain output. This output is enabled when Bit 1 in the Configuration Register is set to 1. The default state is disabled.
DACOut/NTEST_IN	11	1	Analog Output/Digital Input	0V to +1.25V amplitude 8-bit DAC output. When forced high by an external voltage the NAND Tree Test mode is enabled which provides board-level connectivity testing. Refer to Section 11.0 on NAND Tree testing.
$\overline{\text{RESET}}$	12	1	Digital I/O	Master Reset, 5 mA driver (open-drain), active low output with a 20 ms minimum pulse width. Available when enabled via Bit 4 in the Configuration register. It acts as an active low power on RESET input.
GND	13	1	GROUND	Internally connected to all circuitry. The ground reference for all analog inputs and the DAC output. This pin needs to be connected to a low noise analog ground plane for optimum performance of the DAC output.
Vccp2	14	1	Analog Input	Analog input for monitoring −12V or Vccp2. Selectable by choosing the appropriate external resistor divider values such that the input to the LM81 is scaled to +2.5V. See *Section 4.0.*
+12Vin	15	1	Analog Input	Analog input for monitoring +12V.
+5Vin	16	1	Analog Input	Analog input for monitoring +5V.
+3.3Vin	17	1	Analog Input	Analog input for monitoring +3.3V.
+2.5Vin	18	1	Analog Input	Analog input for monitoring +2.5V.
Vccp1	19	1	Analog Input	Analog input for monitoring Vccp, a processor voltage that is nominally at +2.5V.
VID4-VID0	20-24	5	Digital Inputs	Supply Voltage readouts from the Pentium/PRO power supplies that indicate the operating voltage or the processor (e.g. 1.5V to 2.9V). The values are read in the VID/Fan Divisor Register and the VID4 Register.
TOTAL PINS		**24**		

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Positive Supply Voltage (V^+)	+6.0V
Voltage on Any Input or Output Pin:	
+12Vin, $\overline{T\_CRIT\_A}$	−0.3V to +15V
A0, A1, DACOut	−0.3V to (V^++ 0.3V)
+2.5Vin, +3.3Vin	(Note 3)
All other pins	−0.3V to +6V
Input Current at any Pin (Note 4)	±5 mA
Package Input Current (Note 4)	±20 mA
Maximum Junction Temperature (T_J max)	150˚C
ESD Susceptibility (Note 6)	
Human Body Model	2000V
Machine Model	200V
Soldering Information	
MTC Package (Note 7) :	
Vapor Phase (60 seconds)	215˚C
Infrared (15 seconds)	235˚C
Storage Temperature	−65˚C to +150˚C

Operating Ratings (Notes 1, 2)

Operating Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
LM81	$-40˚C \le T_A \le +125˚C$
Specified Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
LM81	$-40˚C \le T_A \le +125˚C$
Junction to Ambient Thermal Resistance (θ_{JA} (Note 5))	
NS Package Number: MTC24B	95˚C/W
Supply Voltage (V^+)	+2.8V to +3.8V
V_{IN} Voltage Range:	
+12Vin	−0.05V to +15V
+5Vin	−0.05V to +6.8V
+3.3Vin	−0.05V to +4.6V
+2.5Vin	−0.05V to +3.6V
VID0 - VID4, Vccp, FAN1-FAN2	−0.05V to +6.0V
All other inputs	−0.05V to (V^+ + 0.05V)

DC Electrical Characteristics

The following specifications apply for $+2.8V_{DC} \le V^+ \le +3.8V_{DC}$, R_S = 500Ω, unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J$ = 25˚C. (Note 8)

Symbol	Parameter		Conditions	Typical (Note 9)	Limits LM81BIM (Note 10)	Limits LM81CIM (Note 10)	Units (Limits)
POWER SUPPLY CHARACTERISTICS							
I^+	Supply Current		Interface Inactive	0.4	**1.4**	**0.9**	mA (max)
TEMPERATURE-TO-DIGITAL CONVERTER CHARACTERISTICS							
	Error		$-40˚C \le T_A \le +125˚C$		**±3**	**±3**	˚C (max)
	Resolution	9-bit mode 12-bit mode			**0.5** **0.0625**	**0.5** **0.0625**	˚C (min) ˚C (min)
LM81 ANALOG-TO-DIGITAL CONVERTER CHARACTERISTICS							
	Resolution			8			bits
TUE	Total Unadjusted Error	+2.5Vin, +3.3Vin, +5Vin	(Notes 11, 12)		**+1.2** **−1.2**	**+2** **+0.8**	% (max) % (min)
		Vccp1, Vccp2	(Note 11)		**+1.2** **−1.2**	**+2.4** **0**	% (max) % (min)
		+12Vin	(Notes 11, 12)		**+1.2** **−1.2**	**+3.1** **+1.2**	% (max) % (min)
DNL	Differential Non-Linearity				**±1**	**±1**	LSB (max)
PSS	Power Supply Sensitivity			±0.4			%/V
t_C	Total Monitoring Cycle Time		(Note 13) 9-bit Temp Resolution 12-bit Temp Resolution	0.4	 **0.82** **1.2**	 **0.82** **1.2**	sec sec (max) sec (max)
ADC INPUT CHARACTERISTICS							
	Input Resistance (All analog inputs except Vccp1 and Vccp2)			115	**90**	**90**	kΩ (min)
	Vccp1 and Vccp2 DC Input Current			±1			µA

DC Electrical Characteristics (Continued)

The following specifications apply for $+2.8V_{DC} \le V^+ \le +3.8V_{DC}$, $R_S = 500\Omega$, unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25^\circ C$. (Note 8)

Symbol	Parameter	Conditions	Typical (Note 9)	Limits LM81BIM (Note 10)	Limits LM81CIM (Note 10)	Units (Limits)
DAC CHARACTERISTICS						
	Resolution		8			Bits
	DAC Error	$V^+ = 3.3V$		±5 ±62.5 **±10** **±125**	±5 ±62.5	% (max) mV (max) % (max) mV (max)
	DAC Error Temperature Sensitivity		100		**100**	ppm/°C (max)
	DAC Error Power Supply Sensitivity		0.5		**0.725**	% (max)
R_L	Output Load Resistance	$V_O = 1.25V$		**625**	**625**	Ω (min)
C_L	Output Load Capacitance			**20**	**20**	pF (max)
FAN RPM-TO-DIGITAL CONVERTER						
	Fan RPM Error	$+25^\circ C \le T_A \le +75^\circ C$		**±10**	**±10**	% (max)
		$-10^\circ C \le T_A \le +100^\circ C$		**±15**	**±15**	% (max)
		$-40^\circ C \le T_A \le +125^\circ C$		**±20**	**±20**	% (max)
	Full-scale Count			**255**	**255**	(max)
	FAN1 and FAN2 Nominal Input RPM (See *Section 6.0*)	Divisor = 1, Fan Count = 153 (Note 14)	8800			RPM
		Divisor = 2, Fan Count = 153 (Note 14)	4400			RPM
		Divisor = 3, Fan Count = 153 (Note 14)	2200			RPM
		Divisor = 4, Fan Count = 153 (Note 14)	1100			RPM
	Internal Clock Frequency	$+25^\circ C \le T_A \le +75^\circ C$	22.5	**20.2** **24.8**	**20.2** **24.8**	kHz (min) kHz (max)
		$-10^\circ C \le T_A \le +100^\circ C$	22.5	**19.1** **25.9**	**19.1** **25.9**	kHz (min) kHz (max)
		$-40^\circ C \le T_A \le +125^\circ C$	22.5	**18** **27**	**18** **27**	kHz (min) kHz (max)

DC Electrical Characteristics (Continued)

The following specifications apply for $+2.8V_{DC} \le V^+ \le +3.8V_{DC}$, $R_S = 500\Omega$, unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25^\circ C$. (Note 8)

Symbol	Parameter	Conditions	Typical (Note 9)	Limits LM81BIM (Note 10)	Limits LM81CIM (Note 10)	Units (Limits)
DIGITAL OUTPUTS (NTEST_OUT)						
$V_{OUT(1)}$	Logical “1” Output Voltage	I_{OUT} = ±3.0 mA at V^+ = +2.8V		**2.4**	**2.4**	V (min)
$V_{OUT(0)}$	Logical “0” Output Voltage	I_{OUT} = ±3.0 mA at V^+ = +3.8V		**0.4**	**0.4**	V (max)
OPEN- DRAIN DIGITAL OUTPUTS (SMBData, $\overline{\text{RESET}}$, CI, $\overline{\text{INT}}$, $\overline{\text{T\_CRIT\_A}}$)						
$V_{OUT(0)}$	Logical “0” Output Voltage	I_{OUT} = −3.0 mA		**0.4**	**0.4**	V (min)
I_{OH}	High Level Output Current	$V_{OUT} = V^+$	0.1	**100**	**100**	µA (max)
	$\overline{\text{RESET}}$ and Chassis Intrusion Pulse Width		45	**20**	**20**	ms (min)
DIGITAL INPUTS: VID0–VID4, NTEST_IN, A0/NTEST_OUT, A1, Chassis Intrusion (CI)						
$V_{IN(1)}$	Logical “1” Input Voltage			**2.0**	**2.0**	V (min)
$V_{IN(0)}$	Logical “0” Input Voltage			**0.8**	**0.8**	V (max)
SMBus DIGITAL INPUTS (SMBCLK, SMBData)						
$V_{IN(1)}$	Logical “1” Input Voltage			**2.1**	**1.4**	V (min)
$V_{IN(0)}$	Logical “0” Input Voltage			**0.8**	**0.6**	V (max)
Tach Pulse Logic Inputs (FAN1, FAN2)						
$V_{IN(1)}$	Logical “1” Input Voltage			**0.7 x V^+**	**0.7 x V^+**	V (min)
$V_{IN(0)}$	Logical “0” Input Voltage			**0.3 x V^+**	**0.3 x V^+**	V (max)
ALL DIGITAL INPUTS						
$I_{IN(1)}$	Logical “1” Input Current	$V_{IN} = V^+$	−0.005	**−1**	**−1**	µA (min)
$I_{IN(0)}$	Logical “0” Input Current	V_{IN} = 0 V_{DC}	0.005	**1**	**1**	µA (max)
C_{IN}	Digital Input Capacitance		20			pF

AC Electrical Characteristics

The following specifications apply for +2.8V_{DC} ≤ V^+ ≤ +3.8V_{DC} on SMBCLK and SMBData, unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25^\circ C$. (Note 15)

Symbol	Parameter	Conditions	Typical (Note 9)	Limits (Note 10)	Units (Limits)
SERIAL BUS TIMING CHARACTERISTICS					
t_1	SMBCLK (Clock) Period			**2.5**	µs (min)
t_{rise}	SMBCLK and SMBData Rise Time			**1**	µs (max)
t_{fall}	SMBCLK and SMBData Fall Time			**300**	ns (max)
t_2	Data In Setup Time to SMBCLK High			**100**	ns (min)
t_3	Data Out Stable After SMBCLK Low			**0**	ns (min)
t_4	SMBData Low Setup Time to SMBCLK Low (start)			**100**	ns (min)
t_5	SMBData High Hold Time After SMBCLK High (stop)			**100**	ns (min)
$t_{TIMEOUT}$	SMBData or SMBCLK low time required to reset the Serial Bus Interface to the Idle State		31	**25** **35**	ms ms (min) ms (max)
C_L	Capacitive Load on SMBCLK and SMBData			**400**	pF (max)

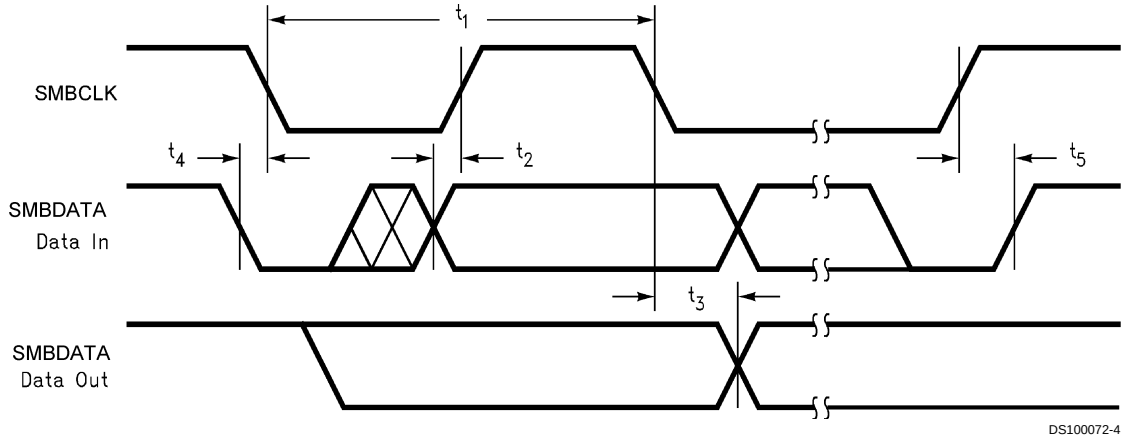


FIGURE 1. Serial Bus Timing Diagram

AC Electrical Characteristics (Continued)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: The Absolute maximum input range for :

+2.5Vin - −0.3V to (1.4 x V^+ + 0.42V or 6V, whichever is smaller

+3.3Vin - −0.3V to (1.8 x V^+ + 0.55V or 6V, whichever is smaller.

Note 4: When the input voltage (V_{IN}) at any pin exceeds the power supplies (V_{IN} < GND or V_{IN} > V^+), the current at that pin should be limited to 5 mA. The 20 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 5 mA to four.

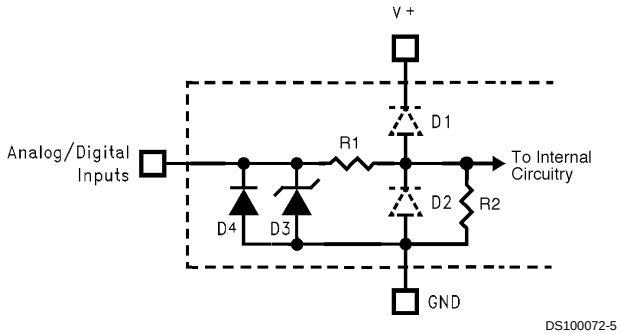
Note 5: The maximum power dissipation must be derated at elevated temperatures and is dictated by $T_J$max, θ_{JA} and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_J \text{ max} - T_A)/\theta_{JA}$.

Note 6: The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin.

Note 7: See the section titled “Surface Mount” found in any post 1986 National Semiconductor Linear Data Book for other methods of soldering surface mount devices.

Note 8: Parasitics and or ESD protection circuitry are shown in the figure below for the LM81's pins. The nominal breakdown voltage of the zener D3 is 6.5V. Care should be taken not to forward bias the parasitic diode, D1, present on pins: A0/NTEST_OUT, A1 and DACOut/NTEST_IN. Doing so by more than 50 mV may corrupt a temperature or voltage measurement.

Pin Name	D1	D2	D3	D4	R1	R2	Pin Name	D1	D2	D3	D4	R1	R2
$\overline{\text{INT}}$		x	x		0	∞	+12Vin	x	x		x	R1+R2 ~120k	
CI		x	x		0	∞	Vccp1, Vccp2		x	x		0	∞
FAN1–FAN2			x		0	∞	+5Vin	x	x		x	R1+R2 ~120k	
SMBCLK			x		0	∞	+3.3Vin, +2.5Vin	x	x	x		R1+R2 ~120k	
SMBData		x	x		0	∞	$\overline{\text{T\_CRIT\_A}}$		x		x	0	∞
$\overline{\text{RESET}}$		x	x		0	∞	VID4–VID0		x	x		0	∞
A0/NTEST_OUT	x	x	x		0	∞	DACOut/NTEST_IN	x	x	x		0	∞
A1	x	x	x		0	∞							



An x indicates that the diode exists.

FIGURE 2. ESD Protection Input Structure

Note 9: Typicals are at $T_J = T_A = 25^\circ C$ and represent most likely parametric norm.

Note 10: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 11: TUE (Total Unadjusted Error) includes Offset, Gain and Linearity errors of the ADC.

Note 12: Guaranteed at 3/4 scale ±15%.

Note 13: Total Monitoring Cycle Time includes temperature conversion, 6 analog input voltage conversions and 2 tachometer readings. Each 9-bit temperature and 8-bit input voltage conversion takes 50 ms typical and 56 ms maximum. Twelve bit temperature conversion takes 400 ms. Fan tachometer readings take 20 ms typical, at 4400 rpm, and 200 ms maximum.

Note 14: The total fan count is based on 2 pulses per revolution of the fan tachometer output.

Note 15: Timing specifications are tested at the specified logic levels, V_{IL} for a falling edge and V_{IH} for a rising edge.

Test Circuit

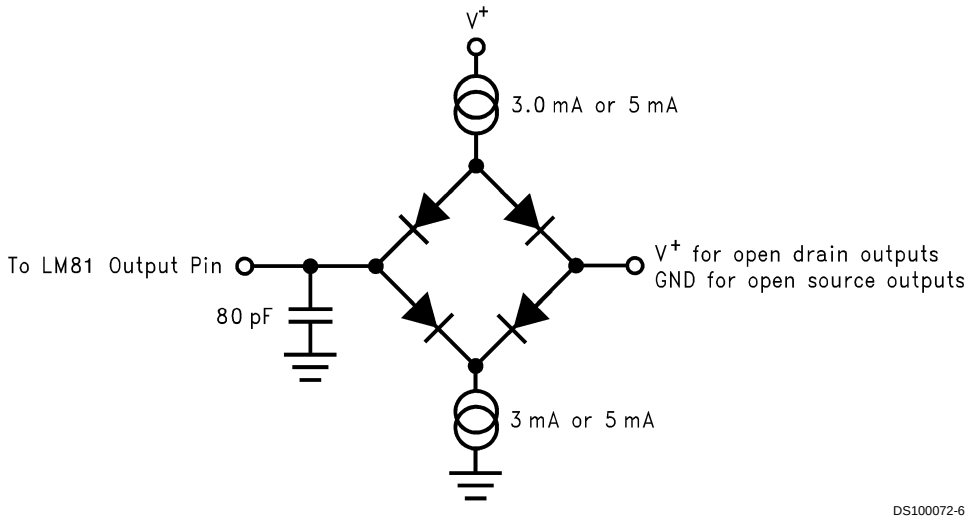


FIGURE 3. Digital Output Load Test Circuitry

Functional Description

1.0 GENERAL DESCRIPTION

The LM81 provides 6 analog inputs, a temperature sensor, a Delta-Sigma ADC (Analog-to-Digital Converter), a DAC output, 2 fan speed counters, WATCHDOG registers, and a variety of inputs and outputs on a single chip. A two wire Serial Bus interface is included. The LM81 performs power supply, temperature, fan control and fan monitoring for personal computers.

The analog inputs are useful for monitoring several power supplies present in a typical computer. The LM81 includes internal resistor dividers that scale and/or offset external Vccp, +2.5V, +3.3V, +5.0V and +12V power supply voltages to a 3/4 scale nominal ADC output. The LM81 ADC then continuously converts the scaled inputs to 8-bit digital words. Measurement of negative voltages (such as -5V and -12V power supplies) can be accommodated with an external resistor divider applied to the Vccp2 input. Temperature is converted to a 9-bit or 12-bit two's-complement digital word with a 0.5˚C LSB or 0.0625˚C LSB, respectively.

Fan inputs measure the period of tachometer pulses from the fans, providing a higher count for lower fan speeds. The fan inputs are Schmitt-Trigger digital inputs with an acceptable range of 0V to V^+ and a transition level of approximately $V^+/2$. Full scale fan counts are 255 (8-bit counter) and this represents a stopped or very slow fan. Nominal speeds, based on a count of 153, are programmable from 1100 to 8800 RPM on FAN1 and FAN2. Schmitt-Trigger input circuitry is included to accommodate slow rise and fall times. A 0V to 1.25V DAC output voltage range can be used for control of fan speed.

The LM81 has several internal registers, as shown in *Figure 4*, *Table 1* and *Section 13.0*. These include:

- **Configuration Register:** Provides control and configuration.
- **Interrupt Status Registers:** Two registers to provide status of each WATCHDOG limit or Interrupt event.
- **Interrupt Mask Registers:** Allows masking of individual Interrupt sources, as well as separate masking for each of the two hardware Interrupt outputs.
- **CI Clear Register:** Allows transmitting a 20 ms low pulse on the chassis intrusion pin (CI).
- **VID/Fan Divisor Register:** This register contains the state of the VID0-VID3 input lines and the divisor bits for FAN1 and FAN2 inputs.
- **Serial Bus Address Register:** Contains the Serial Bus address. At power on it assumes the default value of 01011XX binary, and can be altered by the state of A0 and A1.
- **VID4 Register:** Contains the state of the VID4 input.
- **Temperature Configuration Register:** Selects the interrupt mode and contains the 0.5˚C LSB of the temperature reading.
- **Extended Mode Registers:** Enable and control the Extended Mode which includes the LSBs of the 12-bit temperature reading, T_CRIT, and T_{HYST}
- **Value RAM:** The DAC digital input, monitoring results (temperature, voltages, fan counts), WATCHDOG limits, and Company/Stepping IDs are all contained in the Value RAM. The Value RAM consists of a total of 34 bytes, addresses 15h - 3Fh, containing:
  - — byte 1 at address 15h a manufacturers test register
  - — locations 16h - 18h are unassigned and do not have associated registers
  - — byte 2 at address 19h contains the DAC Data Register
  - — locations 1Ah - 1Fh are unassigned and do not have associated registers
  - — the next 10 bytes at addresses 20h -29h contain all of the results, with address 26h reserved
  - — the next 18 bytes at addresses 2Bh-3Ch are the WATCHDOG limits
  - — the last 2 bytes at addresses 3Eh and 3Fh contain the Company ID and Stepping ID numbers, respectively

When the LM81 is started, it cycles through each measurement in sequence, and it continuously loops through the sequence approximately once every 400 ms. Each measured value is compared to values stored in WATCHDOG, or Limit registers. When the measured value violates the programmed limit the LM81 will set a corresponding Interrupt in the Interrupt Status Registers. The hardware Interrupt line $\overline{INT}$ is fully programmable with separate masking of each

Functional Description (Continued)

Interrupt source. In addition, the Configuration Register has a control bit to enable or disable the hardware Interrupt. Another hardware Interrupt line available T_CRIT_A (Critical Temperature Alarm Output) is used to signal a catastrophic overtemperature event. Having a dedicated interrupt for this purpose allows for the fastest possible response time to a thermal runaway event. This output can be enabled by setting bit 4 of Extended Mode Register 1.

The Chassis Intrusion input is designed to accept an active high signal from an external circuit that latches when the case is removed from the computer.

2.0 INTERFACE

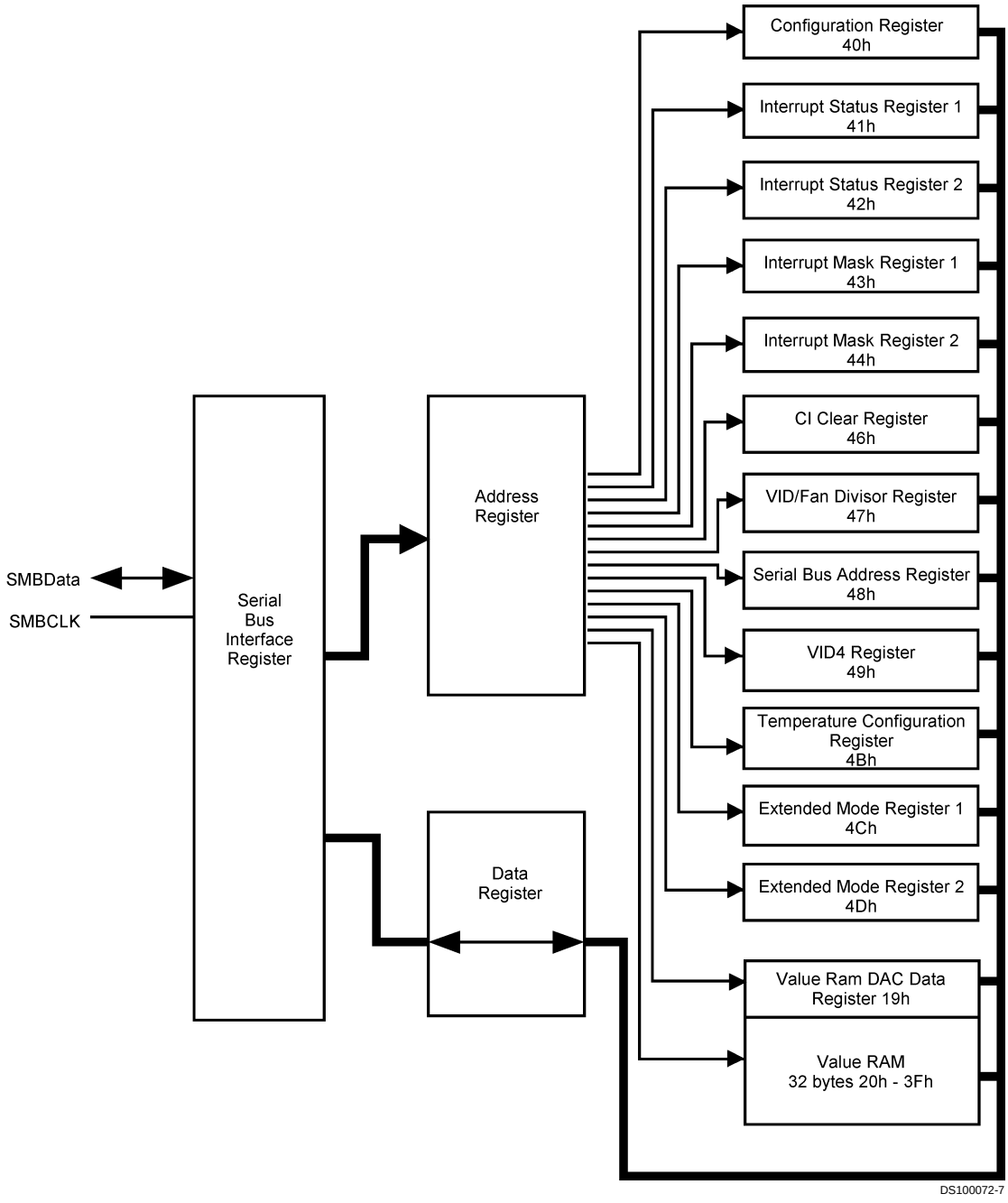


FIGURE 4. LM81 Register Structure

Functional Description (Continued)

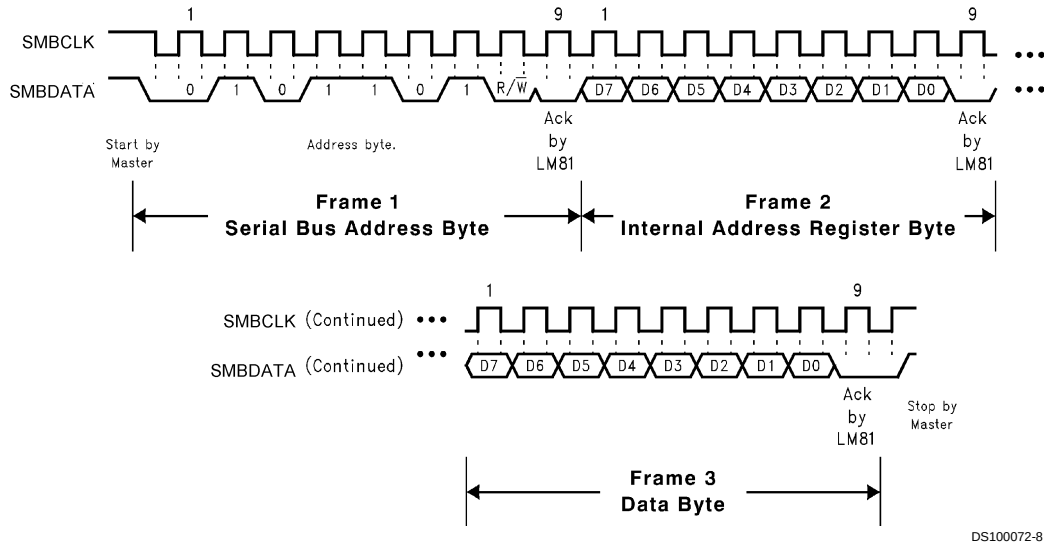
2.1 Internal Registers of the LM81

TABLE 1. The internal registers and their corresponding internal LM81 addresses are as follows:

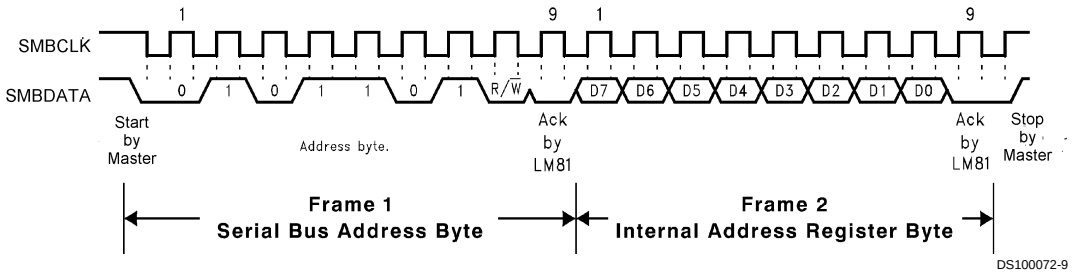
Register	LM81 Internal Hex Address	Power on Value	Notes
Configuration Register	40h	0000 1000	
Interrupt Status Register 1	41h	0000 0000	
Interrupt Status Register 2	42h	0000 0000	
Interrupt Mask Register 1	43h	0000 0000	
Interrupt Mask Register 2	44h	0000 0000	
CI Clear Register	46h	0000 0000	
VID/Fan Divisor Register	47h	0101 XXXX	The upper four bits set the divisor for Fan Counters 1 and 2. The lower four bits reflect the state of the VID0-VID3 inputs.
Serial Bus Address Register	48h	0010 11XX	The lower 2 bits reflect the state of A1 and A0, the Serial Bus address input pins.
VID4 Register	49h	1000 000X	The lower bit reflects the state of VID4 input.
Temperature Configuration Register	4Bh	0000 0001	
Extended Mode Register 1	4Ch	0100 0100	
Extended Mode Register 2	4Dh	0000 0000	
Value RAM DAC Data Register	19h	1111 1111	
Value RAM	20h-3Fh		Contains: monitoring results (temperature, voltages, fan counts), WATCHDOG limits, and Company/Stepping IDs

Functional Description (Continued)

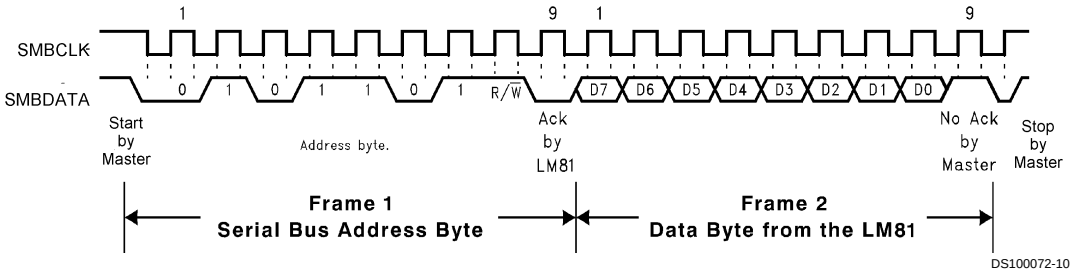
2.2 Serial Bus Interface



(a) Serial Bus Write to the Internal Address Register followed by the Data Byte



(b) Serial Bus Write to the Internal Address Register Only



(c) Serial Bus Read from a Register with the Internal Address Register Preset to Desired Location

FIGURE 5. Serial Bus Timing

The Serial Bus control lines consist of the SMBData (serial data), SMBCLK (serial clock) and A0-A1 (address) pins. The LM81 can operate only as a slave. The SMBCLK line only controls the serial interface, all other clock functions within LM81 such as the ADC and fan counters are done with a separate asynchronous internal clock.

When using the Serial Bus Interface a write will always consist of the LM81 Serial Bus Interface Address byte, followed by the Internal Address Register byte, then the data byte. There are two cases for a read:

1. If the Internal Address Register is known to already be at the desired Address, simply read the LM81 with the Serial Bus Interface Address byte, followed by the data byte read from the LM81.
2. If the Internal Address Register value is unknown, or if it is not the desired value, write to the LM81 with the Serial Bus Interface Address byte, followed by the Internal Address Register byte. Then restart the Serial Communication with a Read consisting of the Serial Bus Interface Address byte, followed by the data byte read from the LM81.

The default Serial Bus address of the LM81 is set to 010 11(A1)(A0). All bits, except for A0 and A1, can be changed by writing to the Serial Bus address register. A0 and A1 will always reflect the state of the A0 and A1 input pins.

All of these communications are depicted in the Serial Bus Interface Timing Diagrams as shown in *Figure 5*.

Serial Bus Timeout can be initiated by holding the SMBCLK and/or SMBData lines low for greater than $t_{TIMEOUT}$ (35 ms max). Serial Bus Timeout resets the serial bus interface circuitry to the idle state and readies the LM81 for a new serial bus communication.

Functional Description (Continued)

3.0 USING THE LM81

3.1 Power On

When power is first applied, the LM81 performs a "power on reset" on several of its registers. The power on condition of the LM81's registers in shown in *Table 1* Registers whose power on values are not shown have power on conditions that are indeterminate (this includes the value RAM ,exclusive of the DAC data, and WATCHDOG limits). When power is first applied the ADC is inactive. In most applications, usually the first action after power on is usually to write WATCHDOG limits into the Value RAM. Register values can be returned to their default values after power is applied to the LM81 by taking $\overline{\text{RESET}}$ low for at least 50 ns.

3.2 Resets

Configuration Register INITIALIZATION accomplishes the same function as power on reset on most registers. The Value RAM conversion results, and Value RAM WATCHDOG limits are not Reset and will be indeterminate immediately after power on. If the Value RAM contains valid conversion results and/or Value RAM WATCHDOG limits have been previously set, they will not be affected by a Configuration Register INITIALIZATION. Power on reset, or Configuration Register INITIALIZATION, clear or initialize the following registers (the initialized values are shown on *Table 1*:

- Configuration Register
- Interrupt Status Register 1
- Interrupt Status Register 2
- $\overline{\text{INT}}$ Mask Register 1
- $\overline{\text{INT}}$ Mask Register 2
- VID/Fan Divisor Register
- Serial Bus Address Register (Power on reset only, not reset by Configuration Register INITIALIZATION)
- VID4 Register
- Temperature Configuration Register
- Extended Mode Register 1
- Extended Mode Register 2

Configuration Register INITIALIZATION is accomplished by setting Bit 7 of the Configuration Register high. This bit automatically clears after being set.

3.3 Using the Configuration Register

The Configuration Register controls the LM81 operation. At power on, the ADC is stopped and INT_Clear is asserted, clearing the $\overline{\text{INT}}$ hardwire output. The Configuration Register starts and stops the LM81, enables and disables interrupt output, and provides the Reset function described in *Section 3.2*.

Bit 0 of the Configuration Register controls the monitoring loop of the LM81. Setting Bit 0 low stops the LM81 monitoring loop and puts the LM81 in shutdown mode, reducing power consumption. Serial Bus communication can take place with any register in the LM81 although activity on the SMBData and SMBCLK lines will increase shutdown current, up to as much as maximum rated supply current, while the activity takes place. Taking Bit 0 high starts the monitoring loop, described in more detail subsequently.

Bit 1 of the Configuration Register enables the $\overline{\text{INT}}$ Interrupt hardwire output when this bit is taken high.

Bit 3 of the Configuration Register clears the $\overline{\text{INT}}$ output when set high, without affecting the contents of the Interrupt Status Registers. The LM81 will stop monitoring. It will resume upon clearing of this bit.

Bit 4 of the Configuration Register provides an active low 20 ms pulse at the $\overline{\text{RESET}}$ output when set high.

The CI_Clear provides an active low 20 ms pulse at the $\overline{\text{CI}}$ output pin when set high. This is intended for resetting the Chassis Intrusion circuitry.

The INITIALIZATION bit resets the internal registers of the LM81 as described in *Section 3.2*.

3.4 Starting Conversions

The monitoring function (Analog inputs, temperature, and fan speeds) in the LM81 is started by writing to the Configuration Register and setting INT_Clear (Bit 3), low, and Start (bit 0), high. The LM81 then performs a "round-robin" monitoring of all analog inputs, temperature, and fan speed inputs approximately once every 400 ms. The sequence of items being monitored corresponds to locations in the Value RAM and is:

1. Temperature
2. Vccp2
3. +12Vin
4. +5Vin
5. +3.3Vin
6. Vccp1
7. +2.5Vin
8. Fan 1
9. Fan 2

DACOut immediately changes after the DAC Data Register in the Value RAM has been updated. For a zero to full scale transition DACOut will typically settle within 100 µsec of the stop by master in the write to the DAC Data Register Serial Bus transaction. The DAC Data Register is not reset by the INITIALIZATION bit found in the Configuration Register.

Functional Description (Continued)

3.5 Reading Conversion Results

The conversion results are available in the Value RAM. Conversions can be read at any time and will provide the result of the last conversion. Because the ADC stops, and starts a new conversion whenever it is read, reads of any single value should not be done more often than once every 56 ms. When reading all values, allow at least 0.82 seconds between reading groups of values. Reading more frequently than once every 0.82 seconds can also prevent complete updates of Interrupt Status Registers and Interrupt Output's.

A typical sequence of events upon power on of the LM81 would consist of:

1. Set WATCHDOG Limits
2. Set Interrupt Masks
3. Start the LM81 monitoring process

3.6 Digital Communication Noise Considerations

The SMBData and SMBCLK logic input levels were changed in the SMBus 1.1 specification. SMBus 1.0 levels were set to 1.4V for a logic high and 0.6V for a logic low. In SMBus 1.1 they were changed to 2.1V for a logic high and 0.8V for a logic low. Devices that meet the SMBus 1.0 specification have issues in that the logic levels did not allow for enough noise immunity for some pcb layouts. This has changed with the SMBus 1.1 specification because the higher logic levels allow for more hysteresis in the schmitt trigger inputs stages and thus more noise immunity. It may be required in some cases to add a series 5.1kΩ resistor connected at the SMBCLK pin of the LM81C to improve its noise immunity. In addition to meeting the SMBus 1.1 logic levels, the LM81B has a built-in glitch filter that rejects 100MHz or greater to make it impervious to noise.

4.0 ANALOG INPUTS

All analog input voltages are digitized to 8-bits of resolution. All analog inputs, except for Vccp1 and Vccp2, include internal resistor attenuators. The theoretical LSB size, theoretical voltage input required for an ADC reading of 192 (3/4 scale) and 255 (full scale) for each analog input is detailed in the table below:

Input	LSB size	Vin for 192	Vin for 255
2.5 Vin	13 mV	2.5V	3.320V
3.3 Vin	17.2 mV	3.3V	4.383V
5 Vin	26 mV	5V	6.641V
12 Vin	62.5 mV	12V	15.93V
Vccp1, Vccp2	14.1 mV	2.7V	3.586V

Thus monitoring power supplies within a system can be easily accomplished by tying the Vccp, +2.5 Vin, +3.3 Vin, +5 Vin and +12 Vin analog inputs to the corresponding system supply. A digital reading can be converted to a voltage by simply multiplying the decimal value of the reading by the LSB size.

For inputs with attenuators the input impedance is greater than 90 kΩ. Vccp inputs do not have resistor attenuators and are are directly tied to the ADC, therefore having a much larger input impedance.

A negative power supply voltage can be applied to a Vccp input through a resistor divider referenced to a known positive DC voltage as show in *Figure 6.* The resistor values shown in the table below for the circuit of *Figure 6* will provide approximately 1.25V at the Vccp analog inputs of the LM81 for a nominal reading of 89.

Voltage Measurements (V_S)	R2	R1	V^+	Voltage at Analog Inputs (ADC code 89)
−12V	40 kΩ	141 kΩ	+5V	+1.25V
−5V	40 kΩ	66.7 kΩ	+5V	+1.25V

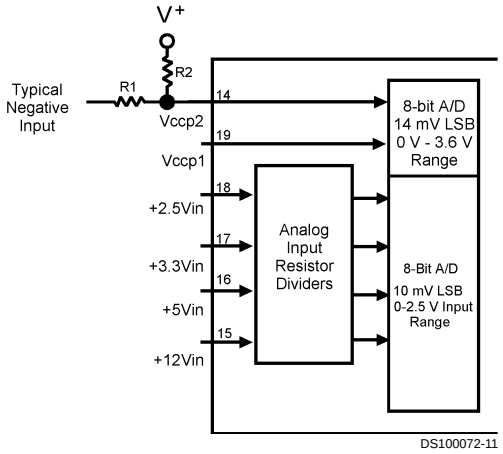


FIGURE 6. Input Examples. Resistor values shown in table provide approximately 1.25V at the Vccp inputs.

The resistors were selected by setting R2 = 40 kΩ and then calculating R2 using the following equation:

$$R1 = [(1.25V - V_S) \div (V^+ - 1.25V)] \times 40\ k\Omega$$

The maximum R1 can be is restricted by the DC input current of a Vccp input.

Inputs with internal resistor dividers (+2.5 Vin, +3.3 Vin or +5 Vin, +12 Vin) can have voltage applied that exceeds the power supply up to: 3.6V for +2.5 Vin, 4.6V for +3.3 Vin, 6.8V for +5 Vin, and 15V for +12 Vin. The Vccp inputs have a parasitic diode to the positive supply, so care should be taken not to forward bias this diode. All analog inputs have internal diodes that clamp the input voltage when going below ground thus limiting the negative analog input voltage range to −50 mV. Violating the analog input voltage range of any analog input has no detrimental effect on the other analog inputs. External resistors should be included to limit input currents to the values given in the ABSOLUTE MAXIMUM RATINGS for Input Current At Any Pin whenever exceeding the analog input voltage range, even on an un-powered LM81. Inputs with external attenuator networks will usually meet these requirements. If it is possible for inputs without attenuators (such as Vccp1 and Vccp2) to be turned on while LM81 is powered off, additional resistors of about 10 kΩ should be added in series with the inputs to limit the input current.

4.1 Analog Input Interrupts

A WATCHDOG window comparison on the analog inputs can activate the $\overline{INT}$ interrupt output. A converted input voltage that is above its respective HIGH limit or less than or

Functional Description (Continued)

equal to its LOW limit will cause a flag to be set in its Interrupt Status Register. This flag will activate the $\overline{INT}$ output when its mask bit is set low. Mask bits are found in the Interrupt Mask Registers.

5.0 LAYOUT AND GROUNDING

A separate, low-impedance ground plane for analog ground, which provides a ground point for both GND pins, voltage dividers and other analog components, will provide best performance but is not mandatory. Analog components such as voltage dividers should be located physically as close as possible to the LM81.

The power supply bypass, the parallel combination of 10 µF (electrolytic or tantalum) and 0.1 µF (ceramic) bypass capacitors connected between pin 12 and ground, should also be located as close as possible to the LM81.

6.0 FAN INPUTS

The FAN1 and FAN2 inputs accept signals from fans equipped with tachometer outputs. These are logic-level inputs with an approximate threshold of $V^+/2$. Signal conditioning in the LM81 accommodates the slow rise and fall times typical of fan tachometer outputs. The maximum input signal range is 0 to V^+. In the event these inputs are supplied from fan outputs which exceed 0 to V^+, either resistive division or diode clamping must be included to keep inputs within an acceptable range, as shown in *Figure 7*. R2 is selected so that it does not develop excessive voltage due to input leakage. R1 is selected based on R2 to provide a minimum input of 2V and a maximum of V^+. R1 should be as low as possible to provide the maximum possible input up to V^+ for best noise immunity. Alternatively, use a shunt reference or zener diode to clamp the input level.

If fans can be powered while the power to the LM81 is off, the LM81 inputs will provide diode clamping. Limit input current to the Input Current at Any Pin specification shown in the ABSOLUTE MAXIMUM RATINGS section. In most cases, open collector outputs with pull-up resistors inherently limit this current. If this maximum current could be exceeded, either a larger pull up resistor should be used or resistors connected in series with the fan inputs.

The Fan Inputs gate an internal 22.5 kHz oscillator for one period of the Fan signal into an 8-bit counter (maximum count = 255). The default divisor, located in the VID/Fan Divisor Register, is set to 2 (choices are 1, 2, 4, and 8) providing a nominal count of 153 for a 4400 rpm fan with two pulses per revolution. Typical practice is to consider 70% of normal RPM a fan failure, at which point the count will be 219.

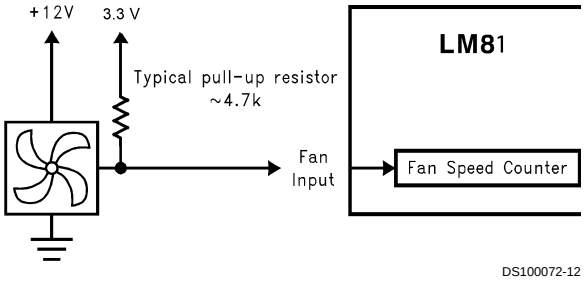
Determine the fan count according to:

$$\text{Count} = \frac{1.35 \times 10^6}{\text{RPM} \times \text{Divisor}}$$

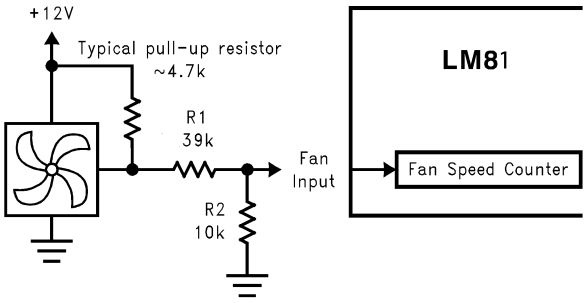
Note that Fan 1 and Fan 2 Divisors are programmable via the VID/Fan Divisor Register.

Fan tachometer outputs that provide one pulse per revolution should use a divisor setting twice that of outputs that provide two pulses per revolution. For example, a 4400 RPM fan that provides one pulse per revolution should have the divisor set to 4 such that the nominal counter output is 153.

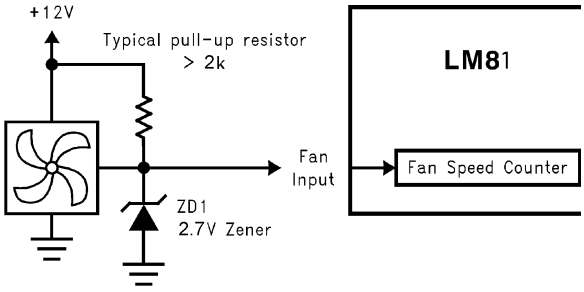
Functional Description (Continued)



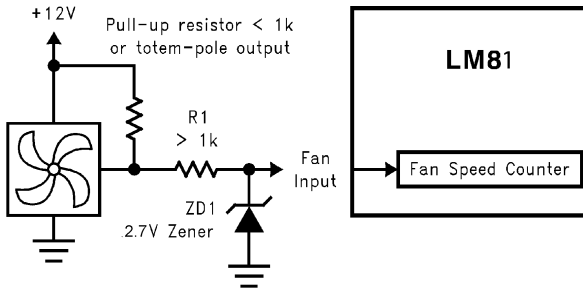
(a) Fan with Tach Pull-Up to +5V



(b) Fan with Tach Pull-Up to +12V, or Totem-Pole Output and Resistor Attenuator



(c) Fan with Tach Pull-Up to +12V and Diode Clamp



(d) Fan with Strong Tach Pull-Up or Totem Pole Output and Diode Clamp

FIGURE 7. Alternatives for Fan Inputs

Counts are based on 2 pulses per revolution tachometer outputs.

RPM	Time per Revolution	Counts for "Divide by 2" (Default) in Decimal	Comments
4400	13.64 ms	153 counts	Typical RPM
3080	19.48 ms	219 counts	70% RPM
2640	22.73 ms	255 counts (maximum counts)	60% RPM

Mode Select	Nominal RPM	Time per Revolution	Counts for the Given Speed in Decimal	70% RPM	Time per Revolution for 70% RPM
Divide by 1	8800	6.82 ms	153	6160	9.74 ms
Divide by 2	4400	13.64 ms	153	3080	19.48 ms
Divide by 4	2200	27.27 ms	153	1540	38.96 ms
Divide by 8	1100	54.54 ms	153	770	77.92 ms

$$\text{Count} = \frac{1.35 \times 10^6}{\text{RPM} \times \text{Divisor}}$$

Functional Description (Continued)

7.0 DAC OUTPUT

The LM81 provides an 8-bit DAC (Digital-to-Analog Converter) with an output range of 0 to 1.25 volts (4.88 mV LSB). This DAC can be used in any way, but in most applications of the LM81 the DAC will be used for fan control. Typically the DAC output would be amplified to provide the up to 12 volt drive required by the fan. At power-on the DAC provides full output, insuring that full fan speed is the default condition. Care should be taken such that the analog circuitry tied to this pin does not drive this pin above 2.5V. Doing so will place the LM81 in NAND tree test mode which will make all pins inputs, thus disabling any response from the LM81.

Fans do not start reliably at reduced voltages, so operation at a reduced voltage should be preceded by a brief (typically 1 second) excursion to full operating voltage, then reduce the voltage. Most fans do not operate at all below 5 to 7 volts. At those lower voltages the fan will simply consume current, dissipate power, and not operate and such conditions should be avoided.

The output of the amplifier can be configured to provide a high or low side pass transistor. A high side pass transistor simplifies the coupling of tachometer outputs to the tachometer inputs of the LM81 since the fan remains grounded. Low side drive will require AC coupling along with clamping at the LM81 input to prevent negative excursions.

A typical circuit for fan drive is shown in *Figure 8*. R4 is used when a negative power supply is available to eliminate offset in the amplifier and provide a 0 to 11.5 volt output (actually 12 volts less saturation). Omitting R4 will create a “dead zone” between approximately 0 to 6 volts output (a potentially unusable region anyway). In many applications protecting the pass transistor Q2 from faults such as a shorted fan can be accomplished by taking advantage of the current limit already existing on the 12 volt supply. Q2 will have to be heat-sunk accordingly. Otherwise, use the suggested current limit circuit as shown.

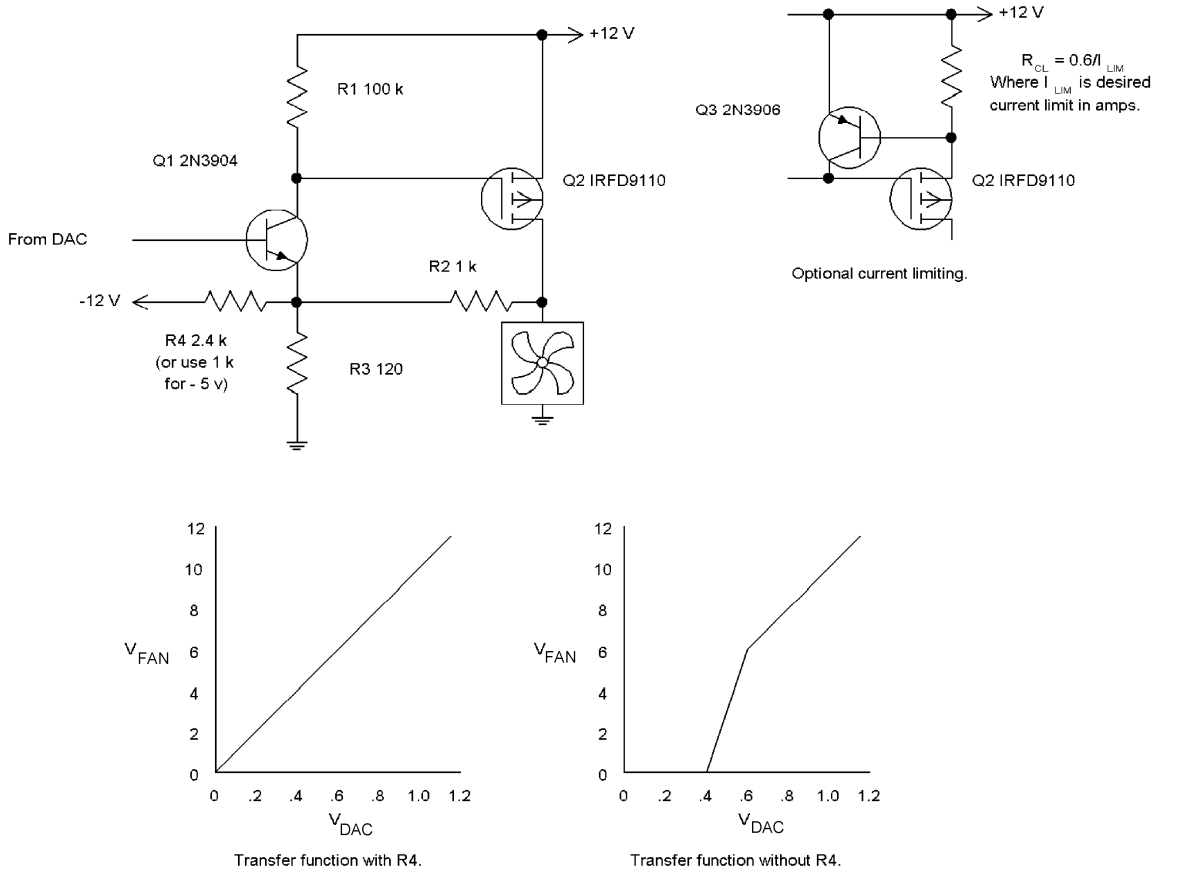
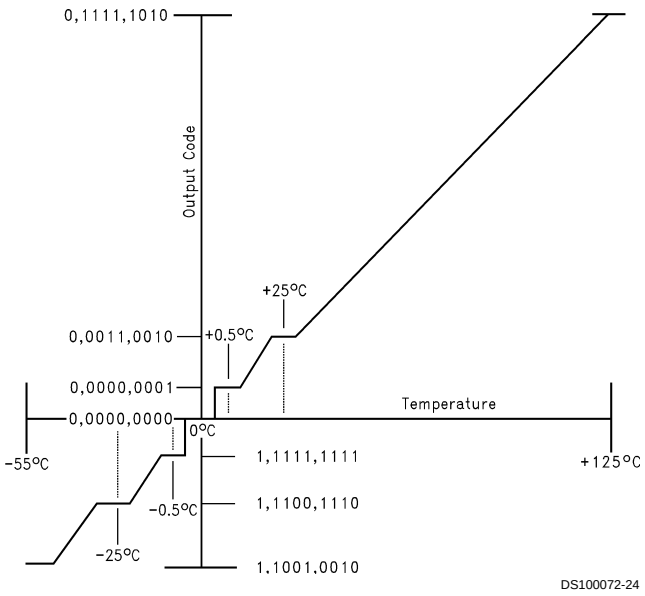


FIGURE 8. Amplifier circuit for connection between DAC output and fan.

Functional Description (Continued)

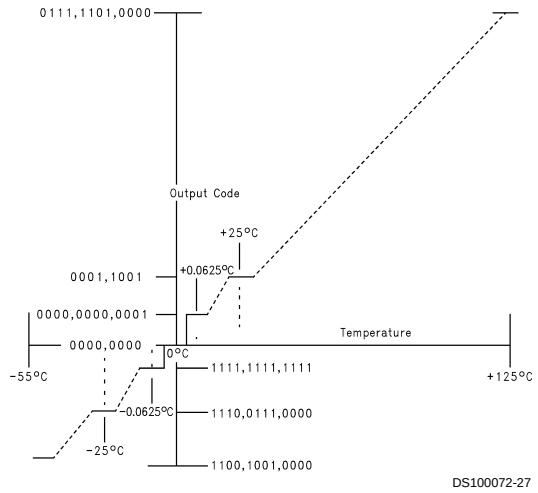
8.0 TEMPERATURE MEASUREMENT SYSTEM

The LM81 temperature sensor and ADC produce 9-bit or 12-bit two's-complement temperature data. A digital comparator compares the temperature data to the user-programmable High, Low, Critical setpoints and Hysteresis values.



(Non-Linear Scale for Clarity)

FIGURE 9. 9-bit Temperature-to-Digital Transfer Function



(Non-Linear Scale for Clarity)

FIGURE 10. 12-bit Temperature-to-Digital Transfer Function

8.1 Temperature Data Format

Temperature data can be read from the Temperature, T_{HIGH} setpoint, T_{HIHYST} setpoint, T_{LOW} setpoint, T_C setpoint and T_{HYST} Offset registers; and written to the T_{HIGH} setpoint, T_{HIHYST}, T_{LOW} setpoint, T_CRIT setpoint and T_{HYST} offset registers. T_{HIGH} setpoint, T_{LOW} setpoint, T_CRIT setpoint temperature data is represented by an 8-bit, two's complement word with an LSB (Least Significant Bit) equal to 1˚C:

Temperature	Digital Output	
	Binary	Hex
+125˚C	0111 1101	7Dh
+25˚C	0001 1001	19h
+1.0˚C	0000 0001	01h
+0˚C	0000 0000	00h
−1.0˚C	1111 1111	FFh
−25˚C	1110 0111	E7h
−40˚C	1101 1000	D8h

By default Temperature Register data is represented by a 9-bit two's complement digital word with the LSB having a resolution of 0.5˚C:

Temperature	Digital Output	
	Binary	Hex
+125˚C	0 1111 1010	0 FAh
+25˚C	0 0011 0010	0 32h
+1.5˚C	0 0000 0011	0 03h
+0˚C	0 0000 0000	0 00h
−0.5˚C	1 1111 1111	1 FFh
−25˚C	1 1100 1110	1 CEh
−40˚C	1 1011 0000	1 B0h

In the extended mode temperature Register data can also be represented by a 12-bit two's complement digital word with an LSB of 0.0625˚C:

Temperature	Digital Output	
	Binary	Hex
+125˚C	0111 1100 0000	7 D0h
+25˚C	0001 1001 0000	1 90h
+1.0˚C	0000 0001 0000	0 10h
+0.0625˚C	0000 0000 0001	0 01h
0˚C	0000 0000 0000	0 00h
−0.0625˚C	1111 1111 1111	F FFh
−1.0˚C	1111 1111 0000	F F0h
−25˚C	1110 0111 0000	E 70h
−40˚C	1101 1000 0000	D 80h

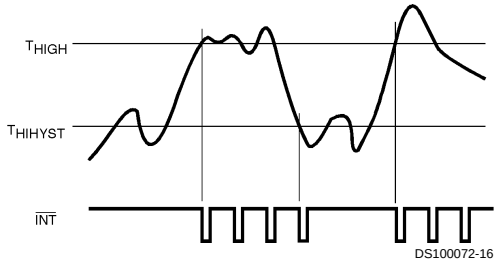
T_{HYST} Offset temperature data is represented by a 3-bit word with an LSB (Least Significant Bit) equal to 1˚C.

Functional Description (Continued)

8.2 Temperature Interrupts

$\overline{INT}$ and $\overline{T\_CRIT\_A}$ outputs are provided for temperature interrupt. Temperature interrupts have a normal and an extended option of operation. Each option has three different modes of operation: Repetitive Interrupt, One-Time Interrupt and Comparator.

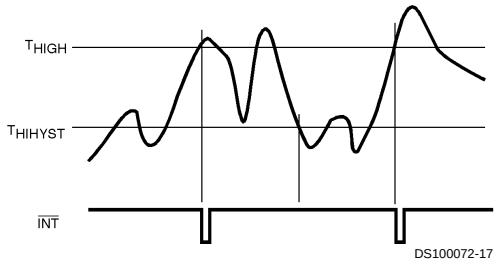
Normal Repetitive Interrupt Mode is shown in *Figure 11* and operates in the following way: $\overline{T\_CRIT\_A}$ is disabled. Exceeding T_{HIGH} causes an interrupt that will remain active indefinitely until reset by reading Interrupt Status Register 1. Once reset if the temperature remains above the T_{HIHYST} setpoint the interrupt will again be activated at the completion of another conversion cycle. If temperature is less than or equal to T_{HIHYST} the interrupt will not be activated.



***Note:** Interrupt resets occur only when interrupt Status Register 1 is read.

FIGURE 11. Normal Repetitive Interrupt Response Diagram

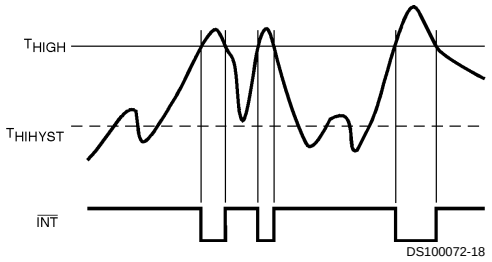
Normal One-Time Interrupt Mode is shown in *Figure 12* and operates in the following way: $\overline{T\_CRIT\_A}$ is disabled. Exceeding T_{HIGH} causes an interrupt that will remain active indefinitely until reset by reading Interrupt Status Register 1. Another interrupt will not occur until the temperature drops to less than or equal to T_{HIHYST} and then exceeds T_{HIGH} during a subsequent conversion. After power up this mode is selected as default.



***Note:** Interrupt resets occur only when interrupt Status Register 1 is read.

FIGURE 12. One-Time Interrupt Response Diagram

Normal Comparator Mode is shown in *Figure 13* and operates in the following way: $\overline{T\_CRIT\_A}$ is disabled. Exceeding T_{HIGH} causes an interrupt that will remain activated until the temperature is less than or equal to T_{HIGH}. T_{LOW} is disabled.

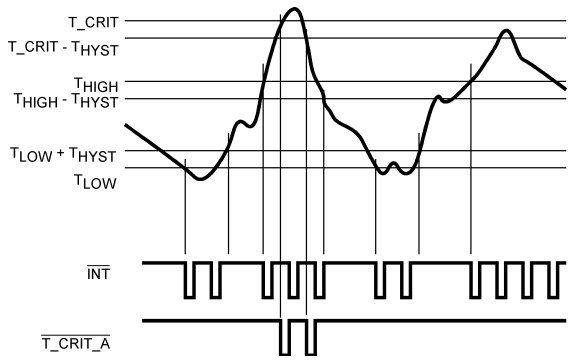


***Note:** Interrupt resets occur only when interrupt Status Register 1 is read.

FIGURE 13. Normal Comparator Mode

Functional Description (Continued)

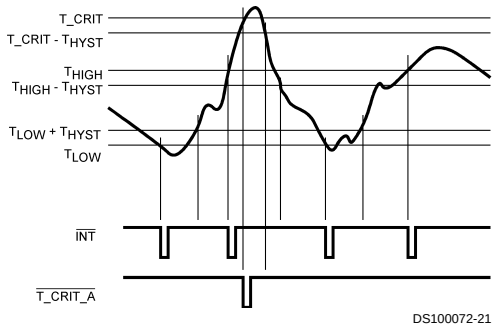
Extended Repetitive Interrupt Mode is shown in *Figure 14* and operates in the following way: Once activated, all interrupts remain activated until reset by a read of the Interrupt Status Register 1. Once activated all $\overline{\text{T\_CRIT\_A}}$ interrupts remain activated until reset by a read of the Extended Mode Register 1. Temperature conversion data less than or equal to T_{LOW} will activate interrupt. Interrupt will continue to be activated until the temperature data exceeds (T_{LOW} + T_{HYST}). Exceeding T_{HIGH} activates interrupt. Interrupt will continue to be activated at the end of a conversion until the temperature data is less than or equal to (T_{HIGH} − T_{HYST}). $\overline{\text{T\_CRIT\_A}}$ interrupts are activated when the temperature exceeds T_CRIT. $\overline{\text{T\_CRIT\_A}}$ interrupts will no longer be activated if the temperature data at the end of a conversion is less than or equal to(T_CRIT − T_{HYST}).



***Note:** Interrupt resets occur only when interrupt Status Register 1 is read.

FIGURE 14. Extended Repetitive Interrupt Mode

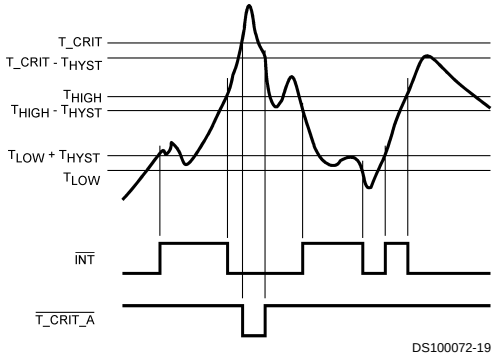
Extended One-Time Interrupt Mode is shown in *Figure 15* and operates in the following way: Once activated all interrupts remain activated until reset by a read of the Interrupt Status Register 1. Once activated all $\overline{\text{T\_CRIT\_A}}$ interrupts remain activated until reset by a read of the Extended Mode Register 1. An interrupt will be activated when the data of a temperature conversion is less than or equal to T_{LOW}. Interrupt cannot again be activated until the data from a temperature conversion is greater than (T_{LOW} + T_{HYST}). An interrupt will be activated when the data of a temperature conversion is greater than T_{HIGH}. Interrupt cannot again be activated until the data of a temperature conversion is less than or equal to (T_{HIGH} − T_{HYST}). $\overline{\text{T\_CRIT\_A}}$ interrupt is activated when the data from a temperature conversion is greater than T_CRIT. Activation of an $\overline{\text{T\_CRIT\_A}}$ interrupt cannot occur until the data from a temperature conversion is less than or equal to (T_CRIT − T_{HYST}).



***Note:** Interrupt resets occur only when interrupt Status Register 1 is read.

FIGURE 15. Extended One-Time Interrupt

Extended Comparator Mode is shown in *Figure 16* and operates in the following way: Interrupt is activated when the data from a temperature conversion is less than or equal to T_{LOW}. Interrupt is reset when the data from a temperature conversion exceeds (T_{LOW} + T_{HIGH}). Exceeding T_{HIGH} will activate interrupt. This interrupt will be reset when data from a temperature conversion is less than or equal to (T_{HIGH} − T_{HYST}). $\overline{\text{T\_CRIT\_A}}$ interrupt is activated when the temperature exceeds T_CRIT. $\overline{\text{T\_CRIT\_A}}$ remains active until the data from a temperature conversion is less than or equal to (T_CRIT − T_{HYST}) resets it.



***Note:** Interrupt resets occur only when interrupt Status Register 1 is read.

FIGURE 16. Extended Comparator Mode

Functional Description (Continued)

9.0 THE LM81 INTERRUPT STRUCTURE

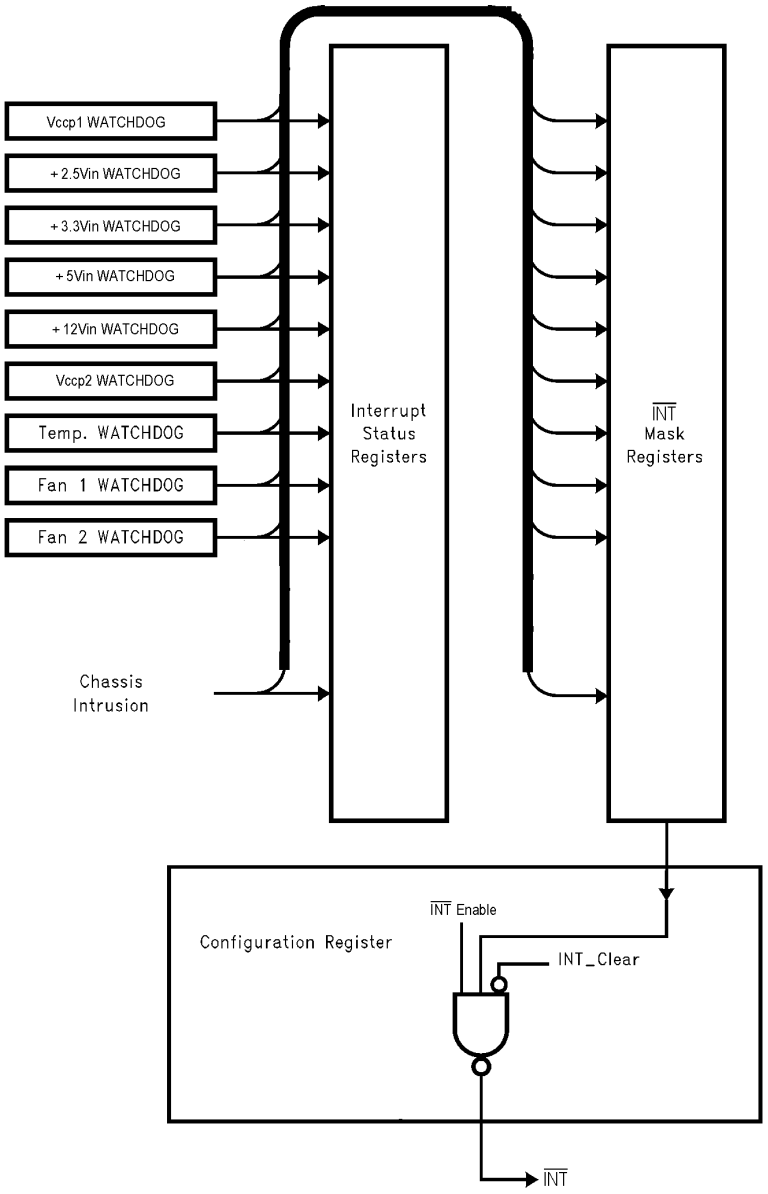


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FIGURE 17. Interrupt Structure

Figure 17 depicts the Interrupt Structure of the LM81. The LM81 can generate Interrupts as a result of each of its internal WATCHDOG registers on the analog, temperature, and fan inputs.

External Interrupts can come from the following source. While the label suggests a specific type or source of Interrupt, this label is not a restriction of its usage, and it could come from any desired source:

- **Chassis Intrusion:** This is an active high interrupt from any type of device that detects and captures chassis intrusion violations. This could be accomplished mechanically, optically, or electrically, and circuitry external to the LM81 is expected to latch the event. The design of the LM81 allows this input to go high even with no power applied to the LM81, and no clamping or other interference with the line will occur. This line can also be pulled low for at least 20 ms by the LM81 to reset a typical Chassis Intrusion circuit. Accomplish this reset by setting Bit 7 of CI Clear Register (45h) high. The bit in the Register is self-clearing.

All interrupts are indicated in the two Interrupt Status Registers. The $\overline{INT}$ output has two mask registers, and individual

Functional Description (Continued)

masks for each Interrupt. As described in Section 3.3, the hardware Interrupt line can also be enabled/disabled in the Configuration Register.

$\overline{\text{T\_CRIT\_A}}$ interrupt is dedicated to temperature and is indicated in Extended Mode Register 1. Extended Mode Register 1 controls $\overline{\text{T\_CRIT\_A}}$.

9.1 Interrupt Clearing

Reading a Status Register will output the contents of the Register, and reset the Register. A subsequent read done before the analog "round-robin" monitoring loop is complete will indicate a cleared Register. Allow at least 820 ms to allow all Registers to be updated between reads. In summary, the Interrupt Status Register clears upon being read, and requires at least 400 ms to be updated. When the Interrupt Status Register clears, the hardware interrupt line will also clear until the Registers are updated by the monitoring loop.

The hardware Interrupt line ($\overline{\text{INT}}$) is cleared with the INT_Clear bit, which is Bit 3 of the Configuration Register. When this bit is high, the LM81 monitoring loop will stop. It will resume when the bit is low.

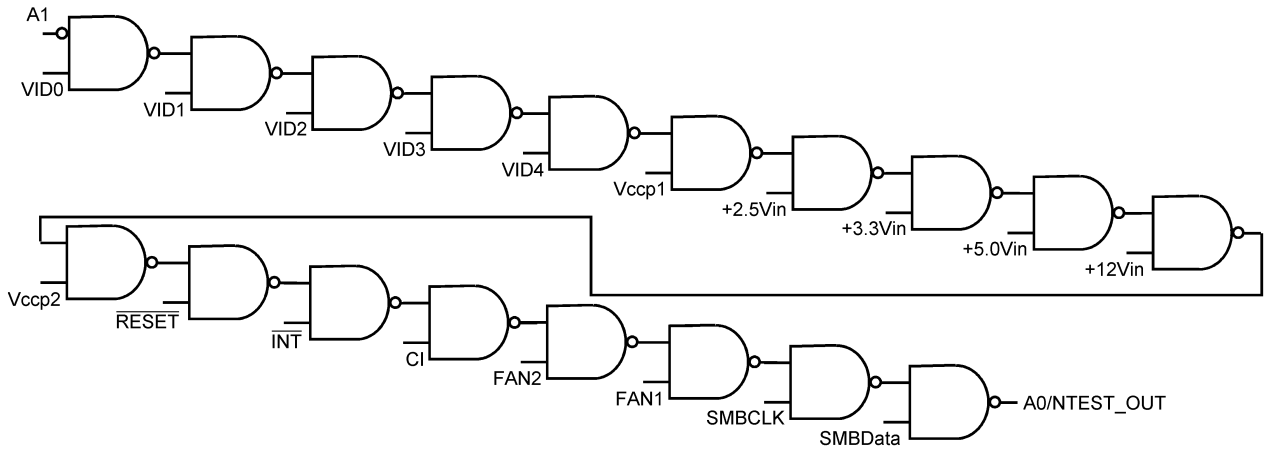
10.0 $\overline{\text{RESET}}$ I/O

$\overline{\text{RESET}}$ is intended to provide a master reset to devices connected to this line. $\overline{\text{INT}}$ Mask Register 2, Bit 7, must be set high to enable this function. Setting Bit 4 in the Configuration Register high outputs a least 20 ms low on this line, at the end of which Bit 4 in the Configuration Register automatically clears. Again, the label for this pin is only its suggested use. In applications where the $\overline{\text{RESET}}$ capability is not needed it can be used for any type of digital control that requires a 20 ms active low open-drain output.

$\overline{\text{RESET}}$ operates as an input when not activated by the Configuration Register. Setting this line low will reset all of the registers in the LM81 to their power on default state. All Value RAM locations will not be affected except for the DAC Data Register.

11.0 NAND TREE TESTS

A NAND tree is provided in the LM81 for Automated Test Equipment (ATE) board level connectivity testing. DACOut/NTEST_IN, $\overline{\text{T\_CRIT\_A}}$, V^+ and GND pins are excluded from NAND tree testing. Taking DACOut/NTEST_IN high before the first write to the configuration register activates the NAND Tree test mode. After the first write to the configuration register the NAND Tree test mode cannot be reactivated. To perform a NAND tree test all pins included in the NAND tree should be driven to 1 forcing the A0/NTEST_OUT high. Each individual pin starting with A1 and concluding with SMBData (excluding DACOut/NTEST_IN, $\overline{\text{T\_CRIT\_A}}$, V^+ and GND) can be taken low with the resulting toggle observed on the A0/NTEST_OUT pin. Allow for a typical propagation delay of 500 ns.



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Functional Description (Continued)

12.0 FAN MANUFACTURERS

Manufacturers of cooling fans with tachometer outputs are listed below:

NMB Tech

9730 Independence Ave.

Chatsworth, California 91311

818 341-3355

818 341-8207

Model Number	Frame Size	Airflow CFM
2408NL	2.36 in sq. X 0.79 in (60 mm sq. X 20 mm)	9-16
2410ML	2.36 in sq. X 0.98 in (60 mm sq. X 25 mm)	14-25
3108NL	3.15 in sq. X 0.79 in (80 mm sq. X 20 mm)	25-42
3110KL	3.15 in sq. X 0.98 in (80 mm sq. X 25 mm)	25-40

Mechatronics Inc.

P.O. Box 20

Mercer Island, WA 98040

800 453-4569

Various sizes available with tach output option.

Sanyo Denki America, Inc.

468 Amapola Ave.

Torrance, CA 90501

310 783-5400

Model Number	Frame Size	Airflow CFM
109P06XXY601	2.36 in sq. X 0.79 in (60 mm sq. X 20 mm)	11-15
109R06XXY401	2.36 in sq. X 0.98 in (60 mm sq. X 25 mm)	13-28
109P08XXY601	3.15 in sq. X 0.79 in (80 mm sq. X 20 mm)	23-30
109R08XXY401	3.15 in sq. X 0.98 in (80 mm sq. X 25 mm)	21-42

Functional Description (Continued)

13.0 REGISTERS AND RAM

13.1 Address Register

The main register is the ADDRESS Register. The bit designations are as follows:

Bit	Name	Read/ Write	Description
7-0	Address Pointer	Write	Address of RAM and Registers. See the tables below for detail.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address Pointer (Power On default 00h)							
A7	A6	A5	A4	A3	A2	A1	A0

13.2 Address Pointer Index (A7–A0)

Registers and RAM	A6–A0 in Hex	Power On Value of Registers: <7:0> in Binary	Notes
Configuration Register	40h	0000 1000	
Interrupt Status Register 1	41h	0000 0000	
Interrupt Status Register 2	42h	0000 0000	
Interrupt Mask Register 1	43h	0000 0000	
Interrupt Mask Register 2	44h	0000 0000	
CI Clear Register	46h	0000 0000	
VID/Fan Divisor Register	47h	<7:4> = 0101; <3:0> = VID3–VID0	
Serial Bus Address Register	48h	<7:2> =0010 11; <1:0> =(A1)(A0)	
VID4 Register	49h	<7:1> =1000 000; <0>=VID4	
Temperature Configuration Register	4Bh	0000 0001	
Extended Mode Register 1	4Ch	0100 0100	
Extended Mode Register 2	4Dh	0000 0000	
Value RAM	19h–3Dh		Address 19h default=1111 1111
Company ID	3Eh	0000 0001	This default designates National Semiconductor.
Stepping	3Fh	0000 0011	Revisions of this device will start with 1 and increment by one.

Functional Description (Continued)

13.3 Configuration Register — Address 40h

Power on default – <7:0> = 00001000 binary

Bit	Name	Read/ Write	Description
0	Start	Read/Write	A one enables startup of monitoring operations, a zero puts the part in standby mode. **Note:** The outputs of Interrupt pins will not be cleared if the user writes a zero to this location after an interrupt has occurred unlike “INT_Clear” bit. At start up, limit checking functions and scanning begin. Note, all limits should be set in the Value RAM before setting this bit HIGH.
1	$\overline{\text{INT}}$ Enable	Read/Write	A one enables the $\overline{\text{INT}}$ Interrupt output.
2	Reserved	Read/Write	
3	INT_Clear	Read/Write	A one disables the $\overline{\text{INT}}$ output without affecting the contents of Interrupt Status Registers. The device will stop monitoring. It will resume upon clearing of this bit.
4	$\overline{\text{RESET}}$	Read/Write	A one outputs at least a 20 ms active low reset signal at $\overline{\text{RESET}}$. This bit is cleared once the pulse has gone inactive.
5	Reserved	Read/Write	
6	CI_Clear	Read/Write	A one outputs a minimum 20 ms active low pulse on the CI pin. The register bit self clears after the pulse has been output. This bit is mirrored in the CI Clear Register bit 7.
7	INITIALIZATION	Read/Write	A one restores power on default value to the Configuration Register, Interrupt Status Registers, Interrupt Mask Registers, CI Clear Register, VID/Fan Divisor Register, VID4, Temperature Configuration Register, and the Extended Mode Registers. This bit clears itself since the power on default is zero.

Functional Description (Continued)

13.4 Interrupt Status Register 1 — Address 41h

Power on default – <7:0> = 0000 0000 binary

Bit	Name	Read/Write	Description
0	+2.5Vin	Read Only	A one indicates a High or Low limit has been exceeded.
1	Vccp1	Read Only	A one indicates a High or Low limit has been exceeded.
2	+3.3Vin	Read Only	A one indicates a High or Low limit has been exceeded.
3	+5Vin	Read Only	A one indicates a High or Low limit has been exceeded.
4	Temperature	Read Only	A one indicates a HIGH or HIHYST temperature error, see *SECTION 8.2.*
5	Reserved	Read Only	
6	FAN1	Read Only	A one indicates the fan count limit has been exceeded.
7	FAN2	Read Only	A one indicates the fan count limit has been exceeded.

13.5 Interrupt Status Register 2 — Address 42h

Power on default – <7:0> = 0000 0000 binary

Bit	Name	Read/Write	Description
0	+12Vin	Read Only	A one indicates a High or Low limit has been exceeded.
1	Vccp2	Read Only	A one indicates a High or Low limit has been exceeded.
2	Reserved	Read Only	
3	Reserved	Read Only	
4	CI	Read Only	A one indicates CI (Chassis Intrusion) has gone high.
5	Reserved	Read Only	
6	Reserved	Read Only	
7	TLOW	Read Only	A one indicates LOW temperature error in **EXTENDED MODE ONLY**, see *SECTION 8.2.*

13.6 Interrupt Mask Register 1 — Address 43h

Power on default – <7:0> = 0000 0000 binary

Bit	Name	Read/ Write	Description
0	+2.5Vin	Read/Write	A one disables the corresponding interrupt status bit for $\overline{INT}$ interrupt.
1	Vccp1	Read/Write	A one disables the corresponding interrupt status bit for $\overline{INT}$ interrupt.
2	+3.3Vin	Read/Write	A one disables the corresponding interrupt status bit for $\overline{INT}$ interrupt.
3	+5Vin	Read/Write	A one disables the corresponding interrupt status bit for $\overline{INT}$ interrupt.
4	Temperature	Read/Write	A one disables the corresponding interrupt status bit for $\overline{INT}$ interrupt.
5	Reserved	Read/Write	
6	FAN1	Read/Write	A one disables the corresponding interrupt status bit for $\overline{INT}$ interrupt.
7	FAN2	Read/Write	A one disables the corresponding interrupt status bit for $\overline{INT}$ interrupt.

Functional Description (Continued)

13.7 Interrupt Mask Register 2 — Address 44h

Power on default – <7:0> = 0000 0000 binary

Bit	Name	Read/ Write	Description
0	+12Vin	Read/Write	A one disables the corresponding interrupt status bit for $\overline{\text{INT}}$ interrupt.
1	Vccp2	Read/Write	A one disables the corresponding interrupt status bit for $\overline{\text{INT}}$ interrupt.
2	Reserved	Read/Write	
3	Reserved	Read/Write	
4	Chassis Intrusion	Read/Write	A one disables the corresponding interrupt status bit for $\overline{\text{INT}}$ interrupt.
5	Reserved	Read/Write	
6	Reserved	Read/Write	
7	$\overline{\text{RESET}}$ Enable	Read/Write	<7> = 1 in $\overline{\text{INT}}$ Mask Register 2 enables the $\overline{\text{RESET}}$ in the Configuration Register.

13.8 Reserved Register — Address 45h

Power on default – <7:0> = 00h. Read/Write for backwards compatibility.

13.9 CI Clear Register — Address 46h

Power on default – <7:0> = 0000 0000 binary

Bit	Name	Read/ Write	Description
0-6	Reserved	Read/Write	
7	CI Clear	Read/Write	A one outputs a minimum 20 ms active low pulse on the Chassis Intrusion pin. The register bit self clears after the pulse has been output. This bit is mirrored in Configuration Register bit 6.

Functional Description (Continued)

13.10 VID/Fan Divisor Register — Address 47h

Power on default – <7:4> is 0101, and <3:0>is mapped to VID <3:0>

Bit	Name	Read/Write	Description
0-3	VID <3:0>	Read Only	The VID <3:0> inputs from the Pentium/PRO power supplies that indicate the operating voltage (e.g. 1.5V to 2.9V).
4-5	FAN1 RPM Control	Read/Write	FAN1 Speed Control. <5:4> = 00 - divide by 1; <5:4> = 01 - divide by 2; <5:4> = 10 - divide by 4; <5:4> = 11 - divide by 8.
6-7	FAN2 RPM Control	Read/Write	FAN2 Speed Control. <7:6> = 00 - divide by 1; <7:6> = 01 - divide by 2; <7:6> = 10 - divide by 4; <7:6> = 11 - divide by 8.

13.11 Serial Bus Address Register — Address 48h

Power on default – Serial Bus address <6:0> = 010 11(A1)(A0) and <7> = 0 binary

Bit	Name	Read/Write	Description
0-1	Serial Bus Address	Read Only	Serial Bus address <1:0> = A1 A0
2-6	Serial Bus Address	Read/Write	Serial Bus address <6:2> = 010 11
7	Reserved	Read/Write	

13.12 VID4 Register — Address 49h

Power on default – <7:1> = 100 000, <0> = VID4.

Bit	Name	Read/Write	Description
0	VID4	Read Only	VID4 input from Pentium/PRO power supply that indicate the operating voltage of the processor (e.g. 1.5V to 2.9V).
1-7	Reserved	Read/Write	

13.13 Temperature Configuration Register — Address 4Bh

Power on default – <7:0> = 0000 0001 binary

Bit	Name	Read/Write	Description
0-1	Temperature Interrupt Mode Select Bits	Read/Write	The state of these bits select the interrupt mode for $\overline{INT}$ as described below. <1:0> = 00 or <1:0> = 11: Repetitive Interrupt Mode <1:0> = 01: One-Time Interrupt Mode <1:0> = 10: Comparator Mode
2-6	Reserved	Read/Write	
7	Temperature Resolution	Read Only	For 8-bit plus sign temperature resolution: <7> = LSB (0.5°C)

Functional Description (Continued)

13.14 Extended Mode Register 1 — Address 4Ch

Power on default – <7:0> = 0100 0100 binary

Bit	Name	Read/Write	Description
0	Extended Mode Enable	Read/Write	A one enables the Extended Interrupt Modes, the $\overline{\text{T\_CRIT\_A}}$ output and all the functions listed in the Extended Mode Registers. Bit 7 of the Interrupt Status register will be activated to reflect the interrupt status of the LOW limit comparison result.
1	LOW Limit Mask Bit	Read/Write	A mask bit for the LOW limit Interrupt. A one disables the interrupt from propagating to the $\overline{\text{INT}}$ pin.
2-3	$\overline{\text{T\_CRIT\_A}}$ Interrupt Mode Select	Read/Write	The state of these bits select the interrupt mode for $\overline{\text{T\_CRIT\_A}}$ as described below. <3:2> = 00 or <3:2> = 11: Repetitive Interrupt Mode <3:2> = 01: One-Time Interrupt Mode <3:2> = 10: Comparator Mode
4	$\overline{\text{T\_CRIT\_A}}$ Enable	Read/Write	A one enables the $\overline{\text{T\_CRIT\_A}}$ pin.
5	$\overline{\text{T\_CRIT\_A}}$ Polarity	Read/Write	A one sets the $\overline{\text{T\_CRIT\_A}}$ pin active HIGH. A zero sets the $\overline{\text{T\_CRIT\_A}}$ pin active LOW.
6	$\overline{\text{T\_CRIT\_A}}$ Mask Enable	Read/Write	A one prevents the $\overline{\text{T\_CRIT\_A}}$ interrupt from propagating to the $\overline{\text{INT}}$ output pin.
7	$\overline{\text{T\_CRIT\_A}}$ Status Bit	Read	A one indicates that a $\overline{\text{T\_CRIT\_A}}$ interrupt has occurred.

13.15 Extended Mode Register 2 — Address 4Dh

Power on default – <7:0> = 0000 0000 binary

Bit	Name	Read/Write	Description
0-2	Hysteresis Offset Value	Read/Write	T_{HYST} value.
3	12-bit Temperature Resolution Enable	Read/Write	A one sets the temperature resolution to 12 bits.
4-7	12-bit Temperature Data	Read Only	12-bit temperature data least significant bits. Bit 7 mirrors bit 7 in the temperature configuration register (4Bh) and has a weight of 0.5˚C; bits 6-4 have a weight of 0.25, 0.125, and 0.0625˚C, respectively.

Functional Description (Continued)

13.16 Value RAM — Address 15h–3Fh

Address A6–A0	Description
15h	Manufacturers Test Register
19h	DAC data register; power on default <7:0>=1111 1111 binary
20h	+2.5Vin reading
21h	Vccp1 reading
22h	+3.3Vin reading
23h	+5Vin reading
24h	+12Vin reading
25h	Vccp2 reading
26h	Reserved reading
27h	Temperature reading (8 MSBs)
28h	FAN1 reading **Note:** This location stores the number of counts of the internal clock per revolution.
29h	FAN2 reading **Note:** This location stores the number of counts of the internal clock per revolution.
2Ah	Reserved
2Bh	+2.5Vin High Limit
2Ch	+2.5Vin Low Limit
2Dh	Vccp1 High Limit
2Eh	Vccp1 Low Limit
2Fh	+3.3Vin High Limit
30h	+3.3Vin Low Limit
31h	+5Vin High Limit
32h	+5Vin Low Limit
33h	+12Vin High Limit
34h	+12Vin Low Limit
35h	Vccp2 High Limit
36h	Vccp2 Low Limit
37h	T_CRIT Limit (Extended Mode)
38h	LOW Limit (Extended Mode)
39h	HIGH Temperature Limit
3Ah	HIHYST Temperature Limit
3Bh	FAN1 Fan Count Limit **Note:** It is the number of counts of the internal clock for the Low Limit of the fan speed.
3Ch	FAN2 Fan Count Limit **Note:** It is the number of counts of the internal clock for the Low Limit of the fan speed.
3Dh	Reserved
3Eh	Company Identification. The number in this register identifies National Semiconductor (0000 0001)
3Fh	Stepping Register LM81 revision number (0000 0011)

Note: Setting all ones to the high limits for voltages and fans (0111 1111 binary for temperature) means interrupts will **never** be generated except the case when voltages go below the low limits.

For voltage input high limits, the device is doing a greater than comparison. For low limits, however, it is doing a less than or equal to comparison.

Typical Application

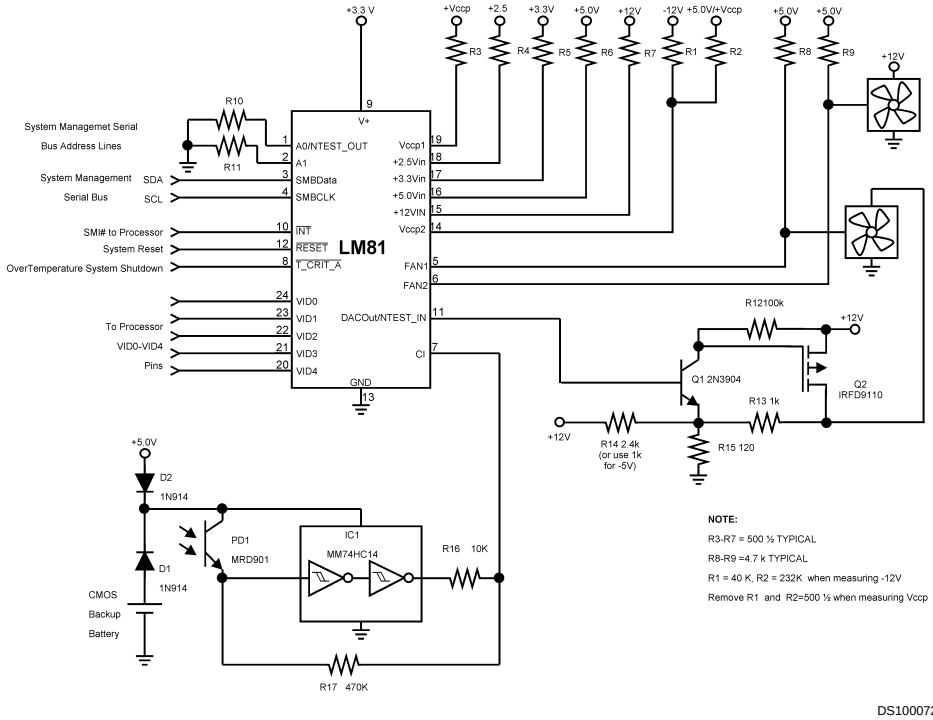

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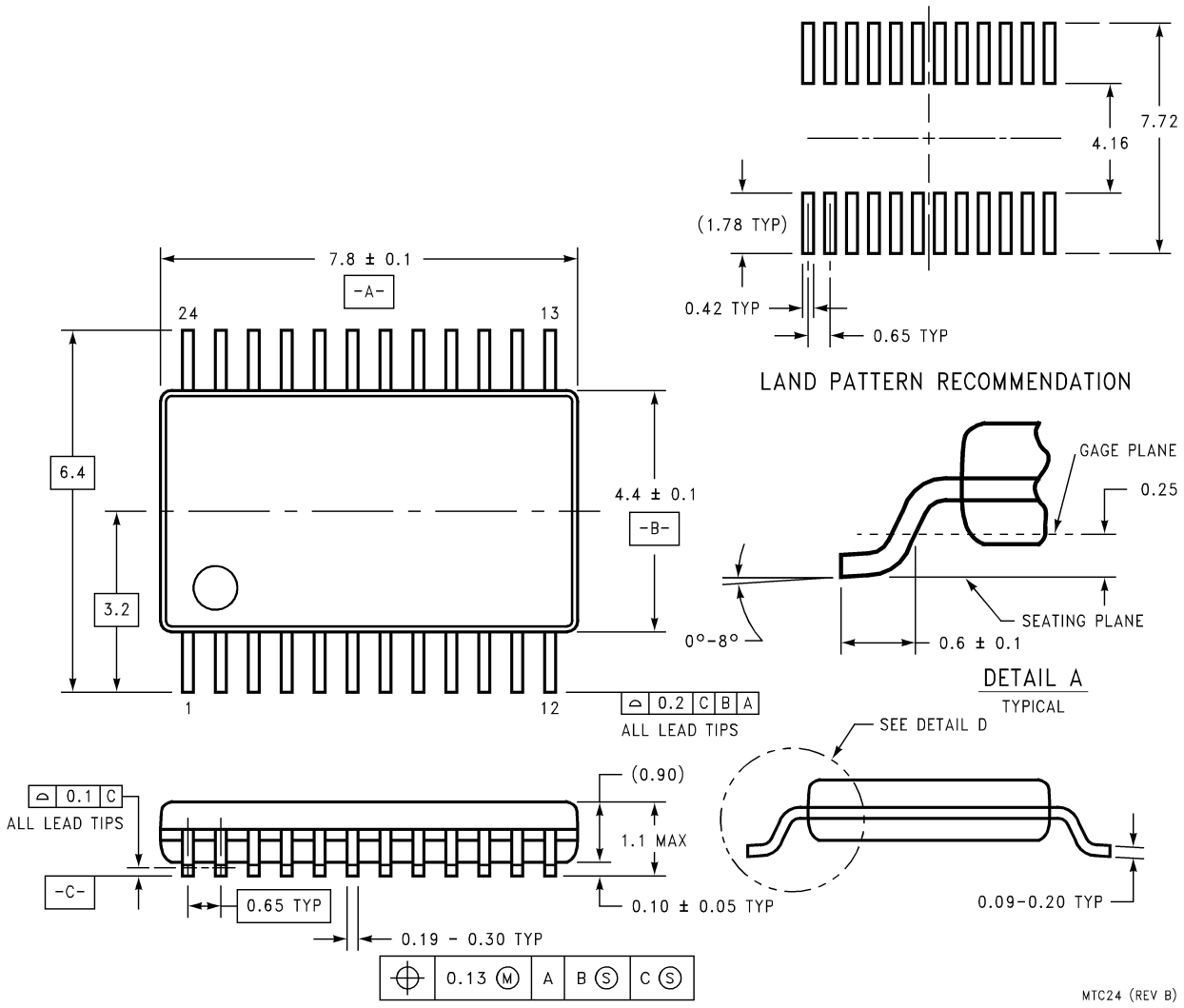
FIGURE 19. In this PC application the LM81 monitors temperature, fan speed for 2 fans, and 6 power supply voltages. It also monitors an optical chassis intrusion detector. The LM81 provides a DAC output that can be used to control fan speed.

Physical Dimensions inches (millimeters) unless otherwise noted



24-Lead TSSOP
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NS Package Number MTC24B

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Audio	www.ti.com/audio	Communications and Telecom	www.ti.com/communications
Amplifiers	amplifier.ti.com	Computers and Peripherals	www.ti.com/computers
Data Converters	dataconverter.ti.com	Consumer Electronics	www.ti.com/consumer-apps
DLP® Products	www.dlp.com	Energy and Lighting	www.ti.com/energy
DSP	dsp.ti.com	Industrial	www.ti.com/industrial
Clocks and Timers	www.ti.com/clocks	Medical	www.ti.com/medical
Interface	interface.ti.com	Security	www.ti.com/security
Logic	logic.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Power Mgmt	power.ti.com	Transportation and Automotive	www.ti.com/automotive
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Mobile Processors	www.ti.com/omap		
Wireless Connectivity	www.ti.com/wirelessconnectivity		
	TI E2E Community Home Page		e2e.ti.com

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