PLLatinum™ Ultra Low Power Dual Frequency Synthesizer for RF Personal Communications LMX2335U 1.2 GHz/1.2 GHZ, LMX2336U 2.0 GHz/1.2 GHz

Check for Samples: LMX2335U, LMX2336U

FEATURES

- **Ultra Low Current Consumption**
- **Upgrade and Compatible to the LMX2335L and LMX2336L Devices**
- **2.7V to 5.5V Operation**
- **Selectable Synchronous or Asynchronous Powerdown Mode:**
  - **$I_{CC-PWDN}$ = 1 µA Typical at 3.0V**
- **Selectable Dual Modulus Prescaler:**
  - **RF1: 64/65 or 128/129**
  - **RF2: 64/65 or 128/129**
- **Selectable Charge Pump TRI-STATE Mode**
- **Programmable Charge Pump Current Levels**
  - **RF1 and RF2: 0.95 or 3.8 mA**
- **Selectable Fastlock Mode for the RF1 Synthesizer**
- **Push-Pull Analog Lock Detect Mode**
- **LMX2335U is Available in 16-Pin TSSOP and 16-Pin LGA**
- **LMX2336U is Available in 20-Pin TSSOP, 24-Pin LGA, and 20-Pin ULGA**

APPLICATIONS

- **Mobile Handsets:**
  - **GSM, GPRS, W-CDMA, CDMA, PCS, AMPS, PDC, DCS**
- **Cordless Handsets (DECT, DCT)**
- **Wireless Data**
- **Cable TV Tuners**

DESCRIPTION

The LMX2335U and LMX2336U devices are high performance frequency synthesizers with integrated dual modulus prescalers. The LMX2335U and LMX2336U devices are designed for use in applications requiring two RF phase-locked loops.

A 64/65 or a 128/129 prescale ratio can be selected for each RF synthesizer. Using a proprietary digital phase locked loop technique, the LMX2335U and LMX2336U devices generate very stable, low noise control signals for the RF voltage controlled oscillators. Both RF synthesizers include a two-level programmable charge pump. The RF1 synthesizer has dedicated Fastlock circuitry.

Serial data is transferred to the devices via a three wire interface (Data, LE, Clock). Supply voltages from 2.7V to 5.5V are supported. The LMX2335U and the LMX2336U feature very low current consumption:

LMX2335U (1.2 GHz)– 3.0 mA, LMX2336U (2.0 GHz)– 3.5 mA at 3.0V.

The LMX2335U device is available in 16-pin TSSOP, and 16-pin Chip Scale Package (LGA) surface mount plastic packages. The LMX2336U device is available in 20-Pin TSSOP, 24-Pin LGA, and 20-Pin ULGA surface mount plastic packages.

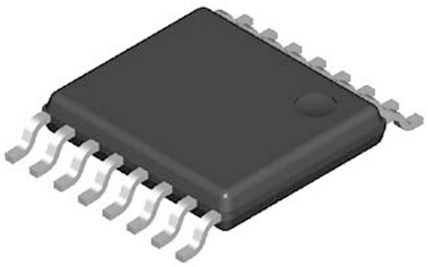


Figure 1. Thin Shrink Small Outline Package (PW0016A)

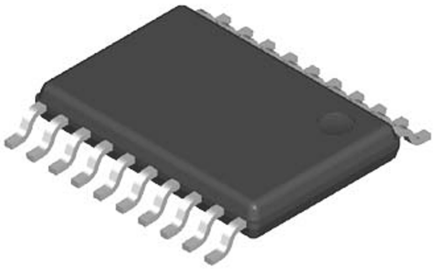


Figure 2. Thin Shrink Small Outline Package (PW0020A)

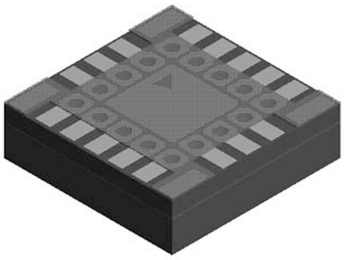


Figure 3. LGA (NPG0016A)

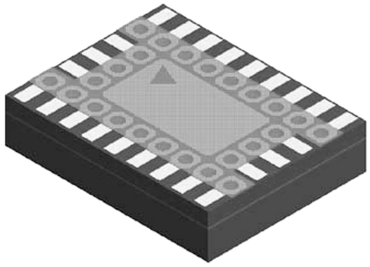


Figure 4. LGA (NPH0024A)

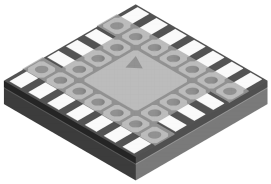
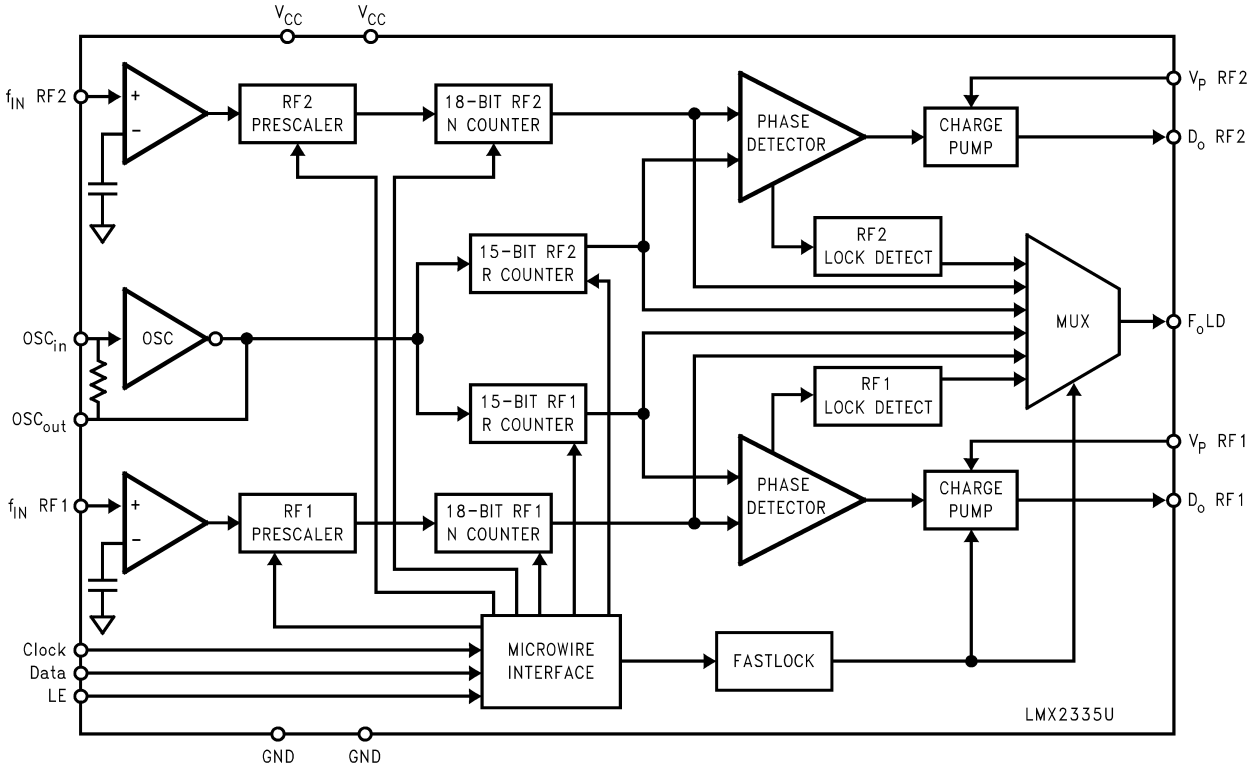
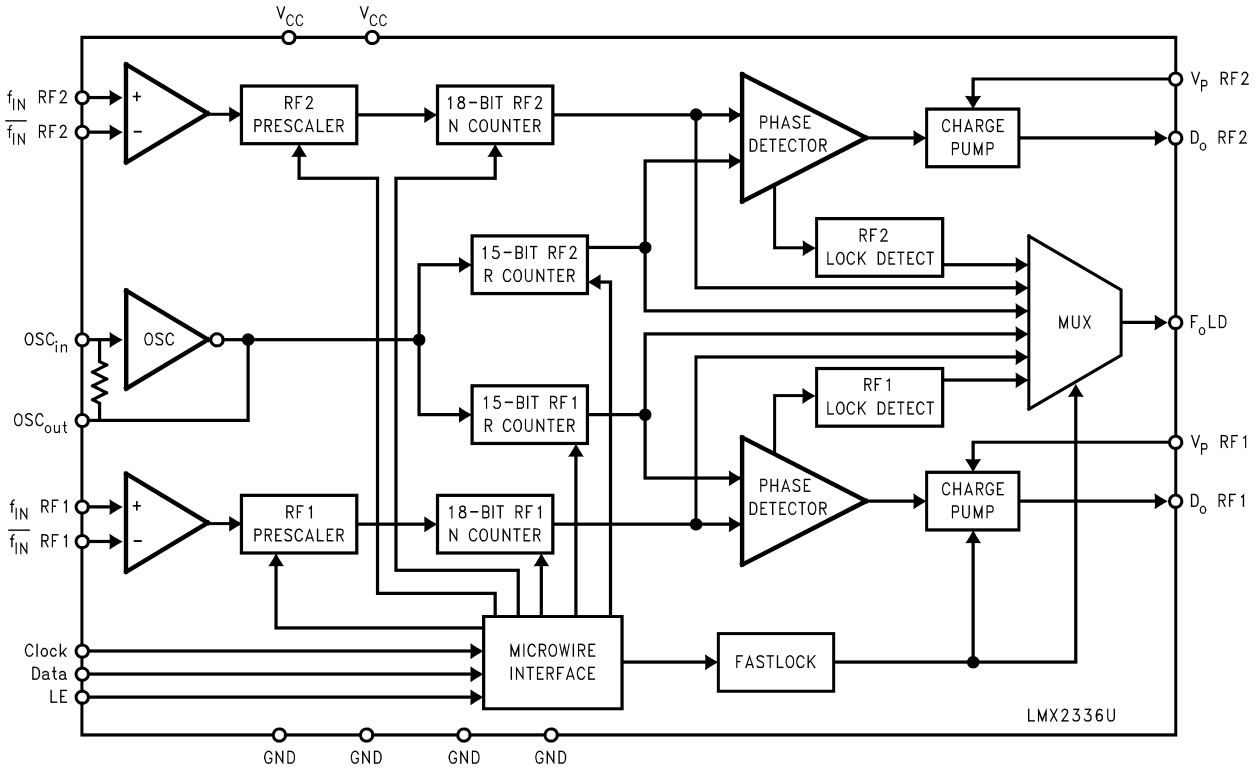


Figure 5. ULGA (NPE0020A)

LMX2335U Functional Block Diagram



LMX2336U Functional Block Diagram



Connection Diagrams

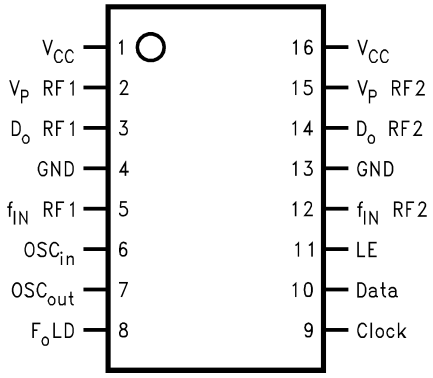


Figure 6. LMX2335U Thin Shrink Small Outline Package (PW) (Top View)

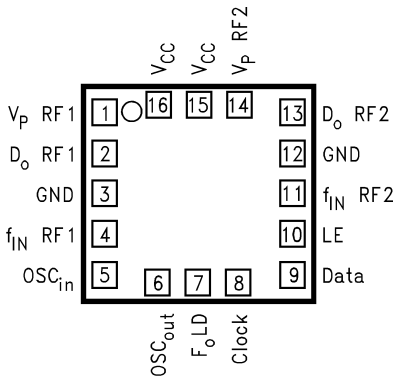


Figure 7. LMX2335U LGA (NPG) (Top View)

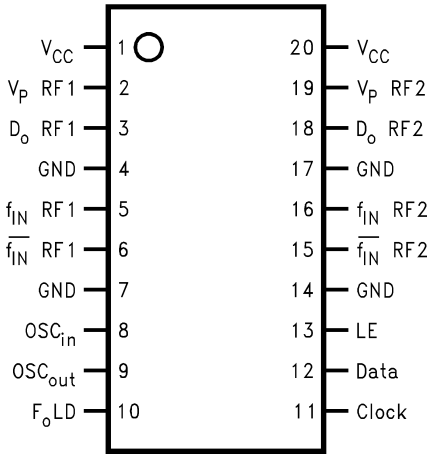


Figure 8. LMX2336U Thin Shrink Small Outline Package (PW) (Top View)

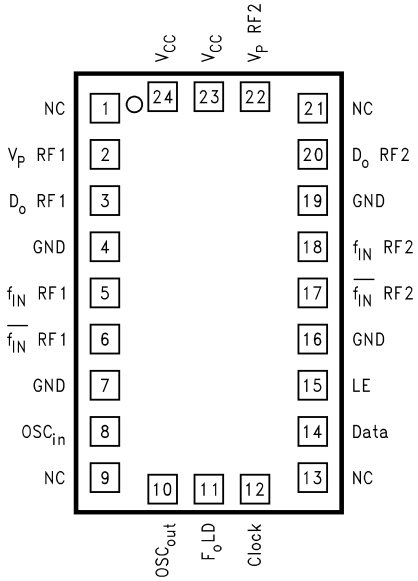


Figure 9. LMX2336U LGA (NPH) (Top View)

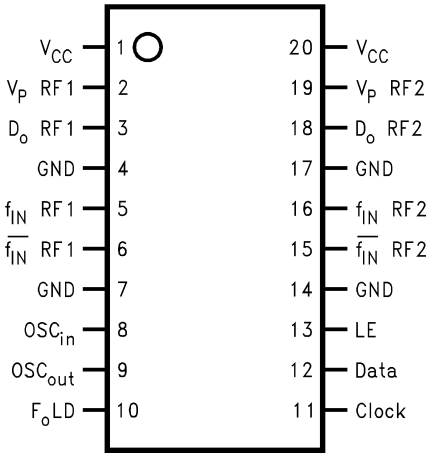


Figure 10. LMX2336U ULGA (NPE) (Top View)

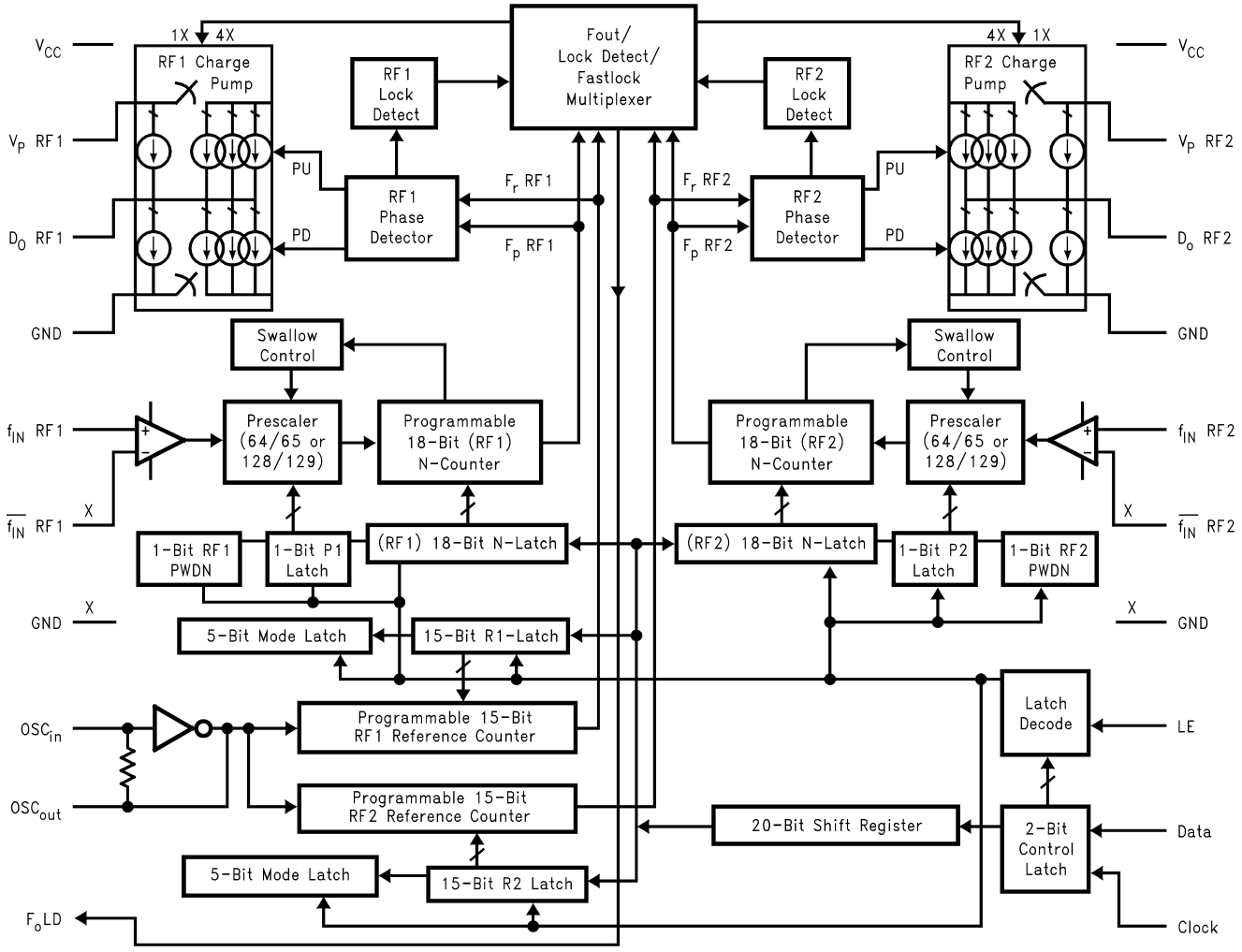
PIN DESCRIPTIONS

Pin Name	Pin No. LMX2336U 20-Pin ULGA	Pin No. LMX2336U 20-Pin TSSOP	Pin No. LMX2336U 24-Pin LGA	Pin No. LMX2335U 16-Pin TSSOP	Pin No. LMX2335U 16-Pin LGA	I/O	Description
V_{CC}	20	1	24	1	16	–	Power supply bias for the RF1 PLL analog and digital circuits. V_{CC} may range from 2.7V to 5.5V. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.
V_P RF1	1	2	2	2	1	–	RF1 PLL charge pump power supply. Must be ≥ V_{CC}.
D_o RF1	2	3	3	3	2	O	RF1 PLL charge pump output. The output is connected to the external loop filter, which drives the input of the VCO.
GND	3	4	4	4	3	–	LMX2335U: Ground for the RF1 PLL analog and digital circuits. LMX2336U: Ground for the RF1 PLL digital circuitry.
f_{IN} RF1	4	5	5	5	4	I	RF1 PLL prescaler input. Small signal input from the VCO.
$\overline{f_{IN}}$ RF1	5	6	6	X	X	I	LMX2335U: Don't care. LMX2336U: RF1 PLL prescaler complementary input. For single ended operation, this pin should be AC grounded. The LMX2336U RF1 PLL can be driven differentially when the bypass capacitor is omitted.
GND	6	7	7	X	X	–	LMX2335U: Don't care. LMX2336U: Ground for the RF1 PLL analog circuitry.
OSC_{in}	7	8	8	6	5	I	Oscillator input. It has an approximate $V_{CC}/2$ input threshold and can be driven from an external CMOS or TTL logic gate.
OSC_{out}	8	9	10	7	6	O	Oscillator output. This output is connected directly to a crystal. If a TCXO is used, it is left open.
F_oLD	9	10	11	8	7	O	Programmable multiplexed output pin. Functions as a general purpose CMOS TRI-STATE output, RF1/RF2 PLL push-pull analog lock detect output, N and R divider output, or Fastlock output, which connects a parallel resistor to the external loop filter.
Clock	10	11	12	9	8	I	MICROWIRE Clock input. High impedance CMOS input. Data is clocked into the 22-bit shift register on the rising edge of Clock.
Data	11	12	14	10	9	I	MICROWIRE Data input. High impedance CMOS input. Binary serial data. The MSB of Data is entered first. The last two bits are the control bits.
LE	12	13	15	11	10	I	MICROWIRE Latch Enable input. High impedance CMOS input. When LE transitions HIGH, Data stored in the shift registers is loaded into one of 4 internal control registers.
GND	13	14	16	X	X	–	LMX2335U: Don't care. LMX2336U: Ground for the RF2 PLL analog circuitry.
$\overline{f_{IN}}$ RF2	14	15	17	X	X	I	LMX2335U: Don't care. LMX2336U: RF2 PLL prescaler complementary input. For single ended operation, this pin should be AC grounded. The LMX2336U RF2 PLL can be driven differentially when the bypass capacitor is omitted.
f_{IN} RF2	15	16	18	12	11	I	RF2 PLL prescaler input. Small signal input from the VCO.

PIN DESCRIPTIONS (continued)

Pin Name	Pin No. LMX2336U 20-Pin ULGA	Pin No. LMX2336U 20-Pin TSSOP	Pin No. LMX2336U 24-Pin LGA	Pin No. LMX2335U 16-Pin TSSOP	Pin No. LMX2335U 16-Pin LGA	I/O	Description
GND	16	17	19	13	12	–	LMX2335U: Ground for the RF2 PLL analog and digital circuits, MICROWIRE, F_oLD and oscillator circuits. LMX2336U: Ground for the RF2 PLL digital circuitry, MICROWIRE, F_oLD and oscillator circuits.
D_o RF2	17	18	20	14	13	O	RF2 PLL charge pump output. The output is connected to the external loop filter, which drives the input of the VCO.
V_P RF2	18	19	22	15	14	–	RF2 PLL charge pump power supply. Must be ≥ V_{CC}.
V_{CC}	19	20	23	16	15	–	Power supply bias for the RF2 PLL analog and digital circuits, MICROWIRE, F_oLD and oscillator circuits. V_{CC} may range from 2.7V to 5.5V. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.
NC	X	X	1, 9, 13, 21	X	X	–	LMX2335U: Don't Care. LMX2336U: No connect.

Detailed Block Diagram



1. V_{CC} supplies power to the RF1 and RF2 prescalers, RF1 and RF2 feedback dividers, RF1 and RF2 reference dividers, RF1 and RF2 phase detectors, the OSC_{in} buffer, MICROWIRE, and F_oLD circuits.
2. V_P RF1 and V_P RF2 supply power to the charge pumps. They can be run separately as long as V_P RF1 ≥ V_{CC} and V_P RF2 ≥ V_{CC}.
3. X signifies a pin that is NOT available on the LMX2335U PLL.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)(3)(4)

Power Supply Voltage	V_{CC} to GND	−0.3V to +6.5V
	V_P RF1 to GND	−0.3V to +6.5V
	V_P RF2 to GND	−0.3V to +6.5V
Voltage on any pin to GND (V_I)	V_I must be < +6.5V	−0.3V to V_{CC}+0.3V
Storage Temperature Range (T_S)		−65°C to +150°C
Lead Temperature (solder 4 s) (T_L)		+260°C
16-Pin TSSOP θ_{JA} Thermal Impedance		137.1°C/W
20-Pin TSSOP θ_{JA} Thermal Impedance		114.5°C/W
16-Pin LGA θ_{JA} Thermal Impedance		130°C/W
24-Pin LGA θ_{JA} Thermal Impedance		112°C/W

(1) This device is a high performance RF integrated circuit with an ESD rating <2 kV and is ESD sensitive. Handling and assembly of this device should only be done at ESD protected work stations.
(2) GND = 0V
(3) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Recommended Operating Conditions indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics . The ensured specifications apply only for the test conditions listed.
(4) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

Recommended Operating Conditions (1)

Power Supply Voltage	V_{CC} to GND	+2.7V to +5.5V
	V_P RF1 to GND	V_{CC} to +5.5V
	V_P RF2 to GND	V_{CC} to +5.5V
Operating Temperature (T_A)		−40°C to +85°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Recommended Operating Conditions indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics . The ensured specifications apply only for the test conditions listed.

Electrical Characteristics

V_{CC} = V_P RF1 = V_P RF2 = 3.0V, −40°C ≤ T_A ≤ +85°C, unless otherwise specified

Symbol	Parameter		Conditions	Value			Units
				Min	Typ	Max	
I_{CC} PARAMETERS							
$I_{CC_{RF1 + RF2}}$	Power Supply Current, RF1 + RF2 Synthesizers	LMX2335U	Clock, Data and LE = GND OSC_{in} = GND PWDN RF1 Bit = 0 PWDN RF2 Bit = 0		3.0	4.0	mA
		LMX2336U			3.5	4.5	mA
$I_{CC_{RF1}}$	Power Supply Current, RF1 Synthesizer Only	LMX2335U	Clock, Data and LE = GND OSC_{in} = GND PWDN RF1 Bit = 0 PWDN RF2 Bit = 1		1.5	2.0	mA
		LMX2336U			2.0	2.5	mA
$I_{CC_{RF2}}$	Power Supply Current, RF2 Synthesizer Only	LMX2335U	Clock, Data and LE = GND OSC_{in} = GND PWDN RF1 Bit = 1 PWDN RF2 Bit = 0		1.5	2.0	mA
		LMX2336U			1.5	2.0	
$I_{CC\text{-}PWDN}$	Powerdown Current	LMX2335U/ LMX2336U	Clock, Data and LE = GND OSC_{in} = GND PWDN RF1 Bit = 1 PWDN RF2 Bit = 1		1.0	10.0	µA
RF1 SYNTHESIZER PARAMETERS							
f_{IN} RF1	RF1 Operating Frequency	LMX2335U		100		1200	MHz
		LMX2336U		200		2000	MHz
N_{RF1}	RF1 N Divider Range		Prescaler = 64/65 (1)	192		131135	
			Prescaler = 128/129 (1)	384		262143	
R_{RF1}	RF1 R Divider Range			3		32767	
$F_{\varphi RF1}$	RF1 Phase Detector Frequency					10	MHz
Pf_{IN} RF1	RF1 Input Sensitivity		2.7V ≤ V_{CC} ≤ 3.0V (2)	−15		0	dBm
			3.0V < V_{CC} ≤ 5.5V (2)	−10		0	dBm
ID_0 RF1 SOURCE	RF1 Charge Pump Output Source Current		VD_0 RF1 = V_P RF1/2 ID_0 RF1 Bit = 0 (3)		-0.95		mA
			VD_0 RF1 = V_P RF1/2 ID_0 RF1 Bit = 1 (3)		-3.80		mA
ID_0 RF1 SINK	RF1 Charge Pump Output Sink Current		VD_0 RF1 = V_P RF1/2 ID_0 RF1 Bit = 0 (3)		0.95		mA
			VD_0 RF1 = V_P RF1/2 ID_0 RF1 Bit = 1 (3)		3.80		mA
ID_0 RF1 TRI-STATE	RF1 Charge Pump Output TRI-STATE Current		0.5V ≤ VD_0 RF1 ≤ V_P RF1 - 0.5V (3)	-2.5		2.5	nA
ID_0 RF1 SINK Vs ID_0 RF1 SOURCE	RF1 Charge Pump Output Sink Current Vs Charge Pump Output Source Current Mismatch		VD_0 RF1 = V_P RF1/2 T_A = +25°C (4)		3	10	%
ID_0 RF1 Vs VD_0 RF1	RF1 Charge Pump Output Current Magnitude Variation Vs Charge Pump Output Voltage		0.5V ≤ VD_0 RF1 ≤ V_P RF1 - 0.5V T_A = +25°C (4)		10	15	%
ID_0 RF1 Vs T_A	RF1 Charge Pump Output Current Magnitude Variation Vs Temperature		VD_0 RF1 = V_P RF1/2 (4)		10		%

(1) Some of the values in this range are illegal divide ratios (B < A). To obtain continuous legal division, the Minimum Divide Ratio must be calculated. Use N ≥ P * (P−1), where P is the value selected for the prescaler.
(2) Refer to Figure 35.
(3) Refer to Figure 34.
(4) Refer to Charge Pump Current Specification Definitions for details on how these measurements are made.

Electrical Characteristics (continued)

V_{CC} = V_P RF1 = V_P RF2 = 3.0V, −40°C ≤ T_A ≤ +85°C, unless otherwise specified

Symbol	Parameter		Conditions	Value			Units
				Min	Typ	Max	
RF2 SYNTHESIZER PARAMETERS							
f_{IN} RF2	RF2 Operating Frequency	LMX2335U		100		1200	MHz
		LMX2336U		100		1200	MHz
N_{RF2}	RF2 N Divider Range		Prescaler = 64/65 (5)	192		131135	
			Prescaler = 128/129 (5)	384		262143	
R_{RF2}	RF2 R Divider Range			3		32767	
$F_{\varphi RF2}$	RF2 Phase Detector Frequency					10	MHz
Pf_{IN} RF2	RF2 Input Sensitivity		2.7V ≤ V_{CC} ≤ 3.0V (6)	-15		0	dBm
			3.0V < V_{CC} ≤ 5.5V (6)	-10		0	dBm
ID_0 RF2 SOURCE	RF2 Charge Pump Output Source Current		VD_0 RF2 = V_P RF2/2 ID_0 RF2 Bit = 0 (7)		-0.95		mA
			VD_0 RF2 = V_P RF2/2 ID_0 RF2 Bit = 1 (7)		-3.80		mA
ID_0 RF2 SINK	RF2 Charge Pump Output Sink Current		VD_0 RF2 = V_P RF2/2 ID_0 RF2 Bit = 0 (7)		0.95		mA
			VD_0 RF2= V_P RF2/2 ID_0 RF2 Bit = 1 (7)		3.80		mA
ID_0 RF2 TRI-STATE	RF2 Charge Pump Output TRI-STATE Current		0.5V ≤ VD_0 RF2 ≤ V_P RF2 - 0.5V (7)	-2.5		2.5	nA
ID_0 RF2 SINK Vs ID_0 RF2 SOURCE	RF2 Charge Pump Output Sink Current Vs Charge Pump Output Source Current Mismatch		VD_0 RF2 = V_P RF2/2 T_A = +25°C (8)		3	10	%
ID_0 RF2 Vs VD_0 RF2	RF2 Charge Pump Output Current Magnitude Variation Vs Charge Pump Output Voltage		0.5V ≤ VD_0 RF2 ≤ V_P RF2 - 0.5V T_A = +25°C (8)		10	15	%
ID_0 RF2 Vs T_A	RF2 Charge Pump Output Current Magnitude Variation Vs Temperature		VD_0 RF2 = V_P RF2/2 (8)		10		%
OSCILLATOR PARAMETERS							
F_{OSC}	Oscillator Operating Frequency			2		40	MHz
V_{OSC}	Oscillator Sensitivity		See (9)	0.5		V_{CC}	V_{PP}
I_{OSC}	Oscillator Input Current		V_{OSC} = V_{CC} = 5.5V			100	µA
			V_{OSC} = 0V, V_{CC} = 5.5V	-100			µA
DIGITAL INTERFACE (Data, LE, Clock, F_0LD)							
V_{IH}	High-Level Input Voltage			0.8 V_{CC}			V
V_{IL}	Low-Level Input Voltage					0.2 V_{CC}	V
I_{IH}	High-Level Input Current		V_{IH} = V_{CC} = 5.5V	−1.0		1.0	µA
I_{IL}	Low-Level Input Current		V_{IL} = 0V, V_{CC} = 5.5V	−1.0		1.0	µA
V_{OH}	High-Level Output Voltage		I_{OH} = −500 µA	V_{CC} − 0.4			V
V_{OL}	Low-Level Output Voltage		I_{OL} = 500 µA			0.4	V

(5) Some of the values in this range are illegal divide ratios (B < A). To obtain continuous legal division, the Minimum Divide Ratio must be calculated. Use N ≥ P * (P−1), where P is the value selected for the prescaler.
(6) Refer to Figure 35.
(7) Refer to Figure 34.
(8) Refer to Charge Pump Current Specification Definitions for details on how these measurements are made.
(9) Refer to Figure 36.

Electrical Characteristics (continued)

V_{CC} = V_P RF1 = V_P RF2 = 3.0V, −40°C ≤ T_A ≤ +85°C, unless otherwise specified

Symbol	Parameter		Conditions	Value			Units
				Min	Typ	Max	
MICROWIRE INTERFACE							
t_{CS}	Data to Clock Set Up Time		See (10)	50			ns
t_{CH}	Data to Clock Hold Time		See (10)	10			ns
t_{CWH}	Clock Pulse Width HIGH		See (10)	50			ns
t_{CWL}	Clock Pulse Width LOW		See (10)	50			ns
t_{ES}	Clock to Load Enable Set Up Time		See (10)	50			ns
t_{EW}	Latch Enable Pulse Width		See (10)	50			ns
PHASE NOISE CHARACTERISTICS							
L_N(f) RF1	RF1 Synthesizer Normalized Phase Noise Contribution (11)		TCXO Reference Source ID_0 RF1 Bit = 1		-212.0		dBc/ Hz
L(f) RF1	RF1 Synthesizer Single Side Band Phase Noise Measured	LMX2335U	f_{IN} RF1 = 900 MHz f = 1 kHz Offset $F_{\varphi RF1}$ = 200 kHz Loop Bandwidth = 12 kHz N = 4500 F_{OSC} = 10 MHz V_{OSC} = 0.632 V_{PP} ID_0 RF1 Bit = 1 PWDN RF2 Bit = 1 T_A = +25°C (12)		-85.94		dBc/ Hz
		LMX2336U	f_{IN} RF1 = 1960 MHz f = 1 kHz Offset $F_{\varphi RF1}$ = 200 kHz Loop Bandwidth = 15 kHz N = 9800 F_{OSC} = 10 MHz V_{OSC} = 0.632 V_{PP} ID_0 RF1 Bit = 1 PWDN RF2 Bit = 1 T_A = +25°C (12)		-79.18		dBc/ Hz
L_N(f) RF2	RF2 Synthesizer Normalized Phase Noise Contribution (11)		TCXO Reference Source ID_0 RF2 Bit = 1		-212.0		dBc/ Hz
L(f) RF2	RF2 Synthesizer Single Side Band Phase Noise Measured	LMX2335U	f_{IN} RF2 = 900 MHz f = 1 kHz Offset $F_{\varphi RF2}$ = 200 kHz Loop Bandwidth = 12 kHz N = 4500 F_{OSC} = 10 MHz V_{OSC} = 0.632 V_{PP} ID_0 RF2 Bit = 1 PWDN RF1 Bit = 1 T_A = +25°C (12)		-85.94		dBc/ Hz
		LMX2336U	f_{IN} RF2 = 900 MHz f = 1 kHz Offset $F_{\varphi RF2}$ = 200 kHz Loop Bandwidth = 12 kHz N = 4500 F_{OSC} = 10 MHz V_{OSC} = 0.632 V_{PP} ID_0 RF2 Bit = 1 PWDN RF1 Bit = 1 T_A = +25°C (12)		-85.94		dBc/ Hz

(10) Refer to LMX2335U and LMX2336U Serial Data Input Timing.

(11) Normalized Phase Noise Contribution is defined as : $L_N(f) = L(f) - 20 \log (N) - 10 \log (F_\varphi)$, where L(f) is defined as the single side band phase noise measured at an offset frequency, f, in a 1 Hz bandwidth. The offset frequency, f, must be chosen sufficiently smaller than the PLL's loop bandwidth, yet large enough to avoid substantial phase noise contribution from the reference source. N is the value selected for the feedback divider and F_φ is the RF1/RF2 phase detector comparison frequency.

(12) The synthesizer phase noise is measured with the LMX2335TMEB/LMX2335SLBEB or LMX2336TMEB/LMX2336SLBEB/LMX2336SLEEB Evaluation boards and the HP8566B Spectrum Analyzer.

Typical Performance Characteristics
Sensitivity

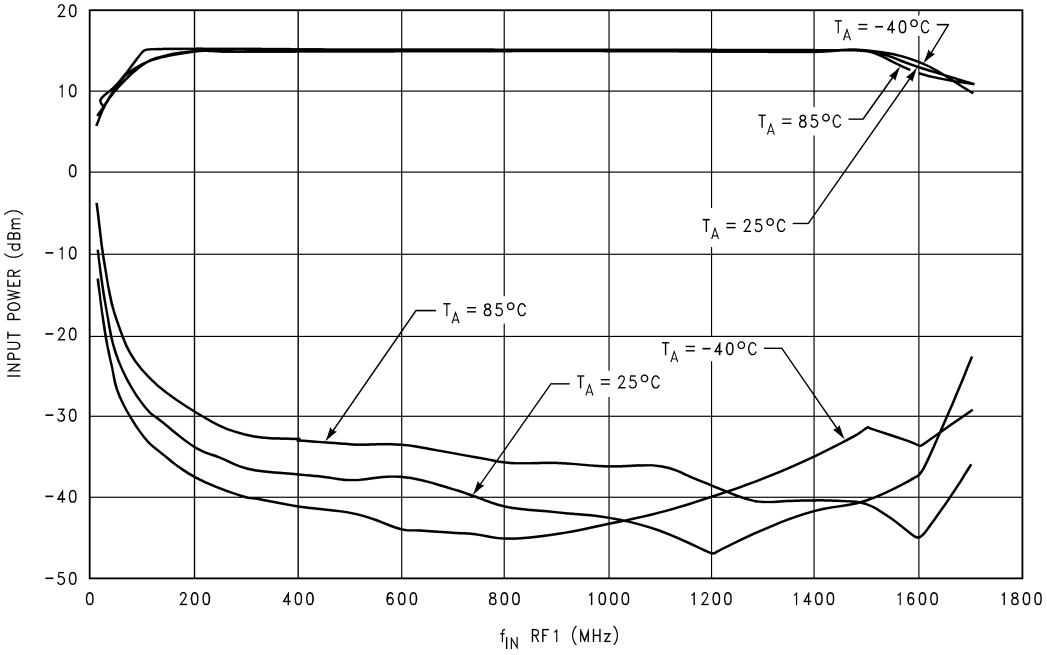


Figure 11. LMX2335U f_{IN} RF1 Input Power Vs Frequency V_{CC} = V_P RF1 = 3.0V

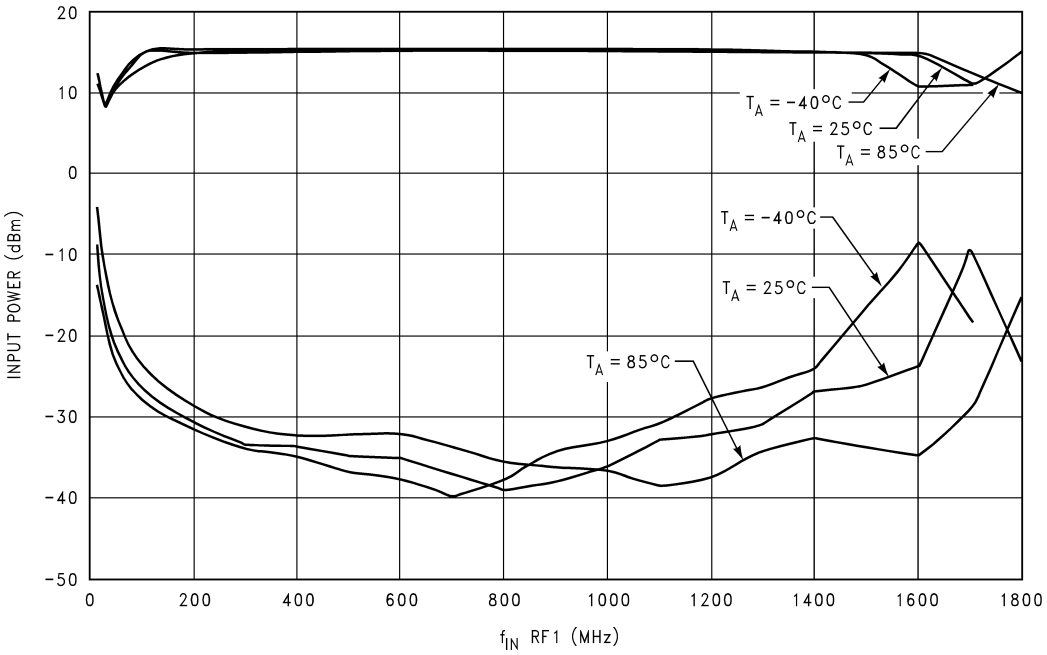


Figure 12. LMX2335U f_{IN} RF1 Input Power Vs Frequency V_{CC} = V_P RF1 = 5.5V

Typical Performance Characteristics
Sensitivity (continued)

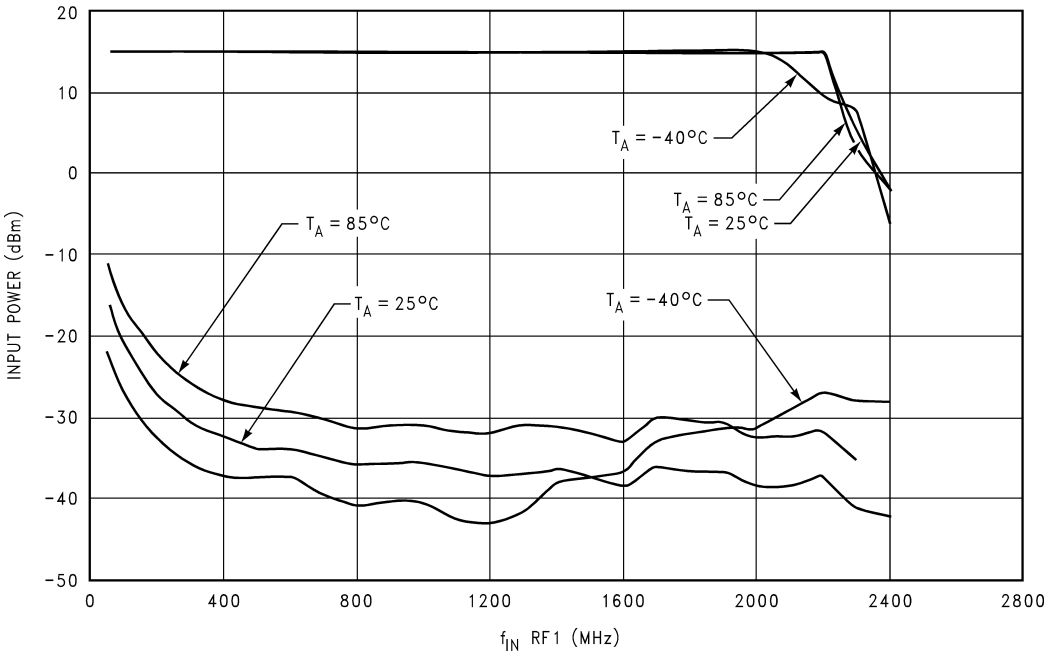


Figure 13. LMX2336U f_{IN} RF1 Input Power Vs Frequency
V_{CC} = V_P RF1 = 3.0V

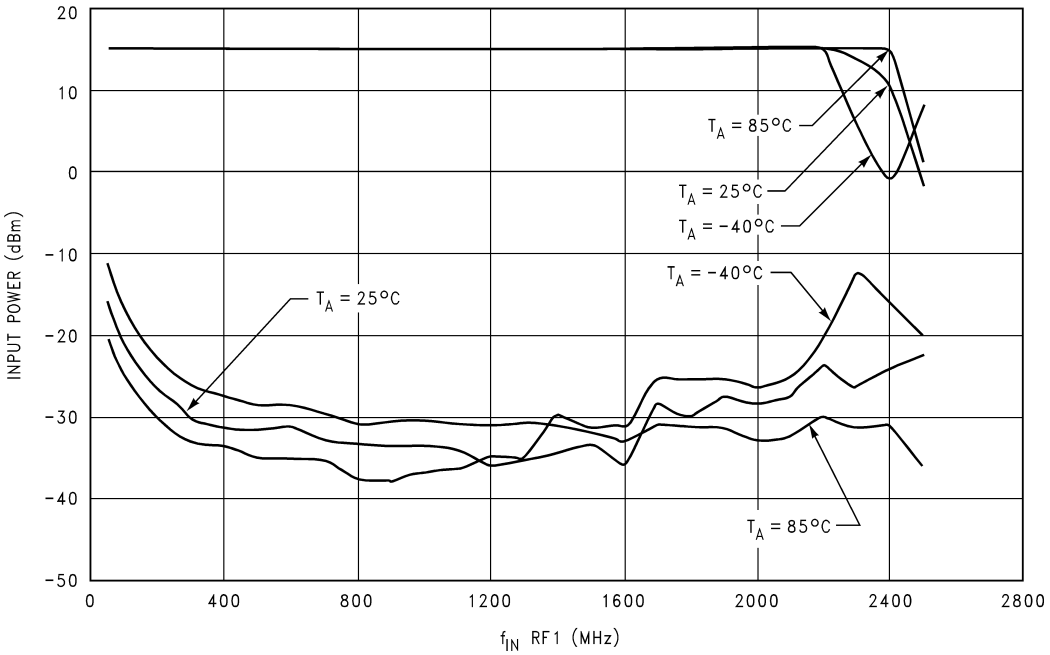


Figure 14. LMX2336U f_{IN} RF1 Input Power Vs Frequency
V_{CC} = V_P RF1 = 5.5V

Typical Performance Characteristics
Sensitivity (continued)

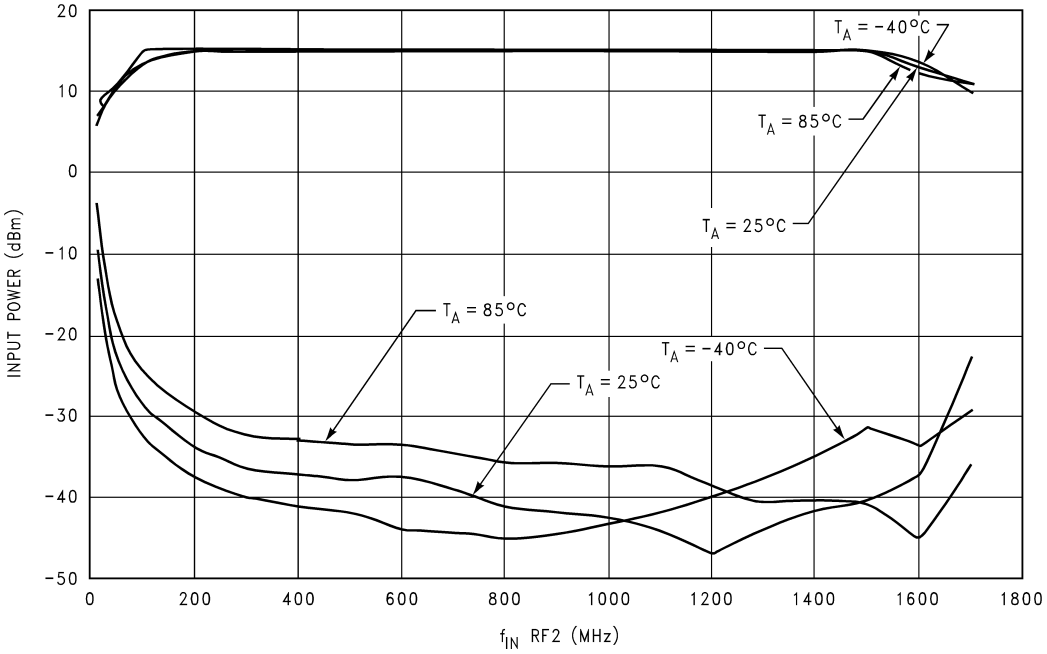


Figure 15. LMX2335U and LMX2336U f_{IN} RF2 Input Power Vs Frequency $V_{CC} = V_P$ RF2 = 3.0V

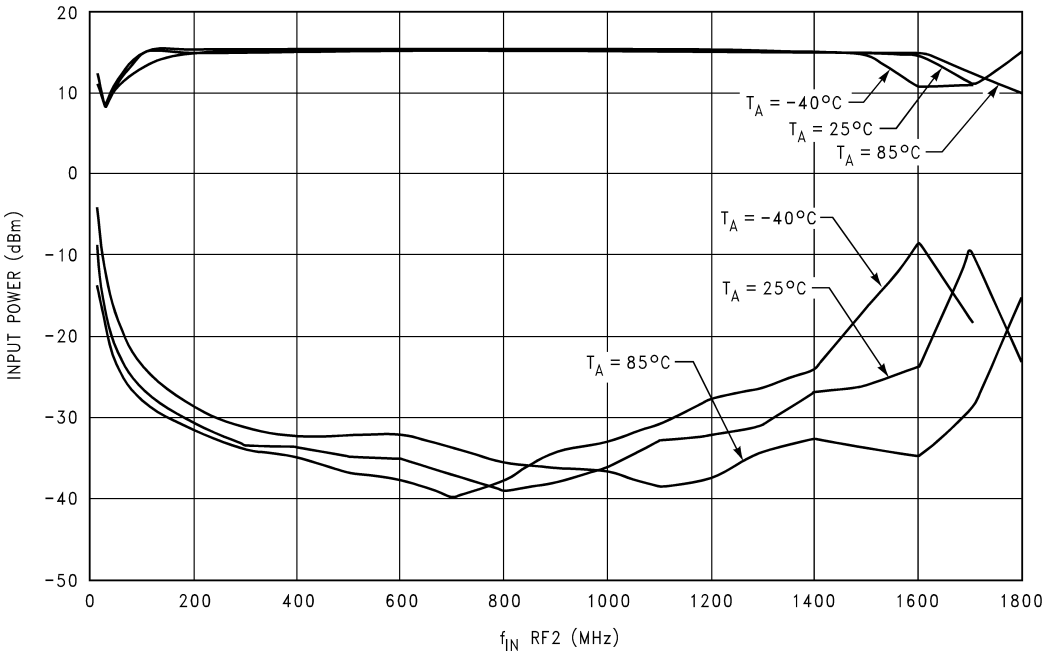


Figure 16. LMX2335U and LMX2336U f_{IN} RF2 Input Power Vs Frequency $V_{CC} = V_P$ RF2 = 5.5V

Typical Performance Characteristics
Sensitivity (continued)

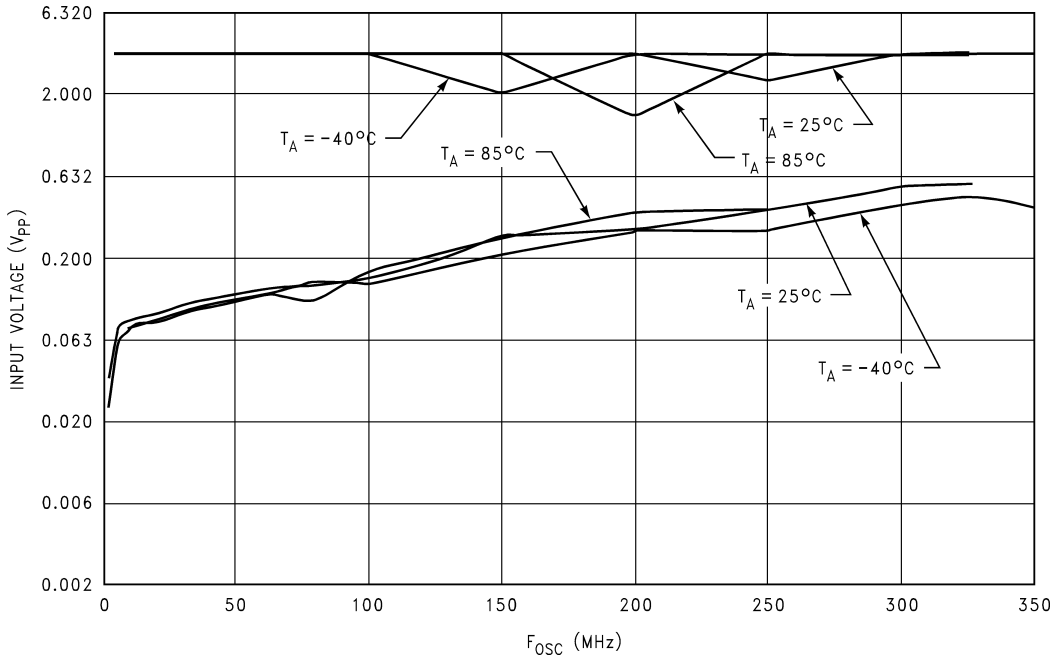


Figure 17. LMX2335U and LMX2336U OSC_{in} Input Voltage Vs Frequency V_{CC} = 3.0V

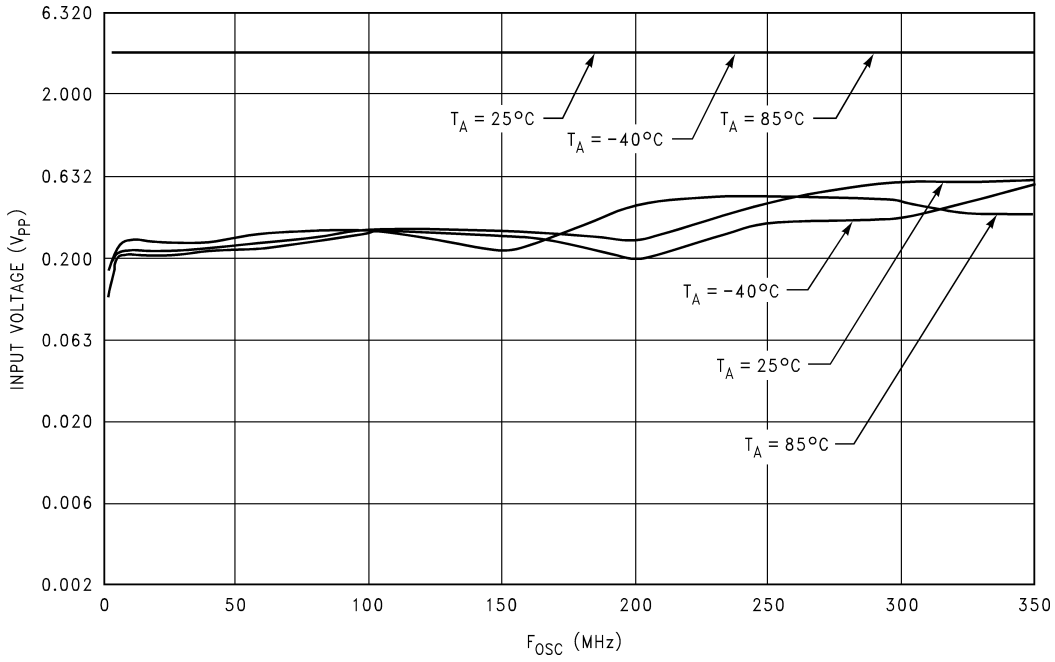


Figure 18. LMX2335U and LMX2336U OSC_{in} Input Voltage Vs Frequency V_{CC} = 5.5V

Typical Performance Characteristics
Charge Pump

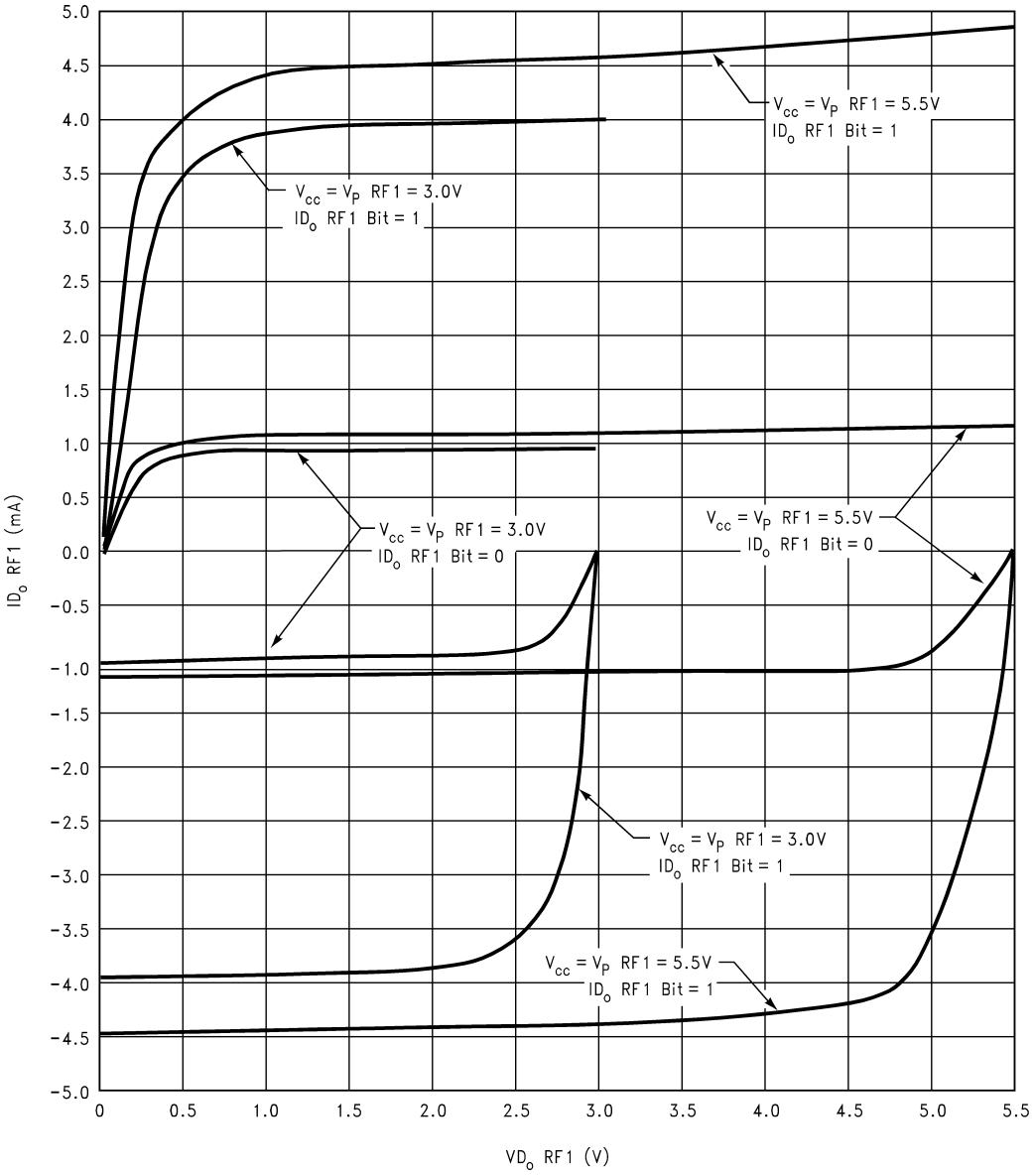


Figure 19. LMX2335U and LMX2336U RF1 Charge Pump Sweeps
−40°C ≤ T_A ≤ +85°C

Typical Performance Characteristics
Charge Pump (continued)

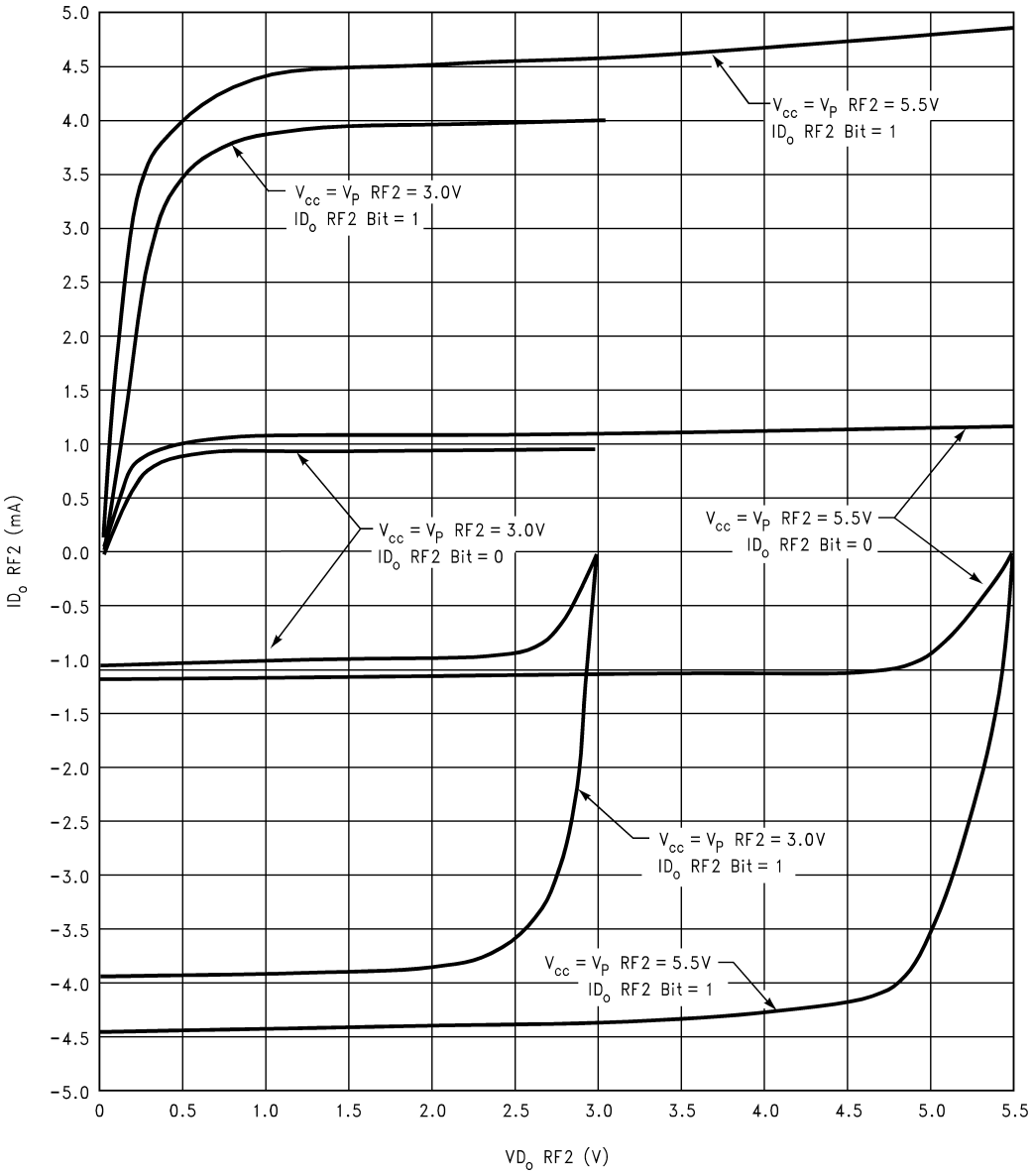
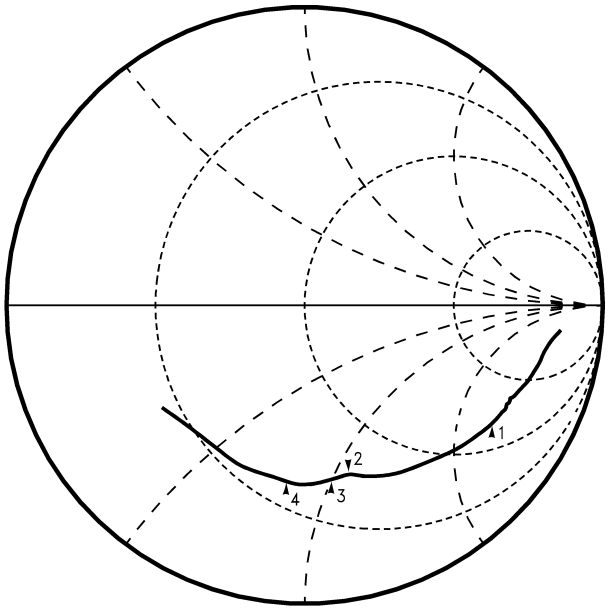


Figure 20. LMX2335U and LMX2336U RF2 Charge Pump Sweeps
−40°C ≤ T_A ≤ +85°C

Typical Performance Characteristics
Input Impedance

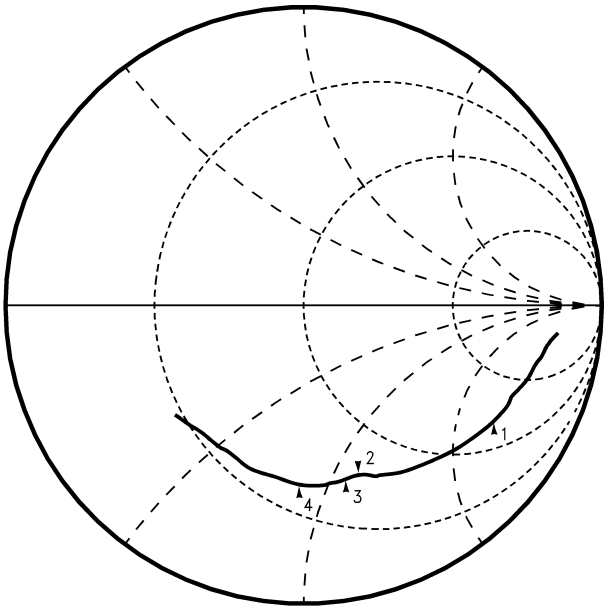
LMX2335U TSSOP and LMX2336U TSSOP
f_{IN} RF1 and f_{IN} RF2 Input Impedance
V_{CC}= 3.0V, T_A = +25°C



Marker 1 = 900 MHz
Marker 2 = 1800 MHz
Marker 3 = 1900 MHz
Marker 4 = 2000 MHz

Figure 21.

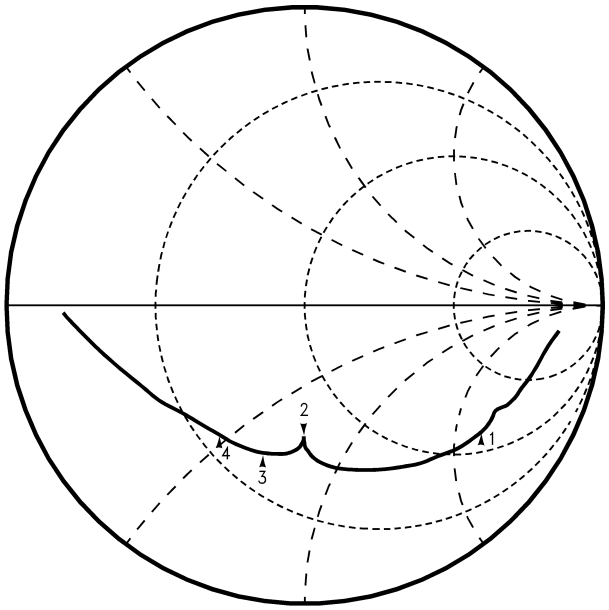
LMX2335U TSSOP and LMX2336U TSSOP
f_{IN} RF1 and f_{IN} RF2 Input Impedance
V_{CC}= 5.5V, T_A = +25°C



Marker 1 = 900 MHz
Marker 2 = 1800 MHz
Marker 3 = 1900 MHz
Marker 4 = 2000 MHz

Figure 22.

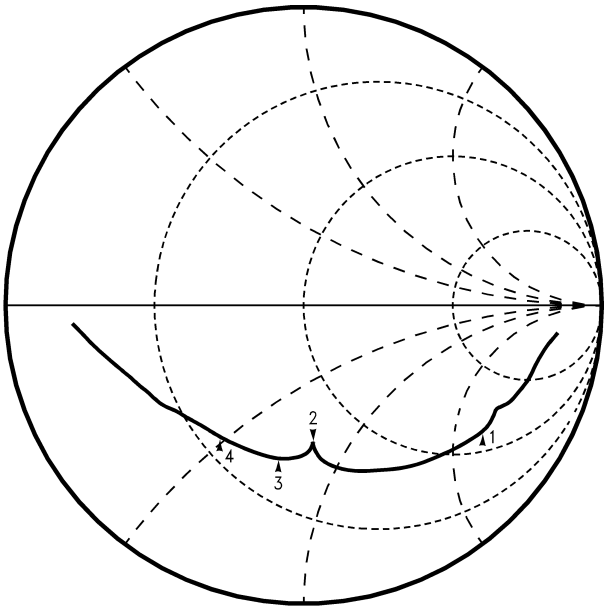
LMX2335U LGA and LMX2336U LGA
f_{IN} RF1 and f_{IN} RF2 Input Impedance
V_{CC}= 3.0V, T_A = +25°C



Marker 1 = 900 MHz
Marker 2 = 1800 MHz
Marker 3 = 1900 MHz
Marker 4 = 2000 MHz

Figure 23.

LMX2335U LGA and LMX2336U LGA
f_{IN} RF1 and f_{IN} RF2 Input Impedance
V_{CC}= 5.5V, T_A = +25°C



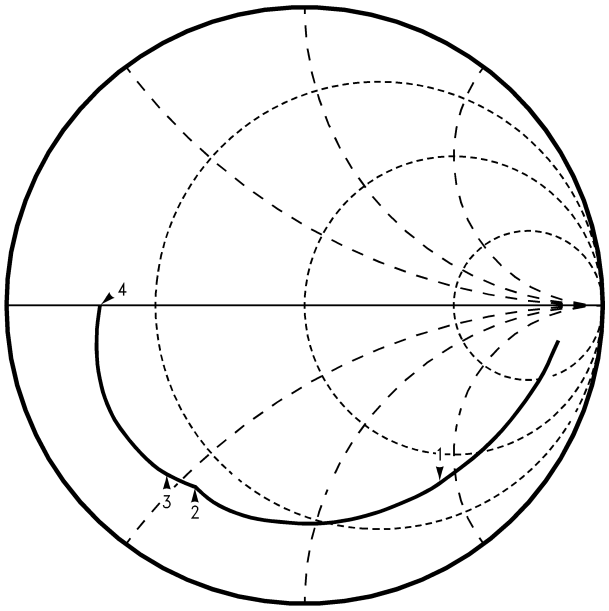
Marker 1 = 900 MHz
Marker 2 = 1800 MHz
Marker 3 = 1900 MHz
Marker 4 = 2000 MHz

Figure 24.

Figure 25. LMX2335U/LMX2336U TSSOP and LMX2335U/LMX2336U LGA f_{IN} RF1 and f_{IN} RF2 Input Impedance Table

	LMX2335U TSSOP/LMX2336U TSSOP (Zf_{IN} RF1 and Zf_{IN} RF2)										LMX2335U CSP/LMX2336U LGA (Zf_{in} RF1 and Zf_{IN} RF2)									
	$V_{CC} = V_P$ RF1 = V_P RF2 = 3.0V (T_A = 25°C)					$V_{CC} = V_P$ RF1 = V_P RF2 = 5.5V (T_A = 25°C)					$V_{CC} = V_P$ RF1 = V_P RF2 = 3.0V (T_A = 25°C)					$V_{CC} = V_P$ RF1 = V_P RF2 = 5.5V (T_A = 25°C)				
f_{IN} (MHz)	|Γ|	∠Γ	Re Zf_{IN} (Ω)	Im Zf_{IN} (Ω)	$\|Zf_{IN}\|$ (Ω)	|Γ|	∠Γ	Re Zf_{IN} (Ω)	Im Zf_{IN} (Ω)	$\|Zf_{IN}\|$ (Ω)	|Γ|	∠Γ	Re Zf_{IN} (Ω)	Im Zf_{IN} (Ω)	$\|Zf_{IN}\|$ (Ω)	|Γ|	∠Γ	Re Zf_{IN} (Ω)	Im Zf_{IN} (Ω)	$\|Zf_{IN}\|$ (Ω)
100	0.862	-6.23	439.774	-319.866	543.798	0.862	-6.07	448.230	-318.841	550.064	0.864	-6.44	431.004	-330.013	542.838	0.864	-6.30	438.240	-327.814	547.281
200	0.834	-9.30	307.614	-272.274	410.803	0.834	-9.00	316.479	-271.581	417.031	0.836	-9.88	291.252	-277.923	402.577	0.836	-9.57	300.190	-277.552	408.838
300	0.820	-12.11	237.700	-249.291	344.452	0.821	-11.66	247.264	-251.098	352.406	0.821	-13.24	215.318	-248.361	328.702	0.821	-12.76	224.624	-249.637	335.819
400	0.808	-15.25	185.048	-227.171	293.001	0.808	-14.61	194.668	-229.054	300.601	0.808	-16.88	163.190	-219.893	273.832	0.808	-16.24	171.345	-222.518	280.844
500	0.796	-18.51	147.785	-203.923	251.843	0.796	-17.66	156.935	-207.313	260.014	0.793	-20.90	126.193	-191.939	229.707	0.794	-20.00	133.885	-196.200	237.528
600	0.781	-21.81	122.091	-181.461	218.710	0.782	-20.70	130.906	-185.850	227.325	0.775	-24.82	102.956	-168.026	197.060	0.777	-23.70	109.531	-172.887	204.663
700	0.765	-24.72	106.107	-163.758	195.129	0.767	-23.45	113.780	-168.514	203.329	0.749	-28.29	90.820	-146.582	172.437	0.752	-27.02	96.279	-151.333	179.363
800	0.760	-28.35	87.984	-150.524	174.352	0.762	-26.97	94.255	-155.481	181.819	0.742	-31.22	79.737	-136.782	158.327	0.746	-29.85	84.470	-141.473	164.772
900	**0.747**	**-32.60**	**73.777**	**-134.500**	**153.406**	**0.750**	**-30.95**	**79.270**	**-139.668**	**160.596**	**0.739**	**-36.04**	**64.577**	**-123.951**	**139.764**	**0.742**	**-34.37**	**69.006**	**-128.610**	**145.954**
1000	0.732	-36.68	64.122	-120.908	136.859	0.735	-34.73	69.215	-126.104	143.851	0.719	-41.44	55.019	-108.415	121.577	0.723	-39.46	58.684	-113.123	127.439
1100	0.717	-41.25	55.780	-108.398	121.908	0.720	-39.12	60.041	-113.215	128.151	0.694	-47.27	48.056	-94.403	105.931	0.698	-45.08	51.159	-98.547	111.035
1200	0.698	-46.24	49.180	-96.605	108.403	0.702	-43.84	52.848	-101.254	114.216	0.669	-53.59	42.269	-82.401	92.610	0.674	-51.01	45.061	-86.388	97.434
1300	0.678	-51.43	43.982	-86.291	96.853	0.683	-48.77	47.173	-90.676	102.212	0.641	-60.42	37.856	-71.653	81.039	0.647	-57.50	40.230	-75.400	85.461
1400	0.663	-56.68	39.397	-77.901	87.296	0.667	-53.71	42.317	-82.070	92.337	0.610	-68.33	34.108	-61.481	70.308	0.613	-64.90	36.477	-64.872	74.424
1500	0.649	-62.08	35.566	-70.500	78.963	0.653	-58.74	38.281	-74.569	83.821	0.577	-77.01	31.049	-52.388	60.898	0.581	-73.18	33.064	-55.554	64.649
1600	0.630	-67.58	32.912	-63.544	71.562	0.634	-63.96	35.335	-67.423	76.121	0.539	-84.86	29.732	-44.952	53.895	0.543	-80.36	31.654	-48.119	57.597
1700	0.608	-72.22	31.565	-57.996	66.030	0.614	-68.51	33.590	-61.632	70.191	0.477	-27.97	100.359	-58.171	115.999	0.487	-84.99	33.106	-42.105	53.562
1800	**0.596**	**-75.66**	**30.440**	**-54.462**	**62.392**	**0.601**	**-71.81**	**32.358**	**-57.943**	**66.366**	**0.455**	**89.90**	**32.829**	**-37.624**	**49.933**	**0.468**	**-85.87**	**33.886**	**-40.554**	**52.847**
1900	**0.598**	**-80.06**	**27.915**	**-51.164**	**58.284**	**0.602**	**-76.22**	**29.678**	**-54.335**	**61.912**	**0.493**	**87.34**	**29.357**	**-38.214**	**48.189**	**0.500**	**-88.90**	**29.576**	**-39.369**	**49.241**
2000	0.607	-85.31	24.914	-47.651	53.771	0.607	-81.32	26.675	-50.603	57.203	0.520	79.89	25.120	-35.225	43.264	0.521	84.05	26.396	-37.576	45.921

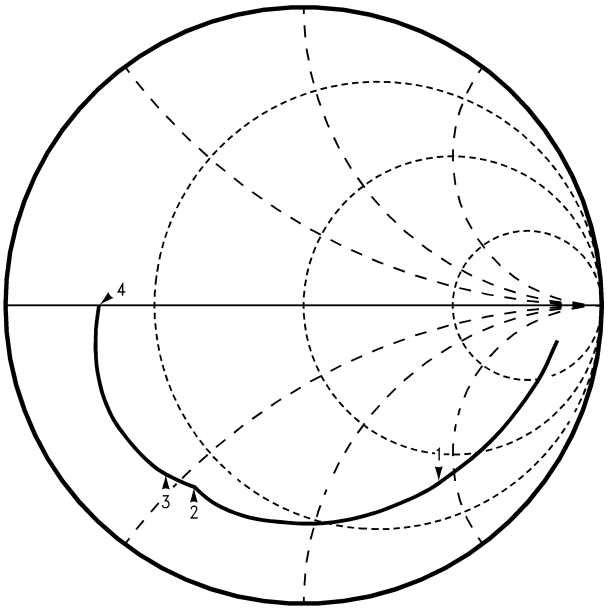
LMX2336U ULGA
f_{IN} RF1 and f_{IN} RF2 Input Impedance
V_{CC}= 3.0V, T_A = +25°C



Marker 1 = 900 MHz
Marker 2 = 1800 MHz
Marker 3 = 1900 MHz
Marker 4 = 2500 MHz

Figure 26.

LMX2336U ULGA
f_{IN} RF1 and f_{IN} RF2 Input Impedance
V_{CC}= 5.5V, T_A = +25°C



Marker 1 = 900 MHz
Marker 2 = 1800 MHz
Marker 3 = 1900 MHz
Marker 4 = 2500 MHz

Figure 27.

Figure 28. LMX2336U ULGA f_{IN} RF1 and f_{IN} RF2 Input Impedance Table

	LMX2336U ULGA Zf_{IN} RF1 and Zf_{IN} RF2									
	$V_{CC} = V_P$ RF1 = V_P RF2 = 3.0V (T_A = 25°C)					$V_{CC} = V_P$ RF1 = V_P RF2 = 5.5V (T_A = 25°C)				
f_{IN} (MHz)	|Γ|	∠Γ	Re Zf_{IN} (Ω)	Im Zf_{IN} (Ω)	|Zf_{IN}| (Ω)	|Γ|	∠Γ	Re Zf_{IN} (Ω)	Im Zf_{IN} (Ω)	|Zf_{IN}| (Ω)
100	0.86	-8.57	335.53	-330.26	470.80	0.86	-8.61	333.98	-330.26	469.70
200	0.83	-13.59	206.36	-258.74	330.95	0.83	-13.55	207.11	-258.92	331.57
300	0.81	-18.53	143.19	-214.36	257.79	0.81	-18.45	144.05	-214.75	258.59
400	0.80	-23.67	103.09	-183.95	210.86	0.80	-23.63	103.36	-184.12	211.15
500	0.79	-29.24	76.58	-157.24	174.89	0.79	-29.07	77.30	-157.87	175.78
600	0.77	-34.87	61.79	-133.64	147.24	0.77	-34.64	62.46	-134.31	148.12
700	0.76	-40.52	50.03	-116.97	127.23	0.76	-40.33	50.42	-117.43	127.80
800	0.76	-46.45	39.82	-103.86	111.24	0.76	-46.18	40.22	-104.42	111.89
900	**0.75**	**-53.27**	**32.87**	**-90.33**	**96.13**	**0.75**	**-52.89**	**33.27**	**-90.97**	**96.86**
1000	0.74	-60.04	27.98	-79.30	84.09	0.74	-59.70	28.24	-79.77	84.63
1100	0.73	-66.62	24.49	-70.27	74.42	0.73	-66.10	24.81	-70.90	75.11
1200	0.73	-74.07	20.63	-62.00	65.34	0.73	-73.57	20.85	-62.52	65.91
1300	0.73	-81.67	17.67	-54.66	57.45	0.73	-81.15	17.85	-55.13	57.95
1400	0.73	-89.59	15.34	-47.95	50.34	0.73	-88.94	15.51	-48.47	50.89
1500	0.73	-97.85	13.48	-41.75	43.87	0.73	-97.12	13.63	-42.27	44.41
1600	0.73	-106.72	11.96	-35.80	37.74	0.73	-105.87	12.09	-36.34	38.30
1700	0.72	-115.82	11.22	-30.21	32.22	0.72	-114.76	11.35	-30.82	32.84
1800	**0.70**	**-123.41**	**11.28**	**-25.85**	**28.20**	**0.70**	**-122.28**	**11.40**	**-26.45**	**28.80**
1900	**0.72**	**-130.68**	**9.80**	**-22.22**	**24.29**	**0.72**	**-129.92**	**9.86**	**-22.61**	**24.66**
2000	0.74	-140.55	8.41	-17.48	19.39	0.74	-139.88	8.44	-17.80	19.70
2100	0.74	-150.74	7.97	-12.74	15.03	0.74	-150.01	7.99	-13.07	15.32
2200	0.73	-160.86	8.02	-8.22	11.48	0.73	-160.03	8.04	-8.58	11.76
2300	0.71	-170.43	8.54	-4.06	9.46	0.71	-169.62	8.55	-4.41	9.62
2400	0.69	-179.08	9.17	-0.39	9.18	0.69	-178.32	9.17	-0.71	9.20
2500	**0.67**	**172.38**	**9.92**	**3.20**	**10.43**	**0.67**	**173.11**	**9.91**	**2.89**	**10.33**

Figure 29. LMX2335U TSSOP and LMX2336U TSSOP
OSC_{in} Input Impedance Vs Frequency
T_A = +25°C

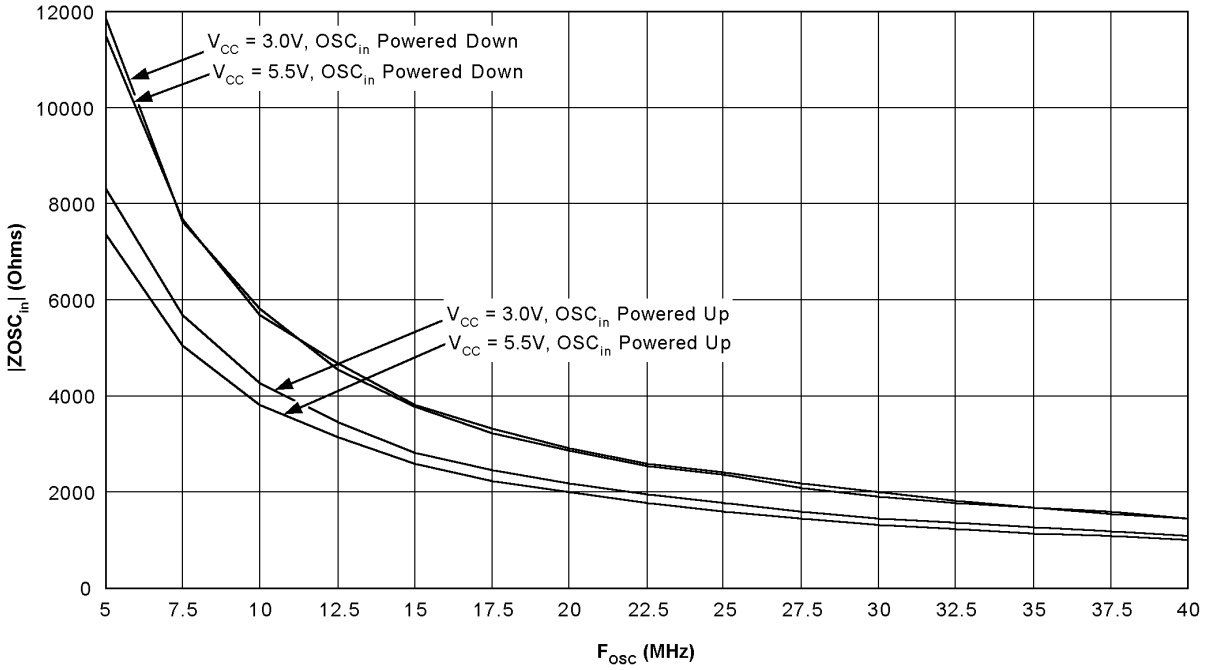


Figure 30. LMX2335U LGA and LMX2336U LGA
OSC_{in} Input Impedance Vs Frequency
T_A = +25°C

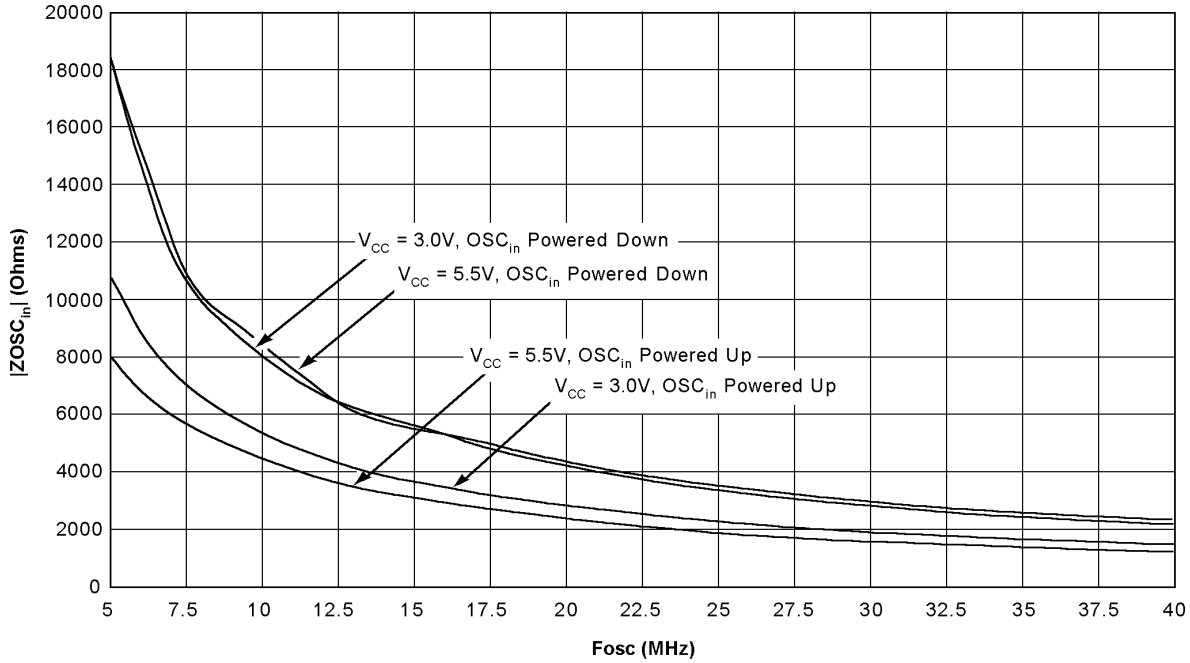


Figure 31. LMX2335U/LMX2336U TSSOP and LMX2335U/LMX2336U LGA OSC_{in} Input Impedance Table

	LMX2335U TSSOP/LMX2336U TSSOP $ZOSC_{in}$												LMX2335U CSP/LMX2336U LGA $ZOSC_{in}$											
	V_{CC} = 3.0V (T_A = 25°C)						V_{CC} = 5.5V (T_A = 25°C)						V_{CC} = 3.0V (T_A = 25°C)						V_{CC} = 5.5V (T_A = 25°C)					
	OSC_{in} BUFFER POWERED ON			OSC_{in} BUFFER POWERED DOWN			OSC_{in} BUFFER POWERED ON			OSC_{in} BUFFER POWERED DOWN			OSC_{in} BUFFER POWERED ON			OSC_{in} BUFFER POWERED DOWN			OSC_{in} BUFFER POWERED DOWN			OSC_{in} BUFFER POWERED DOWN		
F_{OSC} (MHz)	Re $ZOSC_{in}$ (Ω)	Im $ZOSC_{in}$ (Ω)	$\|ZOSC_{in}\|$ (Ω)	Re $ZOSC_{in}$ (Ω)	Im $ZOSC_{in}$ (Ω)	$\|ZOSC_{in}\|$ (Ω)	Re $ZOSC_{in}$ (Ω)	Im $ZOSC_{in}$ (Ω)	$\|ZOSC_{in}\|$ (Ω)	Re $ZOSC_{in}$ (Ω)	Im $ZOSC_{in}$ (Ω)	$\|ZOSC_{in}\|$ (Ω)	Re $ZOSC_{in}$ (Ω)	Im $ZOSC_{in}$ (Ω)	$\|ZOSC_{in}\|$ (Ω)	Re $ZOSC_{in}$ (Ω)	Im $ZOSC_{in}$ (Ω)	$\|ZOSC_{in}\|$ (Ω)	Re $ZOSC_{in}$ (Ω)	Im $ZOSC_{in}$ (Ω)	$\|ZOSC_{in}\|$ (Ω)	Re $ZOSC_{in}$ (Ω)	Im $ZOSC_{in}$ (Ω)	$\|ZOSC_{in}\|$ (Ω)
5.0	2291.113	-8000.376	8321.972	985.863	-11825.209	11866.234	2832.878	-6774.525	7342.982	1246.071	-11436.600	11504.282	5107.688	-9526.374	10809.27	4154.104	-18073.24	18544.50	4698.960	-6544.007	8056.318	4154.104	-18073.24	18544.50
7.5	1202.389	-5538.197	5667.218	294.460	-7640.322	7645.994	1267.479	-4861.053	5023.579	520.098	-7675.309	7692.910	2249.061	-6544.475	6920.146	1571.331	-10205.48	10325.74	2626.329	-4998.105	5646.119	1812.311	-10602.90	10756.68
10.0	791.970	-4218.658	4292.353	266.942	-5793.060	5799.207	739.926	-3754.673	3826.886	484.656	-5659.675	5680.388	1664.886	-5170.920	5432.335	1066.661	-8350.651	8418.499	1625.723	-4209.219	4512.261	976.808	-8800.590	8854.633
12.5	527.664	-3418.978	3459.456	197.874	-4547.094	4551.397	544.280	-3078.845	3126.584	196.239	-4665.169	4669.295	1048.750	-4245.537	4373.153	727.756	-6341.105	6382.730	1182.342	-3466.982	3663.045	899.697	-6248.932	6313.367
15.0	343.020	-2817.993	2838.794	161.801	-3761.566	3765.044	416.644	-2536.243	2570.238	160.236	-3799.626	3803.003	872.629	-3558.426	3663.861	442.319	-5658.273	5675.536	856.006	-2977.931	3098.519	436.542	-5712.788	5729.443
17.5	316.446	-2439.647	2460.085	141.326	-3203.351	3206.467	309.867	-2192.584	2214.372	196.400	-3305.741	3311.570	691.377	-3158.030	3232.825	296.061	-4799.917	4809.039	697.781	-2605.886	2697.692	309.618	-4985.007	4994.613
20.0	228.526	-2179.146	2191.096	63.505	-2879.931	2880.631	227.640	-1974.267	1987.347	73.816	-2917.281	2918.215	559.597	-2791.912	2847.441	194.872	-4242.475	4246.948	554.417	-2318.961	2384.315	303.378	-4345.597	4356.174
22.5	211.659	-1932.535	1944.091	98.108	-2543.330	2545.222	214.873	-1741.101	1754.310	103.131	-2608.411	2610.449	442.147	-2512.522	2551.129	186.123	-3777.847	3782.429	485.437	-2041.170	2098.100	168.163	-3935.873	3939.464
25.0	163.618	-1762.903	1770.480	89.270	-2340.221	2341.923	169.812	-1589.814	1598.857	67.246	-2388.967	2389.913	444.524	-2261.024	2304.307	170.072	-3402.400	3406.648	424.599	-1865.270	1912.986	174.460	-3506.895	3511.232
27.5	163.733	-1589.620	1598.030	69.675	-2106.253	2107.405	160.401	-1435.713	1444.646	69.923	-2161.702	2162.832	367.245	-2060.013	2092.491	191.739	-3114.867	3120.763	379.086	-1714.793	1756.195	159.273	-3213.478	3217.422
30.0	148.446	-1463.071	1470.583	81.310	-1926.889	1928.604	141.501	-1314.929	1322.520	67.843	-1984.769	1985.928	356.692	-1893.442	1926.747	188.280	-2837.317	2843.557	357.340	-1567.979	1608.182	157.424	-2934.223	2938.443
32.5	130.683	-1340.206	1346.562	46.548	-1750.824	1751.443	121.612	-1213.403	1219.482	37.610	-1812.700	1813.090	348.916	-1776.540	1810.480	129.014	-2664.486	2667.608	332.065	-1461.571	1498.818	157.389	-2780.469	2784.920
35.0	126.059	-1255.034	1261.349	38.046	-1662.230	1662.666	116.385	-1131.429	1137.399	45.646	-1689.748	1690.365	302.932	-1648.356	1675.961	95.424	-2471.170	2473.011	299.913	-1358.120	1390.840	125.530	-2600.472	2603.500
37.5	115.848	-1178.954	1184.632	37.202	-1547.816	1548.263	109.381	-1064.461	1070.066	36.346	-1591.439	1591.854	300.020	-1549.601	1578.377	117.732	-2331.694	2334.664	284.654	-1274.370	1305.774	144.727	-2419.904	2424.228
40.0	108.280	-1089.931	1095.296	36.351	-1439.460	1439.919	100.267	-985.544	990.631	39.180	-1470.482	1471.004	281.334	-1454.298	1481.260	81.318	-2182.473	2183.987	273.323	-1199.918	1230.654	152.283	-2302.913	2307.942

Figure 32. LMX2336U ULGA
OSC_{in} Input Impedance Vs Frequency
T_A = +25°C

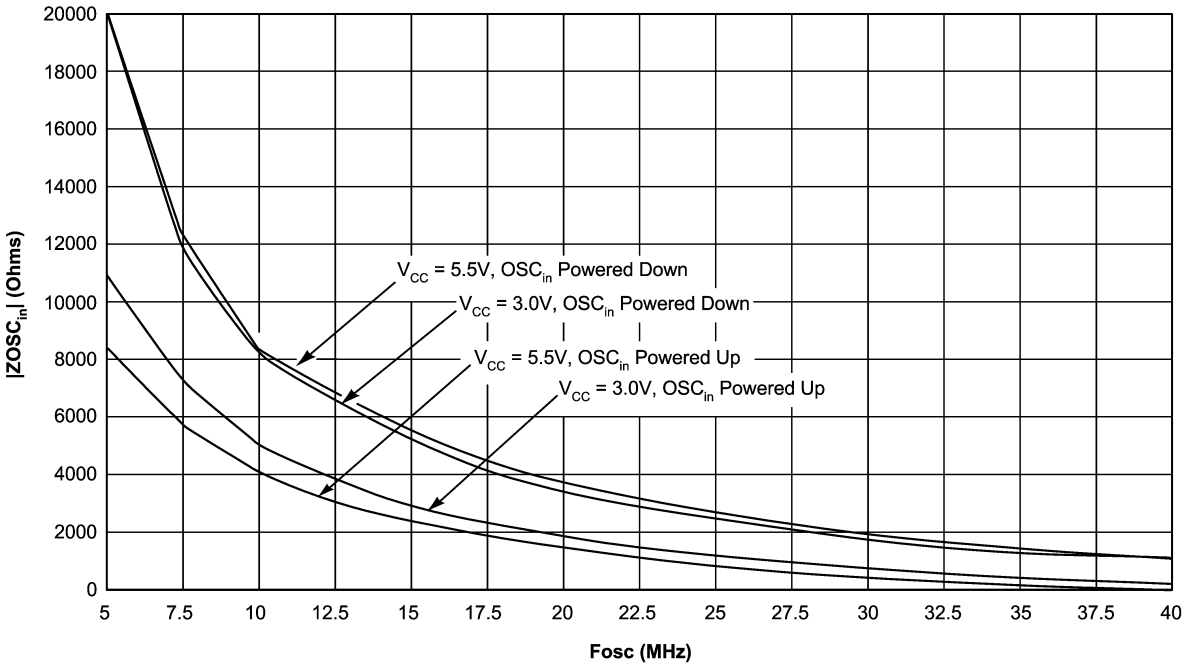
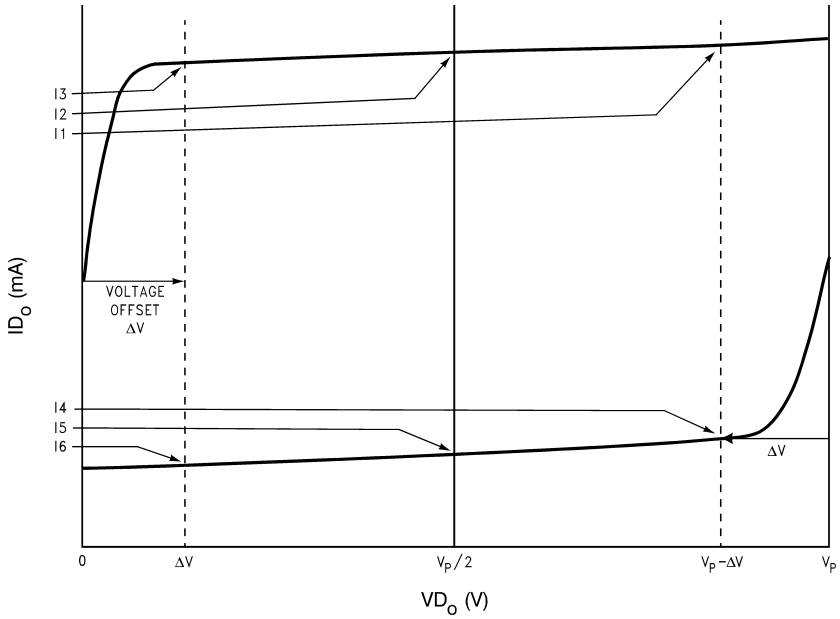


Figure 33. LMX2336U ULGA OSC_{in} Input Impedance Table

	LMX2336U ULGA $ZOSC_{in}$											
	V_{CC} = 3.0V (T_A = 25°C)						V_{CC} = 5.5V (T_A = 25°C)					
	OSC_{in} BUFFER POWERED UP			OSC_{in} BUFFER POWERED DOWN			OSC_{in} BUFFER POWERED UP			OSC_{in} BUFFER POWERED DOWN		
F_{OSC} (MHz)	Re $ZOSC_{in}$ (Ω)	Im $ZOSC_{in}$ (Ω)	$\lvert ZOSC_{in} \rvert$ (Ω)	Re $ZOSC_{in}$ (Ω)	Im $ZOSC_{in}$ (Ω)	$\lvert ZOSC_{in} \rvert$ (Ω)	Re $ZOSC_{in}$ (Ω)	Im $ZOSC_{in}$ (Ω)	$\lvert ZOSC_{in} \rvert$ (Ω)	Re $ZOSC_{in}$ (Ω)	Im $ZOSC_{in}$ (Ω)	$\lvert ZOSC_{in} \rvert$ (Ω)
5.0	5918.57	-9897.80	11532.39	1822.62	-19947.73	20030.82	4982.73	-7668.32	9144.98	2478.02	-19591.11	19747.21
7.5	3097.46	-7441.43	8060.35	2238.93	-12114.22	12319.38	2742.97	-6062.16	6653.85	2483.54	-12531.99	12775.71
10.0	1695.22	-5720.83	5966.72	998.16	-9046.84	9101.74	1582.29	-4875.36	5125.70	1064.38	-9063.97	9126.25
12.5	1241.03	-4759.14	4918.29	660.39	-7338.93	7368.58	1150.39	-4034.66	4195.46	621.48	-7679.86	7704.97
15.0	820.55	-3955.33	4039.55	471.57	-6142.40	6160.48	861.48	-3448.80	3554.76	591.34	-6481.87	6508.79
17.5	646.18	-3417.20	3477.76	317.24	-5165.41	5175.14	599.49	-3009.04	3068.18	154.67	-5518.01	5520.17
20.0	520.20	-3006.22	3050.90	223.35	-4567.95	4573.41	491.78	-2647.38	2692.67	120.99	-4867.07	4868.57
22.5	459.63	-2666.05	2705.38	219.57	-4040.96	4046.92	396.64	-2342.62	2375.96	137.85	-4301.63	4303.84
25.0	391.21	-2398.19	2429.89	172.20	-3664.77	3668.81	323.46	-2108.25	2132.92	89.00	-3864.60	3865.62
27.5	348.79	-2210.66	2238.01	169.02	-3291.50	3295.84	312.14	-1920.70	1945.90	114.48	-3476.68	3478.56
30.0	285.07	-1996.71	2016.96	110.02	-3005.42	3007.43	260.59	-1763.82	1782.97	121.11	-3185.26	3187.56
32.5	267.83	-1847.30	1866.61	117.14	-2725.46	2727.97	239.41	-1612.35	1630.02	111.70	-2876.34	2878.50
35.0	252.27	-1719.32	1737.73	114.38	-2558.44	2561.00	222.16	-1503.76	1520.08	115.42	-2690.37	2692.84
37.5	224.94	-1639.80	1655.15	70.31	-2408.64	2409.67	191.46	-1422.88	1435.71	48.06	-2550.41	2550.86
40.0	208.96	-1512.91	1527.27	76.50	-2242.79	2244.09	180.75	-1329.24	1341.47	72.61	-2353.73	2354.85

Charge Pump Current Specification Definitions



I1 = Charge Pump Sink Current at $VD_o = V_P - \Delta V$
I2 = Charge Pump Sink Current at $VD_o = V_P/2$
I3 = Charge Pump Sink Current at $VD_o = \Delta V$
I4 = Charge Pump Source Current at $VD_o = V_P - \Delta V$
I5 = Charge Pump Source Current at $VD_o = V_P/2$
I6 = Charge Pump Source Current at $VD_o = \Delta V$
ΔV = Voltage offset from the positive and negative rails. Dependent on the VCO tuning range relative to V_{CC} and GND. Typical values are between 0.5V and 1.0V.
V_P refers to either V_P RF1 or V_P RF2
VD_o refers to either VD_o RF1 or VD_o RF2
ID_o refers to either ID_o RF1 or ID_o RF2

Charge Pump Output Current Magnitude Variation Vs Charge Pump Output Voltage

$$ID_o \text{ Vs } VD_o = \frac{(|I1| - |I3|)}{(|I1| + |I3|)} \times 100\% = \frac{(|I4| - |I6|)}{(|I4| + |I6|)} \times 100\% \quad (1)$$

Charge Pump Output Sink Current Vs Charge Pump Output Source Current Mismatch

$$ID_o \text{ SINK Vs } ID_o \text{ SOURCE} = \frac{|I2| - |I5|}{\frac{1}{2}(|I2| + |I5|)} \times 100\% \quad (2)$$

Charge Pump Output Current Magnitude Variation Vs Temperature

$$ID_o \text{ Vs } T_A = \frac{|I_2|\Big|_{T_A} - |I_2|\Big|_{T_A = 25°C}}{|I_2|\Big|_{T_A = 25°C}} \times 100\% = \frac{|I_5|\Big|_{T_A} - |I_5|\Big|_{T_A = 25°C}}{|I_5|\Big|_{T_A = 25°C}} \times 100\% \quad (3)$$

Test Setups

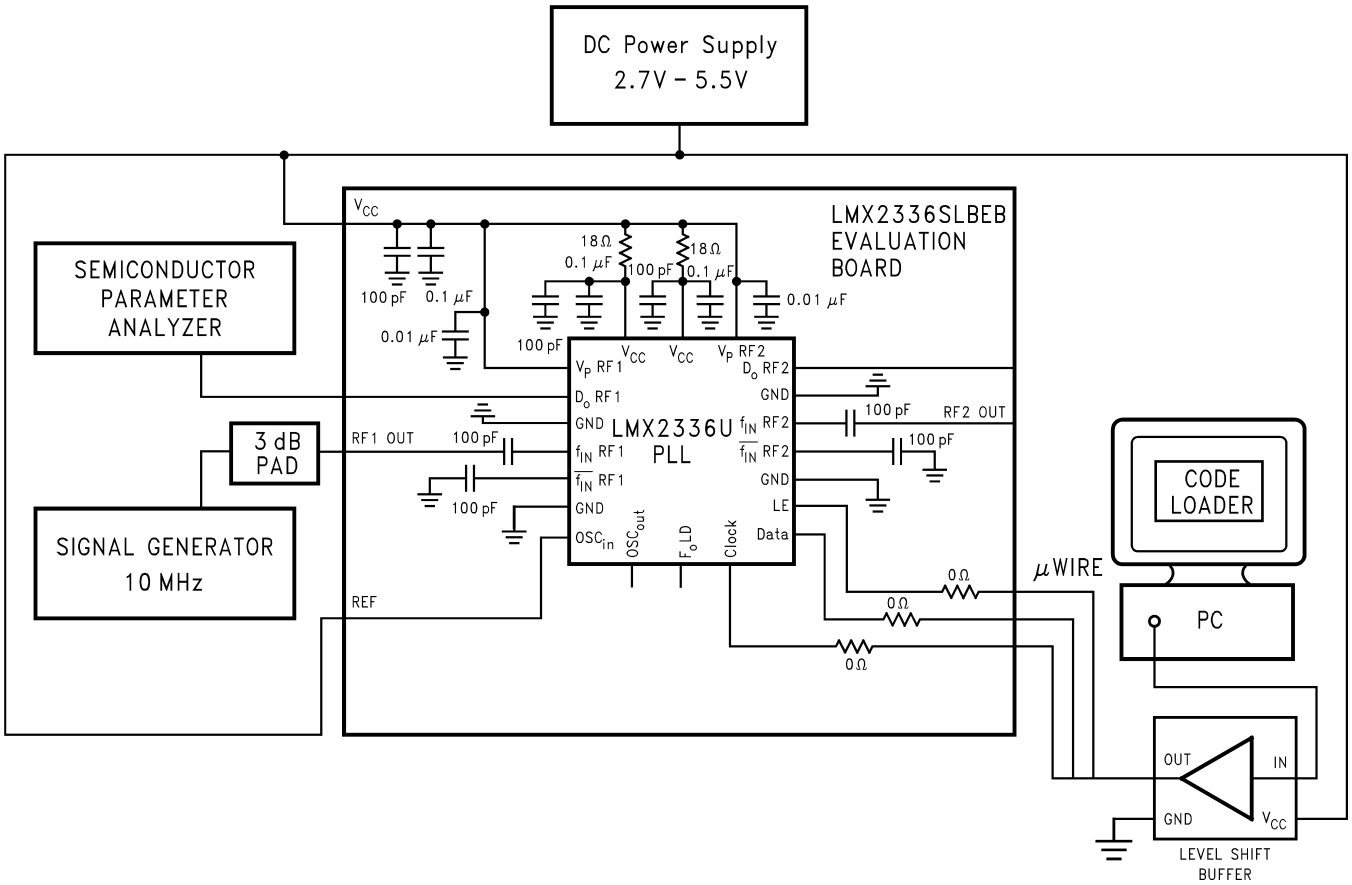


Figure 34. LMX2335U and LMX2336U Charge Pump Test Setup

The block diagram above (Figure 34) illustrates the setup required to measure the LMX2336U device's RF1 charge pump sink current. The same setup is used for the LMX2336TMEB/ LMX2336SLEEB Evaluation Boards. The RF2 charge pump measurement setup is similar to the RF1 charge pump measurement setup. The purpose of this test is to assess the functionality of the RF1 charge pump.

This setup uses an open loop configuration. A power supply is connected to V_{cc} and swept from 2.7V to 5.5V. By means of a signal generator, a 10 MHz signal is typically applied to the f_{IN} RF1 pin. The signal is one of two inputs to the phase detector. The 3 dB pad provides a 50 Ω match between the PLL and the signal generator. The OSC_{in} pin is tied to V_{cc}. This establishes the other input to the phase detector. Alternatively, this input can be tied directly to the ground plane. With the D_o RF1 pin connected to a Semiconductor Parameter Analyzer in this way, the sink, source, and TRI-STATE currents can be measured by simply toggling the **Phase Detector Polarity** and **Charge Pump State** states in Code Loader. Similarly, the LOW and HIGH currents can be measured by switching the **Charge Pump Gain's** state between **1X** and **4X** in Code Loader.

Let F_r represent the frequency of the signal applied to the OSC_{in} pin, which is simply zero in this case (DC), and let F_p represent the frequency of the signal applied to the f_{IN} RF1 pin. The phase detector is sensitive to the rising edges of F_r and F_p. Assuming positive VCO characteristics; the charge pump turns ON and sinks current when the first rising edge of F_p is detected. Since F_r has no rising edge, the charge pump continues to sink current indefinitely.

Toggling the **Phase Detector Polarity** state to negative VCO characteristics allows the measurement of the RF1 charge pump source current. Likewise, selecting **TRI-STATE** (TRI-STATE ID_o RF1 Bit = 1) for **Charge Pump State** in Code Loader facilitates the measurement of the TRI-STATE current.

The measurements are repeated at different temperatures, namely T_A = -40°C, +25°C, and +85°C.

The LMX2335U charge pump test setup is very much similar to the above test setup.

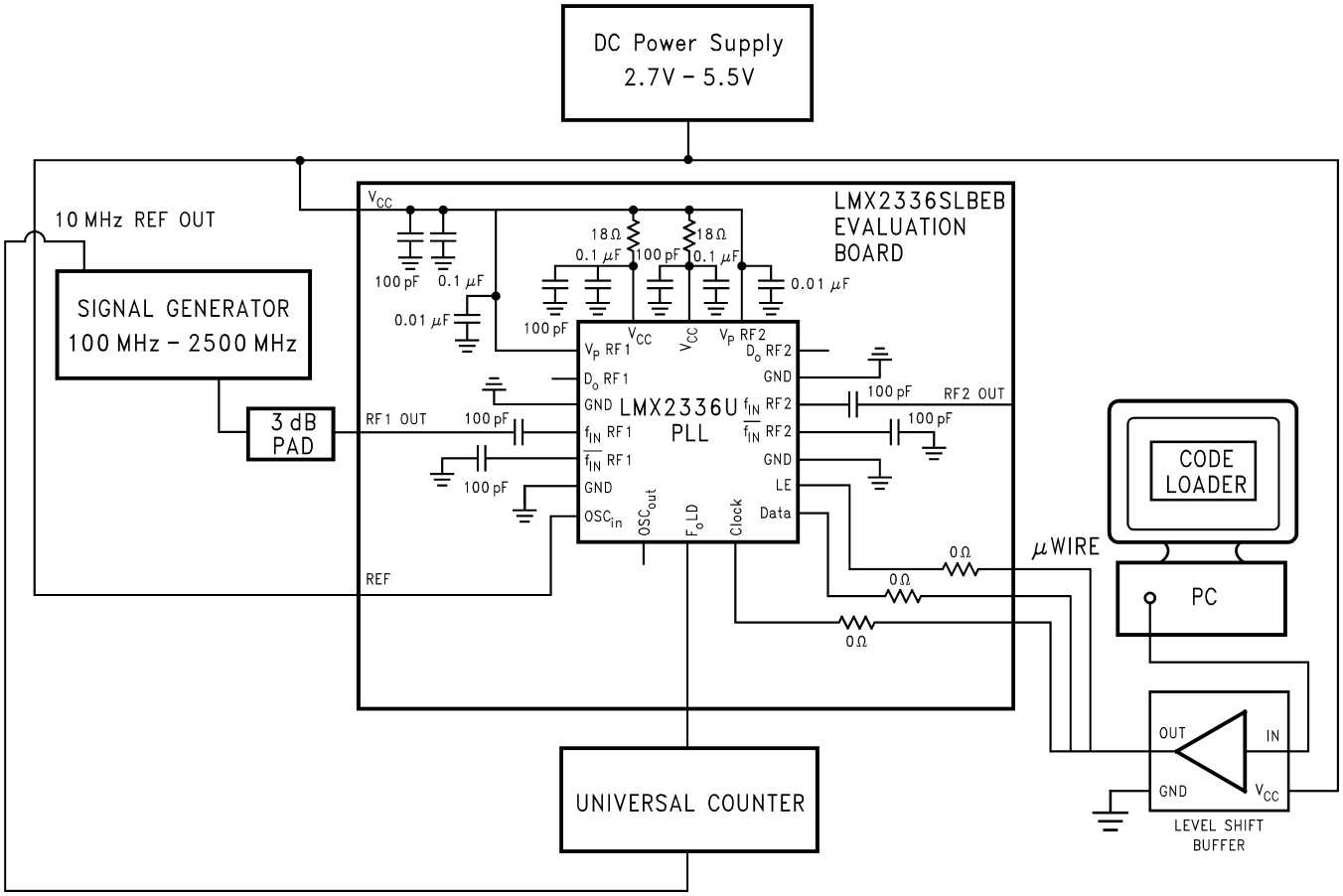


Figure 35. LMX2335U and LMX2336U f_{IN} Sensitivity Test Setup

The block diagram above (Figure 35) illustrates the setup required to measure the LMX2336U device's RF1 input sensitivity level. The same setup is used for the LMX2336TMEB/ LMX2336SLEEB Evaluation Boards. The RF2 input sensitivity test setup is similar to the RF1 sensitivity test setup. The purpose of this test is to measure the acceptable signal level to the f_{IN} RF1 input of the PLL chip. Outside the acceptable signal range, the feedback divider begins to divide incorrectly and miscount the frequency.

The setup uses an open loop configuration. A power supply is connected to V_{cc} and the bias voltage is swept from 2.7V to 5.5V. The RF2 PLL is powered down (PWDN RF2 Bit = 1). By means of a signal generator, an RF signal is applied to the f_{IN} RF1 pin. The 3 dB pad provides a 50 Ω match between the PLL and the signal generator. The OSC_{in} pin is tied to V_{cc}. The N value is typically set to 10000 in Code Loader, i.e. RF1 N_CNTRB Word = 156 and RF1 N_CNTRA Word = 16 for PRE RF1 Bit = 0. The feedback divider output is routed to the F_oLD pin by selecting the **RF1 PLL N Divider Output** word (F_oLD Word = 6 or 14) in Code Loader. A Universal Counter is connected to the F_oLD pin and tied to the 10 MHz reference output of the signal generator. The output of the feedback divider is thus monitored and should be equal to f_{IN} RF1 / N.

The f_{IN} RF1 input frequency and power level are then swept with the signal generator. The measurements are repeated at different temperatures, namely T_A = -40°C, +25°C, and +85°C. Sensitivity is reached when the frequency error of the divided RF input is greater than or equal to 1 Hz. The power attenuation from the cable and the 3 dB pad must be accounted for. The feedback divider will actually miscount if too much or too little power is applied to the f_{IN} RF1 input. Therefore, the allowed input power level will be bounded by the upper and lower sensitivity limits. In a typical application, if the power level to the f_{IN} RF1 input approaches the sensitivity limits, this can introduce spurs and degradation in phase noise. When the power level gets even closer to these limits, or exceeds it, then the RF1 PLL loses lock.

The LMX2335U f_{IN} sensitivity test setup is very much similar to the above test setup.

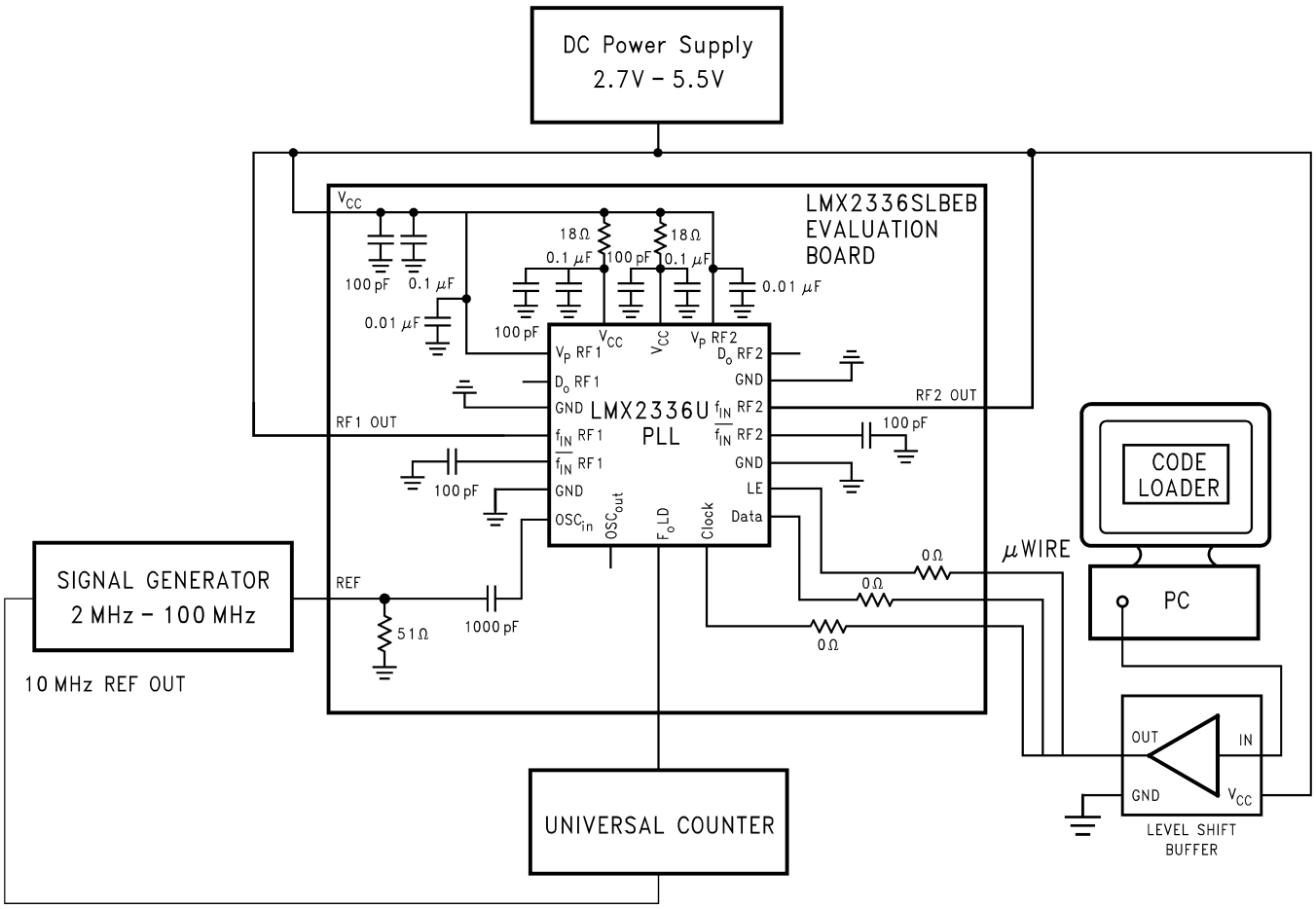


Figure 36. LMX2335U and LMX2336U OSC_{in} Sensitivity Test Setup

The block diagram above (Figure 36) illustrates the setup required to measure the LMX2336U device's OSC_{in} buffer sensitivity level. The same setup is used for the LMX2336TMEB/ LMX2336SLEEB Evaluation Boards. This setup is similar to the f_{IN} sensitivity setup except that the signal generator is now connected to the OSC_{in} pin and both f_{IN} pins are tied to V_{CC}. The 51 Ω shunt resistor matches the OSC_{in} input to the signal generator. The R counter is typically set to 1000, i.e. RF1 R_CNTR Word = 1000 or RF2 R_CNTR Word = 1000. The reference divider output is routed to the F_oLD pin by selecting the **RF1 PLL R Divider Output** word (F_oLD Word = 2 or 10) or the **RF2 PLL R Divider Output** word (F_oLD Word = 1 or 9) in Code Loader. Similarly, a Universal Counter is connected to the F_oLD pin and is tied to the 10 MHz reference output from the signal generator. The output of the reference divider is monitored and should be equal to OSC_{in}/ RF1 R_CNTR or OSC_{in}/ RF2 R_CNTR.

Again, V_{CC} is swept from 2.7V to 5.5V. The OSC_{in} input frequency and voltage level are then swept with the signal generator. The measurements are repeated at different temperatures, namely T_A = -40°C, +25°C, and +85°C. Sensitivity is reached when the frequency error of the divided input signal is greater than or equal to 1 Hz.

The LMX2335U OSC_{in} sensitivity test setup is very much similar to the above test setup.

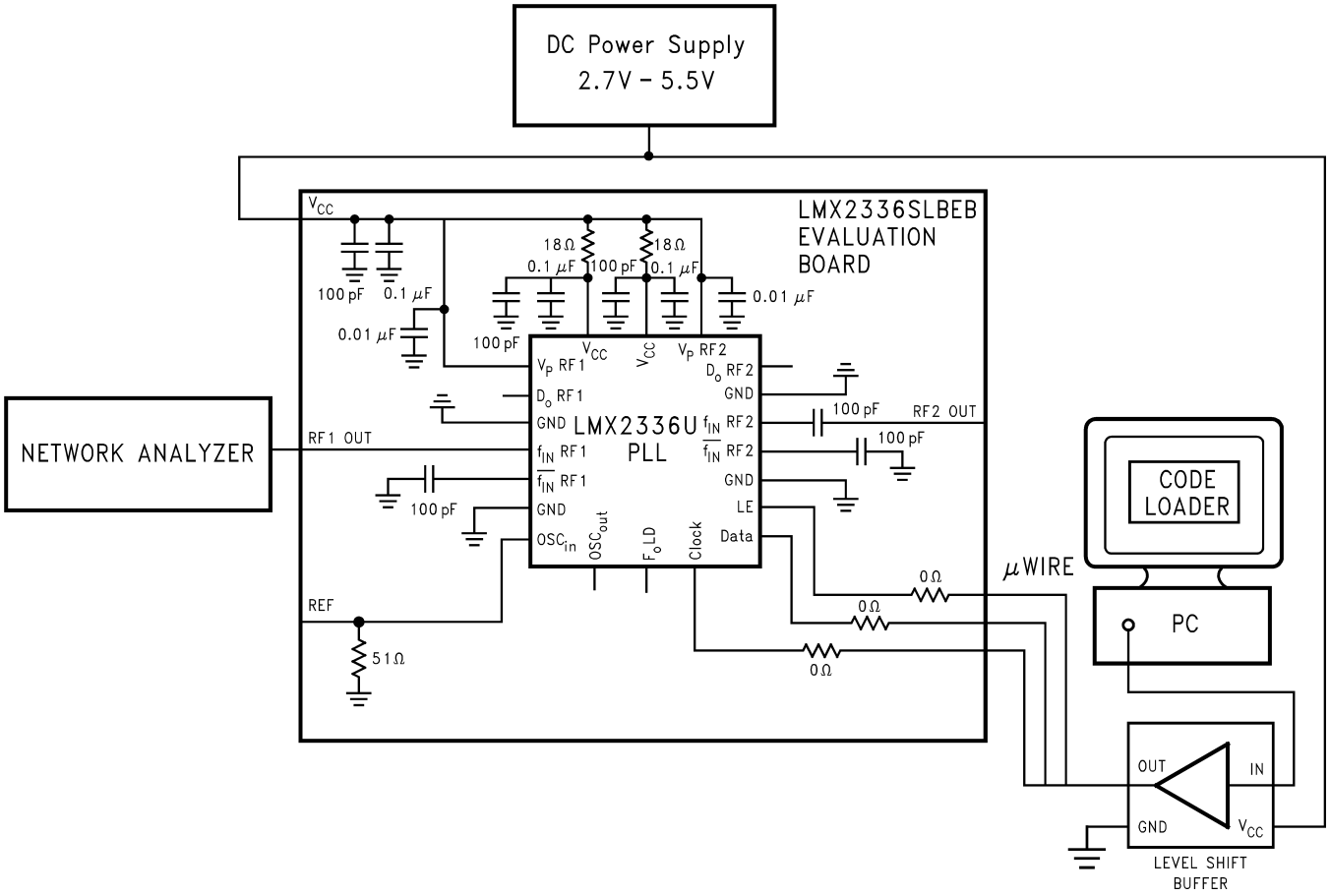


Figure 37. LMX2335U and LMX2336U f_{IN} Impedance Test Setup

The block diagram above (Figure 37) illustrates the setup required to measure the LMX2336U device's RF1 input impedance. The RF2 input impedance and reference oscillator impedance setups are very much similar. The same setup is used for a LMX2336TMEB Evaluation Board. Measuring the device's input impedance facilitates the design of appropriate matching networks to match the PLL to the VCO, or in more critical situations, to the characteristic impedance of the printed circuit board (PCB) trace, to prevent undesired transmission line effects.

Before the actual measurements are taken, the Network Analyzer needs to be calibrated, i.e. the error coefficients need to be calculated. Therefore, three standards will be used to calculate these coefficients: an **open**, **short** and a **matched load**. A 1-port calibration is implemented here.

To calculate the coefficients, the PLL chip is first removed from the PCB. The Network Analyzer port is then connected to the RF1 OUT connector of the evaluation board and the desired operating frequency is set. The typical frequency range selected for the LMX2336U device's RF1 synthesizer is from 100 MHz to 2000 MHz. The standards will be located down the length of the RF1 OUT transmission line. The transmission line adds electrical length and acts as an offset from the reference plane of the Network Analyzer; therefore, it must be included in the calibration. Although not shown, 0 Ω resistors are used to complete the RF1 OUT transmission line (trace).

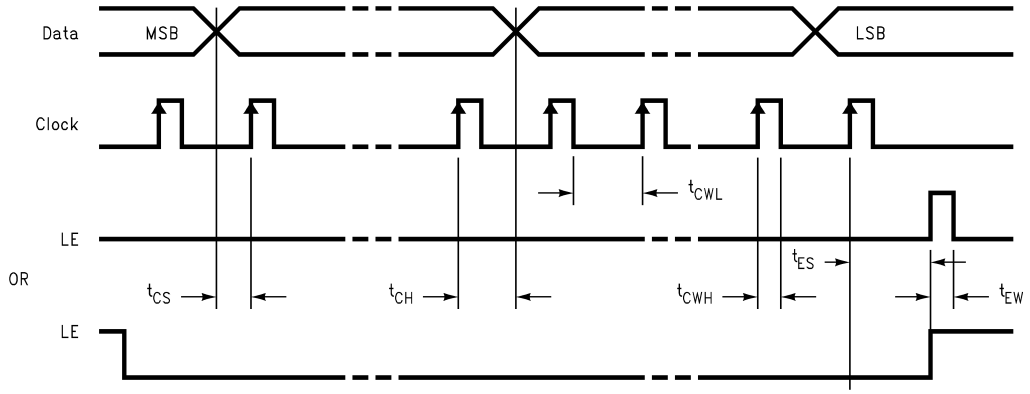
To implement an **open** standard, the end of the RF1 OUT trace is simply left open. To implement a **short** standard, a 0 Ω resistor is placed at the end of the RF1 OUT transmission line. Last of all, to implement a **matched load** standard, two 100 Ω resistors in parallel are placed at the end of the RF1 OUT transmission line. The Network Analyzer calculates the calibration coefficients based on the measured S_{11} parameters. With this all done, calibration is now complete.

The PLL chip is then placed on the PCB. A power supply is connected to V_{CC} and the bias voltage is swept from 2.7V to 5.5V. The OSC_{in} pin is tied to the ground plane. Alternatively, the OSC_{in} pin can be tied to V_{CC}. In this setup, the complementary input ($\overline{f_{IN}}$ RF1) is AC coupled to ground. With the Network Analyzer still connected to RF1 OUT, the measured f_{IN} RF1 impedance is displayed.

Note: The impedance of the reference oscillator is measured when the oscillator buffer is powered up (PWDN RF1 Bit = 0 **or** PWDN RF2 Bit = 0), and when the oscillator buffer is powered down (PWDN RF1 Bit = 1 **and** PWDN RF2 Bit = 1).

The LMX2335U f_{IN} impedance test setup is very much similar to the above test setup. Note that there are no complementary inputs in the LMX2335U device.

LMX2335U and LMX2336U Serial Data Input Timing



1. Data is clocked into the 22-bit shift register on the rising edge of Clock
2. The MSB of Data is shifted in first.

Functional Description

The basic phase-lockedloop (PLL) configuration consists of a high-stability crystal reference oscillator, a frequency synthesizer such as the Texas Instruments LMX2335U or LMX2336U, a voltage controlled oscillator (VCO), and a passive loop filter. The frequency synthesizer includes a phase detector, current mode charge pump, programmable reference R and feedback N frequency dividers. The VCO frequency is established by dividing the crystal reference signal down via the reference divider to obtain a comparison reference frequency. This reference signal, F_r, is then presented to the input of a phase/frequency detector and compared with the feedback signal, F_p, which was obtained by dividing the VCO frequency down by way of the feedback divider. The phase/frequency detector measures the phase error between the F_r and F_p signals and outputs control signals that are directly proportional to the phase error. The charge pump then pumps charge into or out of the loop filter based on the magnitude and direction of the phase error. The loop filter converts the charge into a stable control voltage for the VCO. The phase/frequency detector's function is to adjust the voltage presented to the VCO until the feedback signal's frequency and phase match that of the reference signal. When this “Phase-Locked” condition exists, the VCO frequency will be N times that of the comparison frequency, where N is the feedback divider ratio.

REFERENCE OSCILLATOR INPUT

The reference oscillator frequency for both the RF1 and RF2 PLLs is provided from an external reference via the OSC_{in} pin. The reference buffer circuit supports input frequencies from 5 to 40 MHz with a minimum input sensitivity of 0.5 V_{PP}. The reference buffer circuit has an approximate $V_{CC}/2$ input threshold and can be driven from an external CMOS or TTL logic gate. Typically, the OSC_{in} pin is connected to the output of a crystal oscillator.

REFERENCE DIVIDERS (R COUNTERS)

The reference dividers divide the reference input signal, OSC_{in}, by a factor of R. The output of the reference divider circuits feeds the reference input of the phase detector. This reference input to the phase detector is often referred to as the comparison frequency. The divide ratio should be chosen such that the maximum phase comparison frequency ($F_{\varphi RF1}$ or $F_{\varphi RF2}$) of 10 MHz is not exceeded.

The RF1 and RF2 reference dividers are each comprised of 15-bit CMOS binary counters that support a continuous integer divide ratio from 3 to 32767. The RF1 and RF2 reference divider circuits are clocked by the output of the reference buffer circuit which is common to both.

PRESCALERS

The f_{IN} RF1 (f_{IN} RF2) and $\overline{fin}$ RF1 ($\overline{fin}$ RF2) input pins of the LMX2336U device drives the input of a bipolar, differential-pair amplifier. The output of the bipolar, differential-pair amplifier drives a chain of ECL D-type flip-flops in a dual modulus configuration. The output of the prescaler is used to clock the subsequent feedback dividers. The complementary inputs of both the RF1 and RF2 synthesizers can be driven differentially, or the negative input can be AC coupled to ground through an external capacitor for single ended configuration. A 64/65 or a 128/129 prescale ratio can be selected for the both the RF1 and RF2 synthesizers. On the other hand, the LMX2335U PLL is only intended for single ended operation. Similarly, a 64/65 or a 128/129 prescale ratio can be selected for both the RF1 and RF2 synthesizers.

PROGRAMMABLE FEEDBACK DIVIDERS (N COUNTERS)

The programmable feedback dividers operate in concert with the prescalers to divide the input signal f_{IN} by a factor of N. The output of the programmable reference divider is provided to the feedback input of the phase detector circuit. The divide ratio should be chosen such that the maximum phase comparison frequency ($F_{\varphi RF1}$ or $F_{\varphi RF2}$) of 10 MHz is not exceeded.

The programmable feedback divider circuit is comprised of an A counter (swallow counter) and a B counter (programmble binary counter). The RF1 N_CNTRA counter and RF2 N_CNTRA counter are both 7-bit CMOS swallow counters, programmable from 0 to 127. The RF1 N_CNTRB and RF2 N_CNTRB counters are both 11-bit CMOS binary counters, programmable from 3 to 2047. A continuous integer divide ratio is achieved if N ≥ P * (P−1), where P is the value of the prescaler selected. Divide ratios less than the minimum continuous divide ratio are achievable as long as the binary programmable counter value is greater than the swallow counter value (N_CNTRB ≥ N_CNTRA). Refer to PD_POL RF2, IDo RF2, RF1 R_CNTER[14:0], and PD_POL RF1 for details on how to program the N_CNTRA and N_CNTRB counters. The following equations are useful in determining and programming a particular value of N:

$$N = (P \times N\_CNTRB) + N\_CNTRA \quad (4)$$

$$f_{IN} = N \times F_{\varphi}$$

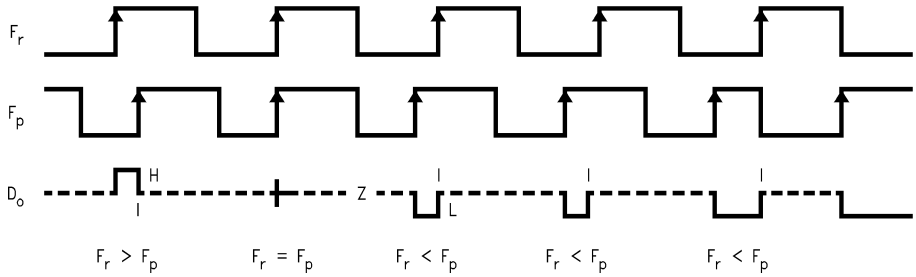
where

- F_{φ}: RF1 or RF2 phase detector comparison frequency
- f_{IN}: RF1 or RF2 input frequency
- N_CNTRA: RF1 or RF2 A counter value
- N_CNTRB: RF1 or RF2 B counter value
- P: Preset modulus of the dual modulus prescaler
  LMX2335U RF1 synthesizer: P = 64 or 128
  LMX2336U RF1 synthesizer: P = 64 or 128
  LMX2335U RF2 synthesizer: P = 64 or 128
  LMX2336U RF2 synthesizer: P = 64 or 128 (5)

PHASE/FREQUENCY DETECTORS

The RF1 and RF2 phase/frequency detectors are driven from their respective N and R counter outputs. The maximum frequency for both the RF1 and RF2 phase detector inputs is 10 MHz. The phase/frequency detector outputs control the respective charge pumps. The polarity of the pump-up or pump-down control signals are programmed using the **PD_POL RF1** or **PD_POL RF2** control bits, depending on whether the RF1 or RF2 VCO characteristics are positive or negative. Refer to PD_POL RF2 and PD_POL RF1 for more details. The phase/frequency detectors have a detection range of −2π to +2π. The phase/frequency detectors also receive a feedback signal from the charge pump in order to eliminate dead zone.

PHASE COMPARATOR AND INTERNAL CHARGE PUMP CHARACTERISTICS



1. The minimum width of the pump-up and pump-down current pulses occur at the D_o RF1 or D_o RF2 pins when the loop is phase locked.
2. The diagram assumes positive VCO characteristics, i.e. PD_POL RF1 or PD_POL RF2 = 1.
3. F_r is the phase detector input from the reference divider (R counter).
4. F_p is the phase detector input from the programmable feedback divder (N counter).
5. D_o refers to either the RF1 or RF2 charge pump output.

CHARGE PUMPS

The charge pump directs charge into or out of an external loop filter. The loop filter converts the charge into a stable control voltage which is applied to the tuning input of the VCO. The charge pump steers the VCO control voltage towards V_P RF1 or V_P RF2 during pump-up events and towards GND during pump-down events. When locked, D_o RF1 or D_o RF2 are primarily in a TRI-STATE mode with small corrections occuring at the phase comparator rate. The charge pump output current magnitude can be selected by toggling the **ID_o RF1** or **ID_o RF2** control bits.

MICROWIRE SERIAL INTERFACE

The programmable register set is accessed via the MICROWIRE serial interface. The interface is comprised of three signal pins: Clock, Data and LE (Latch Enable). Serial data is clocked into the 22-bit shift register on the rising edge of Clock. The last two bits decode the internal control register address. When LE transitions HIGH, data stored in the shift register is loaded into one of four control registers depending on the state of the address bits. The MSB of Data is loaded in first. The synthesizers can be programmed even in power down mode. A complete programming description is provided in Programming Description.

MULTI-FUNCTION OUTPUTS

The F_oLD output pin is a multi-function output that can be configured as the RF1 FastLock output, a push-pull analog lock detect output, counter reset, or used to monitor the output of the various reference divider (R counter) or feedback divider (N counter) circuits. The F_oLD control word is used to select the desired output function. When the PLL is in powerdown mode, the F_oLD output is pulled to a LOW state. A complete programming description of the multi-function output is provided in FoLD [3:0] Multi-Function Output Select.

Push-Pull Analog Lock Detect Output

An analog lock detect status generated from the phase detector is available on the F_oLD output pin if selected. The lock detect output goes HIGH when the charge pump is inactive. It goes LOW when the charge pump is active during a comparison cycle. When viewed with an oscilloscope, narrow negative pulses are observed when the charge pump turns on. The lock detect output signal is a push-pull configuration.

Three separate lock detect signals are routed to the multiplexer. Two of these monitor the ‘lock’ status of the individual synthesizers. The third detects the condition when both the RF1 and RF2 synthesizers are in a ‘locked state’. External circuitry however, is required to provide a steady DC signal to indicate when the PLL is in a locked state. Refer to FoLD[3:0] Multi-Function Output Select for details on how to program the different lock detect options.

Open Drain FastLock Output

The LMX233xU Fastlock feature allows faster loop response time during lock aquisition. The loop response time (lock time) can be approximately halved if the loop bandwidth is doubled. In order to achieve this, the same gain/phase relationship at twice the loop bandwidth must be maintained. This can be achieved by increasing the charge pump current from 0.95 mA (ID_o RF1 Bit = 0) in the steady state mode, to 3.8 mA (ID_o RF1 Bit = 1) in Fastlock. When the F_oLD output is configured as a FastLock output, an open drain device is enabled. The open drain device switches in a parallel resistor R2' to ground, of equal value to resistor R2 of the external loop filter. The loop bandwidth is effectively doubled and stability is maintained. Once locked to the correct frequency, the PLL will return to a steady state condition. Refer to FoLD[3:0] Multi-Function Output Select for details on how to configure the F_oLD output to an open drain Fastlock output.

Counter Reset

Three separate counter reset functions are provided. When the F_oLD is programmed to **Reset RF2 Counters**, both the RF2 feedback divider and the RF2 reference divider are held at their load point. When the **Reset RF1 Counters** is programmed, both the RF1 feedback divider and the RF1 reference divider are held at their load point. When the **Reset All Counters** mode is enabled, all feedback dividers and reference dividers are held at their load point. When the device is programmed to normal operation, both the feedback divider and reference divider are enabled and resume counting in 'close' alignment to each other. Refer to FoLD[3:0] Multi-Function Output Select for more details.

Reference Divider and Feedback Divider Output

The outputs of the various N and R dividers can be monitored by selecting the appropriate F_oLD word. This is essential when performing OSC_{in} or f_{IN} sensitivity measurements. Refer to the **Test Setups** section for more details. Refer to FoLD[3:0] Multi-Function Output Select for more details on how to route the appropriate divider output to the F_oLD pin.

POWER CONTROL

Each synthesizer in the LMX2335U or LMX2336U is individually power controlled by device powerdown bits. The powerdown word is comprised of the **PWDN RF1** (**PWDN RF2**) bit, in conjuction with the **TRI-STATE ID_o RF1** (**TRI-STATE ID_o RF2**) bit. The powerdown control word is used to set the operating mode of the device. Refer to TRI-STATE IDo RF2, TRISTATE IDo RF1, TRI_STATE IDo RF1, and PWDN RF1 for details on how to program the RF1 or RF2 powerdown bits.

When either the RF1 synthesizer or the RF2 synthesizer enters the powerdown mode, the respective prescaler, phase detector, and charge pump circuit are disabled. The D_o RF1 (D_o RF2), f_{IN} RF1 (f_{IN} RF2), and $\overline{f_{IN}}$ RF1 ($\overline{f_{IN}}$ RF2) pins are all forced to a high impedance state. The reference divider and feedback divider circuits are held at the load point during powerdown. The oscillator buffer is disabled when both the RF1 and RF2 synthesizers are powered down. The OSC_{in} pin is forced to a HIGH state through an approximate 100 kΩ resistance when this condition exists. When either synthesizer is activated, the respective prescaler, phase detector, charge pump circuit, and the oscillator buffer are all powered up. The feedback divider, and the reference divider are held at load point. This allows the reference oscillator, feedback divider, reference divider and prescaler circuitry to reach proper bias levels. After a finite delay, the feedback and reference dividers are enabled and they resume counting in 'close' alignment (the maximum error is one prescaler cycle). The MICROWIRE control register remains active and capable of loading and latching data while in the powerdown mode.

Synchronous Powerdown Mode

In this mode, the powerdown function is gated by the charge pump. When the device is configured for synchronous powerdown, the device will enter the powerdown mode upon completion of the next charge pump pulse event.

Asynchronous Powerdown Mode

In this mode, the powerdown function is NOT gated by the completion of a charge pump pulse event. When the device is configured for asynchronous powerdown, the part will go into powerdown mode immediately.

TRI-STATE ID_o (1)	PWDN (2)	Operating Mode
0	0	PLL Active, Normal Operation
1	0	PLL Active, Charge Pump Output in High Impedance State
0	1	Synchronous Powerdown
1	1	Asynchronous Powerdown

(1) TRI-STATE ID_o refers to either the TRI-STATE ID_o RF1 or TRI-STATE ID_o RF2 bit .
(2) PWDN refers to either the PWDN RF1 or PWDN RF2 bit.

Programming Description

MICROWIRE INTERFACE

The 22-bit shift register is loaded via the MICROWIRE interface. The shift register consists of a 20-bit *Data[19:0] Field* and a 2-bit *Address[1:0] Field* as shown below. The Address Field is used to decode the internal control register address. When LE transitions HIGH, data stored in the shift register is loaded into one of 4 control registers depending on the state of the address bits. The MSB of Data is loaded in first. The Data Field assignments are shown in CONTROL REGISTER CONTENT MAP.

MSB		LSB
Data[19:0]		Address[1:0]
21	2 1	0

CONTROL REGISTER LOCATION

The address bits Address[1:0] decode the internal register address. The table below shows how the address bits are mapped into the target control register.

Address[1:0] Field		Target Register
0	0	RF2 R
0	1	RF2 N
1	0	RF1 R
1	1	RF1 N

CONTROL REGISTER CONTENT MAP

The control register content map describes how the bits within each control register are allocated to specific control functions.

Reg.	Most Significant Bit						SHIFT REGISTER BIT LOCATION											Least Significant Bit				
	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Data Field																				*Address Field*	
RF2 R	F_0LD0	F_0LD2	TRI-STATE ID_0 RF2	ID_0 RF2	PD_POL RF2	RF2 R_CNTR[14:0]															0	0
RF2 N	PWDN RF2	PRE RF2	RF2 N_CNTRB[10:0]											RF2 N_CNTRA[6:0]							0	1
RF1 R	F_0LD1	F_0LD3	TRI-STATE ID_0 RF1	ID_0 RF1	PD_POL RF1	RF1 R_CNTR[14:0]															1	0
RF1 N	PWDN RF1	PRE RF1	RF1 N_CNTRB[10:0]											RF1 N_CNTRA[6:0]							1	1

RF2 R REGISTER

The RF2 R register contains the RF2 R_CNTR, PD_POL RF2, ID_0 RF2, and TRI-STATE ID_0 RF2 control words, in addition to two bits that compose the F_0LD control word. The detailed description and programming information for each control word is discussed in the following sections. RF2 R_CNTR[14:0]

Reg.	Most Significant Bit						SHIFT REGISTER BIT LOCATION											Least Significant Bit				
	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Data Field																				*Address Field*	
RF2 R	F_0LD 0	F_0LD 2	TRI-STATE ID_0RF2	ID_0RF2	PD_POL RF2	RF2 R_CNTR[14:0]															0	0

RF2 R_CNTR[14:0] RF2 SYNTHESIZER PROGRAMMABLE REFERENCE DIVIDER (R COUNTER) RF2 R[2:16]

The RF2 reference divider (RF2 R_CNTR) can be programmed to support divide ratios from 3 to 32767. Divide ratios less than 3 are prohibited.

Divide Ratio	RF2 R_CNTR[14:0]														
	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
3	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
32767	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

PD_POL RF2, RF2 SYNTHESIZER PHASE DETECTOR POLARITY RF2 R[17]

The PD_POL RF2 bit is used to control the RF2 synthesizer's phase detector polarity based on the VCO tuning characteristics.

Control Bit	Register Location	Description	Function	
			0	1
PD_POL RF2	RF2 R[17]	RF2 Phase Detector Polarity	RF2 VCO Negative Tuning Characteristics	RF2 VCO Positive Tuning Characteristics

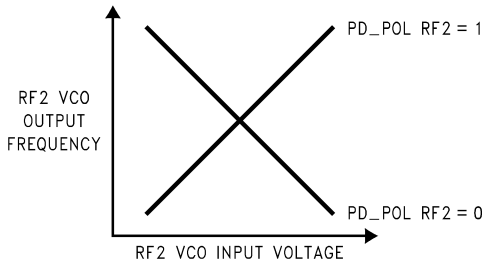


Figure 38. RF2 VCO Characteristics

ID_0 RF2, RF2 SYNTHESIZER CHARGE PUMP CURRENT GAIN RF2 R[18]

The ID_0 RF2 bit controls the RF2 synthesizer's charge pump gain. Two current levels are available.

Control Bit	Register Location	Description	Function	
			0	1
ID_0 RF2	RF2 R[18]	RF2 Charge Pump Current Gain	LOW 0.95 mA	HIGH 3.80 mA

TRI-STATE ID_0 RF2, RF2 SYNTHESIZER CHARGE PUMP TRI-STATE CURRENT RF2 R[19]

The TRI-STATE ID_0 RF2 bit allows the charge pump to be switched between a normal operating mode and a high impedance output state. This happens asynchronously with the change in the TRI-STATE ID_0 RF2 bit.

Furthermore, the TRI-STATE ID_0 RF2 bit operates in conjuction with the PWDN RF2 bit to set a synchronous or an asynchronous powerdown mode.

Control Bit	Register Location	Description	Function	
			0	1
TRI-STATE ID_0 RF2	RF2 R[19]	RF2 Charge Pump TRI-STATE Current	RF2 Charge Pump Normal Operation	RF2 Charge Pump Output in High Impedance State

RF2 N REGISTER

The RF2 N register contains the RF2 N_CNTRA, RF2 N_CNTRB, PRE RF2, and PWDN RF2 control words. The RF2 N_CNTRA and RF2 N_CNTRB control words are used to setup the programmable feedback divider. The detailed description and programming information for each control word is discussed in the following sections.

Reg.	Most Significant Bit						SHIFT REGISTER BIT LOCATION											Least Significant Bit				
	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Data Field																				*Address Field*	
RF2 N	PWDN RF2	PRE RF2	RF2 N_CNTRB[10:0]											RF2 N_CNTRA[6:0]							0	1

RF2 N_CNTRA[6:0] RF2 SYNTHESIZER SWALLOW COUNTER (A COUNTER) RF2 N[2:8]

The RF2 N_CNTRA control word is used to setup the RF2 synthesizer's A counter. The A counter is a 7-bit swallow counter used in the programmable feedback divider. The RF2 N_CNTRA control word can be programmed to values ranging from 0 to 127.

Divide Ratio	RF2 N_CNTRA[6:0]						
	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
127	1	1	1	1	1	1	1

RF2 N_CNTRB[10:0] RF2 SYNTHESIZER PROGRAMMABLE BINARY COUNTER (B COUNTER) RF2 N[9:19]

The RF2 N_CNTRB control word is used to setup the RF2 synthesizer's B counter. The B counter is an 11-bit programmable binary counter used in the programmable feedback divider. The RF2 N_CNTRB control word can be programmed to values ranging from 3 to 2047.

Divide Ratio	RF2 N_CNTRB[10:0]										
	10	9	8	7	6	5	4	3	2	1	0
3	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

PRE RF2, RF2 SYNTHESIZER PRESCALER SELECT RF2 N[20]

The RF2 synthesizer utilizes a selectable dual modulus prescaler.

Control Bit	Register Location	Description	Function	
			0	1
PRE RF2	RF2 N[20]	RF2 Prescaler Select	64/65 Prescaler Selected	128/129 Prescaler Selected

PWDN RF2, RF2 SYNTHESIZER POWERDOWN RF2 N[21]

The PWDN RF2 bit is used to switch the RF2 PLL between a powered up and powered down mode.

Furthermore, the PWDN RF2 bit operates in conjuction with the TRI-STATE ID_o RF2 bit to set a synchronous or an asynchronous powerdown mode.

Control Bit	Register Location	Description	Function	
			0	1
PWDN RF2	RF2 N[21]	RF2 Powerdown	RF2 PLL Active	RF2 PLL Powerdown

RF1 R REGISTER

The RF1 R register contains the RF1 R_CNTR, PD_POL RF1, ID_o RF1, and TRI-STATE ID_o RF1 control words, in addition to two bits that compose the F_oLD control word. The detailed description and programming information for each control word is discussed in the following sections.

Reg.	Most Significant Bit					SHIFT REGISTER BIT LOCATION														Least Significant Bit	
	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Data Field																				*Address Field*	
RF1 R	FoLD 1	FoLD 3	TRI-STAT EIDoR F1	IDoR F1	PD_P OLRF 1	RF1 R_CNTR[14:0]															1	0

RF1 R_CNTR[14:0] RF1 SYNTHESIZER PROGRAMMABLE REFERENCE DIVIDER (R COUNTER) RF1 R[2:16]

The RF1 reference divider (RF1 R_CNTR) can be programmed to support divide ratios from 3 to 32767. Divide ratios less than 3 are prohibited.

Divide Ratio	RF1 R_CNTR[14:0]														
	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
3	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
32767	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

PD_POL RF1, RF1 SYNTHESIZER PHASE DETECTOR POLARITY RF1 R[17]

The PD_POL RF1 bit is used to control the RF1 synthesizer's phase detector polarity based on the VCO tuning characteristics.

Control Bit	Register Location	Description	Function	
			0	1
PD_POL RF1	RF1 R[17]	RF1 Phase Detector Polarity	RF1 VCO Negative Tuning Characteristics	RF1 VCO Positive Tuning Characteristics

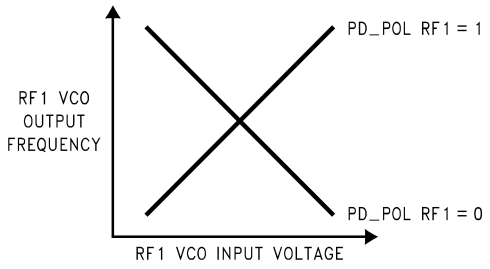


Figure 39. RF1 VCO Characteristics

ID_o RF1, RF1 SYNTHESIZER CHARGE PUMP CURRENT GAIN RF1 R[18]

The ID_o RF1 bit controls the RF1 synthesizer's charge pump gain. Two current levels are available.

Control Bit	Register Location	Description	Function	
			0	1
ID_o RF1	RF1 R[18]	RF1 Charge Pump Current Gain	LOW 0.95 mA	HIGH 3.80 mA

TRI-STATE ID_o RF1, RF1 SYNTHESIZER CHARGE PUMP TRI-STATE CURRENT RF1 R[19]

The TRI-STATE ID_o RF1 bit allows the charge pump to be switched between a normal operating mode and a high impedance output state. This happens asynchronously with the change in the TRI-STATE ID_o RF1 bit.

Furthermore, the TRI-STATE ID_o RF1 bit operates in conjuction with the PWDN RF1 bit to set a synchronous or an asynchronous powerdown mode.

Control Bit	Register Location	Description	Function	
			0	1
TRI-STATE ID_o RF1	RF1 R[19]	RF1 Charge Pump TRI-STATE Current	RF1 Charge Pump Normal Operation	RF1 Charge Pump Output in High Impedance State

RF1 N REGISTER

The RF1 N register contains the RF1 N_CNTRA, RF1 N_CNTRB, PRE RF1, and PWDN RF1 control words. The RF1 N_CNTRA and RF1 N_CNTRB control words are used to setup the programmable feedback divider. The detailed description and programming information for each control word is discussed in the following sections.

Reg.	Most Significant Bit						SHIFT REGISTER BIT LOCATION											Least Significant Bit				
	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Data Field																				*Address Field*	
RF1 N	PWDN RF1	PRE RF1	RF1 N_CNTRB[10:0]											RF1 N_CNTRA[6:0]							1	1

RF1 N_CNTRA[6:0] RF1 SYNTHESIZER SWALLOW COUNTER (A COUNTER) RF1 N[2:8]

The RF1 N_CNTRA control word is used to setup the RF1 synthesizer's A counter. The A counter is a 7-bit swallow counter used in the programmable feedback divider. The RF1 N_CNTRA control word can be programmed to values ranging from 0 to 127.

Divide Ratio	RF1 N_CNTRA[6:0]						
	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
127	1	1	1	1	1	1	1

RF1 N_CNTRB[10:0] RF1 SYNTHESIZER PROGRAMMABLE BINARY COUNTER (B COUNTER) RF1 N[9:19]

The RF1 N_CNTRB control word is used to setup the RF1 synthesizer's B counter. The B counter is an 11-bit programmable binary counter used in the programmable feedback divider. The RF1 N_CNTRB control word can be programmed to values ranging from 3 to 2047.

Divide Ratio	RF1 N_CNTRB[10:0]										
	10	9	8	7	6	5	4	3	2	1	0
3	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

PRE RF1, RF1 SYNTHESIZER PRESCALER SELECT RF1 N[20]

The RF1 synthesizer utilizes a selectable dual modulus prescaler.

Control Bit	Register Location	Description	Function	
			0	1
PRE RF1	RF1 N[20]	RF1 Prescaler Select	64/65 Prescaler Selected	128/129 Prescaler Selected

PWDN RF1, RF1 SYNTHESIZER POWERDOWN RF1 N[21]

The PWDN RF1 bit is used to switch the RF1 PLL between a powered up and powered down mode.

Furthermore, the PWDN RF1 bit operates in conjuction with the TRI-STATE ID_o RF1 bit to set a synchronous or an asynchronous powerdown mode.

Control Bit	Register Location	Description	Function	
			0	1
PWDN RF1	RF1 N[21]	RF1 Powerdown	RF1 PLL Active	RF1 PLL Powerdown

F_oLD[3:0] MULTI-FUNCTION OUTPUT SELECT [RF1 R[20], RF2 R[20], RF1 R[21], RF2 R[21]]

The F_oLD control word is used to select which signal is routed to the F_oLD pin.

F_oLD3	F_oLD2	F_oLD1	F_oLD0	F_oLD Output State
0	0	0	0	LOW Logic State Output
0	0	0	1	RF2 PLL R Divider Output, Push-Pull Output
0	0	1	0	RF1 PLL R Divider Output, Push-Pull Output
0	0	1	1	Open Drain Fastlock Output
0	1	0	0	RF2 PLL Analog Lock Detect, Push-Pull Output
0	1	0	1	RF2 PLL N Divider Output, Push-Pull Output
0	1	1	0	RF1 PLL N Divider Output, Push-Pull Output
0	1	1	1	Reset RF2 Counters, LOW Logic State Output
1	0	0	0	RF1 Analog Lock Detect, Push-Pull Output
1	0	0	1	RF2 PLL R Divider Output, Push-Pull Output
1	0	1	0	RF1 PLL R Divider Output, Push-Pull Output
1	0	1	1	Reset RF1 Counters, LOW Logic State Output
1	1	0	0	RF1 and RF2 Analog Lock Detect, Push-Pull Output
1	1	0	1	RF2 PLL N Divider Output, Push-Pull Output
1	1	1	0	RF1 PLL N Divider Output, Push-Pull Output
1	1	1	1	Reset All Counters, LOW Logic State Output

REVISION HISTORY

Changes from Revision F (April 2013) to Revision G	Page
• Changed layout of National Data Sheet to TI format	41

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