ADC12662 12-Bit, 1.5 MHz, 200 mW A/D Converter with Input Multiplexer and Sample/Hold

Check for Samples: ADC12662

FEATURES

- **Built-In Sample-and-Hold**
- **Single +5V Supply**
- **Single Channel or 2 Channel Multiplexer Operation**
- **Low Power Standby Mode**

APPLICATIONS

- **Digital Signal Processor Front Ends**
- **Instrumentation**
- **Disk Drives**
- **Mobile Telecommunications**
- **Waveform Digitizers**

KEY SPECIFICATIONS

- **Sampling rate: 1.5 MHz (min)**
- **Conversion time: 580 ns (typ)**
- **Signal-to-Noise Ratio, f_{IN}= 100 kHz: 67.5 dB (min)**
- **Power consumption (f_s= 1.5 MHz): 200 mW (max)**
- **No missing codes over temperature: Ensured**

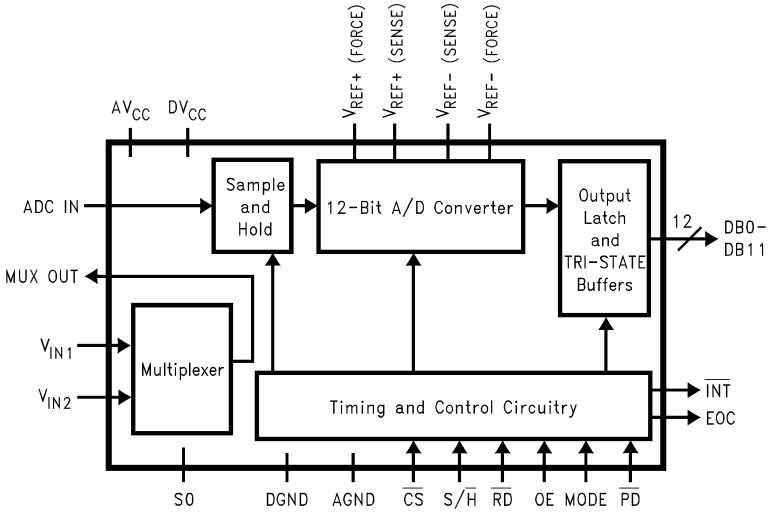
DESCRIPTION

Using an innovative multistep conversion technique, the 12-bit ADC12662 CMOS analog-to-digital converter digitizes signals at a 1.5 MHz sampling rate while consuming a maximum of only 200 mW on a single +5V supply. The ADC12662 performs a 12-bit conversion in three lower-resolution “flash” conversions, yielding a fast A/D without the cost and power dissipation associated with true flash approaches.

The analog input voltage to the ADC12662 is tracked and held by an internal sampling circuit, allowing high frequency input signals to be accurately digitized without the need for an external sample-and-hold circuit. The ADC12662 features two sample-and-hold/flash comparator sections which allow the converter to acquire one sample while converting the previous. This pipelining technique increases conversion speed without sacrificing performance. The multiplexer output is available to the user in order to perform additional external signal processing before the signal is digitized.

When the converter is not digitizing signals, it can be placed in the Standby mode; typical power consumption in this mode is 250 µW.

ADC12662 Block Diagram



Connection Diagram

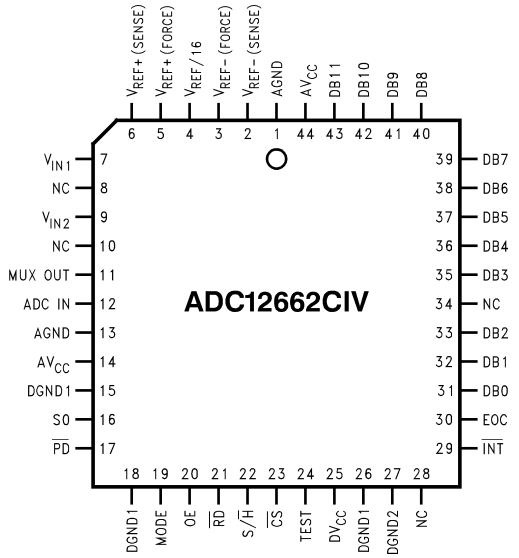


Figure 1. PLCC - Top View
See Package Number FN

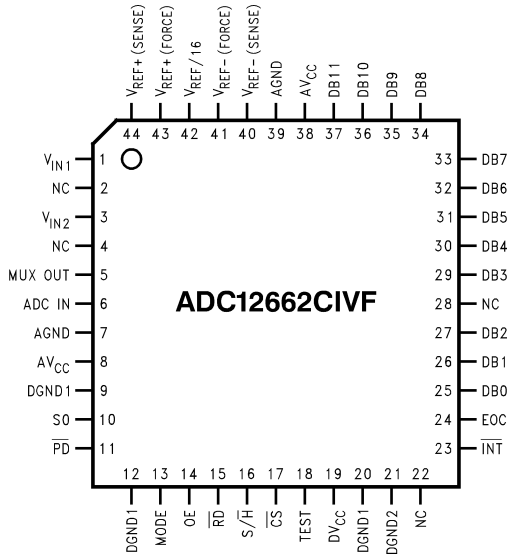


Figure 2. PQFP - Top View
See Package Number PGB

PIN DESCRIPTIONS

AV_{CC} These are the two positive analog supply inputs. They should always be connected to the same voltage source, but are brought out separately to allow for separate bypass capacitors. Each supply pin should be bypassed to AGND with a 0.1 µF ceramic capacitor in parallel with a 10 µF tantalum capacitor.

DV_{CC} This is the positive digital supply input. It should always be connected to the same voltage as the analog supply, AV_{CC}. It should be bypassed to DGND2 with a 0.1 µF ceramic capacitor in parallel with a 10 µF tantalum capacitor.

AGND, DGND1, DGND2 These are the power supply ground pins. There are separate analog and digital ground pins for separate bypassing of the analog and digital supplies. The ground pins should be connected to a stable, noise-free system ground. All of the ground pins should be returned to the same potential. AGND is the analog ground for the converter. DGND1 is the ground pin for the digital control lines. DGND2 is the ground return for the output databus. See section on LAYOUT AND GROUNDING for more information.

DB0–DB11 These are the TRI-STATE output pins, enabled by $\overline{RD}$, $\overline{CS}$, and OE.

V_{IN1}, V_{IN2} These are the analog input pins to the multiplexer. For accurate conversions, no input pin (even one that is not selected) should be driven more than 50 mV below ground or 50 mV above V_{CC}.

MUX OUT This is the output of the on-board analog input multiplexer.

ADC IN This is the direct input to the 12-bit sampling A/D converter. For accurate conversions, this pin should not be driven more than 50 mV below ground or 50 mV above V_{CC}.

S0 This pin selects the analog input that will be connected to the ADC12662 during the conversion. The input is selected based on the state of S0 when EOC makes its high-to-low transition. Low selects V_{IN1}, high selects V_{IN2}.

MODE This pin should be tied to DGND1.

$\overline{CS}$ This is the active low Chip Select control input. When low, this pin enables the $\overline{RD}$, S/$\overline{H}$, and OE inputs. This pin can be tied low.

$\overline{INT}$ This is the active low Interrupt output. When using the Interrupt Interface Mode (Figure 20), this output goes low when a conversion has been completed and indicates that the conversion result is available in the output latches. This output is always high when $\overline{RD}$ is held low (Figure 21).

$\overline{EOC}$ This is the End-of-Conversion control output. This output is low during a conversion.

$\overline{RD}$ This is the active low Read control input. When $\overline{RD}$ is low (and $\overline{CS}$ is low), the $\overline{INT}$ output is reset and (if OE is high) data appears on the data bus. This pin can be tied low.

OE This is the active high Output Enable control input. This pin can be thought of as an inverted version of the $\overline{RD}$ input (see Figure 25). Data output pins DB0–DB11 are TRI-STATE when OE is low. Data appears on DB0–DB11 only when OE is high and $\overline{CS}$ and $\overline{RD}$ are both low. This pin can be tied high.

S/$\overline{H}$ This is the Sample/$\overline{Hold}$ control input. The analog input signal is held and a new conversion is initiated by the falling edge of this control input (when $\overline{CS}$ is low).

$\overline{PD}$ This is the Power Down control input. This pin should be held high for normal operation. When this pin is pulled low, the device goes into a low power standby mode.

$V_{REF+(FORCE)}$, $V_{REF-(FORCE)}$ These are the positive and negative voltage reference force inputs, respectively. See REFERENCE INPUTS for more information.

$V_{REF+(SENSE)}$, $V_{REF-(SENSE)}$ These are the positive and negative voltage reference sense pins, respectively. See REFERENCE INPUTS for more information.

V_{REF}/16 This pin should be bypassed to AGND with a 0.1 µF ceramic capacitor.

TEST This pin should be tied to DV_{CC}.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)(2)(3)

Supply Voltage (V_{CC} = DV_{CC} = AV_{CC})		−0.3V to +6V
Voltage at Any Input or Output		−0.3V to V_{CC} + 0.3V
Input Current at Any Pin(4)		25 mA
Package Input Current(4)		50 mA
Power Dissipation(5)	ADC12662CIV	875 mW
ESD Susceptibility(6)		2000V
Soldering Information	FN Package, Infrared, 15 seconds	+300°C
PQFP Package	Vapor Phase (60 seconds)	215°C
	Infrared (15 seconds)	220°C
Storage Temperature Range		−65°C to +150°C
Maximum Junction Temperature (T_{JMAX})		150°C

(1) All voltages are measured with respect to GND (GND = AGND = DGND), unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional. These ratings do not ensure specific performance limits, however. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(4) When the input voltage (V_{IN}) at any pin exceeds the power supply rails (V_{IN} < GND or V_{IN} > V_{CC}) the absolute value of current at that pin should be limited to 25 mA or less. The 50 mA package input current limits the number of pins that can safely exceed the power supplies with an input current of 25 mA to two.
(5) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA} and the ambient temperature T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. θ_{JA} for the FN (PLCC) package is 55°C/W. θ_{JA} for the PGB (PQFP) package is 62°C/W. In most cases the maximum derated power dissipation will be reached only during fault conditions.
(6) Human body model, 100 pF discharged through a 1.5 kΩ resistor. Machine model ESD rating is 200V.

OPERATING RATINGS(1)(2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC12662CIV, ADC12662CIVF	−40°C ≤ T_A ≤ +85°C
Supply Voltage (DV_{CC} = AV_{CC})	4.75V to 5.25V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional. These ratings do not ensure specific performance limits, however. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) All voltages are measured with respect to GND (GND = AGND = DGND), unless otherwise specified.

CONVERTER CHARACTERISTICS

The following specifications apply for DV_{CC} = AV_{CC} = +5V, $V_{REF+(SENSE)}$ = +4.096V, $V_{REF-(SENSE)}$ = AGND, and f_s = 1.5 MHz, unless otherwise specified. **Boldface limits apply for T_A = T_J from T_{MIN} to T_{MAX};** all other limits T_A = T_J = +25°C.

Symbol	Parameter	Conditions	Typ(1)	Limit(2)	Units (Limit)
	Resolution			**12**	Bits
	Differential Linearity Error	**T_{MIN} to T_{MAX}**	±0.4	**±0.95**	LSB (max)
	Integral Linearity Error(3)	**T_{MIN} to T_{MAX}**	±0.4	**±1.5**	LSB (max)
	Offset Error	**T_{MIN} to T_{MAX}**	±0.3	**±2.0**	LSB (max)
	Full-Scale Error	**T_{MIN} to T_{MAX}**	±0.3	**±1.5**	LSB (max)
	Power Supply Sensitivity(4)	DV_{CC} = AV_{CC} = 5V ±5%		**±0.75**	LSB (max)
R_{REF}	Reference Resistance		1000	**600** **1300**	Ω (min) Ω (max)
$V_{REF(+)}$	$V_{REF+(SENSE)}$ Input Voltage			**AV_{CC}**	V (max)

(1) Typicals are at +25°C and represent most likely parametric norm.
(2) Tested limits are specified to AOQL (Average Outgoing Quality Level).
(3) Integral Linearity Error is the maximum deviation from a straight line between the *measured* offset and full scale endpoints.
(4) Power Supply Sensitivity is defined as the change in the Offset Error or the Full Scale Error due to a change in the supply voltage.

CONVERTER CHARACTERISTICS (continued)

The following specifications apply for DV_{CC} = AV_{CC} = +5V, $V_{REF+(SENSE)}$ = +4.096V, $V_{REF-(SENSE)}$ = AGND, and f_s = 1.5 MHz, unless otherwise specified. **Boldface limits apply for T_A = T_J from T_{MIN} to T_{MAX};** all other limits T_A = T_J = +25°C.

Symbol	Parameter	Conditions	Typ(1)	Limit(2)	Units (Limit)
$V_{REF(-)}$	$V_{REF-(SENSE)}$ Input Voltage			**AGND**	V (min)
V_{IN}	Input Voltage Range	To V_{IN1}, V_{IN2}, or ADC IN		**AV_{CC}+0.05V** **AGND − 0.05V**	V (max) V (min)
	ADC IN Input Leakage	AGND to AV_{CC} − 0.3V	0.1	**3**	µA (max)
C_{ADC}	ADC IN Input Capacitance		25		pF
	MUX On-Channel Leakage	AGND to AV_{CC} − 0.3V	0.1	**3**	µA (max)
	MUX Off-Channel Leakage	AGND to AV_{CC} − 0.3V	0.1	**3**	µA (max)
C_{MUX}	Multiplexer Input Cap		7		pF
	MUX Off Isolation	f_{IN} = 100 kHz	92		dB

DYNAMIC CHARACTERISTICS(1)

The following specifications apply for DV_{CC} = AV_{CC} = +5V, $V_{REF+(SENSE)}$ = +4.096V, $V_{REF-(SENSE)}$ = AGND, R_S = 25Ω, f_{IN} = 100 kHz, 0 dB from fullscale, and f_s = 1.5 MHz, unless otherwise specified. **Boldface limits apply for T_A = T_J from T_{MIN} to T_{MAX};** all other limits T_A = T_J = +25°C.

Symbol	Parameter	Conditions	Typ (2)	Limit (3)	Units (Limit)
SINAD	Signal-to-Noise Plus Distortion Ratio	**T_{MIN} to T_{MAX}**	70	**67.0**	dB (min)
SNR	Signal-to-Noise Ratio(4)	**T_{MIN} to T_{MAX}**	70	**67.5**	dB (min)
THD	Total Harmonic Distortion(5)	**T_{MIN} to T_{MAX}**	−80	**−70**	dBc (max)
ENOB	Effective Number of Bits(6)	**T_{MIN} to t_{MAX}**	11.3	**10.8**	Bits (min)
IMD	Intermodulation Distortion	f_{IN} = 88.7 kHz, 89.5 kHz	−80		dBc

(1) Dynamic testing of the ADC12662 is done using the ADC IN input. The input multiplexer adds harmonic distortion at high frequencies. See the graph in the TYPICAL PERFORMANCE CHARACTERISTICS section for a typical graph of THD performance vs input frequency with and without the input multiplexer.
(2) Typicals are at +25°C and represent most likely parametric norm.
(3) Tested limits are specified to AOQL (Average Outgoing Quality Level).
(4) The signal-to-noise ratio is the ratio of the signal amplitude to the background noise level. Harmonics of the input signal are not included in its calculation.
(5) The contributions from the first nine harmonics are used in the calculation of the THD.
(6) Effective Number of Bits (ENOB) is calculated from the measured signal-to-noise plus distortion ratio (SINAD) using the equation: ENOB = (SINAD − 1.76)/6.02.

DC ELECTRICAL CHARACTERISTICS

The following specifications apply for DV_{CC} = AV_{CC} = +5V, $V_{REF+(SENSE)}$ = +4.096V, $V_{REF-(SENSE)}$ = AGND, and f_s = 1.5 MHz, unless otherwise specified. **Boldface limits apply for T_A = T_J from T_{MIN} to T_{MAX};** all other limits T_A = T_J = +25°C.

Symbol	Parameter	Conditions	Typ(1)	Limit(2)	Units (Limit)
$V_{IN(1)}$	Logical “1” Input Voltage	DV_{CC} = AV_{CC} = +5.5V		**2.0**	V (min)
$V_{IN(0)}$	Logical “0” Input Voltage	DV_{CC} = AV_{CC} = +4.5V		**0.8**	V (max)
$I_{IN(1)}$	Logical “1” Input Current		0.1	**1.0**	µA (max)
$I_{IN(0)}$	Logical “0” Input Current		0.1	**1.0**	µA (max)
$V_{OUT(1)}$	Logical “1” Output Voltage	DV_{CC} = AV_{CC} = +4.5V, I_{OUT} = −360 µA I_{OUT} = −100 µA		 **2.4** **4.25**	 V (min) V (min)
$V_{OUT(0)}$	Logical “0” Output Voltage	DV_{CC} = AV_{CC} = +4.5V, I_{OUT} = 1.6 mA		**0.4**	V (max)

(1) Typicals are at +25°C and represent most likely parametric norm.
(2) Tested limits are specified to AOQL (Average Outgoing Quality Level).

DC ELECTRICAL CHARACTERISTICS (continued)

The following specifications apply for DV_{CC} = AV_{CC} = +5V, $V_{REF+(SENSE)}$ = +4.096V, $V_{REF-(SENSE)}$ = AGND, and f_s = 1.5 MHz, unless otherwise specified. **Boldface limits apply for T_A = T_J from T_{MIN} to T_{MAX};** all other limits T_A = T_J = +25°C.

Symbol	Parameter	Conditions	Typ(1)	Limit(2)	Units (Limit)
I_{OUT}	TRI-STATE Output Leakage Current	Pins DB0–DB11	0.1	**3**	µA (max)
C_{OUT}	TRI-STATE Output Capacitance	Pins DB0–DB11	5		pF
C_{IN}	Digital Input Capacitance		4		pF
DI_{CC}	DV_{CC} Supply Current		2	**3**	mA (max)
AI_{CC}	AV_{CC} Supply Current		32	**37**	mA (max)
$I_{STANDBY}$(3)	Standby Current (DI_{CC} + AI_{CC})	$\overline{PD}$ = 0V	50		µA

(3) The digital power supply current takes up to 10 seconds to decay to its final value after PD is pulled low. This prohibits production testing of the standby current. Some parts may exhibit significantly higher standby currents than the 50 µA typical.

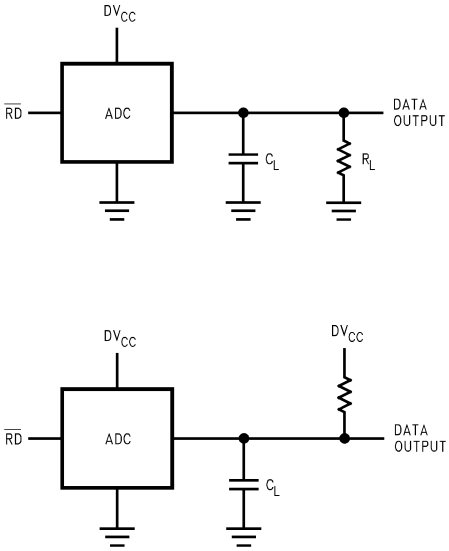
AC ELECTRICAL CHARACTERISTICS

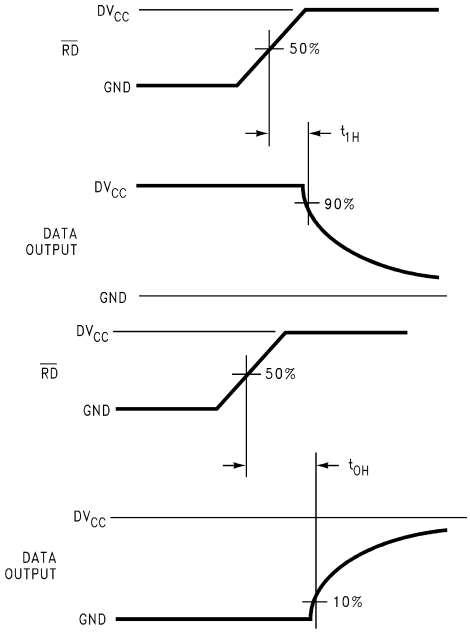
The following specifications apply for DV_{CC} = AV_{CC} = +5V, $V_{REF+(SENSE)}$ = +4.096V, $V_{REF-(SENSE)}$ = AGND, and f_s = 1.5 MHz, unless otherwise specified. **Boldface limits apply for T_A = T_J from T_{MIN} to T_{MAX};** all other limits T_A = T_J = +25°C.

Symbol	Parameter	Conditions	Typ(1)	Limit(2)	Units (Limits)
f_s	Maximum Sampling Rate ($1/t_{THROUGHPUT}$)			**1.5**	MHz (min)
t_{CONV}	Conversion Time (S/$\overline{H}$ Low to EOC High)		580	**510** **660**	ns (min) ns (max)
t_{AD}	Aperture Delay (S/$\overline{H}$ Low to Input Voltage Held)		20		ns
$t_{S/\overline{H}}$	S/$\overline{H}$ Pulse Width		10	**5** **400**	ns (min) ns (max)
t_{EOC}	S/$\overline{H}$ Low to EOC Low		90	**60** **126**	ns (min) ns (max)
t_{ACC}	Access Time ($\overline{RD}$ Low or OE High to Data Valid)	C_L = 100 pF	10	**20**	ns (max)
t_{1H}, t_{0H}	TRI-STATE Control ($\overline{RD}$ High or OE Low to Databus TRI-STATE)	R_L = 1k, C_L = 10 pF	25	**40**	ns (max)
$t_{\overline{INTH}}$	Delay from $\overline{RD}$ Low to $\overline{INT}$ High	C_L = 100 pF	35	**60**	ns (max)
$t_{\overline{INTL}}$	Delay from EOC High to $\overline{INT}$ Low	C_L = 100 pF	−25	**−35** **−5**	ns (min) ns (max)
t_{UPDATE}	EOC High to New Data Valid		5	**15**	ns (max)
t_{MS}	Multiplexer Address Setup Time (MUX Address Valid to EOC Low)			**50**	ns (min)
t_{MH}	Multiplexer Address Hold Time (EOC Low to MUX Address Invalid)			**50**	ns (min)
$t_{\overline{CSS}}$	$\overline{CS}$ Setup Time ($\overline{CS}$ Low to $\overline{RD}$ Low, S/$\overline{H}$ Low, or OE High)			**20**	ns (min)
$t_{\overline{CSH}}$	$\overline{CS}$ Hold Time ($\overline{CS}$ High after $\overline{RD}$ High, S/$\overline{H}$ High, or OE Low)			**20**	ns (min)
t_{WU}	Wake-Up Time ($\overline{PD}$ High to First S/$\overline{H}$ Low)		1		µs

(1) Typicals are at +25°C and represent most likely parametric norm.
(2) Tested limits are specified to AOQL (Average Outgoing Quality Level).

TRI-STATE TEST CIRCUIT AND WAVEFORMS





TYPICAL PERFORMANCE CHARACTERISTICS

Offset and Fullscale Error Change vs Reference Voltage

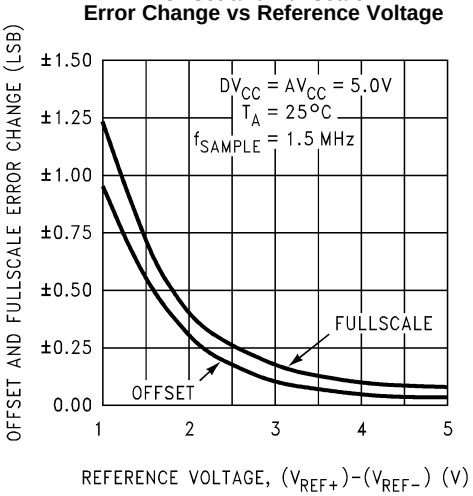


Figure 3.

Linearity Error Change vs Reference Voltage

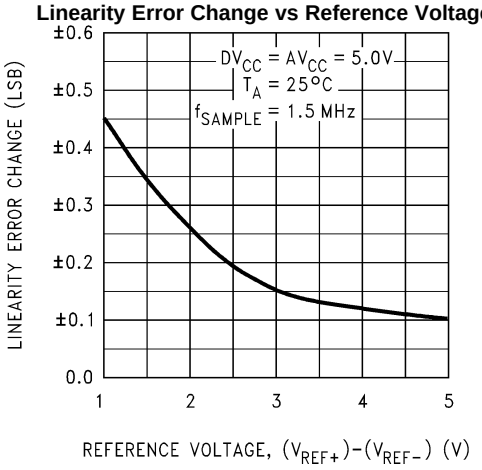


Figure 4.

Mux ON Resistance vs Input Voltage

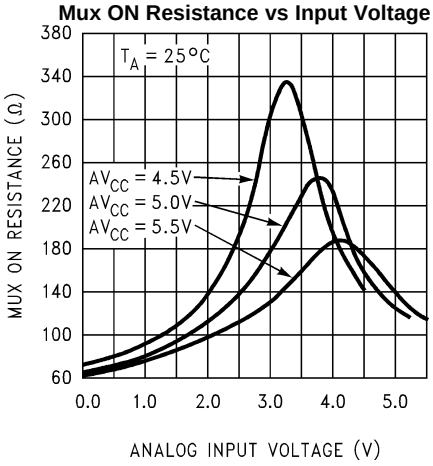


Figure 5.

Digital Supply Current vs Temperature

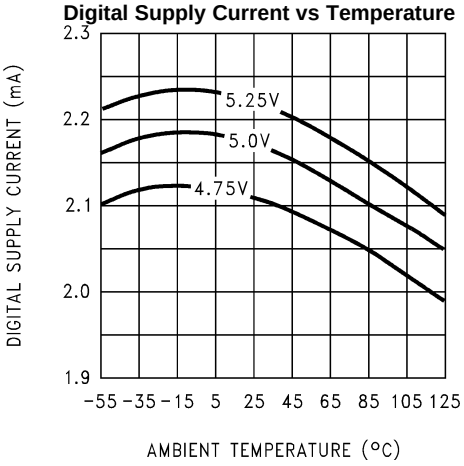


Figure 6.

Analog Supply Current vs Temperature

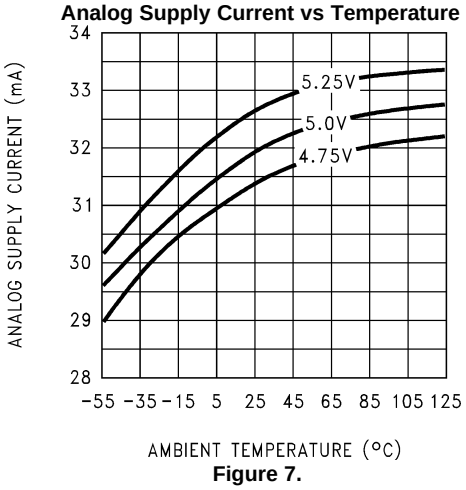


Figure 7.

Current Consumption in Standby Mode vs Voltage on Digital Input Pins

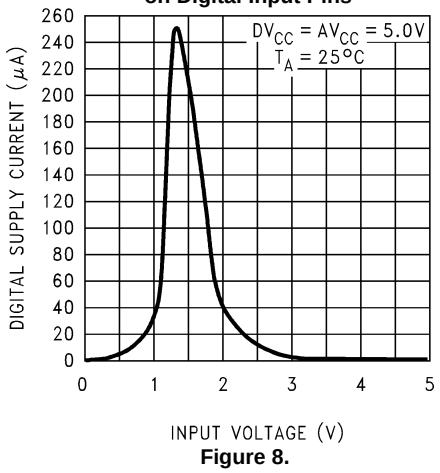


Figure 8.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Conversion Time (t_{CONV}) vs Temperature

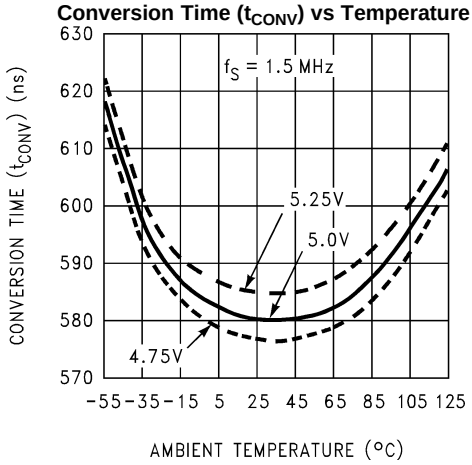


Figure 9.

EOC Delay Time (t_{EOC}) vs Temperature

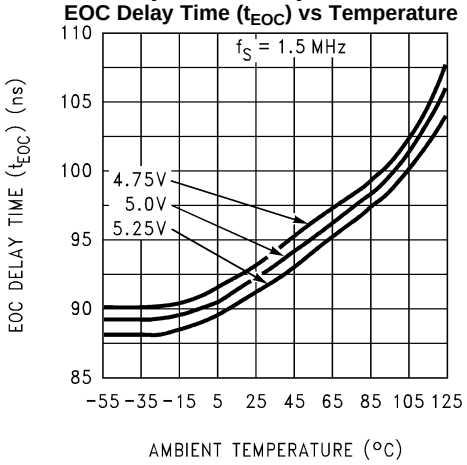


Figure 10.

Spectral Response

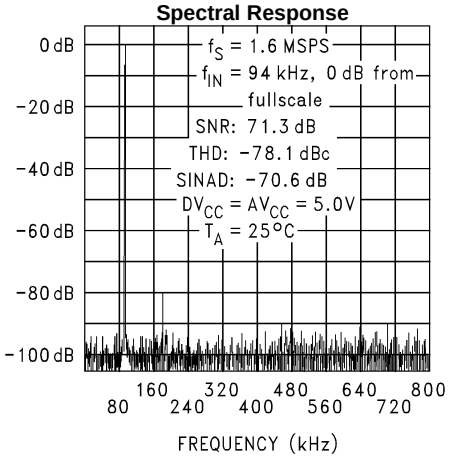


Figure 11.

SINAD vs Input Frequency (ADC In)

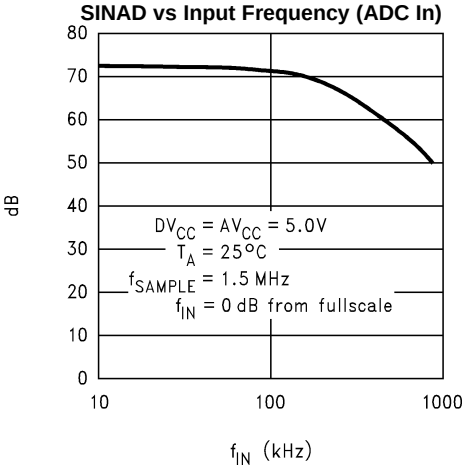


Figure 12.

SNR vs Input Frequency (ADC In)

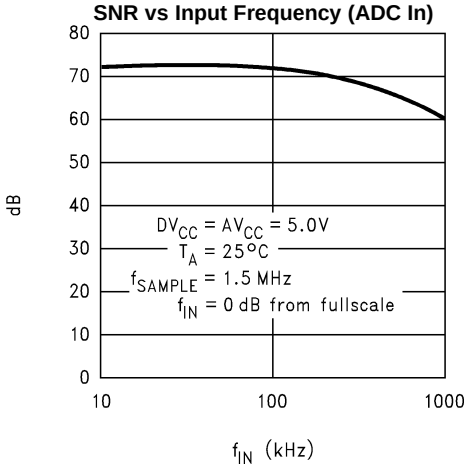


Figure 13.

THD vs Input Frequency (ADC In)

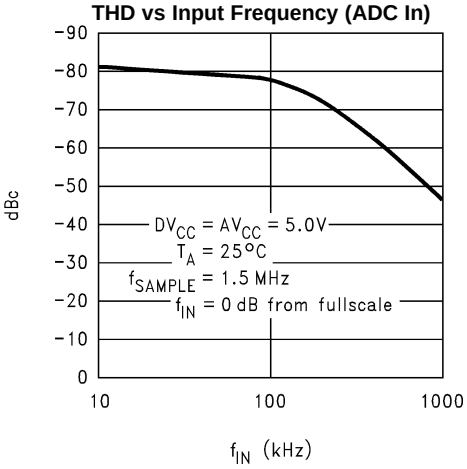


Figure 14.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

SINAD vs Input Frequency (Through Mux)

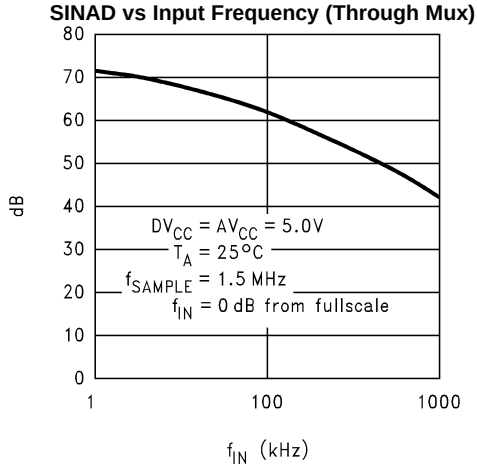


Figure 15.

SNR vs Input Frequency (Through Mux)

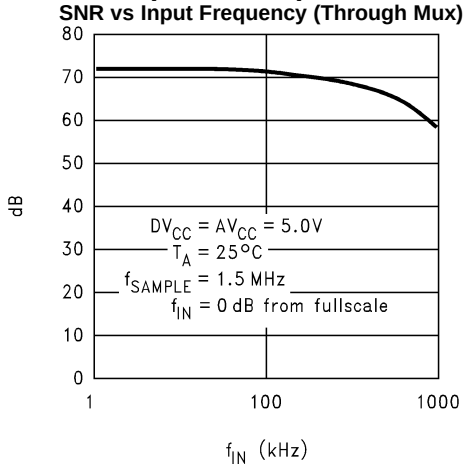


Figure 16.

THD vs Input Frequency (Through Mux)

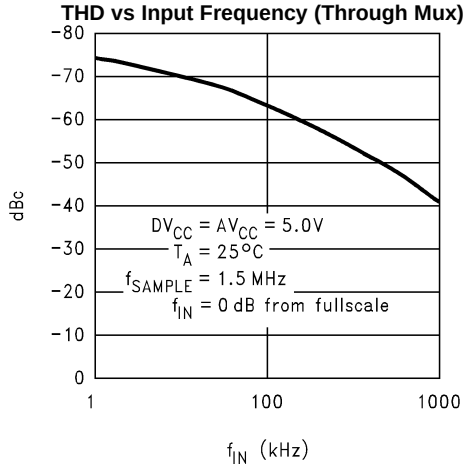


Figure 17.

SNR and THD vs Source Impedance

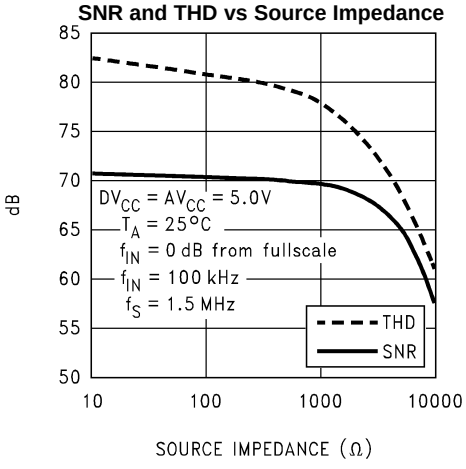


Figure 18.

SNR and THD vs Reference Voltage

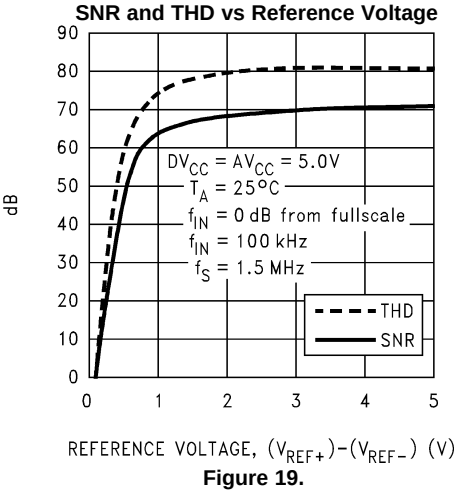


Figure 19.

TIMING DIAGRAMS

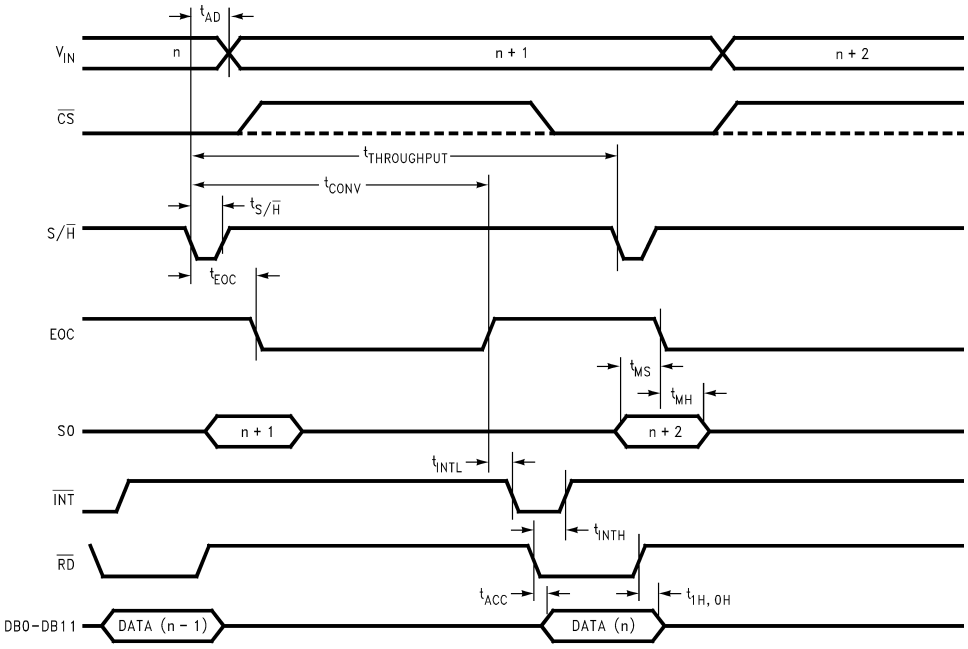


Figure 20. Interrupt Interface Timing (MODE = 0, OE = 1)

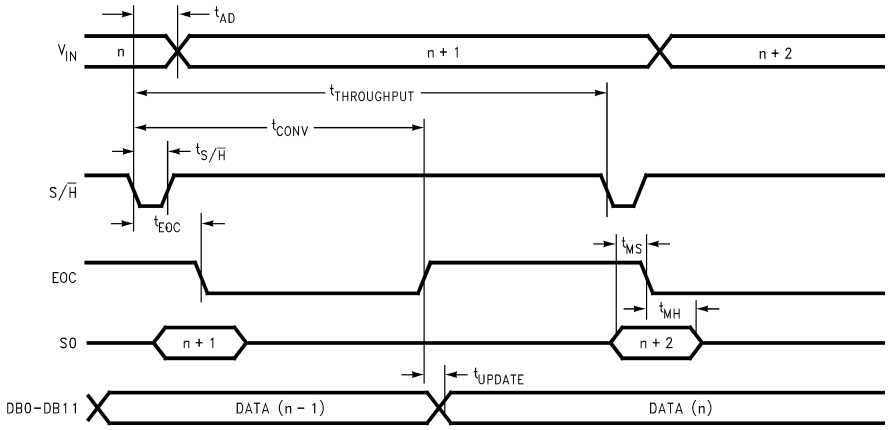


Figure 21. High Speed Interface Timing (MODE = 0, OE = 1, $\overline{CS}$ = 0, $\overline{RD}$ = 0)

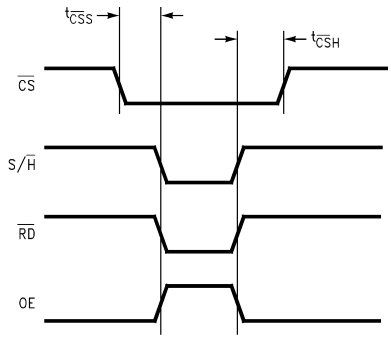


Figure 22. $\overline{CS}$ Setup and Hold Timing for S/$\overline{H}$, $\overline{RD}$, and OE

FUNCTIONAL DESCRIPTION

The ADC12662 performs a 12-bit analog-to-digital conversion using a 3 step flash technique. The first flash determines the six most significant bits, the second flash generates four more bits, and the final flash resolves the two least significant bits. Figure 23 shows the major functional blocks of the converter. It consists of a 2½-bit Voltage Estimator, a resistor ladder with two different resolution voltage spans, a sample/hold capacitor, a 4-bit flash converter with front end multiplexer, a digitally corrected DAC, and a capacitive voltage divider. To pipeline the converter, there are two sample/hold capacitors and 4-bit flash sections, which allows the converter to acquire the next input sample while converting the previous one. Only one of the flash converter pairs is shown in Figure 23 to reduce complexity.

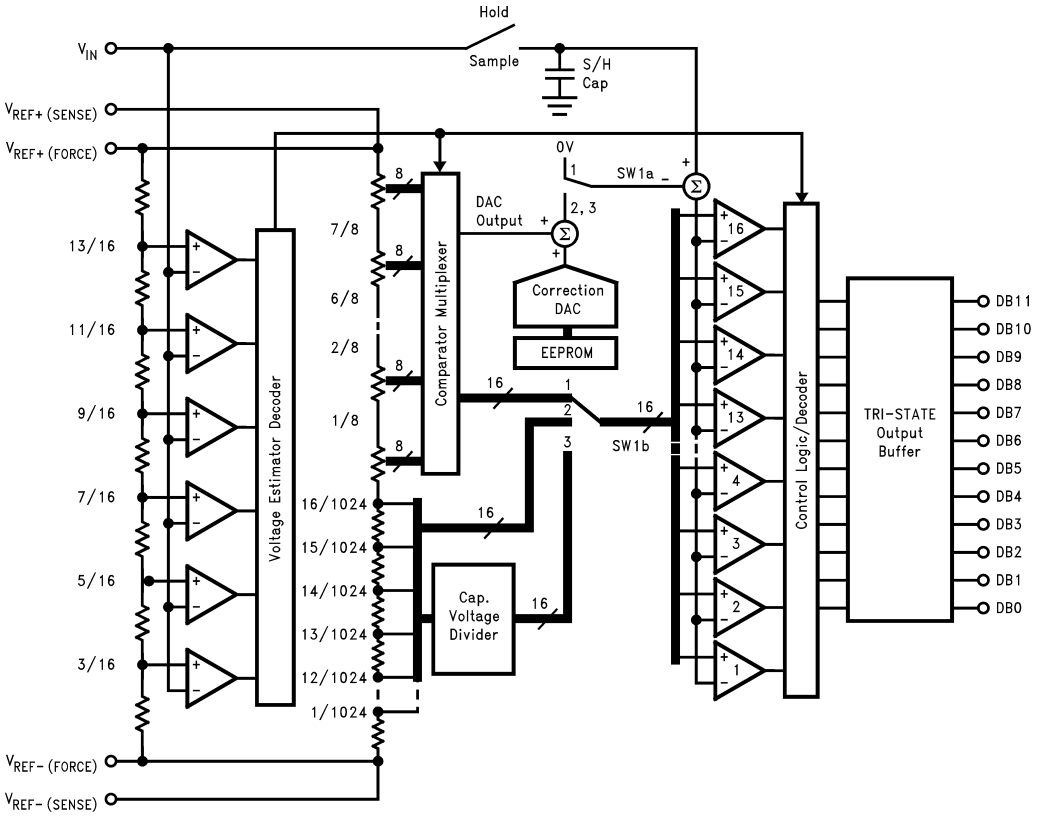


Figure 23. Functional Block Diagram

The resistor string near the center of the block diagram in Figure 23 generates the 6-bit and 10-bit reference voltages for the first two conversions. Each of the 16 resistors at the bottom of the string is equal to 1/1024 of the total string resistance. These resistors form the **LSB Ladder** (The weight of each resistor on the LSB ladder is actually equivalent to four 12-bit LSBs. It is called the LSB ladder because it has the highest resolution of all the ladders in the converter) and have a voltage drop of 1/1024 of the total reference voltage ($V_{REF+} - V_{REF-}$) across each of them. The remaining resistors form the **MSB Ladder**. It is comprised of eight groups of eight resistors each connected in series (the lowest MSB ladder resistor is actually the entire LSB ladder). Each MSB Ladder section has ⅛ of the total reference voltage across it. Within a given MSB ladder section, each of the eight MSB resistors has 1/64 of the total reference voltage across it. Tap points are found between all of the resistors in both the MSB and LSB ladders. The Comparator Multiplexer can connect any of these tap points, in two adjacent groups of eight, to the sixteen comparators shown at the right of Figure 23. This function provides the necessary reference voltages to the comparators during the first two flash conversions.

The six comparators, seven-resistor string (Estimator DAC ladder), and Estimator Decoder at the left of Figure 23 form the Voltage Estimator. The Estimator DAC, connected between V_{REF+} and V_{REF-}, generates the reference voltages for the six Voltage Estimator comparators. The comparators perform a very low resolution A/D conversion to obtain an "estimate" of the input voltage. This estimate is used to control the placement of the Comparator Multiplexer, connecting the appropriate MSB ladder section to the sixteen flash comparators. A total of only 22 comparators (6 in the Voltage Estimator and 16 in the flash converter) is required to quantize the input to 6 bits, instead of the 64 that would be required using a traditional 6-bit flash.

Prior to a conversion, the Sample/Hold switch is closed, allowing the voltage on the S/H capacitor to track the input voltage. Switch 1 is in position 1. A conversion begins by opening the Sample/Hold switch and latching the output of the Voltage Estimator. The estimator decoder then selects two adjacent banks of tap points along the MSB ladder. These sixteen tap points are then connected to the sixteen flash converters. For example, if the input voltage is between 5/16 and 7/16 of V_{REF} ($V_{REF} = V_{REF+} - V_{REF-}$), the estimator decoder instructs the comparator multiplexer to select the sixteen tap points between 2/8 and 4/8 (4/16 and 8/16) of V_{REF} and connects them to the sixteen flash converters. The first flash conversion is now performed, producing the first 6 MSBs of data.

At this point, Voltage Estimator errors as large as 1/16 of V_{REF} will be corrected since the flash converters are connected to ladder voltages that extend beyond the range specified by the Voltage Estimator. For example, if $(7/16)V_{REF} < V_{IN} < (9/16)V_{REF}$, the Voltage Estimator's comparators tied to the tap points below $(9/16)V_{REF}$ will output "1"s (000111). This is decoded by the estimator decoder to "10". The 16 comparators will be placed on the MSB ladder tap points between $(3/8)V_{REF}$ and $(5/8)V_{REF}$. This overlap of $(1/16)V_{REF}$ will automatically cancel a Voltage Estimator error of up to 256 LSBs. If the first flash conversion determines that the input voltage is between $(3/8)V_{REF}$ and $((4/8)V_{REF} - LSB/2)$, the Voltage Estimator's output code will be corrected by subtracting "1", resulting in a corrected value of "01" for the first two MSBs. If the first flash conversion determines that the input voltage is between $(4/8)V_{REF} - LSB/2)$ and $(5/8)V_{REF}$, the voltage estimator's output code is unchanged.

The results of the first flash and the Voltage Estimator's output are given to the factory-programmed on-chip EEPROM which returns a correction code corresponding to the error of the MSB ladder at that tap. This code is converted to a voltage by the Correction DAC. To generate the next four bits, SW1 is moved to position 2, so the ladder voltage and the correction voltage are subtracted from the input voltage. The remainder is applied to the sixteen flash converters and compared with the 16 tap points from the LSB ladder.

The result of this second conversion is accurate to 10 bits and describes the input remainder as a voltage between two tap points (V_H and V_L) on the LSB ladder. To resolve the last two bits, the voltage across the ladder resistor (between V_H and V_L) is divided up into 4 equal parts by the capacitive voltage divider, shown in Figure 24. The divider also creates 6 LSBs below V_L and 6 LSBs above V_H to provide overlap used by the digital error correction. SW1 is moved to position 3, and the remainder is compared with these 16 new voltages. The output is combined with the results of the Voltage Estimator, first flash, and second flash to yield the final 12-bit result.

By using the same sixteen comparators for all three flash conversions, the number of comparators needed by the multi-step converter is significantly reduced when compared to standard multi-step techniques.

APPLICATIONS INFORMATION

MODES OF OPERATION

The ADC12662 has two interface modes: An interrupt/read mode and a high speed mode. Figure 20 and *2* show the timing diagrams for these interfaces.

In order to clearly show the relationship between S/$\overline{H}$, $\overline{CS}$, $\overline{RD}$, and OE, the control logic decoding section of the ADC12662 is shown in Figure 25.

Interrupt Interface

As shown in Figure 20, the falling edge of S/$\overline{H}$ holds the input voltage and initiates a conversion. At the end of the conversion, the EOC output goes high and the $\overline{INT}$ output goes low, indicating that the conversion results are latched and may be read by pulling $\overline{RD}$ low. The falling edge of $\overline{RD}$ resets the $\overline{INT}$ line. Note that $\overline{CS}$ must be low to enable S/$\overline{H}$ or $\overline{RD}$.

High Speed Interface

The Interrupt interface works well at lower speeds, but few microprocessors could keep up with the 1 µs interrupts that would be generated if the ADC12662 was running at full speed. The most efficient interface is shown in Figure 21. Here the output data is always present on the databus, and the $\overline{INT}$ to $\overline{RD}$ delay is eliminated.

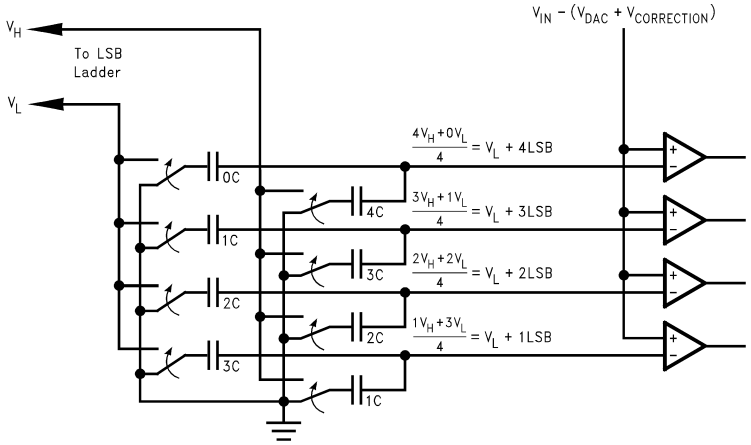


Figure 24. The Capacitive Voltage Divider

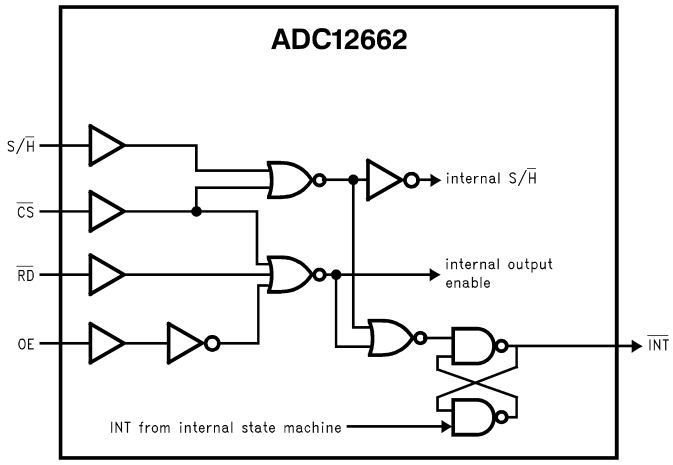


Figure 25. ADC Control Logic

THE ANALOG INPUT

The analog input of the ADC12662 can be modeled as two small resistances in series with the capacitance of the input hold capacitor (C_{IN}), as shown in Figure 26. The S/H switch is closed during the Sample period, and open during Hold. The source has to charge C_{IN} to the input voltage within the sample period. Note that the source impedance of the input voltage (R_{SOURCE}) has a direct effect on the time it takes to charge C_{IN}. If R_{SOURCE} is too large, the voltage across C_{IN} will not settle to within 0.5 LSBs of V_{SOURCE} before the conversion begins, and the conversion results will be incorrect. From a dynamic performance viewpoint, the combination of R_{SOURCE}, R_{MUX}, R_{SW}, and C_{IN} form a low pass filter. Minimizing R_{SOURCE} will increase the frequency response of the input stage of the converter.

Typical values for the components shown in Figure 26 are: R_{MUX} = 100Ω, R_{SW} = 100Ω, and C_{IN} = 25 pF. The settling time to n bits is:

$$t_{SETTLE} = (R_{SOURCE} + R_{MUX} + R_{SW}) * C_{IN} * n * \ln(2). \quad (1)$$

The bandwidth of the input circuit is:

$$f_{-3dB} = 1/(2 * 3.14 * (R_{SOURCE} + R_{MUX} + R_{SW}) * C_{IN}) \quad (2)$$

The ADC12662 is operated in a pipelined sequence, with one hold capacitor acquiring the next sample while a conversion is being performed on the voltage stored on the other hold capacitor. This gives the source over t_{CONV} seconds to charge the hold capacitor to its final value. At 1.5 MHz, the settling time must be less than 667 ns. Using the settling time equation and component values given, the maximum source impedance that will allow the input to settle to ½ LSB (n = 13) at full speed is ~2.8 kΩ. To ensure ½ LSB settling over temperature and device-to-device variation, R_{SOURCE} should be a maximum of 500Ω when the converter is operated at full speed.

If the signal source has a high output impedance, its output should be buffered with an operational amplifier capable of driving a switched 25 pF/100Ω load. Any ringing or instabilities at the op amp's output during the sampling period can result in conversion errors. The LM6361 high speed op amp is a good choice for this application due to its speed and its ability to drive large capacitive loads. Figure 27 shows the LM6361 driving the ADC IN input of an ADC12662. The 100 pF capacitor at the input of the converter absorbs some of the high frequency transients generated by the S/H switching, reducing the op amp transient response requirements. The 100 pF capacitor should only be used with high speed op amps that are unconditionally stable driving capacitive loads.

Another benefit of using a high speed buffer is improved THD performance when using the multiplexer of the ADC12662. The MUX on-resistance is somewhat non-linear over input voltage, causing the RC time constant formed by C_{IN}, R_{MUX}, and R_{SW} to vary depending on the input voltage. This results in increasing THD with increasing frequency. Inserting the buffer between the MUX OUT and the ADC IN terminals as shown in Figure 27 will eliminate the loading on R_{MUX}, significantly reducing the THD of the multiplexed system.

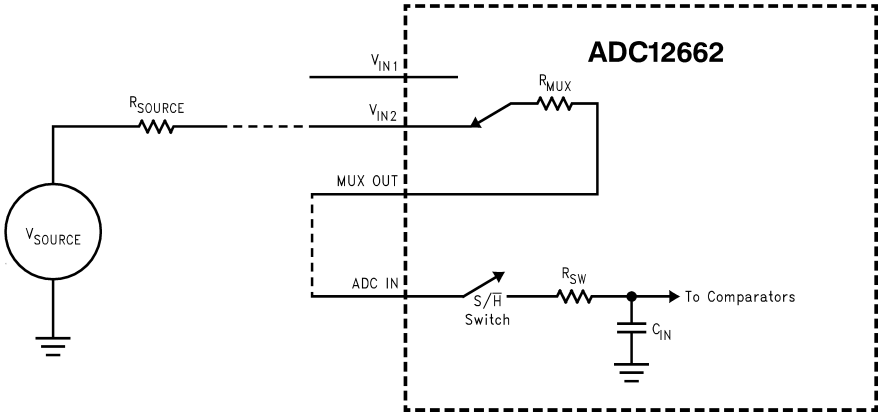


Figure 26. Simplified ADC12662 Input Stage

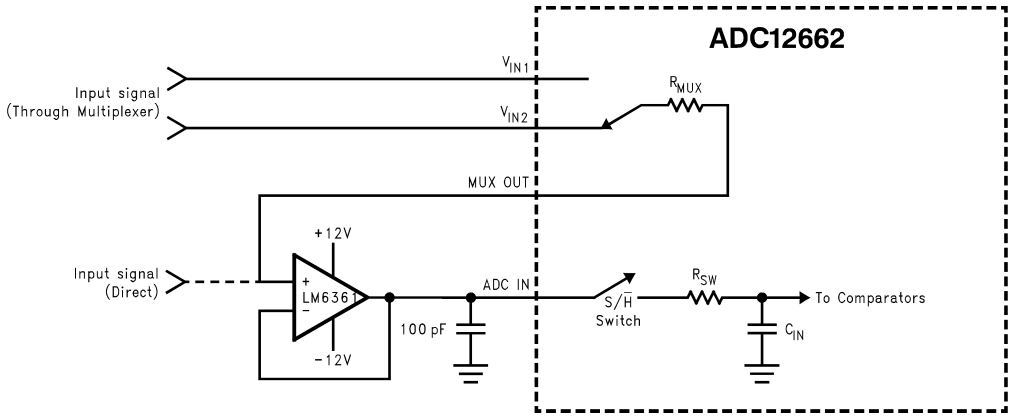


Figure 27. Buffering the Input with an LM6361 High Speed Op Amp

Correct converter operation will be obtained for input voltages greater than AGND − 50 mV and less than AV_{CC} + 50 mV. Avoid driving the signal source more than 300 mV higher than AV_{CC}, or more than 300 mV below AGND. If an analog input pin is forced beyond these voltages, the current flowing through that pin should be limited to 25 mA or less to avoid permanent damage to the IC. The sum of all the overdrive currents into all pins must be less than 50 mA. When the input signal is expected to extend more than 300 mV beyond the power supply limits for any reason (unknown/uncontrollable input voltage range, power-on transients, fault conditions, etc.) some form of input protection, such as that shown in Figure 28, should be used.

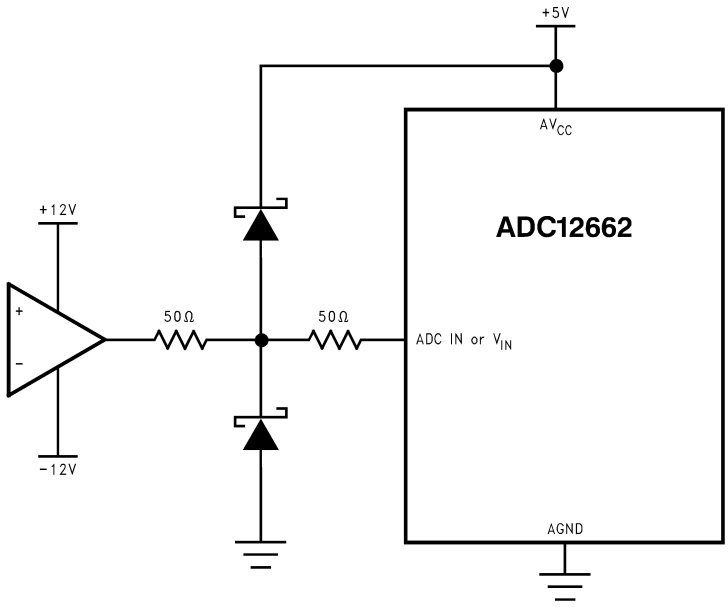


Figure 28. Input Protection

ANALOG MULTIPLEXER

The ADC12662 has an input multiplexer that is controlled by the logic level on pin S0 when EOC goes low, as shown in Figure 20 and Figure 21. Multiplexer setup and hold times with respect to the S/$\overline{H}$ input can be determined by these two equations:

$$t_{MS\ (wrt\ S/\overline{H})} = t_{MS} - t_{EOC\ (min)} = 50 - 60 = -10\ ns \quad (3)$$

$$t_{MH\ (wrt\ S/\overline{H})} = t_{MH} + t_{EOC\ (max)} = 50 + 125 = 175\ ns \quad (4)$$

Note that $t_{MS\ (wrt\ S/\overline{H})}$ is a negative number; this indicates that the data on S0 must become valid within 10 ns after S/$\overline{H}$ goes low in order to meet the setup time requirements. S0 must be valid for a length of

$$(t_{MH} + t_{EOC\ (max)}) - (t_{MS} - t_{EOC\ (min)}) = 185\ ns. \quad (5)$$

Table 1 shows how the input channels are assigned:

Table 1. ADC12662 Input Multiplexer Programming

S0	Channel
0	V_{IN1}
1	V_{IN2}

The output of the multiplexer is available to the user via the MUX OUT pin. This output allows the user to perform additional signal processing, such as filtering or gain, before the signal is returned to the ADC IN input and digitized. If no additional signal processing is required, the MUX OUT pin should be tied directly to the ADC IN pin.

See APPLICATIONS for a simple circuit that will alternate between the two inputs while converting at full speed.

REFERENCE INPUTS

In addition to the fully differential V_{REF+} and V_{REF-} reference inputs used on most Texas Instruments ADCs, the ADC12662 has two sense outputs for precision control of the ladder voltage. These sense inputs compensate for errors due to IR drops between the reference source and the ladder itself. The resistance of the reference ladder is typically 750Ω. The parasitic resistance (R_P) of the package leads, bond wires, PCB traces, etc. can easily be 0.5Ω to 1.0Ω or more. This may not be significant at 8-bit or 10-bit resolutions, but at 12 bits it can introduce voltage drops causing offset and gain errors as large as 6 LSBs.

The ADC12662 provides a means to eliminate this error by bringing out two additional pins that sense the exact voltage at the top and bottom of the ladder. With the addition of two op amps, the voltages on these internal nodes can be forced to the exact value desired, as shown in Figure 29.

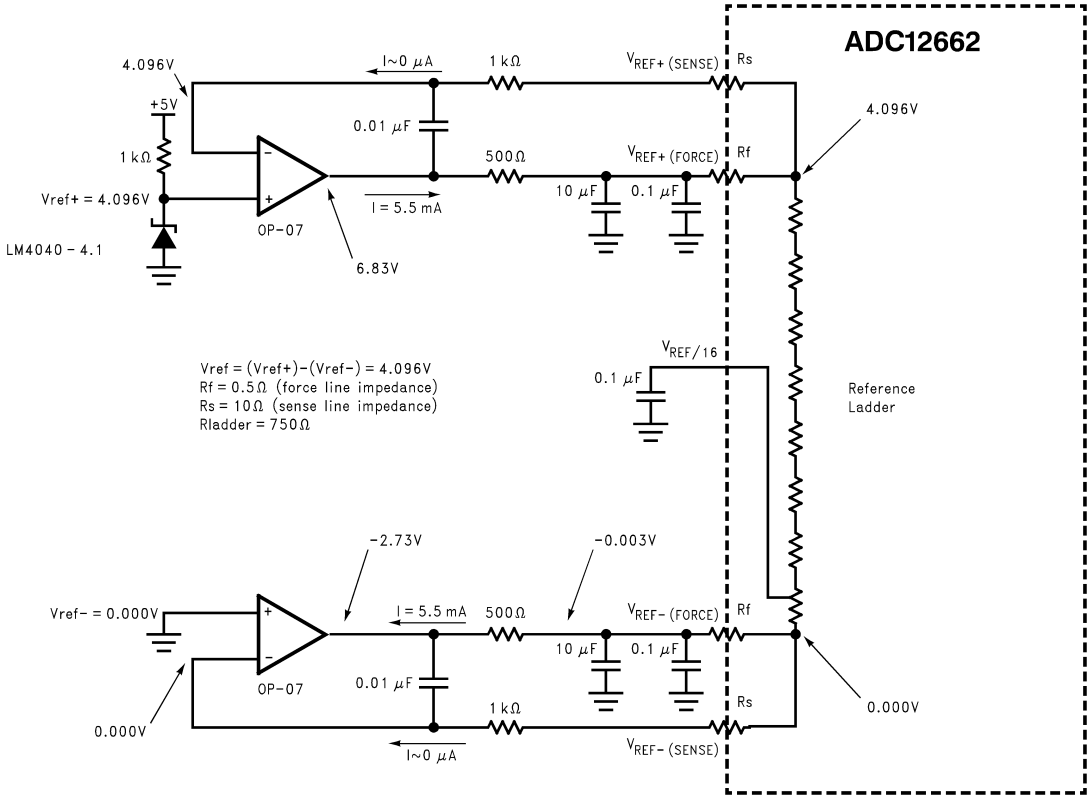


Figure 29. Reference Ladder Force and Sense Inputs

Since the current flowing through the SENSE lines is essentially zero, there is negligible voltage drop across R_S and the 1 kΩ resistor, so the voltage at the inverting input of the op amp accurately represents the voltage at the top (or bottom) of the ladder. The op amp drives the FORCE input and forces the voltage at the ends of the ladder to equal the voltage at the op amps's non-inverting input, plus or minus its input offset voltage. For this reason op amps with low V_{OS}, such as the LM627 or LM607, should be used for this application. When used in this configuration, the ADC12662 has less than 2 LSBs of offset and 1.5 LSB of gain error without any user adjustments.

The 0.1 µF and 10 µF capacitors on the force inputs provide high frequency decoupling of the reference ladder. The 500Ω force resistors isolate the op amps from this large capacitive load. The 0.01 µF/1 kΩ network provides zero phase shift at high frequencies to ensure stability. Note that the op amp supplies in this example must be ±10V to ±15V to meet the input/output voltage range requirements of the LM627 and supply the sub-zero voltage to the $V_{REF-\ (FORCE)}$ pin. The $V_{REF/16}$ output should be bypassed to analog ground with a 0.1 µF ceramic capacitor.

The reference inputs are fully differential and define the zero to full-scale range of the input signal. They can be configured to span up to 5V (V_{REF-} = 0V, V_{REF+} = 5V), or they can be connected to different voltages (within the 0V to 5V limits) when other input spans are required. The ADC12662 is tested at $V_{REF-\ (SENSE)}$ = 0V, $V_{REF+\ (SENSE)}$ = 4.096V. Reducing the reference voltage span to less than 4V increases the sensitivity (reduces the LSB size) of the converter; however noise performance degrades when lower reference voltages are used. A plot of dynamic performance vs reference voltage is given in the TYPICAL PERFORMANCE CHARACTERISTICS section.

If the converter will be used in an application where DC accuracy is secondary to dynamic performance, then a simpler reference circuit may suffice. The circuit shown in Figure 30 will introduce several LSBs of offset and gain error, but INL, DNL, and all dynamic specifications will be unaffected.

All bypass capacitors should be located as close to the ADC12662 as possible to minimize noise on the reference ladder. The $V_{REF/16}$ output should be bypassed to analog ground with a 0.1 µF ceramic capacitor.

The LM4040 shunt voltage reference is available with a 4.096V output voltage. With initial accuracies as low as ± 0.1%, it makes an excellent reference for the ADC12662.

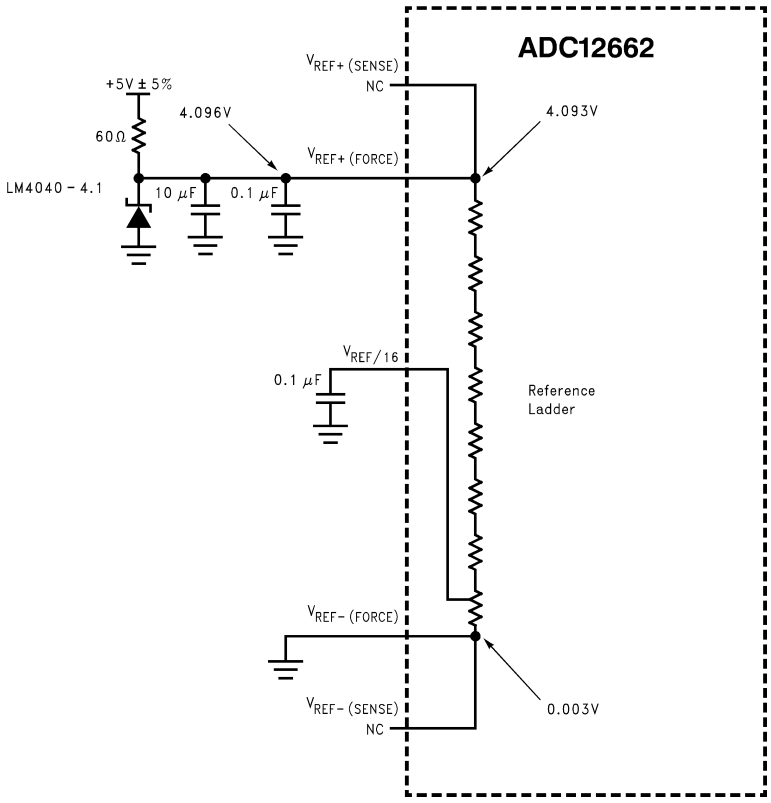


Figure 30. Using the V_{REF} Force Pins Only

POWER SUPPLY CONSIDERATIONS

The ADC12662 is designed to operate from a single +5V power supply. There are two analog supply pins (AV_{CC}) and one digital supply pin (DV_{CC}). These pins allow separate external bypass capacitors for the analog and digital portions of the circuit. To ensure proper operation of the converter, all three supply pins should be connected to the same voltage source. In systems with separate analog and digital supplies, the converter should be powered from the analog supply.

The ground pins are AGND (analog ground), DGND1 (digital input ground), and DGND2 (digital output ground). These pins allow for three separate ground planes for these sections of the chip. Isolating the analog section from the two digital sections reduces digital interference in the analog circuitry, improving the dynamic performance of the converter. Separating the digital outputs from the digital inputs (particularly the S/$\overline{H}$ input) reduces the possibility of ground bounce from the 12 data lines causing jitter on the S/$\overline{H}$ input. The analog ground plane should be connected to the Digital2 ground plane at the ground return for the power supply. The Digital1 ground plane should be tied to the Digital2 ground plane at the DGND1 and DGND2 pins.

Both AV_{CC} pins should be bypassed to the AGND ground plane with 0.1 µF ceramic capacitors. One of the two AV_{CC} pins should also be bypassed with a 10 µF tantalum capacitor. DV_{CC} should be bypassed to the DGND2 ground plane with a 0.1 µF capacitor in parallel with a 10 µF tantalum capacitor.

LAYOUT AND GROUNDING

In order to ensure fast, accurate conversions from the ADC12662, it is necessary to use appropriate circuit board layout techniques. Separate analog and digital ground planes are required to meet datasheet AC and DC limits. The analog ground plane should be low-impedance and free of noise from other parts of the system.

All bypass capacitors should be located as close to the converter as possible and should connect to the converter and to ground with short traces. The analog input should be isolated from noisy signal traces to avoid having spurious signals couple to the input. Any external component (e.g., a filter capacitor) connected across the converter's input should be connected to a very clean analog ground return point. Grounding the component at the wrong point will result in increased noise and reduced conversion accuracy.

Figure 31 gives an example of a suitable layout, including power supply routing, ground plane separation, and bypass capacitor placement. All analog circuitry (input amplifiers, filters, reference components, etc.) should be placed on the analog ground plane. All digital circuitry and I/O lines (excluding the S/$\overline{H}$ input) should use the digital2 ground plane as ground. The digital1 ground plane should only be used for the S/$\overline{H}$ signal generation.

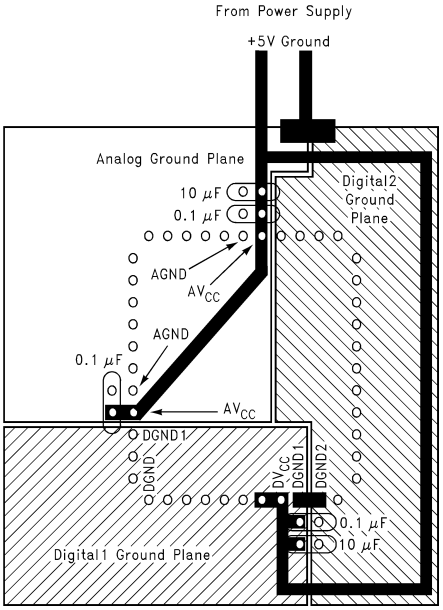


Figure 31. PC Board Layout

DYNAMIC PERFORMANCE

The ADC12662 is AC tested and its dynamic performance is ensured. In order to meet these specifications, the clock source driving the S/$\overline{H}$ input must be free of jitter. For the best AC performance, a crystal oscillator is recommended. For operation at or near the ADC12662's 1.5 MHz maximum sampling rate, a 1.5 MHz square wave will provide a good signal for the S/$\overline{H}$ input. As long as the duty cycle is near 50%, the waveform will be low for about 333 ns, which is within the 400 ns limit. When operating the ADC12662 at a sample rate of 1.25 MHz or below, the pulse width of the S/$\overline{H}$ signal must be smaller than half the sample period.

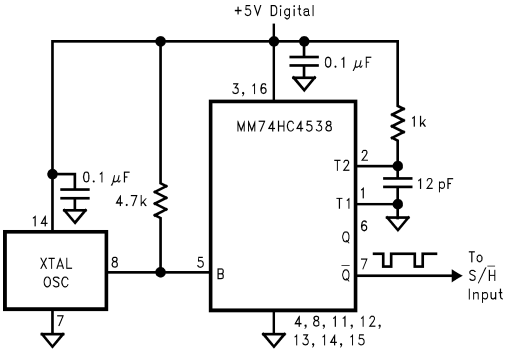


Figure 32. Crystal Clock Source

Figure 32 is an example of a low jitter S/$\overline{H}$ pulse generator that can be used with the ADC12662 and allow operation at sampling rates from DC to 1.5 MHz. A standard 4-pin DIP crystal oscillator provides a stable 1.5 MHz square wave. Since most DIP oscillators have TTL outputs, a 4.7k pullup resistor is used to raise the output high voltage to CMOS input levels. The output is fed to the trigger input (falling edge) of an MM74HC4538 one-shot. The 1k resistor and 12 pF capacitor set the pulse length to approximately 100 ns. The S/$\overline{H}$ pulse stream for the converter appears on the Q output of the HC4538. This is the S/$\overline{H}$ clock generator used on the ADC12062EVAL evaluation board. For lower power, a CMOS inverter-based crystal oscillator can be used in place of the DIP crystal oscillator. See Application Note AN-340 in the Texas Instruments CMOS Logic Databook for more information on CMOS crystal oscillators.

COMMON APPLICATION PITFALLS

Driving inputs (analog or digital) outside power supply rails. The Absolute Maximum Ratings state that all inputs must be between GND − 300 mV and V_{CC} + 300 mV. This rule is most often broken when the power supply to the converter is turned off, but other devices connected to it (op amps, microprocessors) still have power. Note that if there is no power to the converter, DGND = AGND = DV_{CC} = AV_{CC} = 0V, so all inputs should be within ±300 mV of AGND and DGND.

Driving a high capacitance digital data bus. The more capacitance the data bus has to charge for each conversion, the more instantaneous digital current required from DV_{CC} and DGND. These large current spikes can couple back to the analog section, decreasing the SNR of the converter. While adequate supply bypassing and separate analog and digital ground planes will reduce this problem, buffering the digital data outputs (with a pair of MM74HC541s, for example) may be necessary if the converter must drive a heavily loaded databus.

APPLICATIONS

Figure 33. 2's Complement Output

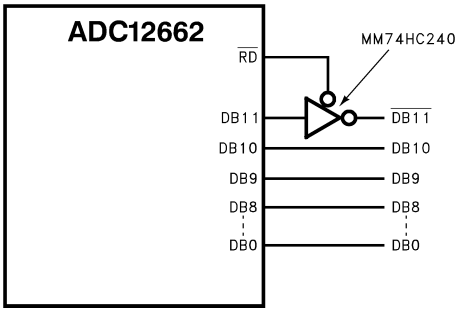


Figure 34. Ping-Ponging between V_{IN1} and V_{IN2}

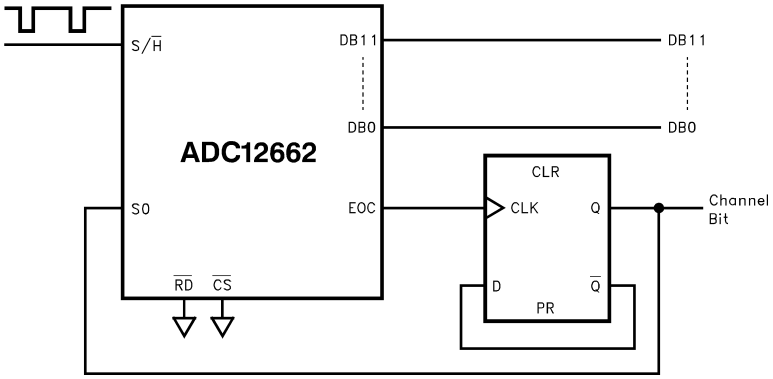
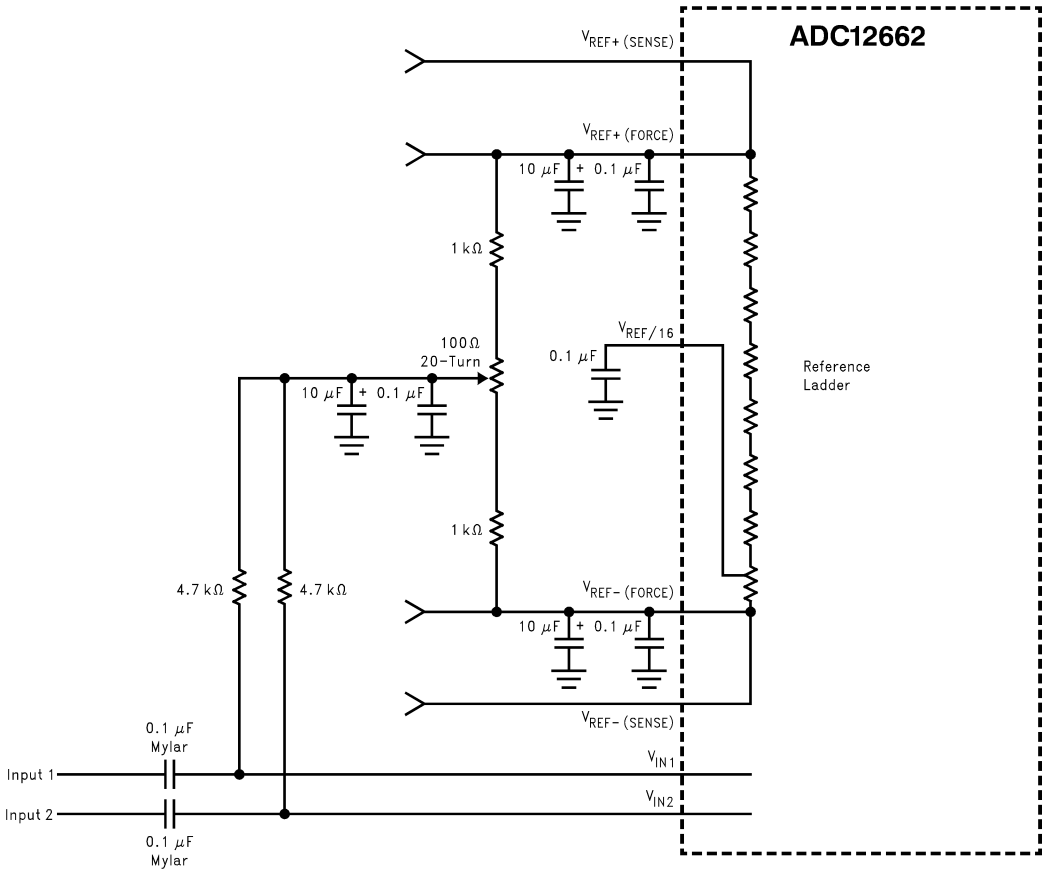


Figure 35. AC Coupling Bipolar Inputs



REVISION HISTORY

Changes from Revision B (April 2013) to Revision C **Page**

- Changed layout of National Data Sheet to TI format 22

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