PLLatinum™ Frequency Synthesizer for RF Personal Communications
LMX2325 2.5 GHz
LMX2320 2.0 GHz
LMX2315 1.2 GHz

Check for Samples: LMX2315, LMX2320, LMX2325

FEATURES

- **RF Operation up to 2.5 GHz**
- **2.7V to 5.5V Operation**
- **Low Current Consumption**
- **Dual Modulus Prescaler:**
  - **LMX2325: 32/33 or 64/65**
  - **LMX2320/LMX2315: 64/65 or 128/129**
- **Internal Balanced, Low Leakage Charge Pump**
- **Power Down Feature for Sleep Mode: I_{CC} = 30 µA (typ) at V_{CC} = 3V**
- **Small-Outline, Plastic, Surface Mount TSSOP, 0.173″ Wide**

APPLICATIONS

- **Cellular Telephone Systems**
  - **(GSM, IS-54, IS-95, (RCR-27)**
- **Portable Wireless Communications (DECT, PHS)**
- **CATV**
- **Other Wireless Communication Systems**

DESCRIPTION

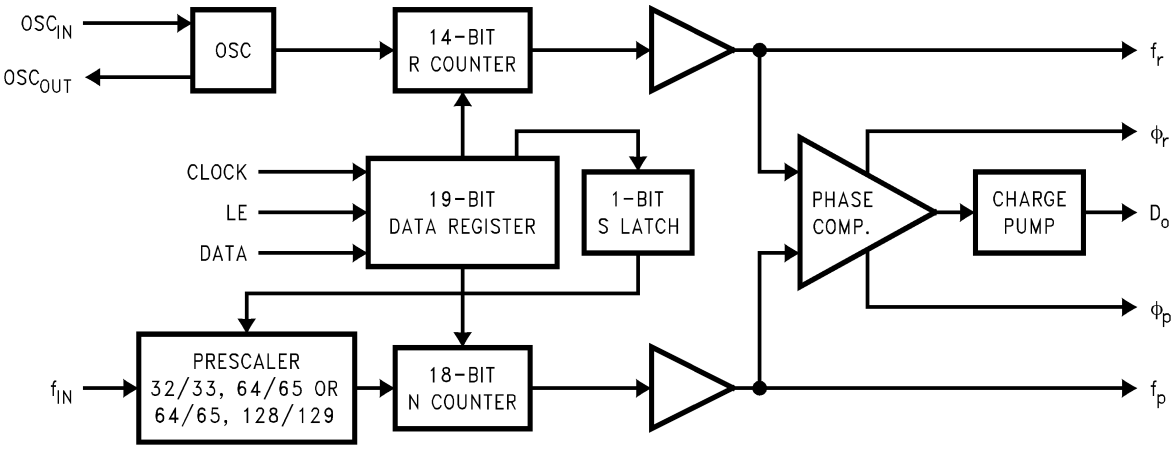
The LMX2315/2320/2325's are high performance frequency synthesizers with integrated prescalers designed for RF operation up to 2.5 GHz. They are fabricated using TI's ABiC IV BiCMOS process.

A 64/65 or a 128/129 divide ratio can be selected for the LMX2315 and LMX2320 RF synthesizer at input frequencies of up to 1.2 GHz and 2.0 GHz, while 32/33 and 64/65 divide ratios are available in the 2.5 GHz LMX2325. Using a proprietary digital phase locked loop technique, the LMX2315/2320/2325's linear phase detector characteristics can generate very stable, low noise signals for controlling a local oscillator.

Serial data is transferred into the LMX2320 and the LMX2325 via a three line MICROWIRE interface (Data, Enable, Clock). Supply voltage can range from 2.7V to 5.5V. The LMX2315, LMX2320 and the LMX2325 feature very low current consumption, typically 6 mA, 10 mA and 11 mA respectively.

The LMX2315, LMX2320 and the LMX2325 are available in a TSSOP 20-pin surface mount plastic package.

Block Diagram



Connection Diagram

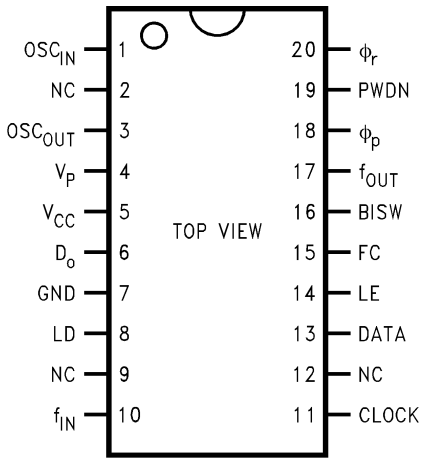
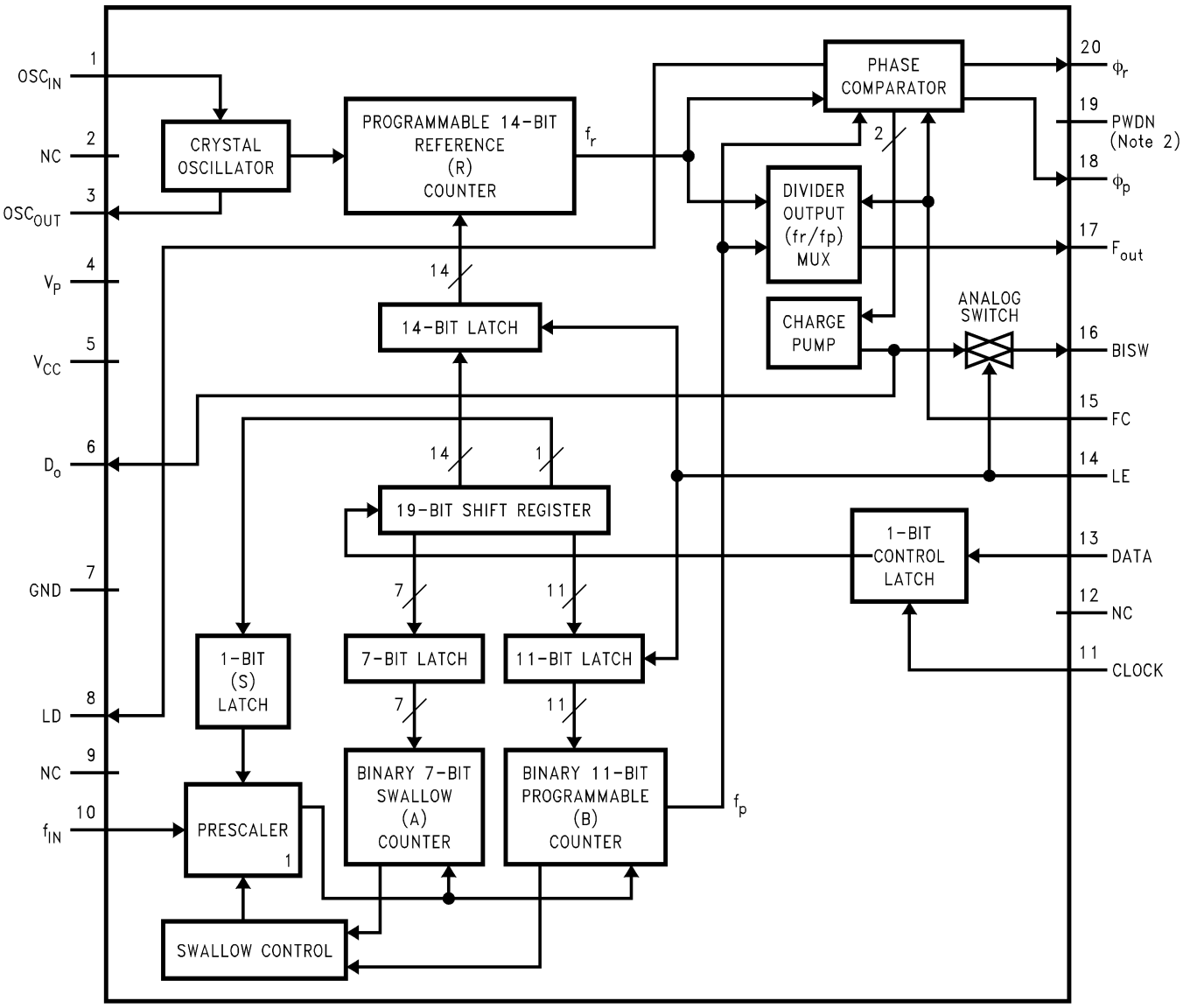


Figure 1. 20-Lead (0.173″ Wide) Thin Shrink Small Outline Package (PW)
LMX2315/LMX2320/LMX2325

PIN DESCRIPTIONS

Pin No.	Pin Name	I/O	Description
1	OSC_{IN}	I	Oscillator input. A CMOS inverting gate input intended for connection to a crystal resonator for operation as an oscillator. The input has a $V_{CC}/2$ input threshold and can be driven from an external CMOS or TTL logic gate. May also be used as a buffer for an externally provided reference oscillator.
3	OSC_{OUT}	O	Oscillator output.
4	V_P		Power supply for charge pump. Must be ≥ V_{CC}.
5	V_{CC}		Power supply voltage input. Input may range from 2.7V to 5.5V. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.
6	D_o	O	Internal charge pump output. For connection to a loop filter for driving the input of an external VCO.
7	GND		Ground.
8	LD	O	Lock detect. Output provided to indicate when the VCO frequency is in “lock”. When the loop is locked, the pin's output is HIGH with narrow low pulses.
10	f_{IN}	I	Prescaler input. Small signal input from the VCO.
11	CLOCK	I	High impedance CMOS Clock input. Data is clocked in on the rising edge, into the various counters and registers.
13	DATA	I	Binary serial data input. Data entered MSB first. LSB is control bit. High impedance CMOS input.
14	LE	I	Load enable input (with internal pull-up resistor). When LE transitions HIGH, data stored in the shift registers is loaded into the appropriate latch (control bit dependent). Clock must be low when LE toggles high or low. See Serial Data Input Timing Diagram.
15	FC	I	Phase control select (with internal pull-up resistor). When FC is LOW, the polarity of the phase comparator and charge pump combination is reversed.
16	BISW	O	Analog switch output. When LE is HIGH, the analog switch is ON, routing the internal charge pump output through BISW (as well as through D_o).
17	f_{OUT}	O	Monitor pin of phase comparator input. CMOS output.
18	φ_p	O	Output for external charge pump. φ_p is an open drain N-channel transistor and requires a pull-up resistor.
19	PWDN	I	Power Down (with internal pull-up resistor). PWDN = HIGH for normal operation. PWDN = LOW for power saving. Power down function is gated by the return of the charge pump to a TRI-STATE condition.
20	φ_r	O	Output for external charge pump. φ_r is a CMOS logic output.
2,9,12	NC		No connect.

Functional Block Diagram



The prescalar for the LMX2315 and LMX2320 is either 64/65 or 128/129, while the prescalar for the LMX2325 is 32/33 or 64/65.

The power down function is gated by the charge pump to prevent unwanted frequency jumps. Once the power down pin is brought low the part will go into power down mode when the charge pump reaches a TRI-STATE condition.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)(3)

Power Supply Voltage	
V_{CC}	−0.3V to +6.5V
V_P	−0.3V to +6.5V
Voltage on Any Pin with GND = 0V (V_I)	−0.3V to +6.5V
Storage Temperature Range (T_S)	−65°C to +150°C
Lead Temperature (T_L) (solder, 4 sec.)	+260°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed.
(2) This device is a high performance RF integrated circuit with an ESD rating < 2 kV and is ESD sensitive. Handling and assembly of this device should be done at ESD workstations.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

Recommended Operating Conditions

Power Supply Voltage	
V_{CC}	2.7V to 5.5V
V_P	V_{CC} to +5.5V
Operating Temperature (T_A)	−40°C to +85°C

Electrical Characteristics

LMX2325 and LMX2320 $V_{CC} = V_P = 3.0V$; LMX2315 $V_{CC} = V_P = 5.0V$; −40°C < T_A < 85°C, except as specified

Symbol	Parameter		Conditions	Min	Typ	Max	Units
I_{CC}	Power Supply Current	LMX2315	V_{CC} = 3.0V		6.0	8.0	mA
			V_{CC} = 5.0V		6.5	8.5	mA
		LMX2320	V_{CC} = 3.0V		10	13.5	mA
		LMX2325	V_{CC} = 3.0V		11	15	mA
$I_{CC-PWDN}$	Power Down Current		V_{CC} = 3.0V		30	180	µA
			V_{CC} = 5.0V		60	350	µA
f_{IN}	Maximum Operating Frequency	LMX2315				1.2	GHz
		LMX2320				2.0	
		LMX2325		1.2		2.5	
f_{OSC}	Oscillator Frequency			5		20	MHz
			No Load on OSC_{out}	5		40	MHz
f_φ	Phase Detector Frequency			10			MHz
Pf_{IN}	Input Sensitivity		V_{CC} = 2.7V to 3.3V	−15		+6	dBm
			V_{CC} = 3.3V to 5.5V	−10		+6	
V_{OSC}	Oscillator Sensitivity		OSC_{IN}	0.5			V_{PP}
V_{IH}	High-Level Input Voltage		(1)	0.7 V_{CC}			V
V_{IL}	Low-Level Input Voltage		(1)			0.3 V_{CC}	V
I_{IH}	High-Level Input Current (Clock, Data)		$V_{IH} = V_{CC}$ = 5.5V	−1.0		1.0	µA
I_{IL}	Low-Level Input Current (Clock, Data)		V_{IL} = 0V, V_{CC} = 5.5V	−1.0		1.0	µA
I_{IH}	Oscillator Input Current		$V_{IH} = V_{CC}$ = 5.5V			100	µA
I_{IL}			V_{IL} = 0V, V_{CC} = 5.5V	−100			µA

(1) Except f_{IN} and OSC_{IN}

Electrical Characteristics (continued)

LMX2325 and LMX2320 $V_{CC} = V_P = 3.0V$; LMX2315 $V_{CC} = V_P = 5.0V$; −40°C < T_A < 85°C, except as specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{IH}	High-Level Input Current (LE, FC)	$V_{IH} = V_{CC} = 5.5V$	−1.0		1.0	µA
I_{IL}	Low-Level Input Current (LE, FC)	$V_{IL} = 0V$, $V_{CC} = 5.5V$	−100		1.0	µA
$I_{Do\text{-}source}$	Charge Pump Output Current	$V_{CC} = V_P = 3.0V$, $V_{Do} = V_P/2$		−2.5		mA
$I_{Do\text{-}sink}$		$V_{CC} = V_P = 3.0V$, $V_{Do} = V_P/2$		2.5		mA
$I_{Do\text{-}source}$	Charge Pump Output Current	$V_{CC} = V_P = 5.0V$, $V_{Do} = V_P/2$		−5.0		mA
$I_{Do\text{-}sink}$		$V_{CC} = V_P = 5.0V$, $V_{Do} = V_P/2$		5.0		mA
$I_{Do\text{-}Tri}$	Charge Pump TRI-STATE Current	$0.5V \le V_{Do} \le V_P - 0.5V$ T = 85°C	−2.5		2.5	nA
I_{Do} vs V_{Do}	Charge Pump Output Current Magnitude Variation vs Voltage (2)	$0.5V \le V_{Do} \le V_P - 0.5V$ T = 25°C			15	%
$I_{Do\text{-}sink}$ vs $I_{Do\text{-}source}$	Charge Pump Output Current Sink vs Source Mismatch (2)	$V_{Do} = V_P/2$ T = 25°C			10	%
I_{Do}vs T	Charge Pump Output Current Magnitude Variation vs Temperature (2)	−40°C < T < 85°C $V_{Do} = V_P/2$		10		%
V_{OH}	High-Level Output Voltage	$I_{OH} = -1.0$ mA (3)	V_{CC} − 0.8			V
V_{OL}	Low-Level Output Voltage	$I_{OL} = 1.0$ mA (3)			0.4	V
V_{OH}	High-Level Output Voltage (OSC_{OUT})	$I_{OH} = -200$ µA	V_{CC} − 0.8			V
V_{OL}	Low-Level Output Voltage (OSC_{OUT})	$I_{OL} = 200$ µA			0.4	V
I_{OL}	Open Drain Output Current (φ_p)	$V_{CC} = 5.0V$, $V_{OL} = 0.4V$	1.0			mA
I_{OH}	Open Drain Output Current (φ_p)	$V_{OH} = 5.5V$			100	µA
R_{ON}	Analog Switch ON Resistance (2315)			100		Ω
t_{CS}	Data to Clock Set Up Time	See SERIAL DATA INPUT TIMING	50			ns
t_{CH}	Data to Clock Hold Time	See SERIAL DATA INPUT TIMING	10			ns
t_{CWH}	Clock Pulse Width High	See SERIAL DATA INPUT TIMING	50			ns
t_{CWL}	Clock Pulse Width Low	See SERIAL DATA INPUT TIMING	50			ns
t_{ES}	Clock to Enable Set Up Time	See SERIAL DATA INPUT TIMING	50			ns
t_{EW}	Enable Pulse Width	See SERIAL DATA INPUT TIMING	50			ns

(2) See related equations in Charge Pump Current Specification Definitions
(3) Except OSC_{OUT}

Typical Performance Characteristics

I_{CC} vs V_{CC} LMX2320/25

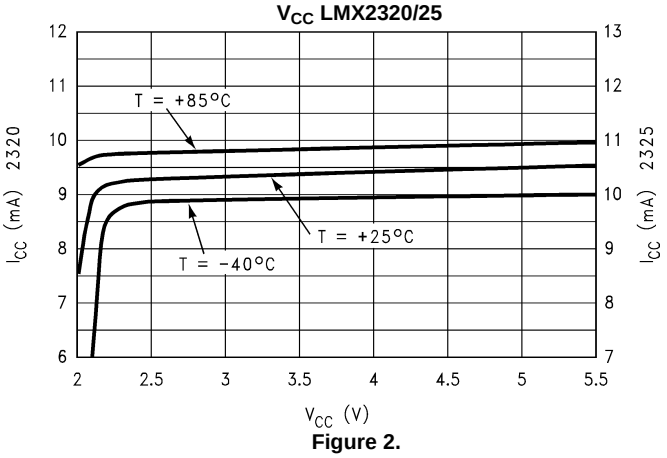


Figure 2.

I_{CC} vs V_{CC} LMX2315

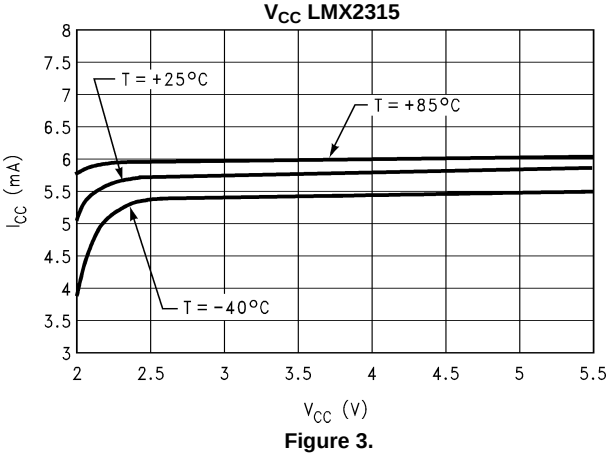


Figure 3.

Charge Pump Current vs D_o Voltage

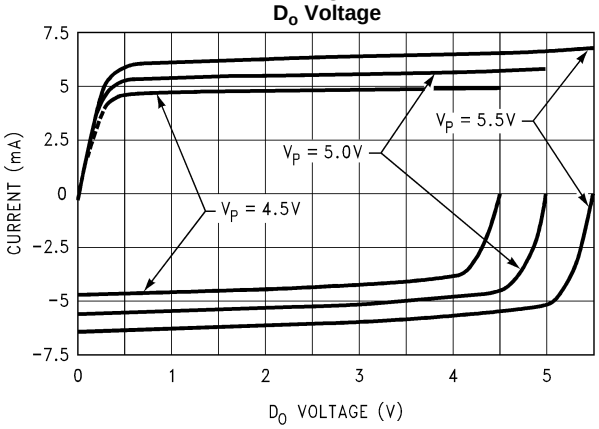


Figure 4.

Charge Pump Current vs D_o Voltage

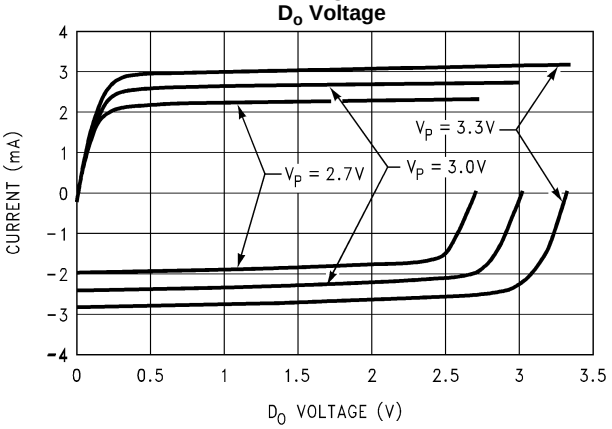


Figure 5.

Charge Pump Current Variation

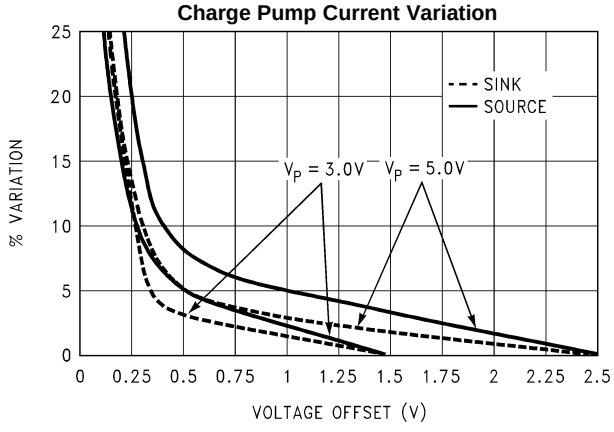


Figure 6.

Sink vs Source Mismatch vs D_o Voltage

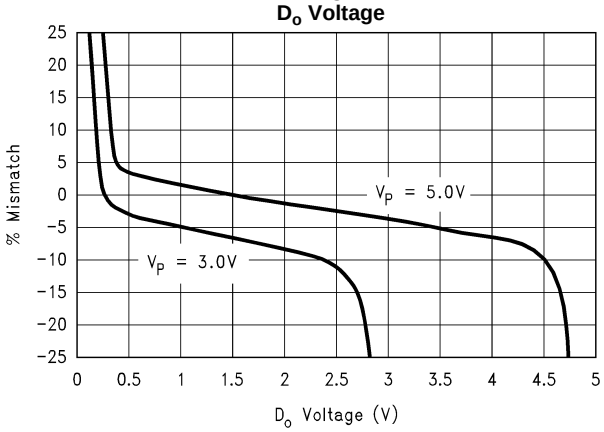


Figure 7.

Typical Performance Characteristics (continued)

I_{Do} TRI-STATE vs D_o Voltage

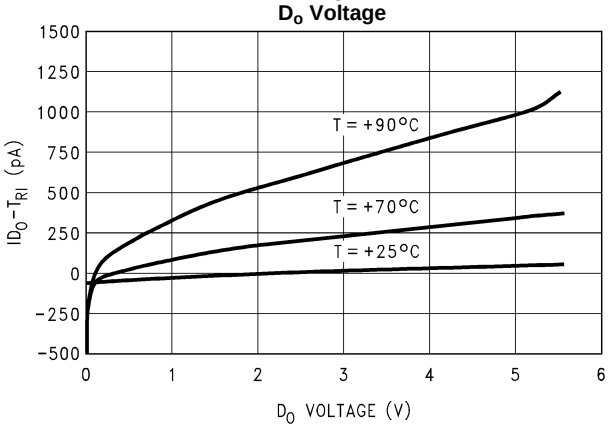


Figure 8.

Oscillator Input Sensitivity

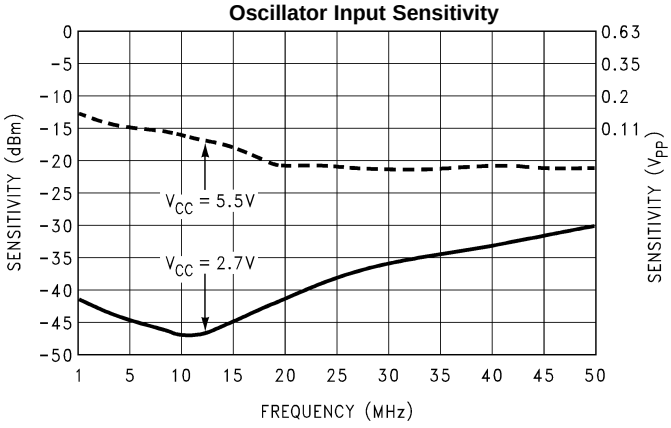


Figure 9.

LMX2320/25 Input Sensitivity vs Frequency

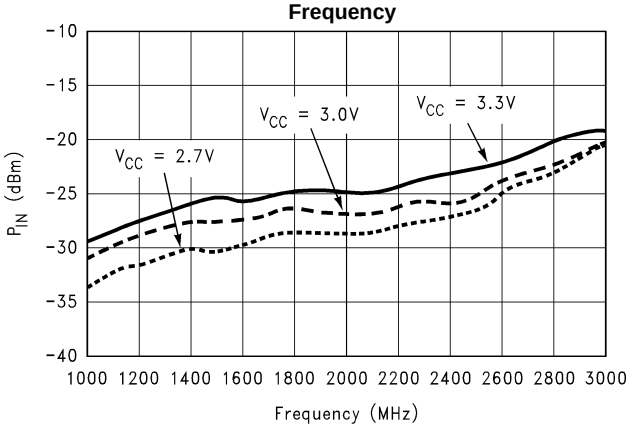


Figure 10.

LMX2320/25 Input Sensitivity vs Frequency

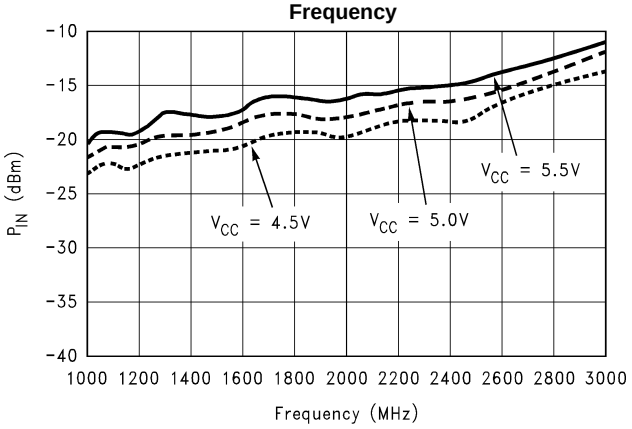


Figure 11.

LMX2315 Input Sensitivity vs Frequency

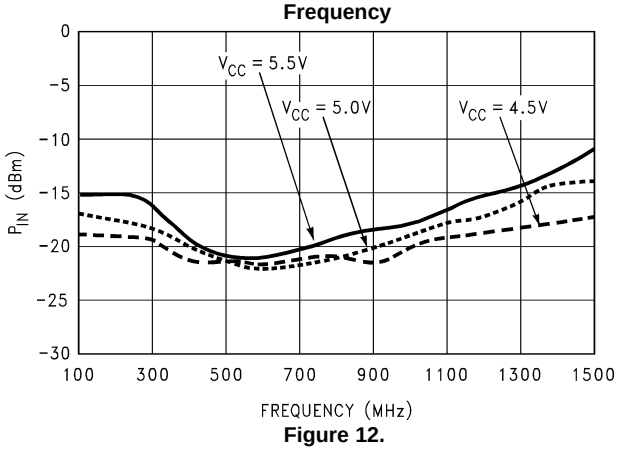


Figure 12.

LMX2315 Input Sensitivity vs Frequency

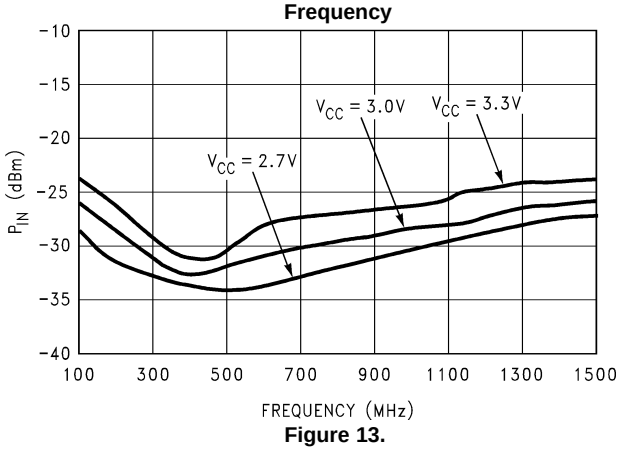


Figure 13.

Typical Performance Characteristics (continued)

LMX2320/25 Input Sensitivity at Temperature Variation, V_{CC} = 3V

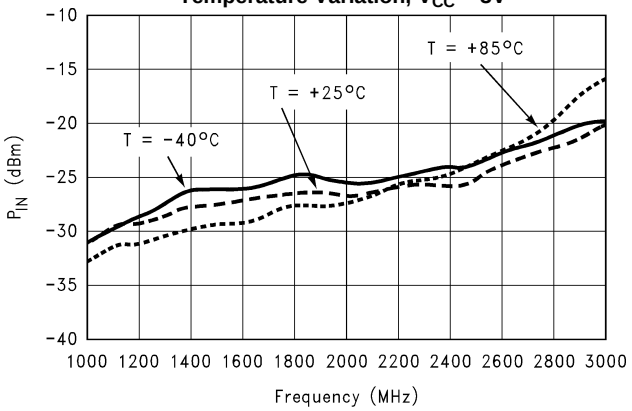


Figure 14.

LMX2320/25 Input Sensitivity at Temperature Variation, V_{CC} = 5V

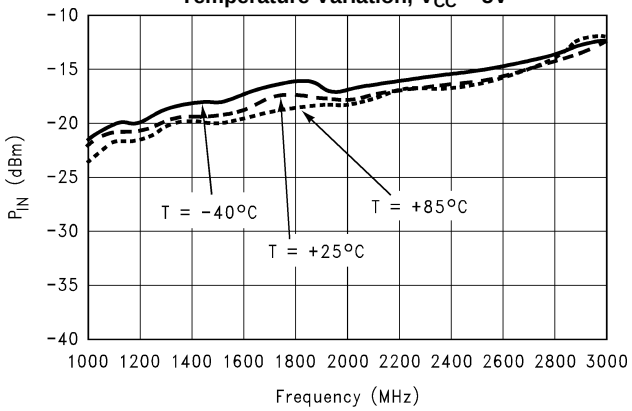


Figure 15.

LMX2315 Input Sensitivity at Temperature Variation, V_{CC} = 5V

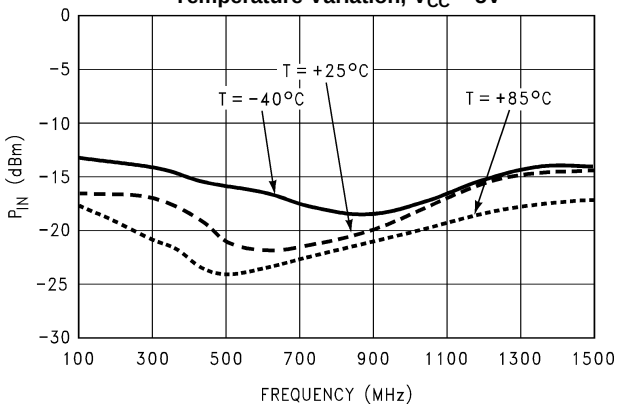


Figure 16.

LMX2315 Input Sensitivity at Temperature Variation, V_{CC} = 3V

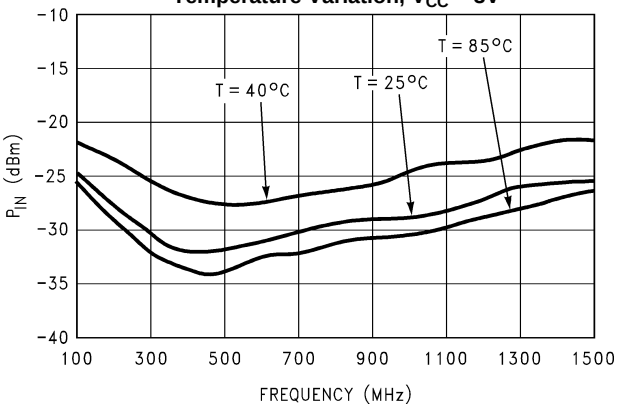
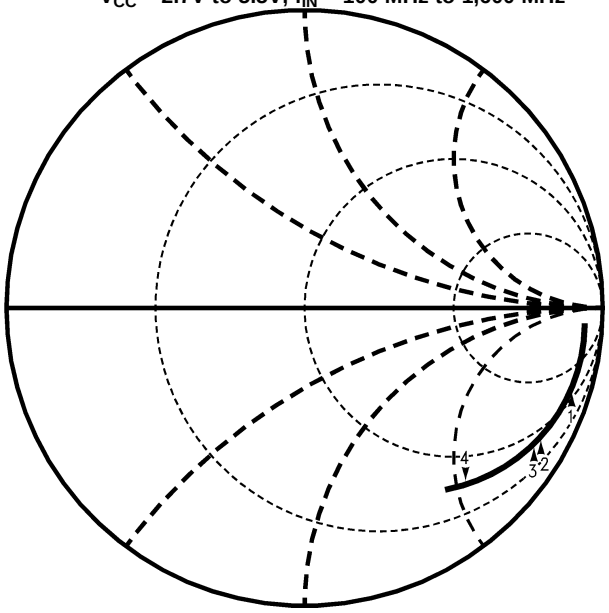


Figure 17.

Typical Performance Characteristics (continued)

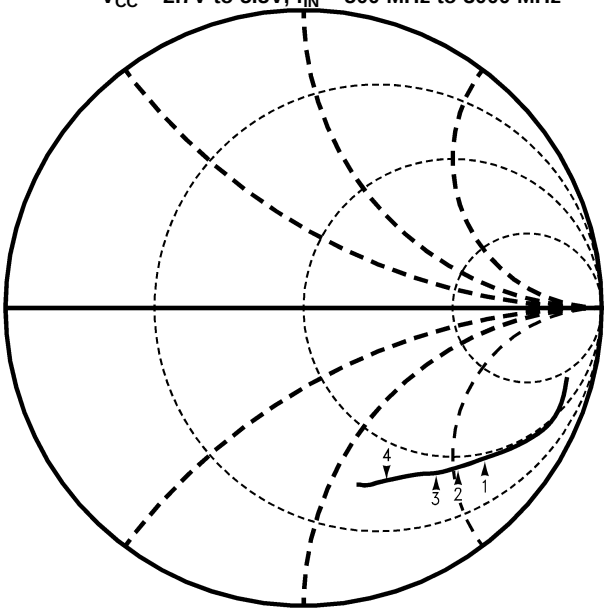
LMX2315 Input Impedance vs Frequency
V_{CC} = 2.7V to 5.5V, f_{IN} = 100 MHz to 1,600 MHz



Marker 1 = 500 MHz, Real = 69, Imag. = −330
Marker 2 = 900 MHz, Real = 36, Imag. = −193
Marker 3 = 1 GHz, Real = 35, Imag. = −172
Marker 4 = 1,500 MHz, Real = 30, Imag. = −106

Figure 18.

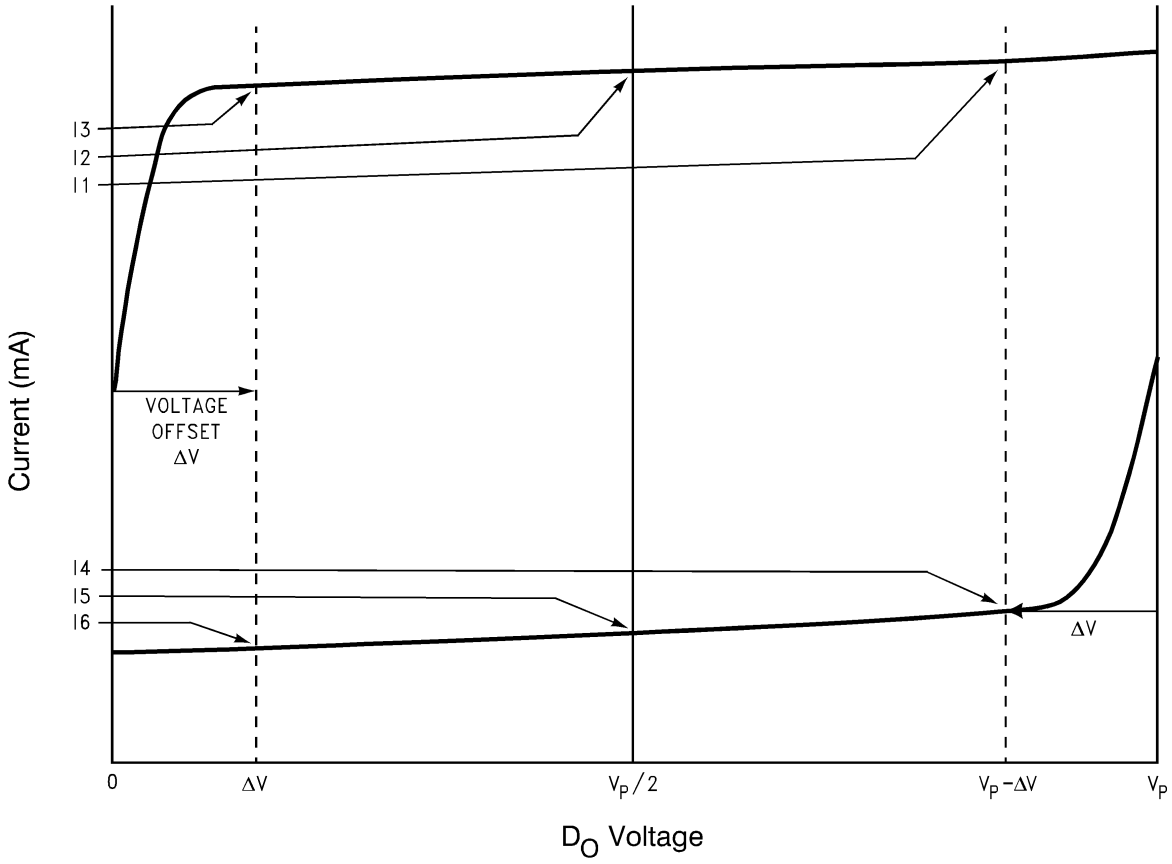
LMX2320/25 Input Impedance vs Frequency
V_{CC} = 2.7V to 5.5V, f_{IN} = 500 MHz to 3000 MHz



1 = 1.5 GHz, Real = 48, Im = −128
2 = 1.8 GHz, Real = 44, Im = −102
3 = 2.0 GHz, Real = 42, Im = −90
4 = 2.5 GHz, Real = 36, Im = −72

Figure 19.

Charge Pump Current Specification Definitions

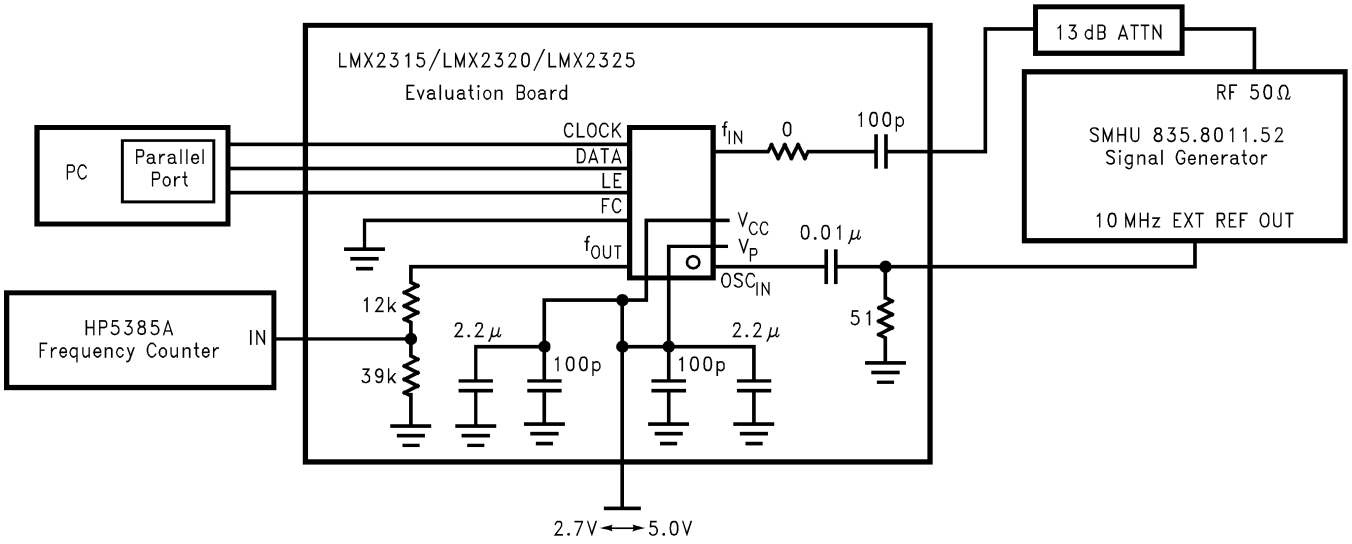


I1 = CP sink current at $V_{Do} = V_P - \Delta V$
I2 = CP sink current at $V_{Do} = V_P/2$
I3 = CP sink current at $V_{Do} = \Delta V$
I4 = CP source current at $V_{Do} = V_P - \Delta V$
I5 = CP source current at $V_{Do} = V_P/2$
I6 = CP source current at $V_{Do} = \Delta V$
ΔV = Voltage offset from positive and negative rails. Dependent on VCO tuning range relative to V_{CC} and ground. Typical values are between 0.5V and 1.0V.

1. I_{Do} vs V_{Do} = Charge Pump Output Current magnitude variation vs Voltage =
   [½ * |I1| − |I3|]/[½ * {|I1| + |I3|}] * 100% and [½ * |I4| − |I6|]/[½ * {|I4| + |I6|}] * 100%
2. $I_{Do\text{-}sink}$ vs $I_{Do\text{-}source}$ = Charge Pump Output Current Sink vs Source Mismatch =
   [|I2| − |I5|]/[½ * {|I2| + |I5|}] * 100%
3. I_{Do} vs T_A = Charge Pump Output Current magnitude variation vs Temperature =
   [|I2 @ temp| − |I2 @ 25°C|]/|I2 @ 25°C| * 100% and [|I5 @ temp| − |I5 @ 25°C|]/|I5 @ 25°C| * 100%
4. Kφ = Phase detector/charge pump gain constant =
   ½ * {|I2| + |I5|}

Figure 20.

RF Sensitivity Test Block Diagram



N = 10,000 R = 50 P = 64

Sensitivity limit is reached when the error of the divided RF output, f_{OUT}, is greater than or equal to 1 Hz.

Figure 21.

FUNCTIONAL DESCRIPTION

The simplified block diagram, Figure 22, below shows the 19-bit data register, the 14-bit R Counter and the S Latch, and the 18-bit N Counter (intermediate latches are not shown). The data stream is clocked (on the rising edge) into the DATA input, MSB first. If the Control Bit (last bit input) is HIGH, the DATA is transferred into the R Counter (programmable reference divider) and the S Latch (prescaler select: LMX2315 and LMX2320: 64/65 or 128/129; LMX2325 32/33 or 64/65). If the Control Bit (LSB) is LOW, the DATA is transferred into the N Counter (programmable divider).

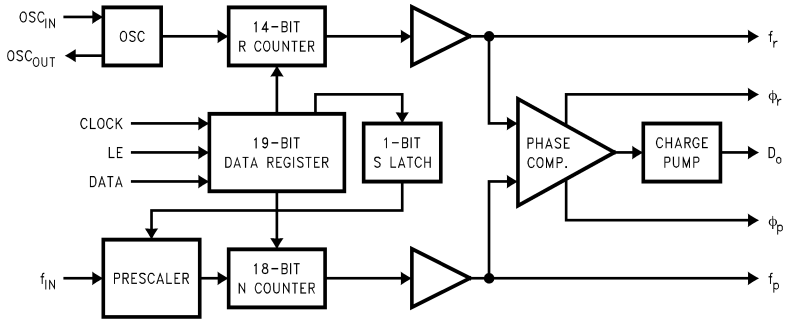
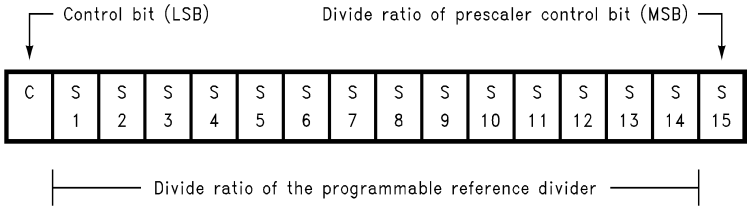


Figure 22.

PROGRAMMABLE REFERENCE DIVIDER (R COUNTER) AND PRESCALER SELECT (S LATCH)

If the Control Bit (last bit shifted into the Data Register) is HIGH, data is transferred from the 19-bit shift register into a 14-bit latch (which sets the 14-bit R Counter) and the 1-bit S Latch (S15, which sets the prescaler: 64/65 or 128/129 for the LMX2315/20 or 32/33 or 64/65 for the LMX2325). Serial data format is shown below.



14-BIT PROGRAMMABLE REFERENCE DIVIDER RATIO(1)

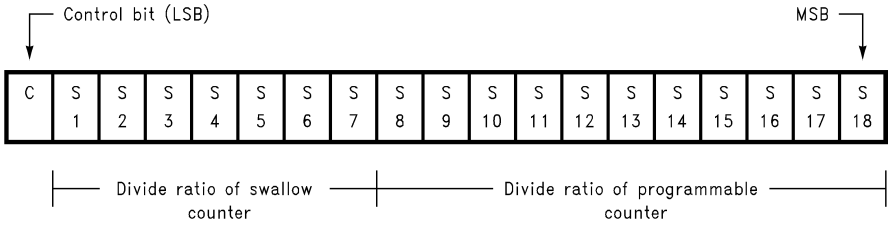
Divide Ratio R	S 14	S 13	S 12	S 11	S 10	S 9	S 8	S 7	S 6	S 5	S 4	S 3	S 2	S 1
3	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

(1) Divide ratios less than 3 are prohibited.
Divide ratio: 3 to 16383
S1 to S14: These bits select the divide ratio of the programmable reference divider.
C: Control bit (set to HIGH level to load R counter and S Latch)
Data is shifted in MSB first.

Prescaler Select		S 15
LMX2315/20	LMX2325	
128/129	64/65	0
64/65	32/33	1

PROGRAMMABLE DIVIDER (N COUNTER)

The N counter consists of the 7-bit swallow counter (A counter) and the 11-bit programmable counter (B counter). If the Control Bit (last bit shifted into the Data Register) is LOW, data is transferred from the 19-bit shift register into a 7-bit latch (which sets the 7-bit Swallow (A) Counter) and an 11-bit latch (which sets the 11-bit programmable (B) Counter). Serial data format is shown below.



Note: S8 to S18: Programmable counter divide ratio control bits (3 to 2047)

7-BIT SWALLOW COUNTER DIVIDE RATIO (A COUNTER)(1)

Divide Ratio A	S 7	S 6	S 5	S 4	S 3	S 2	S 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
127	1	1	1	1	1	1	1

(1) Divide ratio: 0 to 127
B ≥ A

11-BIT PROGRAMMABLE COUNTER DIVIDE RATIO (B COUNTER)(1)

Divide Ratio B	S 18	S 17	S 16	S 15	S 14	S 13	S 12	S 11	S 10	S 9	S 8
3	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

(1) Divide ratio: 3 to 2047 (Divide ratios less than 3 are prohibited)
B ≥ A

PULSE SWALLOW FUNCTION

$f_{VCO} = [(P \times B) + A] \times f_{OSC}/R$

f_{VCO}: Output frequency of external voltage controlled oscillator (VCO)

B: Preset divide ratio of binary 11-bit programmable counter (3 to 2047)

A: Preset divide ratio of binary 7-bit swallow counter

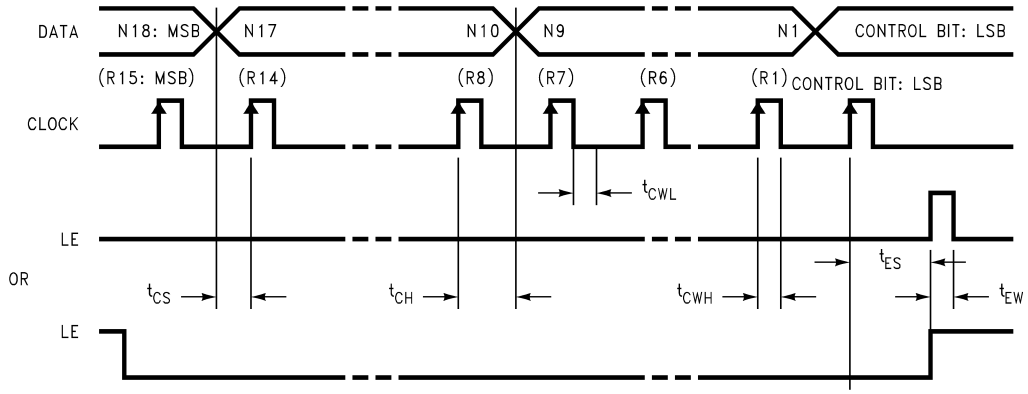
(0 ≤ A ≤ 127, A ≤ B)

f_{OSC}: Output frequency of the external reference frequency oscillator

R: Preset divide ratio of binary 14-bit programmable reference counter (3 to 16383)

P: Preset modulus of dual modulus prescaler (64 or 128 for 2315/20 or 32 or 64 for 2325)

SERIAL DATA INPUT TIMING



Notes:
Parenthesis data indicates programmable reference divider data.
Data shifted into register on clock rising edge.
Data is shifted in MSB first.
Test Conditions:
The Serial Data Input Timing is tested using a symmetrical waveform around $V_{CC}/2$. The test waveform has an edge rate of 0.6 V/ns with amplitudes of 2.2V @ V_{CC} = 2.7V and 2.6V @ V_{CC} = 5.5V.

Phase Characteristics

In normal operation, the FC pin is used to reverse the polarity of the phase detector. Both the internal and any external charge pump are affected.

Depending upon VCO characteristics, shown in Figure 23, FC pin should be set accordingly:

When VCO characteristics are like (1), FC should be set HIGH or OPEN CIRCUIT;

When VCO characteristics are like (2), FC should be set LOW.

When FC is set HIGH or OPEN CIRCUIT, the monitor pin of the phase comparator input, f_{out}, is set to the reference divider output, f_r. When FC is set LOW, f_{out} is set to the programmable divider output, f_p.

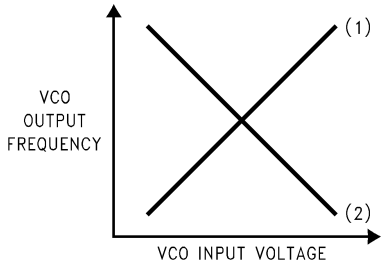
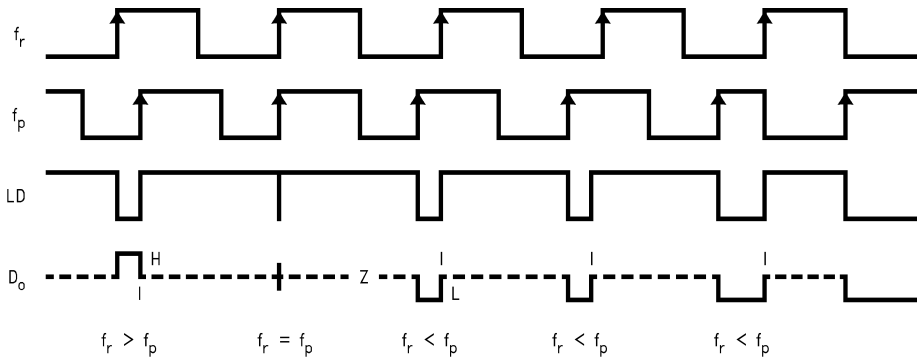


Figure 23. VCO Characteristics

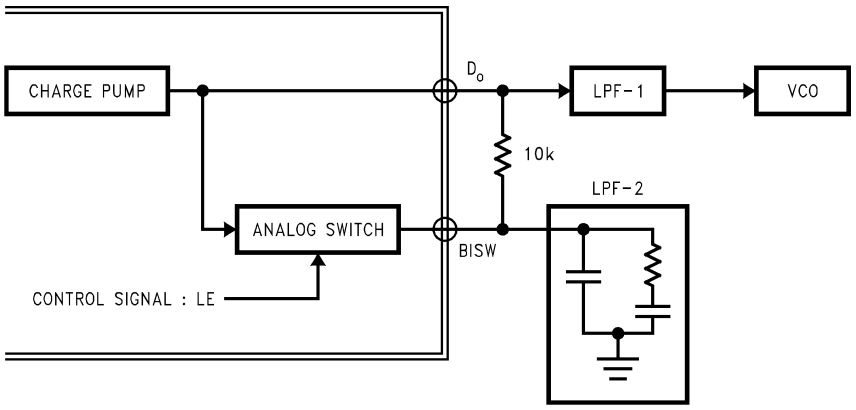


Notes:
Phase difference detection range: −2π to +2π
The minimum width pump up and pump down current pulses occur at the D_o pin when the loop is locked.
FC = HIGH

Figure 24. PHASE COMPARATOR AND INTERNAL CHARGE PUMP CHARACTERISTICS

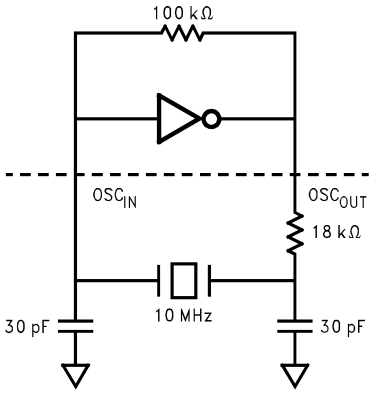
Analog Switch

The analog switch is useful for radio systems that utilize a frequency scanning mode and a narrow band mode. The purpose of the analog switch is to decrease the loop filter time constant, allowing the VCO to adjust to its new frequency in a shorter amount of time. This is achieved by adding another filter stage in parallel. The output of the charge pump is normally through the D_o pin, but when LE is set HIGH, the charge pump output also becomes available at BISW. A typical circuit is shown below. The second filter stage (LPF-2) is effective only when the switch is closed (in the scanning mode).



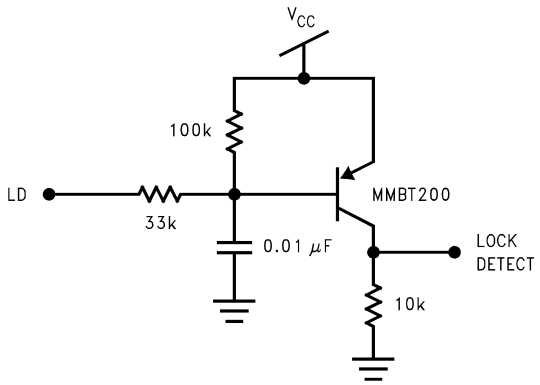
Typical Crystal Oscillator Circuit

A typical circuit which can be used to implement a crystal oscillator is shown below.

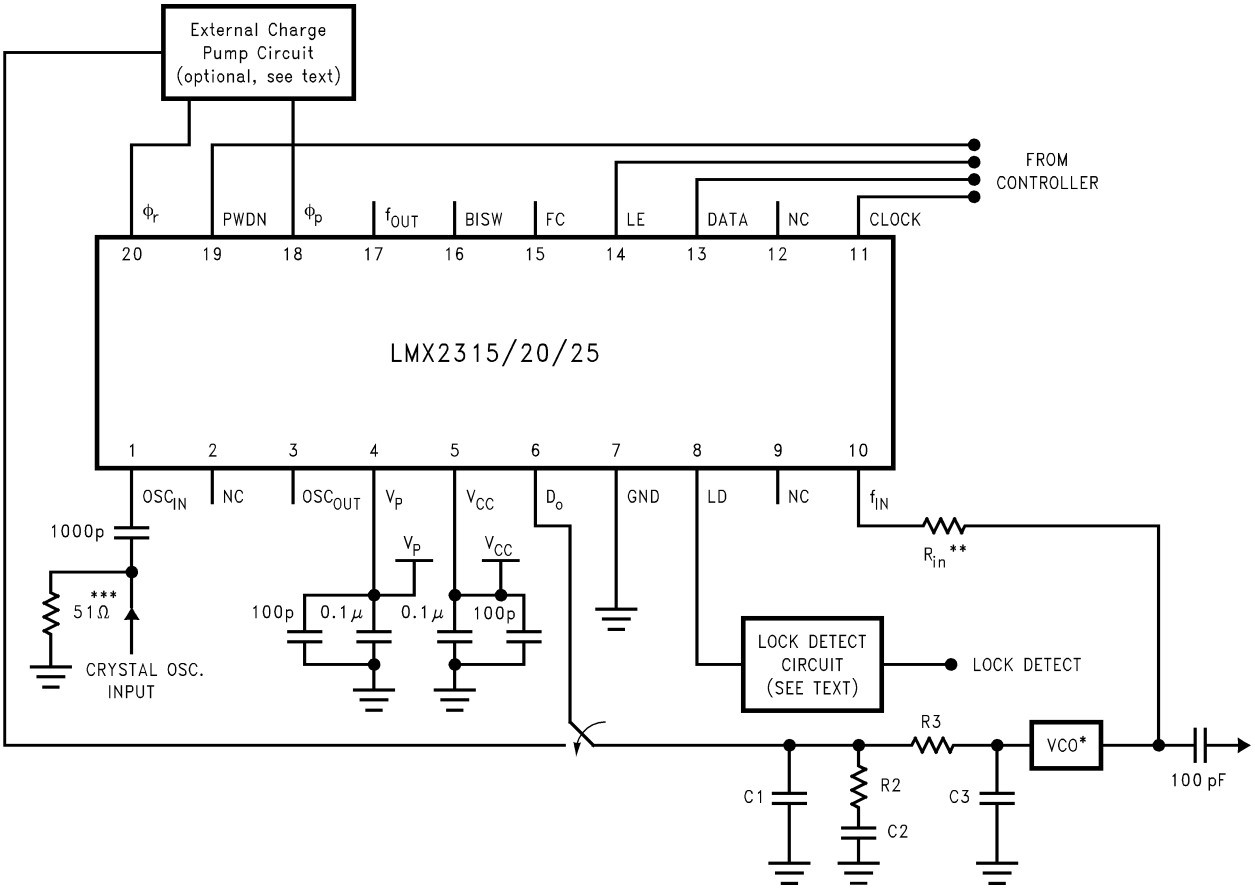


Typical Lock Detect Circuit

A lock detect circuit is needed in order to provide a steady LOW signal when the PLL is in the locked state. A typical circuit is shown below.



Typical Application Example

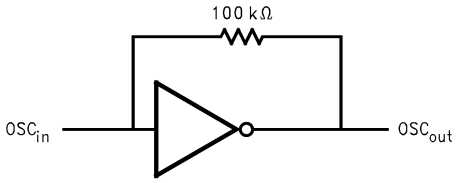


Operational Notes:

* VCO is assumed AC coupled.

** R_{IN} increases impedance so that VCO output power is provided to the load rather than the PLL. Typical values are 10Ω to 200Ω depending on the VCO power level. f_{IN} RF impedance ranges from 40Ω to 100Ω.

*** 50Ω termination is often used on test boards to allow use of external reference oscillator. For most typical products a CMOS clock is used and no terminating resistor is required. OSC_{IN} may be AC or DC coupled. AC coupling is recommended because the input circuit provides its own bias. (See *Figure* below)



Layout Hints:
Proper use of grounds and bypass capacitors is essential to achieve a high level of performance.
Crosstalk between pins can be reduced by careful board layout.
This is a static sensitive device. It should be handled only at static free work stations.

Application Information

LOOP FILTER DESIGN

A block diagram of the basic phase locked loop is shown.

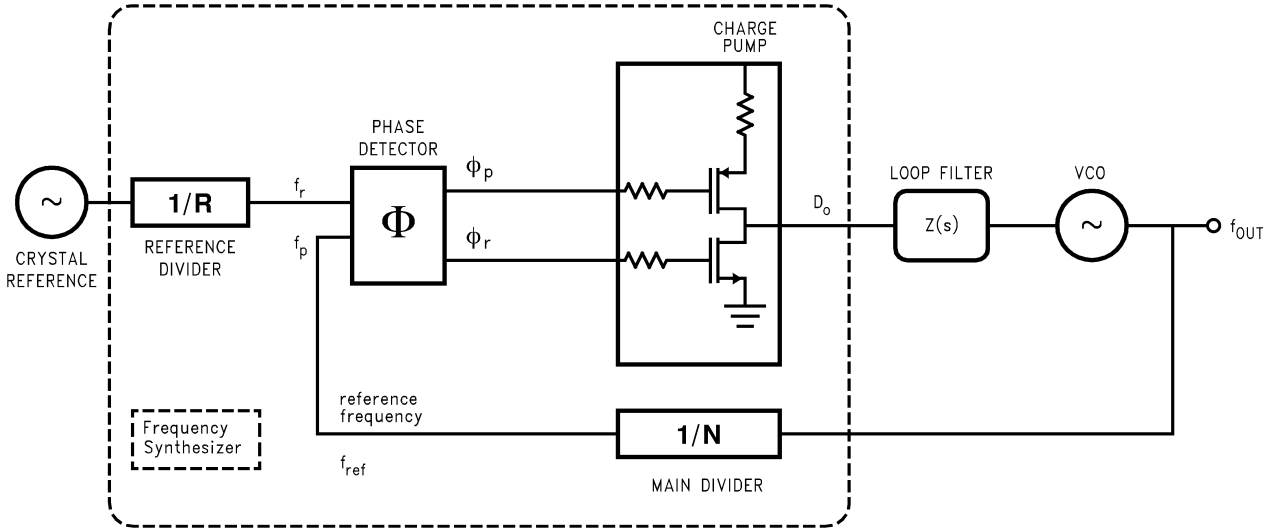


Figure 25. Basic Charge Pump Phase Locked Loop

An example of a passive loop filter configuration, including the transfer function of the loop filter, is shown in Figure 26.

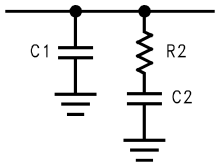


Figure 26. 2nd Order Passive Filter

$$Z(s) = \frac{s\,(C2 \bullet R2) + 1}{s^2\,(C1 \bullet C2 \bullet R2) + sC1 + sC2} \quad (1)$$

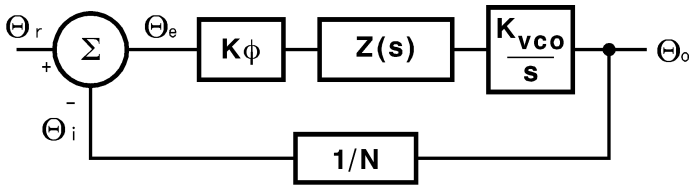
Define the time constants which determine the pole and zero frequencies of the filter transfer function by letting

$$T2 = R2 \bullet C2 \quad (2)$$

and

$$T1 = R2 \bullet \frac{C1 \bullet C2}{C1 + C2} \quad (3)$$

The PLL linear model control circuit is shown along with the open loop transfer function in Figure 27. Using the phase detector and VCO gain constants [Kφ and K_{VCO}] and the loop filter transfer function [Z(s)], the open loop Bode plot can be calculated. The loop bandwidth is shown on the Bode plot (ωp) as the point of unity gain. The phase margin is shown to be the difference between the phase at the unity gain point and −180°.



Open Loop Gain = θ_i/θ_e = H(s) G(s)

= Kφ Z(s) K_{VCO}/Ns

Closed Loop Gain = θ_o/θ_i = G(s)/[1 + H(s) G(s)]

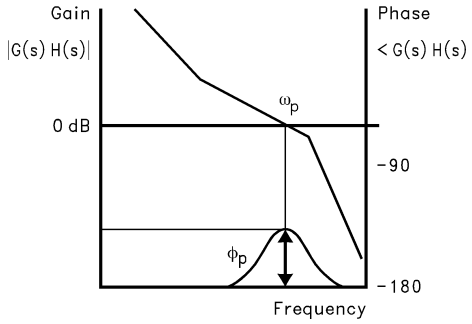


Figure 27. Open Loop Transfer Function

Thus we can calculate the 3rd order PLL Open Loop Gain in terms of frequency

$$G(s) \bullet H(s)\big|_{s = j \bullet \omega} = \frac{-K\phi \bullet K_{VCO}\,(1 + j\omega \bullet T2)}{\omega^2 C1 \bullet N(1 + j\omega \bullet T1)} \bullet \frac{T1}{T2} \tag{4}$$

From Equation 4 we can see that the phase term will be dependent on the single pole and zero such that

$$\varphi(\omega) = \tan^{-1}(\omega \bullet T2) - \tan^{-1}(\omega \bullet T1) + 180° \tag{5}$$

By setting

$$\frac{d\phi}{d\omega} = \frac{T2}{1 + (\omega \bullet T2)^2} - \frac{T1}{1 + (\omega \bullet T1)^2} = 0 \tag{6}$$

we find the frequency point corresponding to the phase inflection point in terms of the filter time constants T1 and T2. This relationship is given in Equation 7.

$$\omega_p = 1/\sqrt{T2 \bullet T1} \tag{7}$$

For the loop to be stable the unity gain point must occur before the phase reaches −180 degrees. We therefore want the phase margin to be at a maximum when the magnitude of the open loop gain equals 1.Equation 4 then gives

$$C1 = \frac{K\phi \bullet K_{VCO} \bullet T1}{\omega_p^2 \bullet N \bullet T2} \left\| \frac{(1 + j\omega_p \bullet T2)}{(1 + j\omega_p \bullet T1)} \right\| \tag{8}$$

Therefore, if we specify the loop bandwidth, ω_p, and the phase margin, φ_p, Equation 2 through Equation 8 allow us to calculate the two time constants, T1 and T2, as shown in equations 8 and 9. A common rule of thumb is to begin your design with a 45° phase margin.

$$T1 = \frac{\sec\phi_p - \tan\phi_p}{\omega_p} \tag{9}$$

$$T2 = \frac{1}{\omega_p^2 \bullet T1} \tag{10}$$

From the time constants T1, and T2, and the loop bandwidth, ω_p, the values for C1, R2, and C2 are obtained in Equation 11 to Equation 13.

$$C1 = \frac{T1}{T2} \bullet \frac{K\phi \bullet K_{VCO}}{\omega_p^2 \bullet N} \sqrt{\frac{1 + (\omega_p \bullet T2)^2}{1 + (\omega_p \bullet T1)^2}} \tag{11}$$

$$C2 = C1 \bullet \left(\frac{T2}{T1} - 1\right) \tag{12}$$

$$R2 = \frac{T2}{C2} \tag{13}$$

K_{VCO} (MHz/V) Voltage Controlled Oscillator (VCO) Tuning Voltage constant. The frequency vs voltage tuning ratio.

Kφ (mA) Phase detector/charge pump gain constant. The ratio of the current output to the input phase differential.

N Main divider ratio. Equal to RF_{opt}/f_{ref}

RF_{opt} (MHz) Radio Frequency output of the VCO at which the loop filter is optimized.

f_{ref} (kHz) Frequency of the phase detector inputs. Usually equivalent to the RF channel spacing.

In choosing the loop filter components a trade off must be made between lock time, noise, stability, and reference spurs. The greater the loop bandwidth the faster the lock time will be, but a large loop bandwidth could result in higher reference spurs. Wider loop bandwidths generally improve close in phase noise but may increase integrated phase noise depending on the reference input, VCO and division ratios used. The reference spurs can be reduced by reducing the loop bandwidth or by adding more low pass filter stages but the lock time will increase and stability will decrease as a result.

THIRD ORDER FILTER

A low pass filter section may be needed for some applications that require additional rejection of the reference sidebands, or spurs. This configuration is given in Figure 28. In order to compensate for the added low pass section, the component values are recalculated using the new open loop unity gain frequency. The degradation of phase margin caused by the added low pass is then mitigated by slightly increasing C1 and C2 while slightly decreasing R2.

The added attenuation from the low pass filter is:

$$ATTEN = 20 \log[(2\pi f_{ref} \bullet R3 \bullet C3)^2 + 1] \tag{14}$$

Defining the additional time constant as

$$T3 = R3 \bullet C3 \tag{15}$$

Then in terms of the attenuation of the reference spurs added by the low pass pole we have

$$T3 = \sqrt{\frac{10^{ATTEN/20} - 1}{(2\pi \bullet f_{ref})^2}} \tag{16}$$

We then use the calculated value for loop bandwidth ω_c in Equation 13, to determine the loop filter component values in equations 16–18. ω_c is slightly less than ω_p, therefore the frequency jump lock time will increase.

$$T2 = \frac{1}{\omega_c^2 \bullet (T1 + T3)} \tag{17}$$

$$\omega_c = \frac{\tan\phi \bullet (T1 + T3)}{[(T1 + T3)^2 + T1 \bullet T3]} \bullet \left[\sqrt{1 + \frac{(T1 + T3)^2 + T1 \bullet T3}{[\tan\phi \bullet (T1 + T3)]^2}} - 1\right] \tag{18}$$

$$C1 = \frac{T1}{T2} \bullet \frac{K\phi \bullet K_{VCO}}{\omega_c^2 \bullet N} \bullet \left[\frac{(1 + \omega_c^2 \bullet T2^2)}{(1 + \omega_c^2 \bullet T1^2)(1 + \omega_c^2 \bullet T3^2)} \right]^{1/2} \tag{19}$$

Consider the following application examples:

Example #1

K_{VCO} = 20 MHz/V

Kφ = 5 mA (*)

RF_{opt} = 900 MHz

F_{ref} = 200 kHz

$N = RF_{opt}/f_{ref}$ = 4500

$\omega_p = 2\pi * 20$ kHz = 1.256e5

φ_p = 45°

ATTEN = 20 dB

$$T1 = \frac{\sec\phi_p - \tan\phi_p}{\omega_p} = 3.29e-6$$

$$T3 = \sqrt{\frac{10^{(20/20)} - 1}{(2\pi \bullet 200e3)^2}} = 2.387e-6$$

$$\omega_c = \frac{(3.29e-6 + 2.387e-6)}{[(3.29e-6 + 2.387e-6)^2 + 3.29e-6 \bullet 2.387e-6]} \bullet \left[\sqrt{1 + \frac{(3.29e-6 + 2.387e-6)^2 + 3.29e-6 \bullet 2.387e-6}{[(3.29e-6 + 2.387e-6)]^2}} - 1 \right]$$

$$= 7.045e4$$

$$T2 = \frac{1}{(7.045e4)^2 \bullet (3.29e-6 + 2.387e-6)} = 3.549e-5$$

$$C1 = \frac{3.29e-6}{3.549e-5} \frac{(5e-3) \bullet 20e6}{(7.045e4)^2 \bullet 4500} \bullet \left[\frac{[1 + (7.045e4)^2 \bullet (3.549e-5)^2]}{[1 + (7.045e4)^2 \bullet (3.29e-6)^2][1 + (7.045e4)^2 \bullet (2.387e-6)^2]} \right]^{1/2}$$

$$= 1.085 \text{ nF}$$

$$C2 = 1.085 \text{ nF} \bullet \left(\frac{3.55e-5}{3.29e-6} - 1 \right) = 10.6 \text{ nF};$$

$$R2 = \frac{3.55e-5}{10.6e-9} = 3.35 \text{ k}\Omega;$$

$$\text{if we choose R3} = 22\text{k; then C3} = \frac{2.34e-6}{22e3} = 106 \text{ pF}. \tag{20}$$

Converting to standard component values gives the following filter values, which are shown in Figure 28.

C1 = 1000 pF

R2 = 3.3 kΩ

C2 = 10 nF

R3 = 22 kΩ

C3 = 100 pF

NOTE

See related equation for Kφ in Charge Pump Current Specification Definitions. For this example V_P = 5.0V. The value of Kφ can then be approximated using Figure 4 and Figure 5 in the Typical Performance Characteristics. The units for Kφ are in mA. You may also use Kφ = (5 mA/2π rad), but in this case you must convert K_{VCO} to (rad/V) multiplying by 2π.

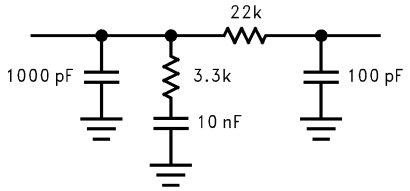


Figure 28. ~20 kHz Loop Filter

MEASUREMENT RESULTS (Example #1)

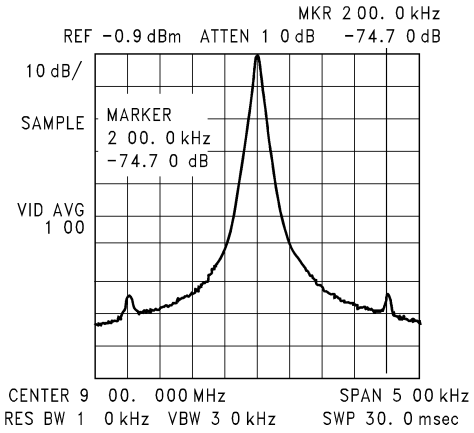


Figure 29. PLL Reference Spurs

The reference spurious level is < −74 dBc, due to the loop filter attenuation and the low spurious noise level of the LMX2315.

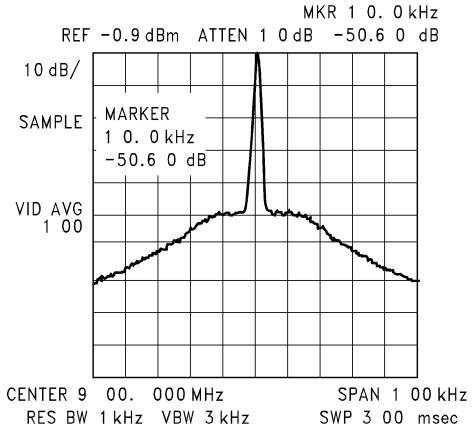


Figure 30. PLL Phase Noise 10 kHz Offset

The phase noise level at 10 kHz offset is −80 dBc/Hz.

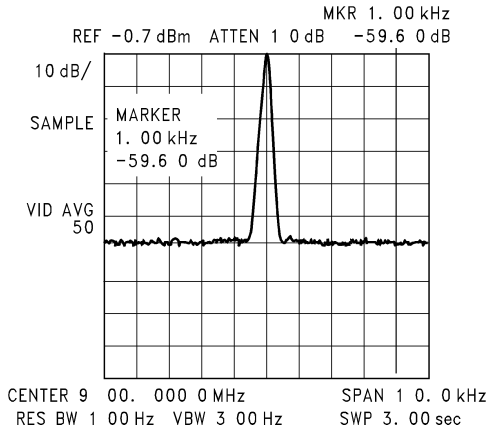


Figure 31. PLL Phase Noise @ 1 kHz Offset

The phase noise level at 1 kHz offset is −79.5 dBc/Hz.

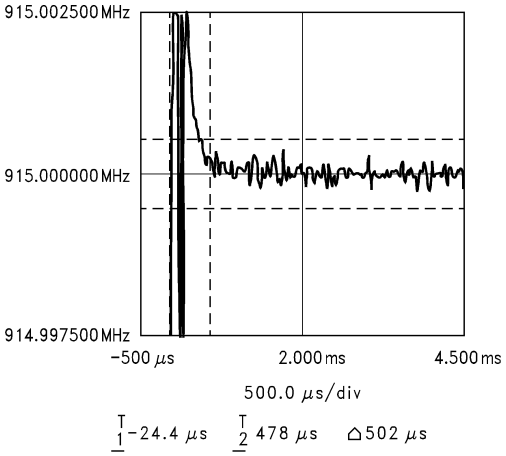


Figure 32. Frequency Jump Lock Time

Of concern in any PLL loop filter design is the time it takes to lock in to a new frequency when switching channels. Figure 32 shows the switching waveforms for a frequency jump of 865 MHz to 915 MHz. By narrowing the frequency span of the HP53310A Modulation Domain Analyzer enables evaluation of the frequency lock time to within ±500 Hz. The lock time is seen to be less than 500 µs for a frequency jump of 50 MHz.

Example #2

K_{VCO} = 34 MHz/V

Kφ = 2.8 mA (*)

RF_{opt} = 1665 MHz

F_{ref} = 300 kHz

$N = RF_{opt}/f_{ref}$ = 5550

$\omega_p = 2\pi * 20$ kHz = 1.256e5

φ_p = 43

ATTEN = 12 dB

$$T1 = \frac{\sec\phi - \tan\phi}{\omega_p} = 3.462e-6$$

$$T3 = \sqrt{\frac{10^{(12/20)} - 1}{(2\pi \bullet 300e3)^2}} = 9.16e-7$$

$$\omega_c = \frac{\tan 43\ (3.862e-6 + 9.16e-7)}{(3.462e-6 + 9.16e-7)^2 + 3.462e-6 \bullet 9.16e-7)} \bullet \left[\sqrt{1 + \frac{(3.462e-6 + 9.16e-7)^2 + 3.462e-6 \bullet 9.16e-7}{[\tan 43\ (3.462e-6 + 9.16e-7)]^2}} - 1\right]$$

$$T2 = \frac{1}{(9.682e4)^2\ (3.462e-6 + 9.1(} T3 = \sqrt{\frac{10^{ATTEN/20} - 1}{(2\pi \bullet f_{ref})^2}}$$

$$C1 = \frac{3.462e-6}{2.437e-5} \frac{(2.8e-3) \bullet 34e6}{(9.682e4)^2 \bullet 5550} \bullet \left[\frac{[1 + (9.682e4)^2 \bullet (2.437e-5)^2]}{[1 + (9.682e4)^2\ (3.462e-6)^2]\ [1 + (9.682e4)^2 \bullet (9.16e-7)^2]}\right]^{1/2}$$

$$= 0.63\ nF$$

$$C2 = 0.63\ nF \left(\frac{2.437e-5}{3.402e-6} - 1\right) = 3.88\ nF;$$

$$R2 = \frac{2.437e-5}{3.88e-9} = 6.28\ k\Omega;$$

$$\text{if we choose R3} = 27k; \text{ then C3} = \frac{9.16e-7}{27e3} = 34\ pF. \tag{21}$$

Converting to standard component values gives the following filter values, which are shown in Figure 28.

C1 = 560 pF

R2 = 6.8 kΩ

C2 = 2700 pF

R3 = 27 kΩ

C3 = 56 pF

NOTE

*See related equation for Kφ in Charge Pump Current Specification Definitions. For this example V_P = 3.3V. The value for Kφ can then be approximated using Figure 4 and Figure 5 in the Typical Performance Characteristics. The units for Kφ are in mA. You may also use Kφ = (2.8 mA/2π rad), but in this case you must convert K_{VCO} to (rad/V) multiplying by 2π.

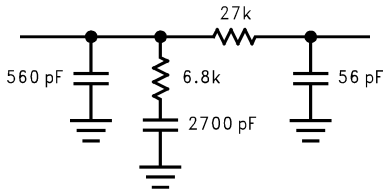


Figure 33. ~20 kHz Loop Filter

MEASUREMENT RESULTS

(Example #2)

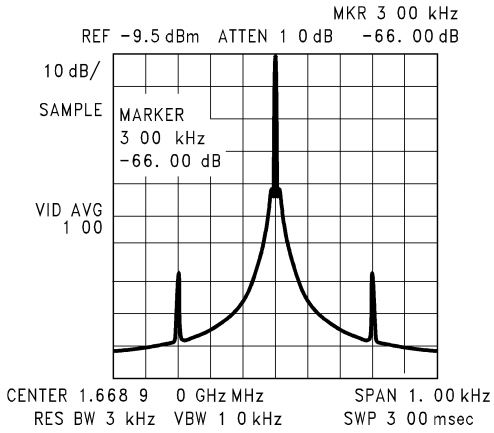


Figure 34. PLL Reference Spurs

The reference spurious level is < −65 dBc, due to the loop filter attenuation and the low spurious noise level of the LMX2320.

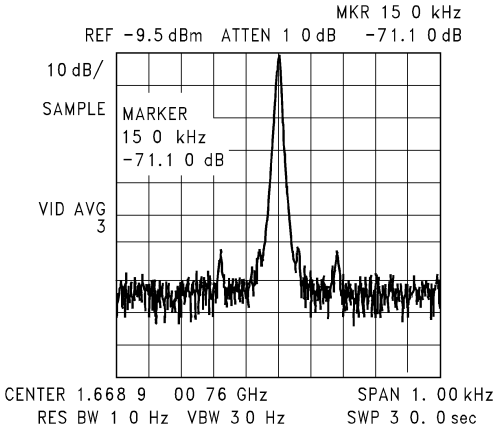


Figure 35. PLL Phase Noise @ 150 Hz Offset

The phase noise level at 150 Hz offset is −81.1 dBc/Hz. The spurs at 60 and 180 Hz offset are due to 60 Hz line noise from the power supply.

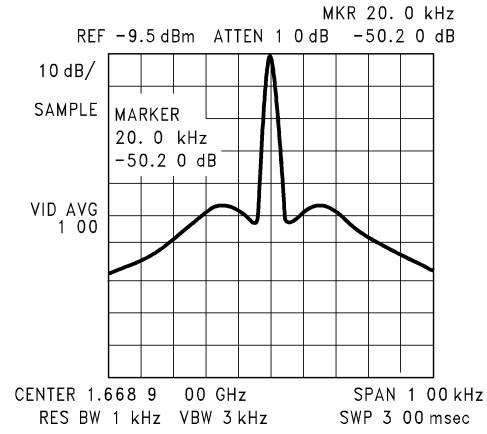


Figure 36. PLL Phase Noise 20 kHz Offset

The phase noise level at 20 kHz offset is −80 dBc/Hz.

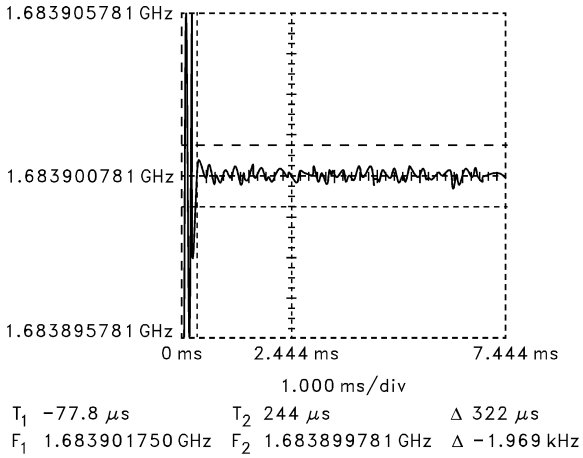


Figure 37. Frequency Jump Lock Time

Of concern in any PLL loop filter design is the time it takes to lock in to a new frequency when switching channels. Figure 37 shows the switching waveforms for a frequency jump of 1650.9 MHz to 1683.9 MHz. By narrowing the frequency span of the HP53310A Modulation Domain Analyzer enables evaluation of the frequency lock time to within ±1 kHz. The lock time is seen to be less than 500 µs for a frequency jump of 33 MHz.

EXTERNAL CHARGE PUMP

The LMX PLLatinum series of frequency synthesizers are equipped with an internal balanced charge pump as well as outputs for driving an external charge pump. Although the superior performance of NSC's on board charge pump eliminates the need for an external charge pump in most applications, certain system requirements are more stringent. In these cases, using an external charge pump allows the designer to take direct control of such parameters as charge pump voltage swing, current magnitude, TRI-STATE leakage, and temperature compensation.

One possible architecture for an external charge pump current source is shown in Figure 38. The signals φ_p and φ_r in the diagram, correspond to the phase detector outputs of the 2315/20/25 frequency synthesizers. These logic signals are converted into current pulses, using the circuitry shown in Figure 38, to enable either charging or discharging of the loop filter components to control the output frequency of the PLL.

Referring to Figure 38, the design goal is to generate a 5 mA current which is relatively constant to within 5V of the power supply rail. To accomplish this, it is important to establish as large of a voltage drop across R5, R8 as possible without saturating Q2, Q4. A voltage of approximately 300 mV provides a good compromise. This allows the current source reference being generated to be relatively repeatable in the absence of good Q1, Q2/Q3, Q4 matching. (Matched transistor pairs is recommended.) The φp and φr outputs are rated for a maximum output load current of 1 mA while 5 mA current sources are desired. The voltages developed across R4, 9 will consequently be approximately 258 mV, or 42 mV less than R8, 5, due to the current density differences {0.026*1n (5 mA/1 mA)} through the Q1, Q2/Q3, Q4 pairs.

In order to calculate the value of R7 it is necessary to first estimate the forward base to emitter voltage drop (Vfn,p) of the transistors used, the V_{OL} drop of φp, and the V_{OH} drop of φr's under 1 mA loads. (φp's V_{OL} < 0.1V and (φr,s V_{OH} < 0.1V).

Knowing these parameters along with the desired current allow us to design a simple external charge pump. Separating the pump up and pump down circuits facilitates the nodal analysis and give the following equations.

$$R_4 = \frac{V_{R5} - V_T \bullet 1n\left(\frac{i_{source}}{i_{p\,max}}\right)}{i_{source}}$$

$$R_9 = \frac{V_{R8} - V_T \bullet 1n\left(\frac{i_{sink}}{i_{n\,max}}\right)}{i_{sink}}$$

$$R_5 = \frac{V_{R5} \bullet (\beta_p + 1)}{i_{p\,max} \bullet (\beta_p + 1) - i_{source}}$$

$$R_8 = \frac{V_{R8} \bullet (\beta_n + 1)}{i_{r\,max} \bullet (\beta_n + 1)\, i_{sink}}$$

$$R_6 = \frac{(V_p - V_{VOL\phi p}) - (V_{R5} + Vfp)}{i_{p\,max}}$$

$$R_7 = \frac{(V_P - V_{VOH\phi p}) - (V_{R8} + Vfn)}{i_{max}} \quad (22)$$

EXAMPLE

Typical Device Parameters β_n =100, β_p = 50

Typical System Parameters V_P = 5.0V;

V_{cntl} = 0.5V–4.5V;
$V_{\varphi p}$ = 0.0V, $V_{\varphi r}$ = 5.0V

Design Parameters $I_{SINK} = I_{SOURCE}$ = 5.0 mA;
Vfn = Vfp = 0.8V
$I_{rmax} = I_{pmax}$ = 1 mA
$V_{R8} = V_{R5}$ = 0.3V
$V_{OL\varphi p} = V_{OH\varphi p}$ = 100 mV

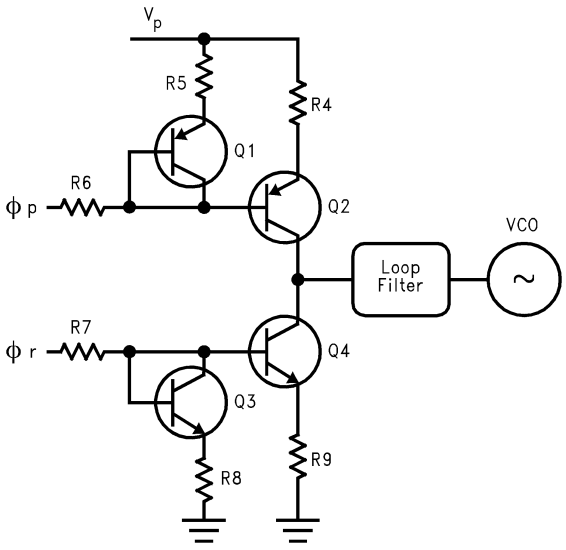


Figure 38.

Therefore select

$$R_4 = R_9 = \frac{0.3V - 0.026 \bullet 1n(5.0\ mA/1.0\ mA)}{5\ mA} = 51.6\Omega$$

$$R_5 = \frac{0.3V \bullet (50 + 1)}{1.0\ mA \bullet (50 + 1) - 5.0\ mA} = 332\Omega$$

$$R_8 = \frac{0.3V \bullet (100 + 1)}{1.0\ mA \bullet (100 + 1) - 5.0\ mA} = 315.6\Omega$$

$$R_6 = R_7 = \frac{(5V - 0.1V) - (0.3V + 0.8V)}{1.0\ mA} = 3.8\ k\Omega \quad (23)$$

REVISION HISTORY

Changes from Revision D (March 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	27

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