LMX2346/LMX2347 PLLatinum™ Frequency Synthesizer for RF Personal Communications

LMX2346 2.0 GHz

LMX2347 2.5 GHz

Check for Samples: LMX2346, LMX2347

FEATURES

- **RF Operation up to 2.5 GHz**
- **2.7V to 5.5V Operation**
- **Digital & Analog Lock Detect**
- **32/33 Dual Modulus Prescaler**
- **Excellent Phase Noise**
- **Internal Balanced, Low Leakage Charge Pump**
- **Pin Compatible to LMX2323**

APPLICATIONS

- **Cellular DCS/PCS/3G Infrastructure Equipment**
- **Wireless Local Area Networks (WLANs)**
- **Other Wireless Communication Systems**

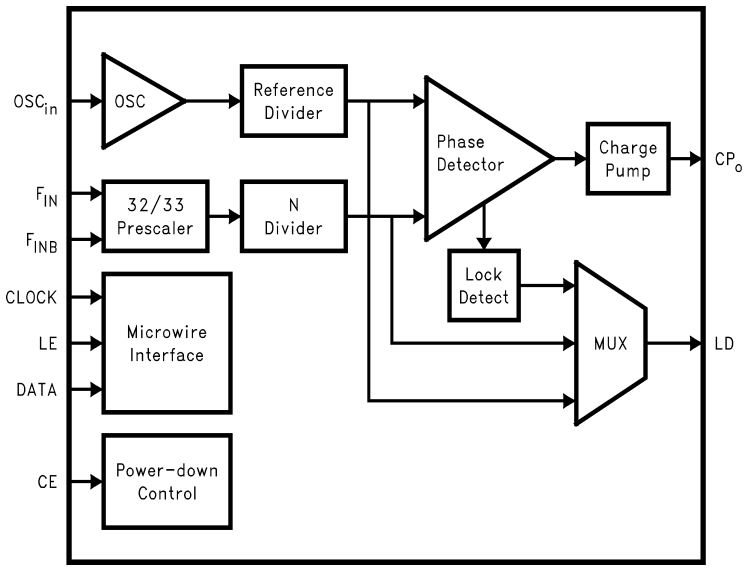
DESCRIPTION

The LMX2346/7 are high performance frequency synthesizers with an integrated 32/33 dual modulus prescaler. The LMX2346 is designed for RF operation up to 2.0 GHz. The LMX2347 is designed for RF operation up to 2.5 GHz. Using a proprietary digital phase locked loop technique, the LMX2346/7 generates very stable, low noise control signals for UHF and VHF voltage controlled oscillators.

Serial data is transferred into the LMX2346/7 via a three-line MICROWIRE interface (DATA, LE, CLOCK). Supply voltage range is from 2.7V to 5.5V. The charge pump provides 4 mA output current.

The LMX2346/7 are manufactured using TI's 0.5µ ABiC V silicon BiCMOS process and is available in 16-pin TSSOP and 16-pin LGA packages.

Functional Block Diagram



Connection Diagrams

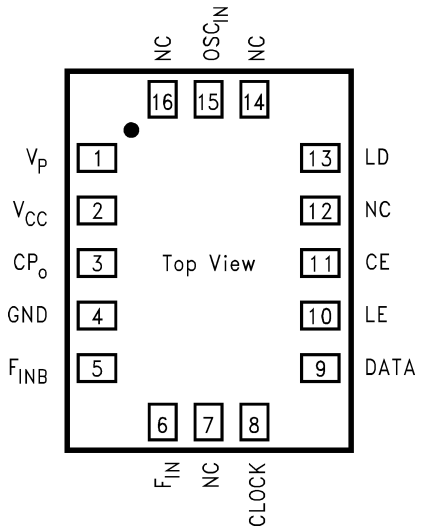


Figure 1. 16-Pin LGA
See Package Number NPG0016A

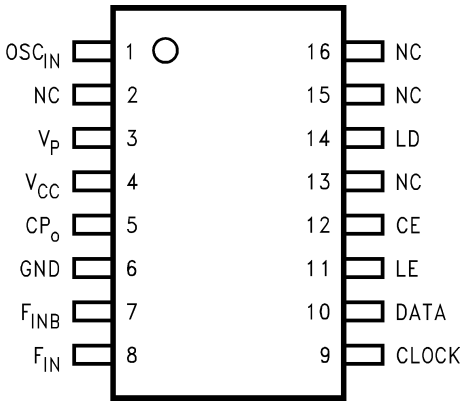
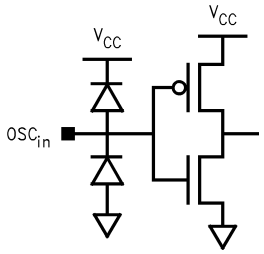
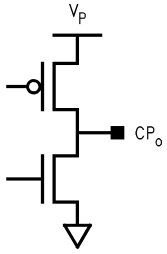
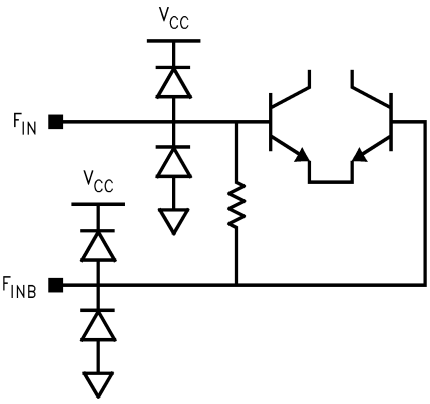
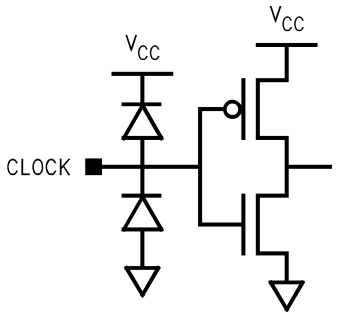
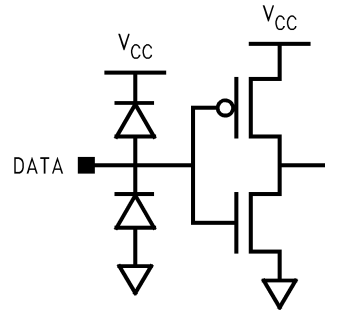


Figure 2. 16-Pin TSSOP Package
See Package Number PW0016A

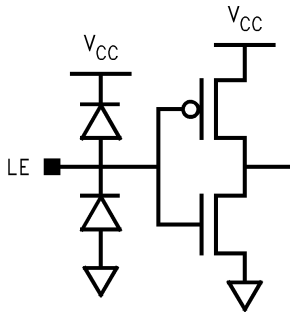
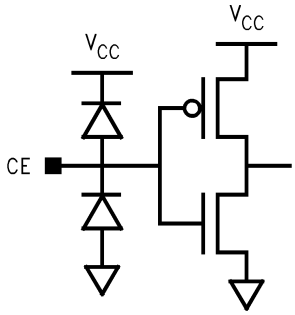
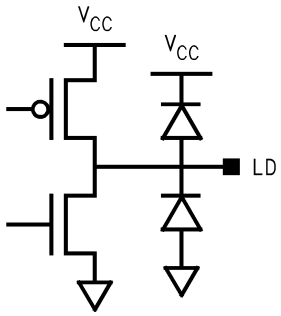
PIN DESCRIPTIONS

Pin Name	Pin Number		I/O	Description	I/O Circuit Configuration
	16-Pin LGA	16-Pin TSSOP			
OSC_{IN}	15	1	I	Reference oscillator input. A CMOS inverting gate input. The input has a $V_{CC}/2$ input threshold and can be driven from an external CMOS or TTL logic gate.	
V_P	1	3	—	Charge Pump Power Supply. Must be ≥ V_{CC}.	
V_{CC}	2	4	—	Main Power Supply. V_{CC} may range from 2.7V to 5.5V. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.	
CP_o	3	5	O	Charge Pump output. For connection to a loop filter for driving the voltage control input of an external VCO.	

PIN DESCRIPTIONS (continued)

Pin Name	Pin Number		I/O	Description	I/O Circuit Configuration
	16-Pin LGA	16-Pin TSSOP			
GND	4	6	—	Ground.	
F_{INB}	5	7	I	RF prescaler complementary input. For single ended operation, this pin should be AC grounded. The LMX2346/7 can be driven differentially when a bypass capacitor is omitted.	
F_{IN}	6	8	I	RF PLL prescaler input. Small signal input from the VCO.	
CLOCK	8	9	I	High impedance CMOS Clock input. Data is clocked in on the rising edge, into the 18-bit shift register.	
DATA	9	10	I	Binary serial data input. Data entered MSB first. LSB is control bit. High impedance CMOS input.	

PIN DESCRIPTIONS (continued)

Pin Name	Pin Number		I/O	Description	I/O Circuit Configuration
	16-Pin LGA	16-Pin TSSOP			
LE	10	11	I	Latch Enable input. When Latch Enable transitions HIGH, data stored in the 18-bit shift register is loaded into one of the 2 control registers, based on the address bit. High impendance CMOS input.	
CE	11	12	I	Chip Enable input. Provides logical power-down control of the device. Pull-up to V_{CC} if unused. High impedance CMOS input.	
LD	13	14	O	Locked Detect output. Multi-function CMOS output pin that provides multiplexed access to digital lock detect, open-drain analog lock detect, as well as the outputs of the R and N counters.	
NC	7, 12, 14, 16	2, 13, 15, 16		No Connect.	

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)(3)

Power Supply Voltage, (V_{CC})	−0.3V to +6.5V
Power Supply for Charge Pump, (V_P)	−0.3V to +6.5V
Voltage on any pin with GND=0V, except V_P (V_i)	−0.3V to V_{CC} +0.3V
Storage Temperature Range, (T_S)	−65°C to +150°C
Lead Temp. (solder 4 sec.), (T_L)	+260°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Recommended Operating Conditions indicate conditions for which the device is intended to be functional. For ensured specifications and test conditions see the Electrical Characteristics.
(2) This device is a high performance RF integrated circuit with an ESD rating <2 kV. Handling and assembly of this device should only be done at ESD protected workstations.
(3) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.

Recommended OperatingConditions(1)

	Min	Max	Unit
Power Supply Voltage, (V_{CC})	2.7	5.5	V
Power Supply for Charge Pump, (V_P)	V_{CC}	6.0	V
Operating Temperature, (T_A)	−40	+85	°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Recommended Operating Conditions indicate conditions for which the device is intended to be functional. For ensured specifications and test conditions see the Electrical Characteristics.

Electrical Characteristics

The following conditions apply; V_{CC} = 3.0V, V_P = 3.0V; −40°C ≤ T_A ≤ 85°C, unless specified differently.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{CC}						
I_{CC}	Power Supply Current, LMX2346			3.5	4.5	mA
		V_{CC} = 5.5V			7.0	mA
	Power Supply Current, LMX2347			4.5	5.5	mA
		V_{CC} = 5.5V			8.0	mA
I_{CC}-pwdn	Power Down Current	CLOCK, DATA, LE = GND CE = GND		1	10	µA
RF PRESCALER						
F_{IN}	Operating Frequency, RF Prescaler, LMX2346		0.2		2.0	GHz
	Operating Frequency, RF Prescaler, LMX2347		0.2		2.5	GHz
PF_{IN}	Input Sensitivity, RF Prescaler	2.7V ≤ V_{CC} ≤ 3.0V (1)	−15		+0	dBm
		3.0V < V_{CC} ≤ 5.5V (1)	−10		+0	dBm
PHASE DETECTOR						
F_φ	Phase Detector Frequency				10	MHz
REFERENCE OSCILLATOR						
F_{OSC}	Operating Frequency, Reference Oscillator Input	See (2)	5		104	MHz
V_{OSC}	Input Sensitivity, Reference Oscillator Input	See (3)	0.4		V_{CC} − 0.3	V_{PP}
I_{IH}	OSC_{in} High-Level Input Current	V_{IH} = V_{CC} = 5.5V			100	µA
I_{IL}	OSC_{in} Low-Level Input Current	V_{IL} = 0V, V_{CC} = 5.5V	−100			µA
CHARGE PUMP						
$ICPo_{-source}$	Charge Pump Source Current	VCPo = Vp/2V		−4.0		mA
$ICPo_{-sink}$	Charge Pump Sink Current	VCPo = Vp/2V		4.0		mA
$ICPo_{-tri}$	Charge Pump TRI-STATE Current	0.5V ≤ VCPo ≤ V_P − 0.5V	−2.5		2.5	nA
$ICPo_{-sink}$ vs. $ICPo_{-source}$	CP Sink vs. Source Mismatch	VCPo = Vp/2 T_A = 25° (4)		3	10	%
ICPo vs VCPo	CP Current vs. Voltage	0.5V ≤ VCPo ≤ V_P − 0.5V T_A = 25° (4)		10	15	%
ICPo vs T_A	CP Current vs. Temperature	VCPo = Vp/2V (4)		10		%
LOGICAL INTERFACE (CE, CLOCK, LE, DATA, LD)						
V_{IH}	High-level Input Voltage		0.8 V_{CC}			V
V_{IL}	Low-level Input Voltage				0.2 V_{CC}	V
I_{IH}	High-level Input Current	V_{IH} = V_{CC} = 5.5V	−1.0		1.0	µA
I_{IL}	Low-level Input Current	V_{IL} = 0V, V_{CC} = 5.5V	−1.0		1.0	µA
V_{OH}	High-level Output Voltage	I_{OH} = −500 µA	V_{CC} − 0.4			V
V_{OL}	Low-level Output Voltage	I_{OL} = 500 µA			0.4	V
MICROWIRE INTERFACE (CLOCK, LE, DATA)						
t_{CS}	Data to Clock Set Up Time	See (5)	50			ns
t_{CH}	Data to Clock Hold Time	See (5)	10			ns
t_{CWH}	Clock Pulse Width High	See (5)	50			ns
t_{CWL}	Clock Pulse Width Low	See (5)	50			ns
t_{ES}	Clock to Latch Enable Set Up Time	See (5)	50			ns

(1) See F_{IN} Sensitivity Test Setup.
(2) For F_{OSC} frequencies below 10 MHz, it is recommended that the rise time of the signal does not exceed 25ns.
(3) See OSC_{in} Sensitivity Test Setup.
(4) See Charge Pump Measurement Definitions for detail on how these measurements are made.
(5) See Serial Input Data Timing.

Electrical Characteristics (continued)

The following conditions apply; V_{CC} = 3.0V, V_P = 3.0V; −40°C ≤ T_A ≤ 85°C, unless specified differently.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{EW}	Latch Enable Pulse Width	See (5)	50			ns
PHASE NOISE						
L(f)	Single Side-Band Phase Noise	F_{IN} = 900 MHz F_φ = 200 kHz F_{OSC} = 10 MHz V_{OSC} = 1.0 V_{PP} T_A = 25°C (6)		−91		dBc/Hz
		F_{IN} = 1750 MHz F_φ = 200 kHz F_{OSC} = 10 MHz V_{OSC} = 1.0 V_{PP} T_A = 25°C (6) (7)		−86		dBc/Hz
		F_{IN} = 1960 MHz F_φ = 200 kHz F_{OSC} = 10 MHz V_{OSC} = 1.0 V_{PP} T_A = 25°C (6)		−85		dBc/Hz
		F_{IN} = 2450 MHz F_φ = 200 kHz F_{OSC} = 10 MHz V_{OSC} = 1.0 V_{PP} T_A = 25°C (6)		−83		dBc/Hz
L_N(f)	Normalized Single Side-Band Phase Noise	F_φ = 200 kHz F_{OSC} = 10 MHz V_{OSC} = 1.0 V_{PP} T_A = 25°C (8)		−164.5		dBc/Hz

(6) Phase Noise is measured using a reference evaluation board with a loop bandwidth of approximately 12 kHz. The phase noise specification is the composite average of 3 measurements made at frequency offsets of 2.0, 2.5 and 3.0 kHz.
(7) This parameter is derived from Normalized Single Side-Phase Noise, L_n(f).
(8) Normalized Single-Side Band Phase Noise is defined as: $L_N(f) = L(f) - 20 \log (F_{IN}/ F_\varphi)$, where L(f) is defined as the Single Side-Band Phase Noise.

Typical Performance Characteristics

I_{CC} vs V_{CC} LMX2346/7

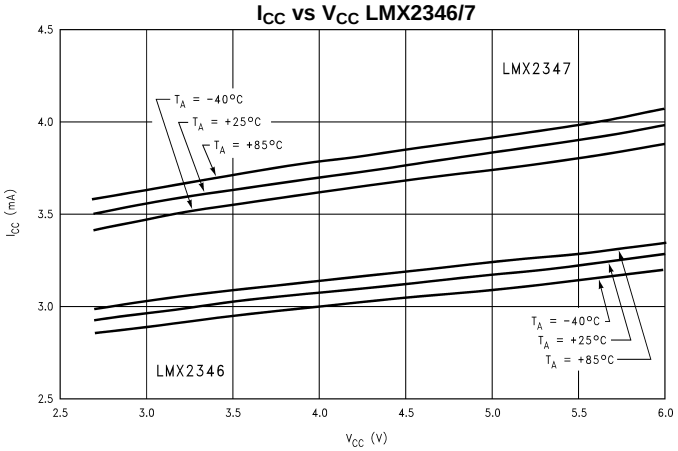


Figure 3.

CP_O Tri-State vs CP_O Voltage at 85°C

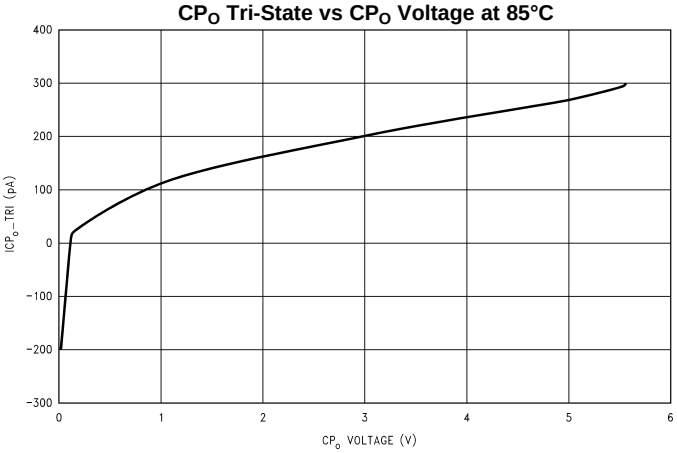


Figure 4.

LMX2346/7 Charge Pump Sweeps

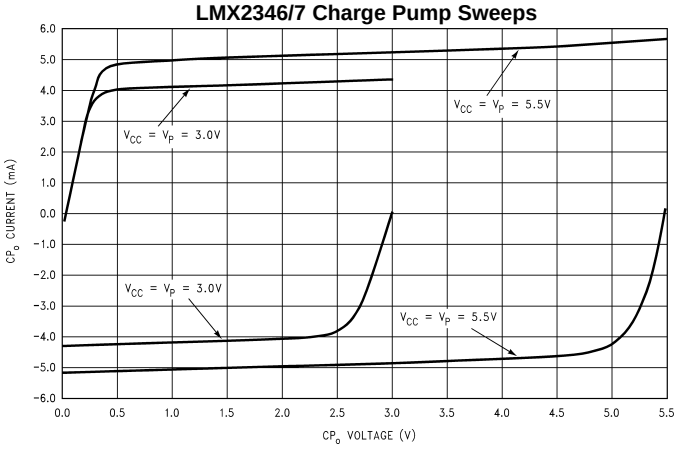


Figure 5.

Sink vs Source Mismatch (See formula under Charge Pump Current Specifications Definitions)

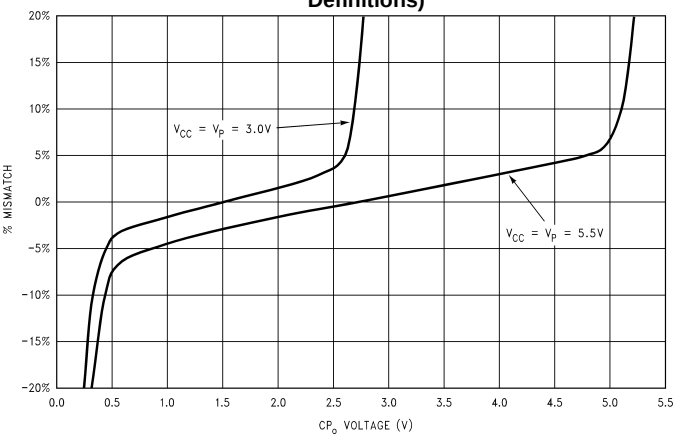


Figure 6.

Charge Pump Current Variation (See formula under Charge Pump Current Specifications Definitions)

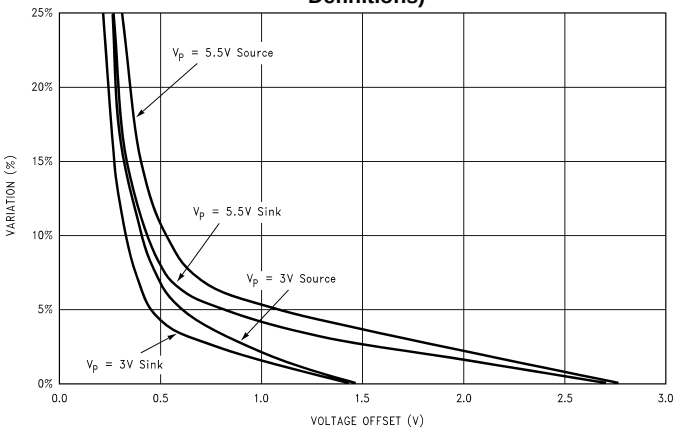


Figure 7.

LMX2346 F_{IN} Sensitivity vs Frequency at 3.0V

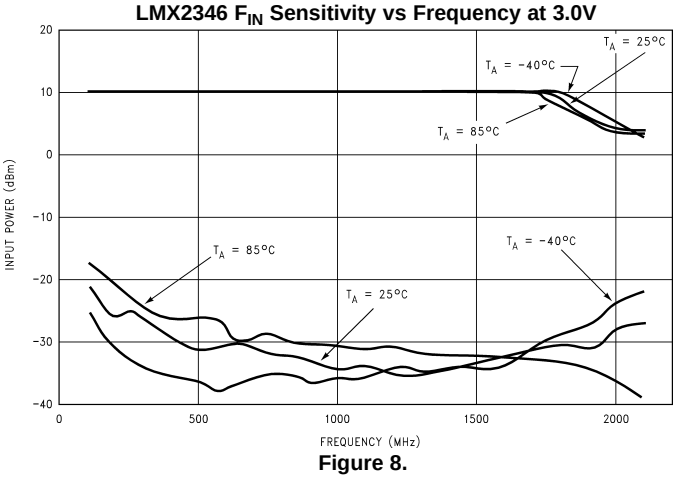


Figure 8.

Typical Performance Characteristics (continued)

LMX2346 F_{IN} Sensitivity vs Frequency at 5.5V

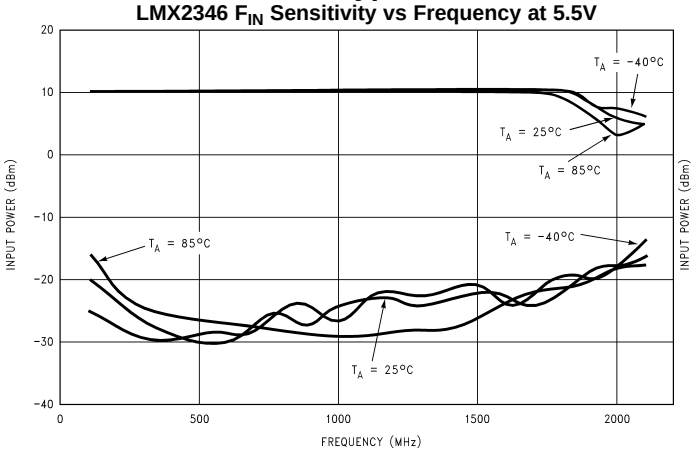


Figure 9.

LMX2347 F_{IN} Sensitivity vs Frequency at 3.0V

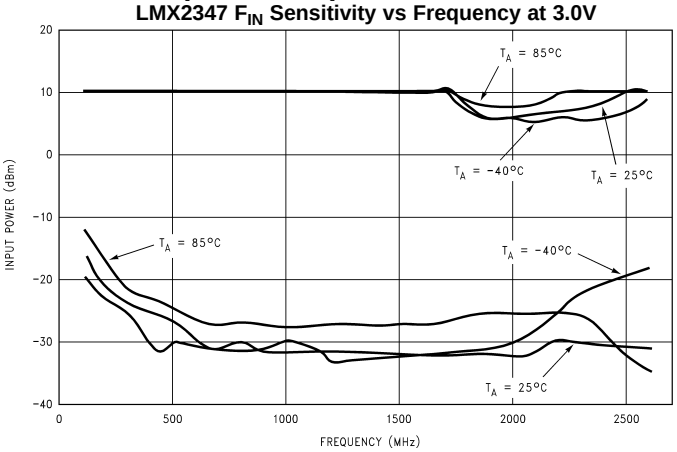


Figure 10.

LMX2347 F_{IN} Sensitivity vs Frequency at 5.5V

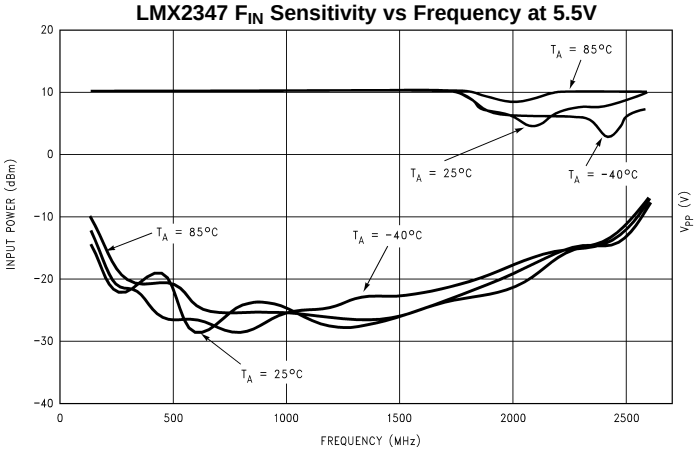


Figure 11.

LMX2346/7 OSC_{IN} Sensitivity vs Frequency at 3.0V

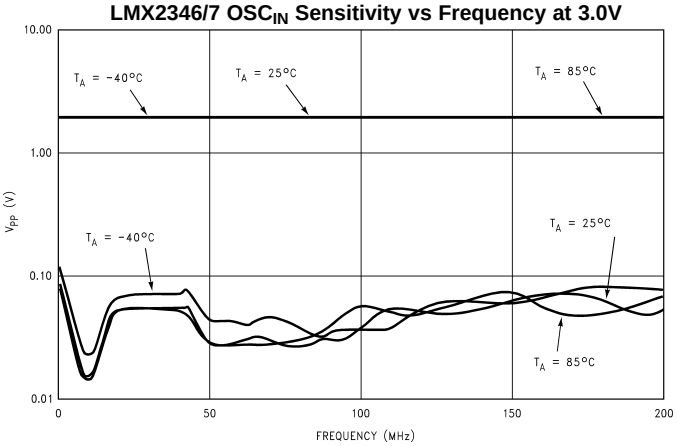


Figure 12.

LMX2346/7 OSC_{IN} Sensitivity vs Frequency at 5.5V

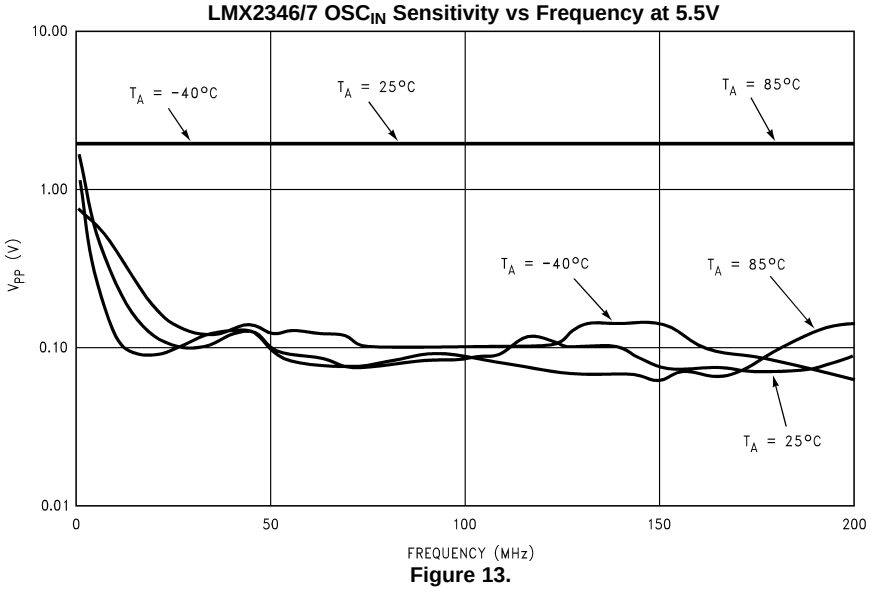
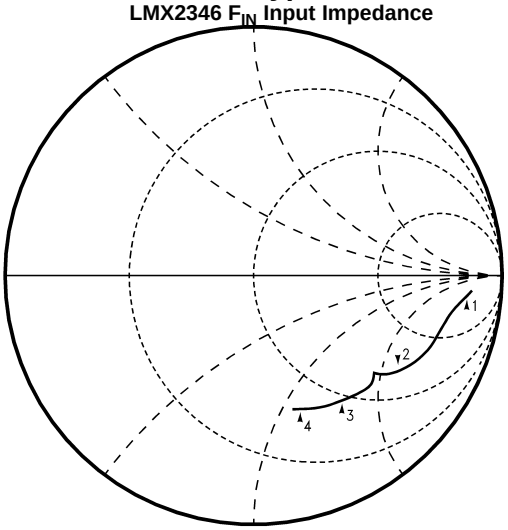


Figure 13.

Typical Performance Characteristics (continued)

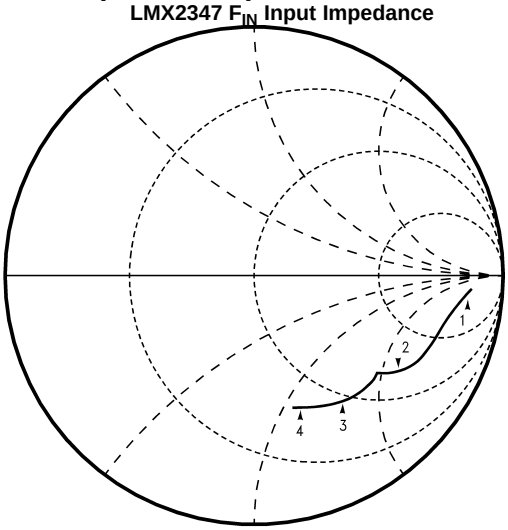
LMX2346 F_{IN} Input Impedance



Marker 1 = 200 MHz
Marker 2 = 1.2 GHz
Marker 3 = 2 GHz
Marker 4 = 2.5 GHz

Figure 14.

LMX2347 F_{IN} Input Impedance



Marker 1 = 200 MHz
Marker 2 = 1.2 GHz
Marker 3 = 2 GHz
Marker 4 = 2.5 GHz

Figure 15.

Table 1. LMX2346/7SLB F_{IN} IMPEDANCE

	LMX2346/7SLB F_{IN} IMPEDANCE											
	V_{CC} = 3.0V (T_A = 25°C)						V_{CC} = 5.5V (T_A = 25°C)					
	F_{IN} POWERED-UP			F_{IN} POWERED-DOWN			F_{IN} POWERED-UP			F_{IN} POWERED-DOWN		
F_{IN} (MHz)	Real ZF_{IN} (Ω)	Imaginary ZF_{IN} (Ω)	$\|ZF_{IN}\|$ (Ω)	Real ZF_{IN} (Ω)	Imaginary ZF_{IN} (Ω)	$\|ZF_{IN}\|$ (Ω)	Real ZF_{IN} (Ω)	Imaginary ZF_{IN} (Ω)	$\|ZF_{IN}\|$ (Ω)	Real ZF_{IN} (Ω)	Imaginary ZF_{IN} (Ω)	$\|ZF_{IN}\|$ (Ω)
100	500	−270	568	490	−292	570	510	−270	577	492	−291	572
200	376	−256	455	365	−257	446	374	−253	452	377	−257	456
300	297	−246	386	297	−245	385	302	−245	389	300	−245	387
400	244	−234	338	245	−234	339	250	−234	342	249	−234	342
500	203	−217	297	198	−215	292	208	−218	301	207	−217	300
600	168	−198	260	168	−198	260	173	−199	264	173	−199	264
700	145	−180	231	145	−180	231	150	−182	236	148	−182	235
800	128	−163	207	129	−163	208	133	−166	213	131	−164	210
900	114	−153	191	113	−153	190	117	−154	193	116	−153	192
1000	100	−139	171	99	−140	171	103	−141	175	101	−140	173
1100	88	−125	153	88	−125	153	93	−128	158	90	−125	154
1200	80	−113	138	80	−113	138	83	−115	142	82	−114	140
1300	75	−100	125	75	−100	125	78	−102	128	76	−101	126
1400	76	−85	114	73	−84	111	79	−87	118	75	−88	116
1500	87	−83	120	85	−78	115	88	−85	122	84	−79	115
1600	80	−94	123	82	−93	124	82	−96	126	84	−92	125
1700	66	−91	112	66	−91	112	67	−92	114	69	−92	115
1800	57	−85	102	57	−84	102	59	−86	104	60	−86	105
1900	51	−79	94	51	−78	93	53	−80	96	53	−79	95
2000	46	−73	86	46	−71	85	48	−73	87	47	−73	87
2100	42	−67	79	42	−66	78	43	−68	80	43	−68	80
2200	39	−62	73	39	−62	73	41	−64	76	40	−63	75
2300	37	−58	69	37	−57	68	39	−60	72	38	−58	69
2400	35	−56	66	35	−55	65	37	−57	68	36	−56	67
2500	32	−55	64	31	−54	62	33	−57	66	32	−55	64

LMX2346/7SLB OSC_{IN} Input Impedance vs Frequency (R_OPT= 0 or set to 5 - 50 MHz)

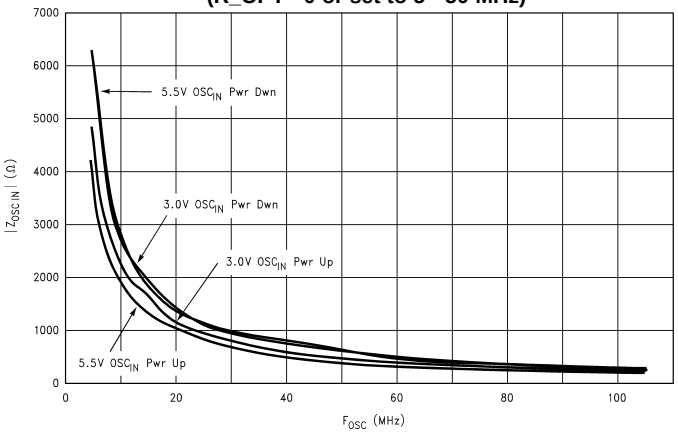


Figure 16.

LMX2346/7SLB OSC_{IN} Input Impedance vs Frequency (R_OPT= 7or set to 55 - 104MHz)

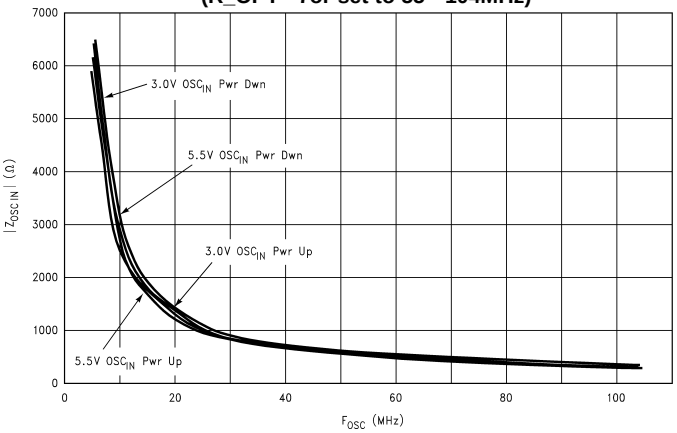


Figure 17.

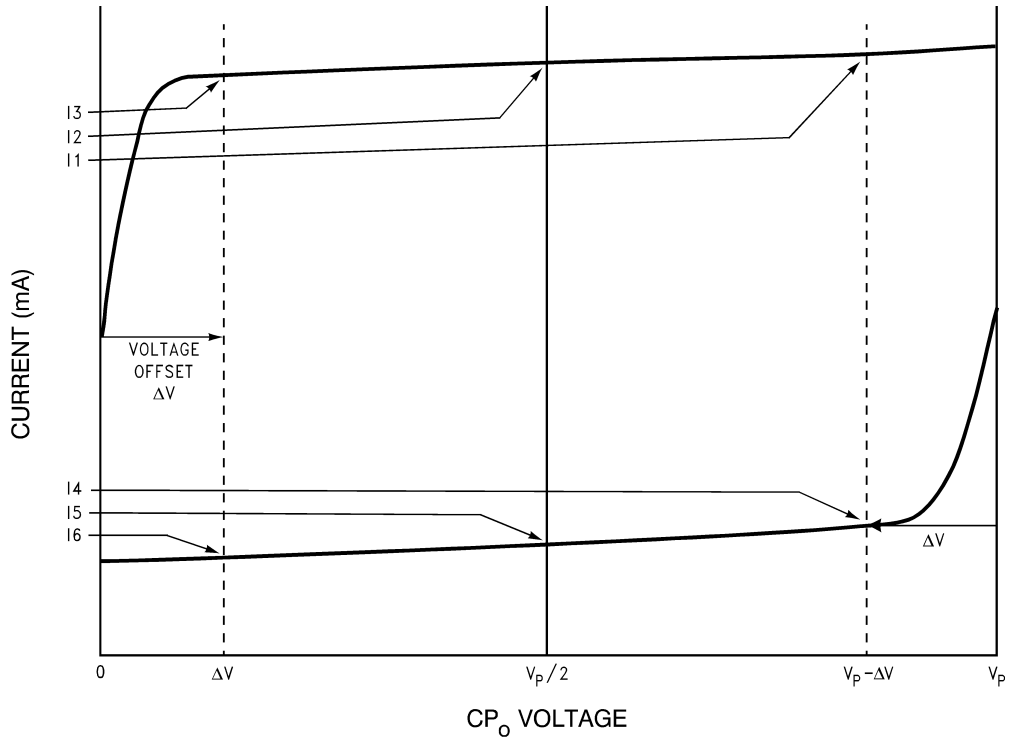
Table 2. LMX2346/7SLB OSC_{IN} IMPEDANCE (R_OPT set to 5 MHz–50 MHz)

	LMX2346/7SLB OSC_{IN} IMPEDANCE (R_OPT set to 5 MHz–50 MHz)											
	V_{CC} = 3.0V (T_A = 25°C)						V_{CC} = 5.5V (T_A = 25°C)					
	OSC_{IN} BUFFER NORMAL OPERATION			OSC_{IN} BUFFER POWERED-DOWN MODE			OSC_{IN} BUFFER NORMAL OPERATION			OSC_{IN} BUFFER POWERED-DOWN MODE		
F_{OSC} (MHz)	Real $ZOSC_{IN}$ (Ω)	Imag-inary $ZOSC_{IN}$ (Ω)	$\|ZOSC_{IN}\|$ (Ω)	Real $ZOSC_{IN}$ (Ω)	Imag-inary $ZOSC_{IN}$ (Ω)	$\|ZOSC_{IN}\|$ (Ω)	Real $ZOSC_{IN}$ (Ω)	Imag-inary $ZOSC_{IN}$ (Ω)	$\|ZOSC_{IN}\|$ (Ω)	Real $ZOSC_{IN}$ (Ω)	Imag-inary $ZOSC_{IN}$ (Ω)	$\|ZOSC_{IN}\|$ (Ω)
5	1100	−4800	4920	200	−6100	6100	1250	−4100	4290	100	−6200	6200
10	340	−2200	2230	80	−3000	3000	310	−1950	1970	130	−2750	2750
15	170	−1600	1610	60	−1900	1900	170	−1360	1370	50	−1970	1970
20	120	−1120	1130	35	−1400	1400	105	−1050	1060	32	−1380	1380
25	85	−953	957	28	−1150	1150	78	−840	844	28	−1130	1130
30	75	−800	804	33	−958	959	66	−704	707	28	−945	945
35	68	−692	695	30	−835	836	58	−610	613	28	−818	818
40	64	−612	615	28	−738	739	52	−538	541	28	−722	723
45	58	−530	533	27	−638	639	48	−478	480	22	−630	630
50	57	−492	495	24	−580	580	43	−422	424	21	−570	570
55	53	−447	450	23	−537	537	40	−386	388	20	−520	520
60	52	−410	413	22	−485	485	38	−354	356	18	−478	478
65	49	−373	376	22	−447	448	37	−327	329	19	−442	442
70	48	−347	350	21	−417	418	36	−303	305	18	−410	410
75	46	−326	329	20	−391	392	35	−285	287	16	−385	385
80	45	−305	308	19	−365	365	33	−266	268	16	−360	360
85	44	−289	292	18	−342	342	32	−250	252	15	−336	336
90	44	−274	278	19	−326	327	32	−236	238	16	−318	318
95	42	−260	263	18	−309	310	31	−224	226	15	−304	304
100	41	−244	247	18	−290	291	30	−212	214	15	−285	285
104	41	−234	238	17	−277	278	30	−203	205	14	−272	272

Table 3. LMX2346/7SLB OSC_{IN} IMPEDANCE (R_OPT set to 50 MHz–104 MHz)

	LMX2346/7SLB OSC_{IN} IMPEDANCE (R_OPT set to 50 MHz–104 MHz)											
	V_{CC} = 3.0V (T_A = 25°C)						V_{CC} = 5.5V (T_A = 25°C)					
	OSC_{IN} BUFFER NORMAL OPERATION			OSC_{IN} BUFFER POWERED-DOWN MODE			OSC_{IN} BUFFER NORMAL OPERATION			OSC_{IN} BUFFER POWERED-DOWN MODE		
F_{OSC} (MHz)	Real $ZOSC_{IN}$ (Ω)	Imag-inary $ZOSC_{IN}$ (Ω)	$\|ZOSC_{IN}\|$ (Ω)	Real $ZOSC_{IN}$ (Ω)	Imag-inary $ZOSC_{IN}$ (Ω)	$\|ZOSC_{IN}\|$ (Ω)	Real $ZOSC_{IN}$ (Ω)	Imag-inary $ZOSC_{IN}$ (Ω)	$\|ZOSC_{IN}\|$ (Ω)	Real $ZOSC_{IN}$ (Ω)	Imag-inary $ZOSC_{IN}$ (Ω)	$\|ZOSC_{IN}\|$ (Ω)
5	1500	−5750	5940	150	−6400	6400	1800	−5200	5500	225	−6200	6200
10	390	−2700	2730	110	−3000	3000	450	−2600	2640	110	−2700	2700
15	190	−2010	2020	70	−2000	2000	190	−1660	1670	75	−1850	1850
20	110	−1510	1510	30	−1400	1400	130	−1350	1360	39	−1390	1390
25	83	−1210	1210	30	−1150	1150	85	−1100	1100	26	−1120	1120
30	62	−972	974	32	−967	968	72	−926	929	27	−945	945
35	53	−842	844	31	−835	836	59	−802	804	25	−822	822
40	50	−743	745	29	−736	737	50	−705	707	26	−724	724
45	44	−658	659	26	−640	641	44	−630	632	22	−630	630
50	39	−597	598	24	−595	595	37	−558	559	22	−573	573
55	35	−541	542	23	−538	538	33	−510	511	21	−522	522
60	33	−490	491	23	−485	486	30	−468	469	20	−479	479
65	30	−459	460	22	−450	451	28	−431	432	18	−441	441
70	30	−420	421	21	−417	418	26	−402	403	17	−412	412
75	28	−394	395	20	−392	393	25	−378	379	17	−386	386
80	27	−369	370	19	−366	366	23	−352	353	16	−361	361
85	27	−349	350	19	−342	343	21	−330	331	15	−338	338
90	27	−330	331	19	−323	324	21	−311	312	15	−318	318
95	25	−312	313	18	−309	310	21	−298	299	16	−305	305
100	24	−294	295	18	−290	291	19	−280	281	14	−286	286
104	24	−280	281	18	−278	279	19	−267	268	14	−274	274

Charge Pump Current Specification Definitions



I1 = Charge Pump Sink Current at $VCP_o = V_P - \Delta V$
I2 = Charge Pump Sink Current at $VCP_o = V_P/2$
I3 = Charge Pump Sink Current at $VCP_o = \Delta V$
I4 = Charge Pump Source Current at $VCP_o = V_P - \Delta V$
I5 = Charge Pump Source Current at $VCP_o = V_P/2$
I6 = Charge Pump Source Current at $VCP_o = \Delta V$
ΔV = Voltage offset from the positive and negative rails. Dependent on the VCO tuning range relative to V_{CC} and GND. Typical values are between 0.5V and 1.0V.

Figure 18. Charge Pump Output Current Magnitude Variation Vs Charge Pump Output Voltage

$$ICP_o \text{ Vs } VCP_o = \frac{\frac{1}{2}(|I1| - |I3|)}{\frac{1}{2}(|I1| + |I3|)} \times 100\%$$

$$= \frac{\frac{1}{2}(|I4| - |I6|)}{\frac{1}{2}(|I4| + |I6|)} \times 100\%$$

Figure 19. Charge Pump Output Current Sink Vs Charge Pump Output Current Source Mismatch

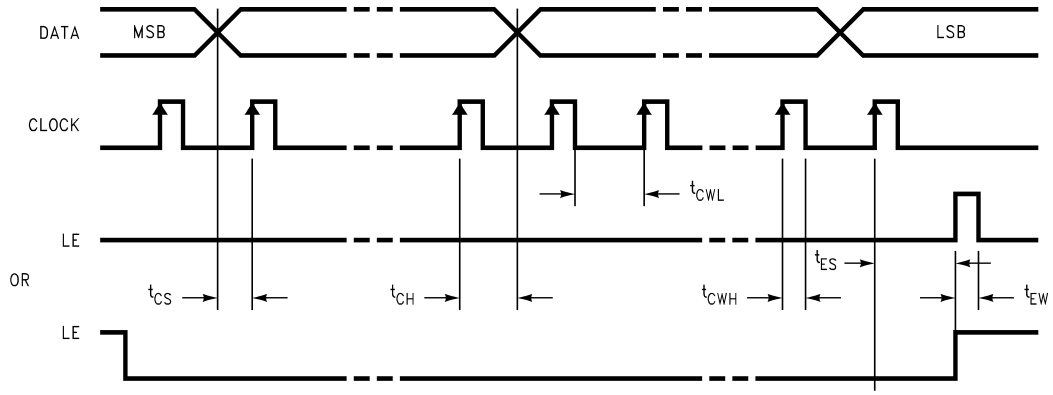
$$ICP_o \text{ SINK Vs } ICP_o \text{ SOURCE} = \frac{|I2| - |I5|}{\frac{1}{2}(|I2| + |I5|)} \times 100\%$$

Figure 20. Charge Pump Output Current Magnitude Variation Vs Temperature

$$ICP_o \text{ Vs } T_A = \frac{|I_2|_{T_A} - |I_2|_{T_A = 25°C}}{|I_2|_{T_A = 25°C}} \times 100\%$$

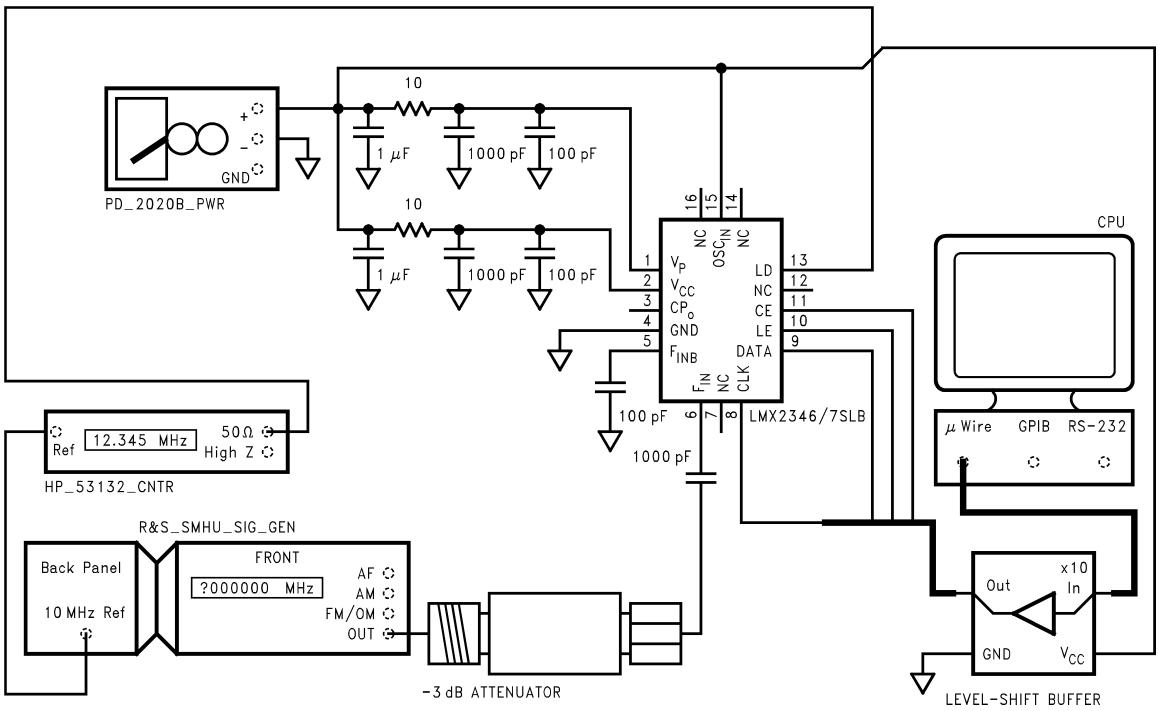
$$= \frac{|I_5|_{T_A} - |I_5|_{T_A = 25°C}}{|I_5|_{T_A = 25°C}} \times 100\%$$

Serial Data Input Timing



Notes:
1. Data is shifted into register on clock rising edge.
2. Data is shifted in MSB first.

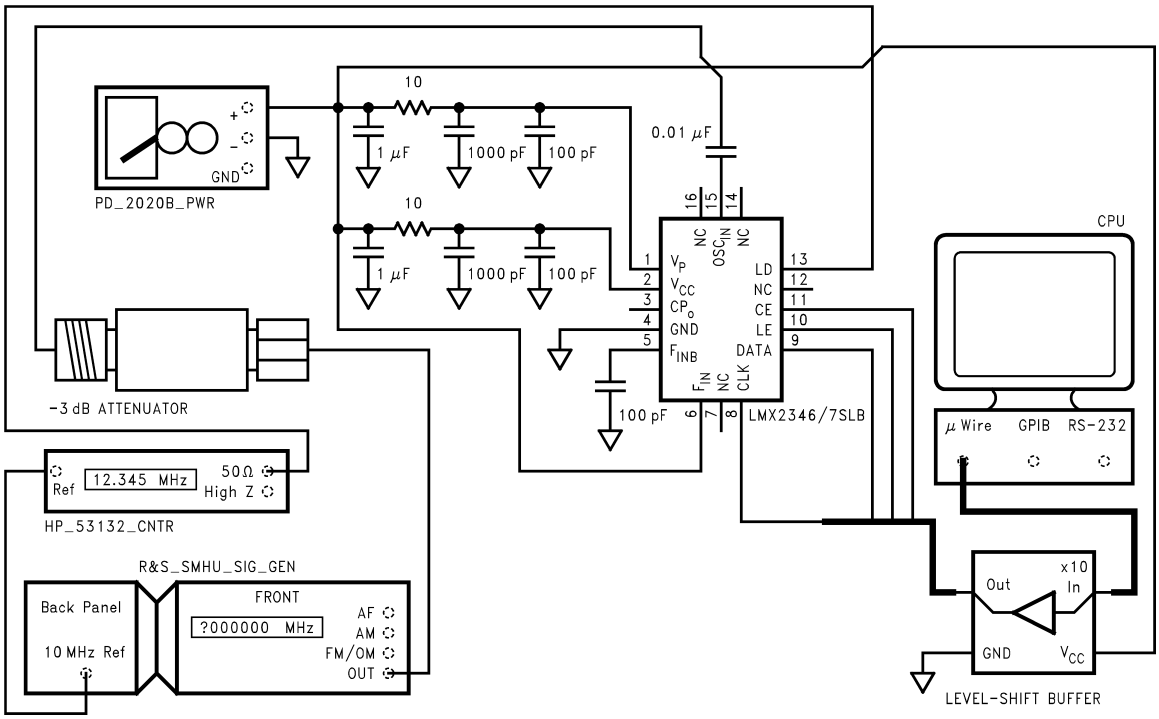
F_{IN} Sensitivity Test Setup



Notes:

1. Test Conditions: NA_CNTR = 16, NB_CNTR = 312, LD_OUT = 3, PD = 0.
2. Sensitivity limit is reached when the frequency error of the divided RF input is greater than or equal to 1 Hz.

OSC_{IN} Sensitivity Test Setup

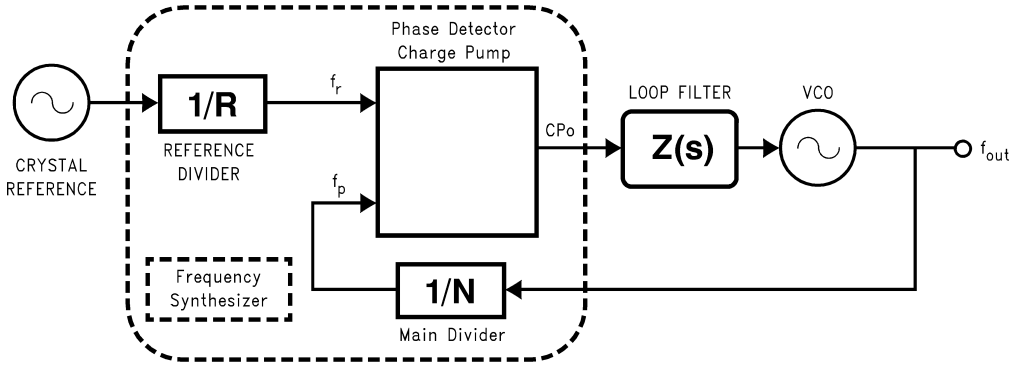


Notes:

1. Test Conditions: R_CNTR = 1000, LD_OUT = 2, PD = 0.
2. Sensitivity limit is reached when the frequency error of the divided RF input is greater than or equal to 1 Hz.

FUNCTIONAL DESCRIPTION

The basic phase-lock-loop (PLL) configuration consists of a high-stability crystal reference oscillator, a frequency synthesizer such as the Texas Instruments LMX2346/7, a voltage controlled oscillator (VCO), and a passive loop filter. The frequency synthesizer includes a phase detector, current mode charge pump, a programmable reference divider, and a programmable feedback divider. The VCO frequency is established by dividing the crystal reference signal down via the reference divider to obtain a frequency that sets the comparison frequency. This reference signal, f_r, is then presented to the input of a phase/frequency detector and compared with another signal, f_p, the feedback signal, which was obtained by dividing the VCO frequency down by way of the feedback divider. The phase/frequency detector measures the phase error between the f_r and f_p signals and outputs control signals that are directly proportional to the phase error. The charge pump then pumps charge into or out of the loop filter based on the magnitude and direction of the phase error. The loop filter converts the charge into a stable control voltage for the VCO. The phase/frequency detector's function is to adjust the voltage presented to the VCO until the feedback signal's frequency and phase match that of the reference signal. When this “phase-locked” condition exists, the RF VCO's frequency will be N times that of the comparison frequency, where N is the feedback divider ratio.



REFERENCE OSCILLATOR

The reference oscillator frequency for the PLL is provided from an external source via the OSC_{in} pin. The reference buffer circuit supports input frequencies from 5 MHz to 104 MHz with a minimum input sensitivity of 0.4 V_{PP}. The reference buffer circuit has a $V_{CC}/2$ input threshold and can be driven from an external CMOS or TTL logic gate. The R_OPT control word is used to optimize the performance of the reference buffer circuit for best Phase Noise and power consumption performance based on the frequency of the reference source. Refer to the Reference Oscillator Optimization section for details on programming the R_OPT control word.

REFERENCE DIVIDER (R COUNTER)

The reference divider is comprised of a 10-bit CMOS binary counter that supports a continuous integer divide range from 2 to 1,023. The divide ratio should be chosen such that the maximum phase comparison frequency of 10 MHz is not exceeded. The reference divider circuit is clocked by the output of the reference buffer circuit. The output of the reference divider circuit feeds the reference input of the phase detector circuit. The frequency of the reference input to the phase detector (also referred to as the comparison frequency) is equal to reference oscillator frequency divided by the reference divider ratio. Refer to the Reference Divider Counter section for details on programming the R Counter.

RF PRESCALER

The LMX2346/7 contain a fixed 32/33 dual modulus RF prescaler. The RF Prescaler operates from 100 MHz to 2000 MHz on the LMX2346 and from 100 MHz to 2500 MHz on the LMX2347.

The complementary F_{IN} and F_{INB} input pins drive the input of a bipolar, differential-pair amplifier. The output of the bipolar, differential-pair amplifier drives a chain of ECL D-type flip-flops in a dual modulus configuration. The output of the prescaler is used to clock the subsequent programmable feedback divider.

PROGRAMMABLE FEEDBACK DIVIDER (N COUNTER)

The programmable feedback divider operates in concert with the RF prescaler to divide the input RF signal (F_{IN}) by a factor of N. The output of the programmable reference divider is provided to the feedback input of the phase detector circuit. The programmable divider supports a continuous integer divide range from 992 to 32,767. The divide ratio should be chosen such that the maximum phase comparison frequency (Fφ) of 10 MHz is not exceeded.

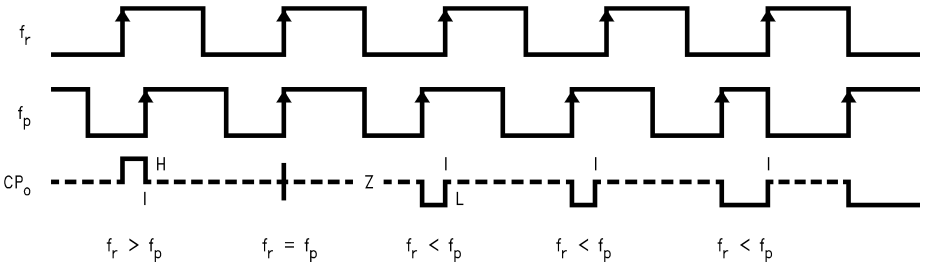
The programmable divider circuit is comprised of an A Counter and a B Counter. The A counter is a 5-bit CMOS swallow counter programmable from 0 to 31. The B Counter is a 10-bit CMOS binary counter, programmable from 3 to 1023. Divide ratios less than 992 are achievable as long as the binary counter value is greater or equal to the swallow counter value (NB_CNTR ≥ NA_CNTR). Refer to the A Counter and B Counter section for details on programming the NA and NB Counter. The following equations are useful in determining and programming a particular value of N:

$N = (32 \times NB\_CNTR) + NA\_CNTR$	
$F_{IN} = N \times F_{\varphi}$	
	Definitions
F_{φ}	Phase Detector Comparison Frequency
F_{IN}	RF Input Frequency
NA_CNTR	A Counter Value
NA_CNTR	B Counter Value

PHASE/FREQUENCY DETECTOR

The phase/frequency detector is driven from the N and R counter outputs. The maximum frequency at the phase detector inputs is 10 MHz. The phase detector outputs control the charge pump. The polarity of the pump-up or pump-down control signals are programmed using the PD_POL control bit, depending on whether the RF VCO tuning characteristics are positive or negative (see programming description in the Phase Detector Polarity section). The phase/frequency detector has a detection range of −2π to +2π.

Figure 21. Phase Comparator And Internal Charge Pump Characteristics



The minimum width of the pump up and pump down current pulses occur at the CPo pin when the loop is phase-locked.

The diagram assumes that PD_POL = 1

f_R is the phase comparator input from the R Divider

f_P is the phase comparator input from the N Divider

CPo is charge pump output

CHARGE PUMP

The charge pumps directs charge into or out of an external loop filter. The loop filter converts the charge into a stable control voltage which is applied to the tuning input of a VCO. The charge pump steers the VCO control voltage towards V_P during pump-up events and towards GND during pump-down events. When locked, CPo is primarily in a Tri-State condition with small corrections occurring at the phase comparison rate.

MICROWIRE INTERFACE

The programmable register set is accessed via the Microwire serial interface. The interface is comprised of three signal pins: CLOCK, DATA, and LE (Latch Enable). Serial data is clocked in from DATA on the rising edge of CLOCK, into an 18-bit shift register. The serial data is clocked in MSB first. The last bit of data decodes the internal register address. On the rising edge of LE, the data stored in the shift register is loaded into one of the two appropriate latches based on the address bit. A complete programming description is provided in the Programming Description section .

MULTI-FUNCTION OUTPUT

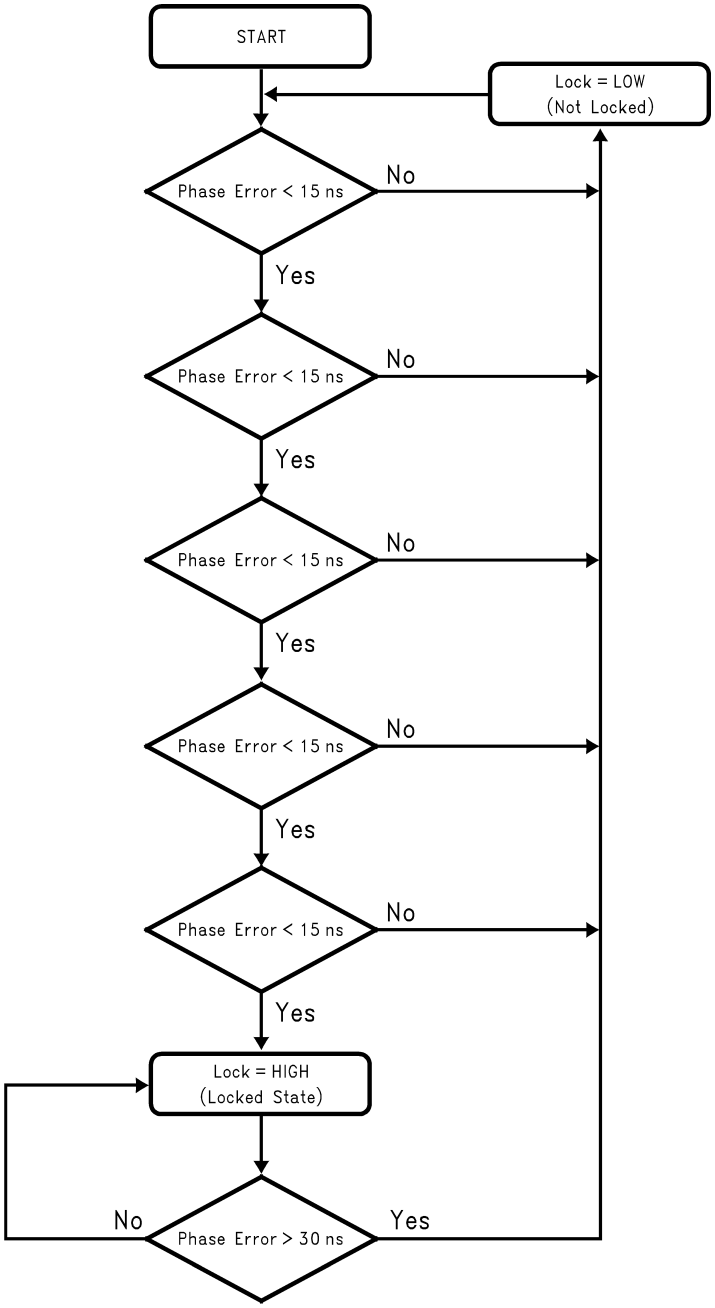
The LMX2346/7 LD pin is a multi-function output that can be configured as a digital lock detect, an analog lock detect, as well as monitor the output of the reference divider, or feedback divider circuits. The LD_OUT control word is used to select the desired output function. When the PLL is in power-down mode, the LD output is always set to a high impedance. A complete programming description of the multi-function output is provided in the LD Output Select section.

Analog Lock Detect

When LD_OUT = 1, an analog lock detect status generated from the phase detector is available on the LD output pin. The lock detect output goes to high impedance when the charge pump is inactive. It goes low when the charge pump is active during a comparison cycle. The analog lock detect signal output is an open drain configuration.

1.8.2 Digital Lock Detect

When LD_OUT = 0, a digital lock detect status is available on the LD output pin. The digital lock detect filter compares the phase difference of the inputs from the phase detector to a RC generated delay of approximately 15 ns. To enter the locked state (LD = High), the phase error must be less than the 15 ns RC delay for 5 consecutive reference cycles. Once in lock, the RC delay is changed to approximately 30 ns. To exit the locked state, the phase error must be greater than the 30 ns RC delay. A flow chart of the digital lock detect filter follows.



POWER-DOWN

CE	PD[1:0]	Operating Mode
0	X	Power-down (Asynchronous)
1	0	Normal Operation
1	1	Power-down (Synchronous)
1	2	Counter Reset
1	3	Power-down (Asynchronous)

The LMX2346/7 are power controlled through logical control of the CE pin in conjunction with programming of the PD control word. A truth table is provided that describes how the state of the CE pin and the PD control word set the operating mode of the device. A complete programming description for the PD control word is provided in the Power-Down section.

When the device enters the power-down mode, the oscillator buffer, RF prescaler, phase detector, and charge pump circuits are all disabled. The OSC_{IN}, CP_O, F_{IN}, F_{INB}, LD pins are all forced to a high impedance state. The reference divider and feedback divider circuits are disabled and held at the load point during power-down. When the device is programmed to normal operation, the oscillator buffer, RF prescaler, phase detector, and charge pump circuits are all powered on. The feedback divider and the reference divider are held at the load point. This allows the RF Prescaler, feedback divider, reference oscillator, and the reference divider circuitry to reach proper bias levels. After a 1.5 µs delay, the feedback and reference divider are enabled and they resume counting in "close" alignment (The maximum error is one prescaler cycle). The MICROWIRE control register remains active and capable of loading and latching in data while in the power-down mode.

The synchronous power-down function is gated by the charge pump. When the device is configured for synchronous power-down, the device will enter the power-down mode upon the completion of the next charge pump pulse event.

The asynchronous power-down function is NOT gated by the completion of a charge pump pulse event. When the device is configured for asynchronous power-down, the part will go into power down mode immediately.

A counter reset function is provided. When the PD control word is programmed to Counter Reset, both the feedback divider and the reference divider are disabled and held at their load point. When the device is programmed to normal operation, both the feedback divider and the reference divider are enabled (without a delay) and resume counting in "close" alignment (The maximum error is one prescaler cycle).

Programming Description

MICROWIRE INTERFACE

The MICROWIRE interface is comprised of an 18-bit shift register, and two control registers. The shift register consists of a 17-bit DATA field and a 1-bit address (ADDR) field as shown below. When Latch Enable transitions HIGH, data stored in the shift register is loaded into either the R or N register depending on the state of the ADDR bit. The data is loaded MSB first. The DATA field assignments for the R and N registers are shown in the Register Map section.

MSB	LSB
DATA	ADDR
17	1 0

ADDR	Target Register
1	R register
0	N register

Register Map

Register	Most Significant Bit						SHIFT REGISTER BIT LOCATION						Least Significant Bit					
	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Data Field																	*ADDR*
R	R_OPT [2:0]			LD_OUT [1:0]		PD_POL	CP_TRI	R_CNTR [9:0]										1
N	NB_CNTR [9:0]										NA_CNTR [4:0]					PD [1:0]		0

R REGISTER

The R register contains the R_CNTR, CP_TRI, PD_POL, LD_OUT, R_OPT control words. The detailed descriptions and programming information for each control word is discussed in the following sections.

Register	Most Significant Bit						SHIFT REGISTER BIT LOCATION						Least Significant Bit					
	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Data Field																	*ADDR*
R	R_OPT [2:0]			LD_OUT [1:0]		PD_POL	CP_TRI	R_CNTR [9:0]										1

R_CTR[9:0] Reference Divider (R COUNTER) R[10:1]

The reference divider can be programmed to support divide ratios from 2 to 1023. Divide ratios of less than 2 are prohibited.

	R_CNTR [9:0]									
Reference Divider Ratio	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
2	0	0	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	0	0	1	1
•	•	•	•	•	•	•	•	•	•	•
1,023	1	1	1	1	1	1	1	1	1	1

CP_TRI Charge Pump Tri-State R[11]

The CP_TRI control bit allows the charge pump to be switched between a normal operating mode and a high impedance output state. This happens asynchronously or immediately with the change in CP_TRI bit.

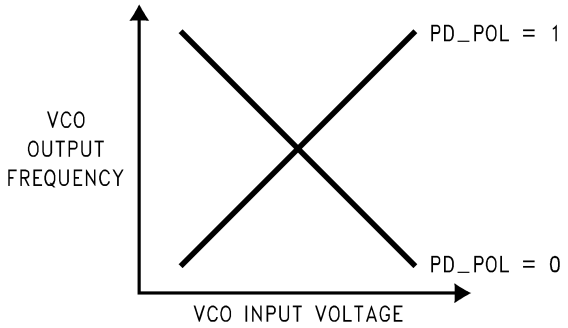
Control Bit	Register Location	Description	Function	
			0	**1**
CP_TRI	R[11]	Charge Pump TRI-STATE	Charge Pump Operates Normal	Charge Pump Output in High Impedance State

PD_POL Phase Detector Polarity R[12]

The PD_POL control bit is used to set the polarity of the phase detector based on the VCO tuning characteristic.

Control Bit	Register Location	Description	Function	
			0	**1**
PD_POL	R[12]	Phase Detector Polarity	Negative VCO Tuning Characteristic	Positive VCO Tuning Characteristic

Figure 22. VCO Characteristics



LD_OUT[1:0] LD Output Select R[14:13]

The LD_Out control word is used to select which signal is routed the the LD pin.

LD_OUT[1:0]	LD Pin Output Mode	Output Circuit Configuration
0	Digital Lock Detect	Push-Pull
1	Analog Lock Detect	Open-Drain
2	R divider output	Push-Pull
3	N divider output	Push-Pull

R_OPT[2:0] Reference Oscillator Optimization R[17:15]

The R_OPT control words are used to optimize the performance of the reference buffer circuit for best Phase Noise and power consumption performance based on the frequency of the reference source.

R_OPT[2:0]	Optimization Frequency Range
0	5 MHz–50 MHz
7	50 MHz–104 MHz
1-6	Reserved—Do not use.

N REGISTER

The N register contains the PD (Power-Down), NA_CNTR, and NB_CNTR control words. The NA_CNTR, and NB_CNTR control words are used to setup the programmable feedback divider. The PWR-DN control word is used to switch the device between the normal operating mode and various power-down modes.

Register	Most Significant Bit						SHIFT REGISTER BIT LOCATION						Least Significant Bit					
	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Data Field																	*ADDR*
N	NB_CNTR [9:0]										NA_CNTR [4:0]					PD [1:0]		0

PD[1:0] Power-Down N[2:1]

The PD control word is used to switch the device between the normal operating mode and various power-down modes.

PD [1:0]	Operating Mode
0	Normal Operation
1	Synchronous Power-down
2	Counter Reset
3	Asynchronous Power-down

NA_CNTR[4:0] A Counter N[7:3]

The NA_CNTR control word is used to program the A counter. The A counter is a 5-bit swallow counter used in the programmable feedback divider. The A counter can be programmed to values ranging from 0 to 31. See the PROGRAMMABLE FEEDBACK DIVIDER (N COUNTER) section for details on how the value of the A counter should be selected.

A Counter Value	NA_CNTR[4:0]				
0	0	0	0	0	0
1	0	0	0	0	1
•	•	•	•	•	•
31	1	1	1	1	1

NB_CNTR[9:0] B Counter N[17:8]

The NB_CNTR control word is used to program the B counter. The B counter is a 10-bit binary counter used in the programmable feedback divider. The B counter can be programmed to values ranging from 3 to 1023. See the PROGRAMMABLE FEEDBACK DIVIDER (N COUNTER) section for details on how the value of the B counter should be selected.

B Counter Value	NB_CNTR[9:0]									
3	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•
1023	1	1	1	1	1	1	1	1	1	1

REVISION HISTORY

Changes from Revision E (April 2013) to Revision F	Page
• Changed layout of National Data Sheet to TI format	25

IMPORTANT NOTICE

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