LMV1024/LMV1026 (Stereo) PDM Output with Pre-Amplifier for Electret Microphones

Check for Samples: LMV1024, LMV1026

FEATURES

- **(Typical V_{DD} = 1.8V, CLOCK = 1.2 MHz, f_{INPUT} = 1 kHz, V_{INPUT} = 18 mV_{PP}, Unless Otherwise Specified)**
- **Enhanced High-Performance, Full PDM Output from the Element**
- **Stereo Chipset and Array Routing**
- **SNR A-Weighted 59 dB**
- **Digital A-Weighted Noise Floor −89 dBFS**
- **Supply Current 518 µA**
- **Clock Frequency 400 kHz to 2.4 MHz**
- **Total Harmonic Distortion 0.03%**
- **Power Supply Rejection Ratio 100 dB**
- **Adhesion Technology >1 kg**
- **Highly Integrated Stereo or Mono Signaling**
- **Maximized System Performance**
- **Reduced Components and Layout**
- **RF (buzz noise) Managed with 4 Wire Signaling**
- **Thinnest 0.35 mm DSBGA Packaging**

APPLICATIONS

- **Digital Output Audio Subsystems and Stereo Arrays**
- **Electret Condenser Microphones with all Digital Output**
- **Portable Communications and Small Form Factor**
- **Digital Audio Computing or Voice Security**
- **Automotive or Array Systems**
- **Headphone and Headset Accessories**

DESCRIPTION

TI's LMV1024 and LMV1026 stereo amplifiers are solutions for the new generation of voice enrichment capabilities. TI has integrated sigma delta modulation and analog cores to improve the voice quality and the performance and to support designer's choices.

Each 20 kHz preamplifier drives a Pulse Density Modulated (PDM) signal at an over sampled 60 bit stream, offering versatility. These solutions provide immediate conversion to high performance audio spectrum, thus completing a high quality audio system. The LMV1024 and LMV1026 operate from 1.6V to 3V.

TI's new adjustable clock frequency technology is designed for stereo, performance and ease of use. The stereo function is either a rising or falling edge clock command. The high drive, robust PDM signal directly from an ECM (Electret Condenser Microphone), upgrades existing lower quality, low-level signal constraints.

These advanced mixed signal preamplifiers cleanly, accurately and creatively eliminate older, poorer quality systems, which restricted performance and versatility. The 4-wire PDM signaling reduces RF noise and simplifies layout. Using TI's PDM solutions is the choice for higher quality mono or stereo and multi-array applications.

TI's 518µA circuits deliver stereo portability with audio quality bandwidth. These solutions enable rapid system evaluation and enhance consumer satisfaction. TI provides the LMV1024 and LMV1026 in 6-bump DSBGA packages with 1 kg adhesion properties.

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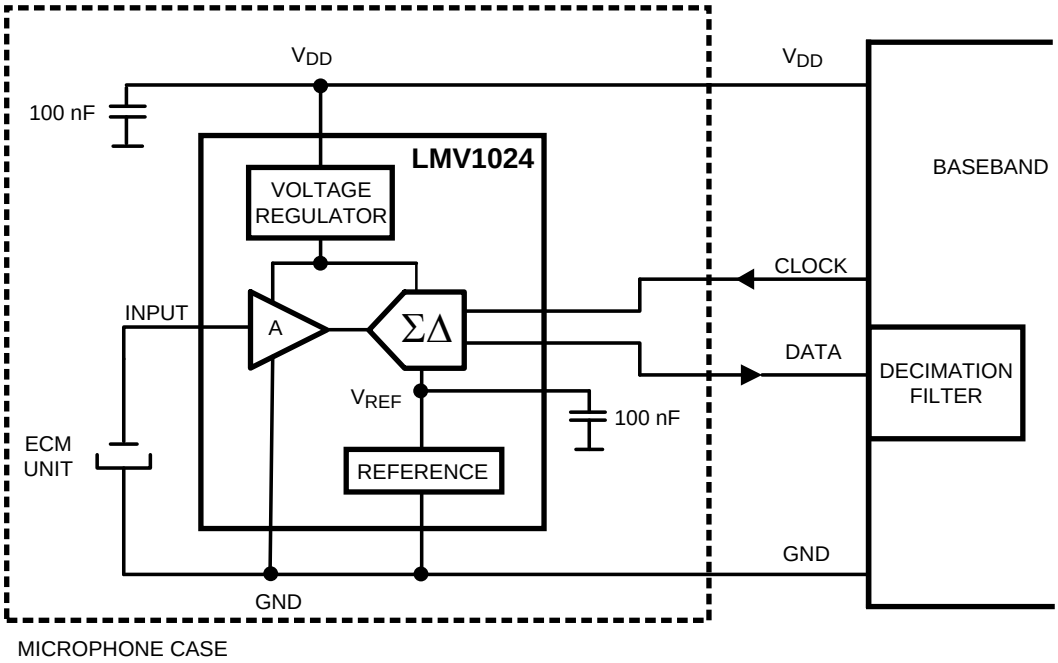
Typical Application



For a stereo application, see STEREO OPERATION in the APPLICATION SECTION.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

ESD Tolerance (3)	
Human Body Model	2500V
Machine Model	250V
Supply Voltage	
V_{DD} - GND	3.3V
Storage Temperature Range	−65°C to 150°C
Junction Temperature (4)	150°C max
Mounting Temperature	
Infrared or Convection (20 sec.)	235°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) The Human Body Model (HBM) is 1.5 kΩ in series with 100 pF. The Machine Model is 0Ω in series with 200 pF.
(4) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Operating Ratings(1)

Supply Voltage	1.6V to 3.0V
Input Clock Frequency	400 kHz to 2.4 MHz
Duty Cycle	40% to 60%
Operating Temperature Range	−40°C to 85°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.

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1.8V Electrical Characteristics[1]

Unless otherwise specified, all limits are ensured for T_J = 25°C, V_{DD} = 1.8V, V_{IN} = 18 mV_{PP}, f_{CLK} = 1.2 MHz, Duty Cycle = 50% and 100 nF capacitor between V_{REF} and GND. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min[2]	Typ[3]	Max[2]	Units
SNR	Signal to Noise Ratio	f_{IN} = 1 kHz, A-Weighted		59		dB
e_N	Digital Noise Floor (Integrated)	f = 20 Hz to 10 kHz, A-Weighted, 4.7 pF Capacitor Connected from Input to GND to Simulate ECM, No Signal		−89		dBFS(A)
THD	Total Harmonic Distortion	f_{IN} = 1 kHz, V_{IN} = 18 mV_{PP}		0.03		%
I_{DD}	Supply Current	V_{IN} = GND, CLK = ON, High Impedance Load[4]		518		µA
		V_{IN} = GND, CLK = OFF		503	**600**	
V_{IL}	CLOCK Input Logic Low Level				**0.3**	V
V_{IH}	CLOCK Input Logic High Level		**1.5**			V
V_{OL}	DATA Output Logic Low Level				**0.1**	V
V_{OH}	DATA Output Logic High Level		**1.7**			V
V_{IN}	Max Input Signal	f_{IN} = 1 kHz, THD < 1%		243		mV_{PP}
V_{OUT}	Max Output Signal	f_{IN} = 1 kHz, THD < 1%		−6.8		dBFS
PSRR	Power Supply Rejection Ratio	V_{IN} = GND, Test Signal on V_{DD} = 217 Hz, 100 mV_{PP}		100		dB
t_A	Time from CLOCK Transition to DATA Becoming High Impedance (See also Figure 46 in the APPLICATION SECTION)	LMV1024: On Rising Edge of the CLOCK		65		ns
		LMV1026: On Falling Edge of the CLOCK				
t_B	Time from CLOCK Transition to DATA Becoming Valid (See also Figure 46 in the APPLICATION SECTION)	LMV1024: On Falling Edge of the CLOCK		90		ns
		LMV1026: On Rising Edge of the CLOCK				
C_{IN}	Input Capacitance			2		pF
R_{IN}	Input Impedance			1000		MΩ

(1) Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$.
(2) All limits are ensured by design or statistical analysis.
(3) Typical values represent the most likely parametric norm.
(4) The Supply Current depends on the applied Clock Frequency and the load on the DATA output.

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2.7V Electrical Characteristics[1]

Unless otherwise specified, all limits are ensured for T_J = 25°C, V_{DD} = 2.7V, V_{IN} = 18 mV_{PP}, f_{CLK} = 1.2 MHz, Duty Cycle = 50% and 100 nF capacitor between V_{REF} and GND. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min[2]	Typ[3]	Max[2]	Units
SNR	Signal to Noise Ratio	f_{IN} = 1 kHz, A-Weighted		59		dB
e_n	Digital Noise Floor (Integrated)	f = 20 Hz to 10 kHz, A-Weighted, 4.7 pF Capacitor Connected from Input to GND to Simulate ECM, No Signal		−89		dBFS(A)
THD	Total Harmonic Distortion	f_{IN} = 1 kHz, V_{IN} = 18 mV_{PP}		0.03		%
I_{DD}	Supply Current	V_{IN} = GND, CLK = ON, High Impedance Load[4]		535		µA
		V_{IN} = GND, CLK = OFF		519	**650**	
V_{LOW}	CLOCK Logic Low Level				**0.3**	V
V_{HIGH}	CLOCK Logic High Level		**2.4**			V
V_{OL}	DATA Output Logic Low Level				**0.1**	V
V_{OH}	DATA Output Logic High Level		**2.6**			V
V_{IN}	Max Input Signal	f_{IN} = 1 kHz, THD < 1%		249		mV_{PP}
V_{OUT}	Max Output Signal	f_{IN} = 1 kHz, THD < 1%		−6.6		dBFS
PSRR	Power Supply Rejection Ratio	V_{IN} = GND, Test Signal on V_{DD} = 217 Hz, 100 mV_{PP}		100		dB
t_A	Time from CLOCK Transition to DATA Becoming High Impedance (See also Figure 46 in the APPLICATION SECTION)	LMV1024: On Rising Edge of the CLOCK		65		ns
		LMV1026: On Falling Edge of the CLOCK				
t_B	Time from CLOCK Transition to DATA Becoming Valid (See also Figure 46 in the APPLICATION SECTION)	LMV1024: On Falling Edge of the CLOCK		90		ns
		LMV1026: On Rising Edge of the CLOCK				
C_{IN}	Input Capacitance			2		pF
R_{IN}	Input Impedance			1000		MΩ

(1) Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$.
(2) All limits are ensured by design or statistical analysis.
(3) Typical values represent the most likely parametric norm.
(4) The Supply Current depends on the applied Clock Frequency and the load on the DATA output.

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Connection Diagram

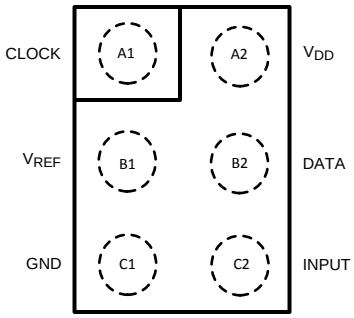
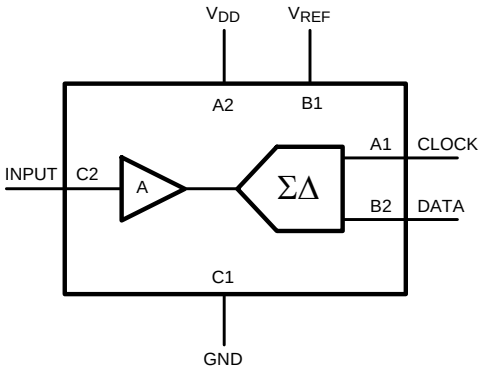


Figure 1. Top View
6-Bump DSBGA
See YPD0006 Package

PIN DESCRIPTIONS

	Pin	Name	Description
Power Supply	A2	V_{DD}	Positive supply voltage
	C1	GND	Ground
Input	C2	Input	The microphone is connected to this input pin.
Reference	B1	V_{REF}	A capacitor of 100 nF is connected between V_{REF} and ground. This capacitor is used to filter the internal converter reference voltage.
Clock Input	A1	Clock	The user adjustable clock frequency ranges from 400 kHz to 2.4 MHz.
Data Output	B2	Data	Over sampled bitstream output. Data is valid if clock is LOW (LMV1024). The data of the LMV1026 data is valid when clock is HIGH. When the data is not valid the data output is Hi-Z. For exact specifications see the Application Section.

Block Diagram



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TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified, measurements are performed on an LMV1024 with V_{DD} = 1.8V, Clock Duty Cycle = 50% and a 100 nF capacitor is placed between V_{REF} and GND, T_J = 25°C.

Supply Current vs. Supply Voltage @ CLOCK = 1.2 MHz

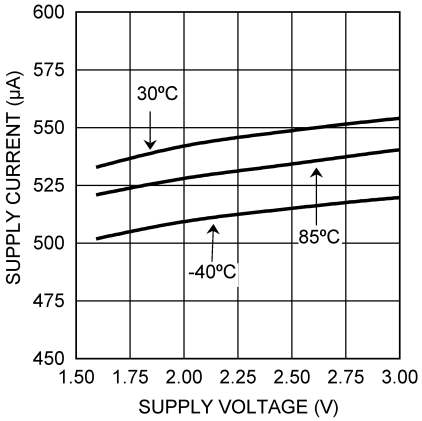

Figure 2.

Supply Current vs. Supply Voltage @ CLOCK = 2.4 MHz

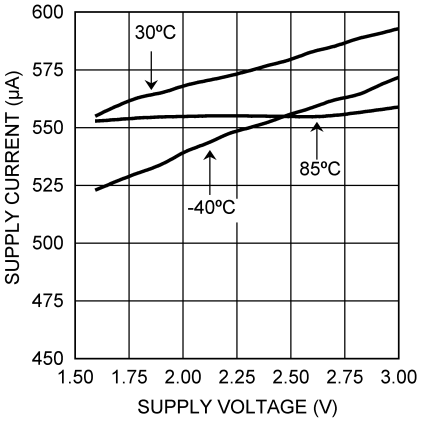

Figure 3.

Supply Current vs. Supply Voltage CLOCK = OFF

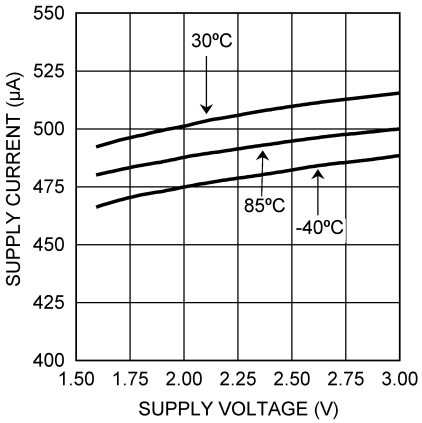

Figure 4.

SNR, SINAD and -THD vs. Input Amplitude @ CLOCK = 408 kHz, 3.4 kHz Audio BW

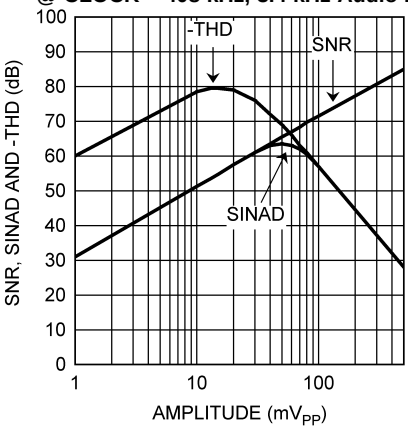

Figure 5.

SNR, SINAD and -THD vs. Input Amplitude @ CLOCK = 960 kHz, 8 kHz Audio BW

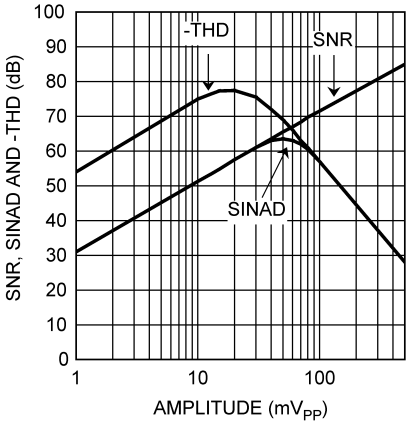

Figure 6.

SNR, SINAD and -THD vs. Input Amplitude @ CLOCK = 1.2 MHz, 10 kHz Audio BW

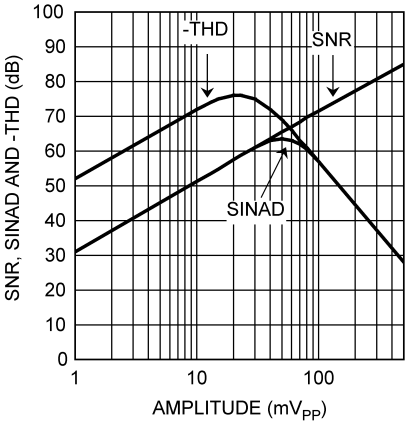

Figure 7.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, measurements are performed on an LMV1024 with V_{DD} = 1.8V, Clock Duty Cycle = 50% and a 100 nF capacitor is placed between V_{REF} and GND, T_J = 25°C.

SNR, SINAD and -THD vs. Input Amplitude @ CLOCK = 1.92 MHz, 16 kHz Audio BW

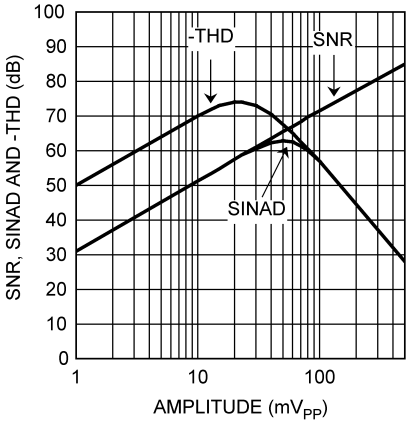

Figure 8.

SNR, SINAD and -THD vs. Input Amplitude @ CLOCK = 2.4 MHz, 20 kHz Audio BW

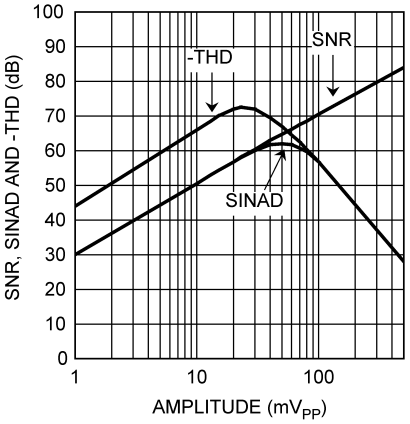

Figure 9.

SNR, SINAD and -THD vs. Output @ CLOCK = 408 kHz, 3.4 kHz Audio BW

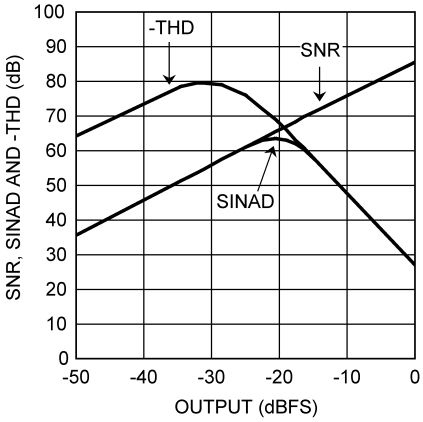

Figure 10.

SNR, SINAD and -THD vs. Output @ CLOCK = 960 kHz, 8 kHz Audio BW

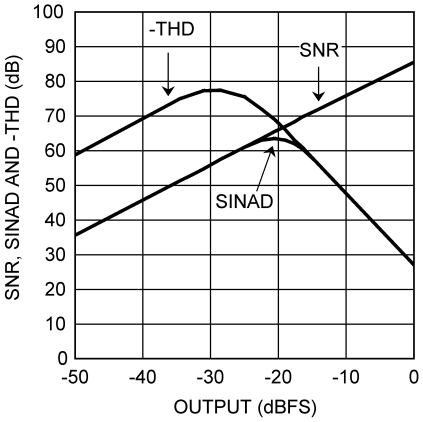

Figure 11.

SNR, SINAD and -THD vs. Output @ CLOCK = 1.2 MHz, 10 kHz Audio BW

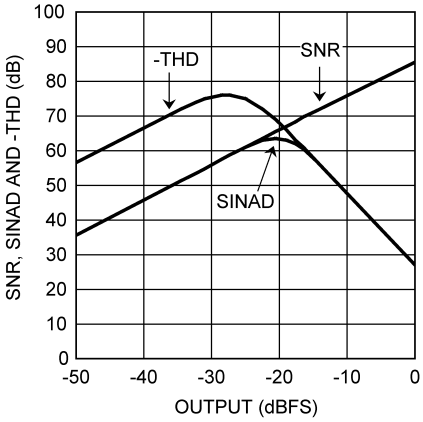

Figure 12.

SNR, SINAD and -THD vs. Output @ CLOCK = 1.92 MHz, 16 kHz Audio BW

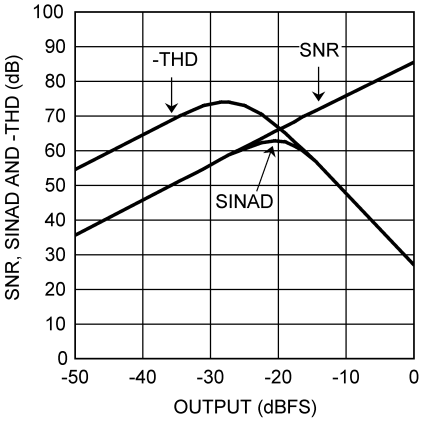

Figure 13.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, measurements are performed on an LMV1024 with V_{DD} = 1.8V, Clock Duty Cycle = 50% and a 100 nF capacitor is placed between V_{REF} and GND, T_J = 25°C.

SNR, SINAD and -THD vs. Output @ CLOCK = 2.4 MHz, 20 kHz Audio BW

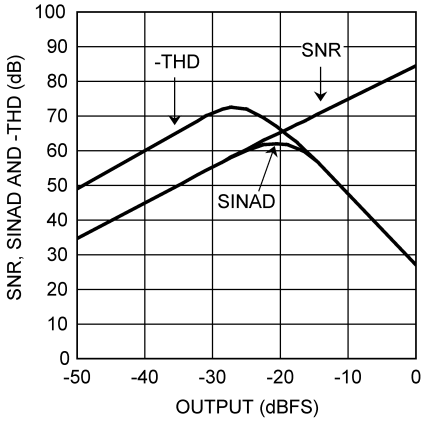

Figure 14.

SINAD vs. Frequency @ CLOCK = 408 kHz, 3.4 kHz Audio BW

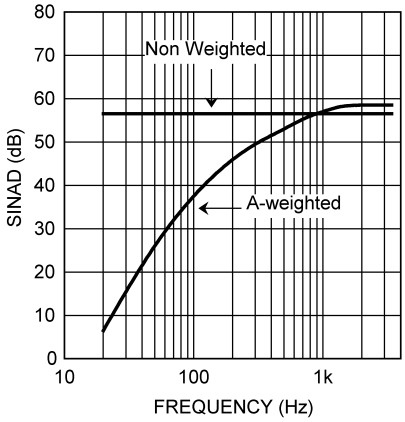

Figure 15.

SINAD vs. Frequency @ CLOCK = 960 kHz, 8 kHz Audio BW

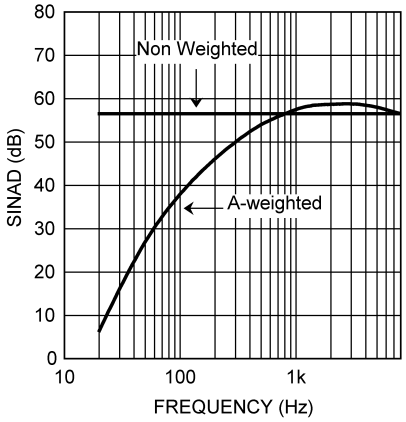

Figure 16.

SINAD vs. Frequency @ CLOCK = 1.2 MHz, 10 kHz Audio BW

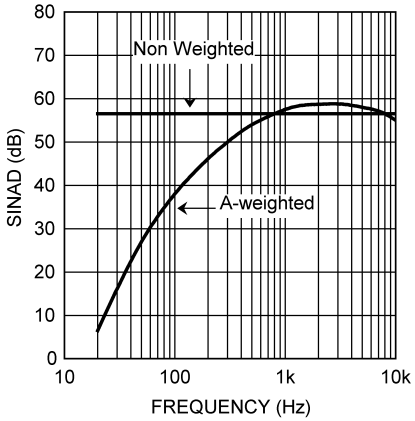

Figure 17.

SINAD vs. Frequency @ CLOCK = 1.92 MHz, 16 kHz Audio BW

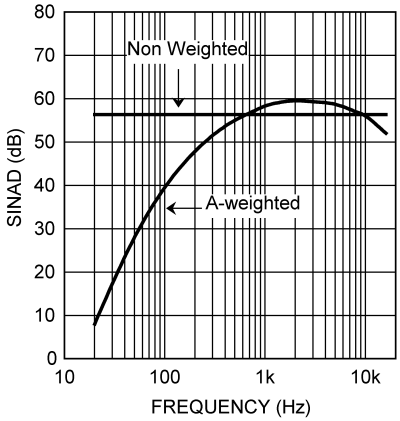

Figure 18.

SINAD vs. Frequency @ CLOCK = 2.4 MHz, 20 kHz Audio BW

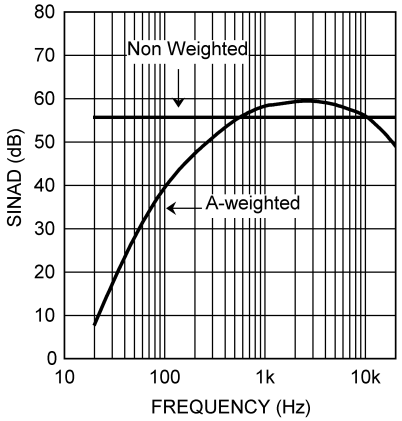

Figure 19.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, measurements are performed on an LMV1024 with V_{DD} = 1.8V, Clock Duty Cycle = 50% and a 100 nF capacitor is placed between V_{REF} and GND, T_J = 25°C.

Noise vs. Frequency
@ CLOCK = 408 kHz, 3.4 kHz Audio BW

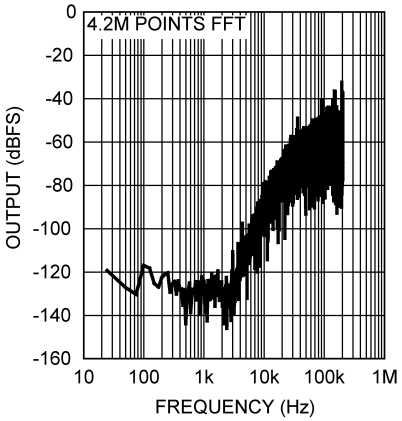

Figure 20.

Noise vs. Frequency
@ CLOCK = 960 kHz, 8 kHz Audio BW

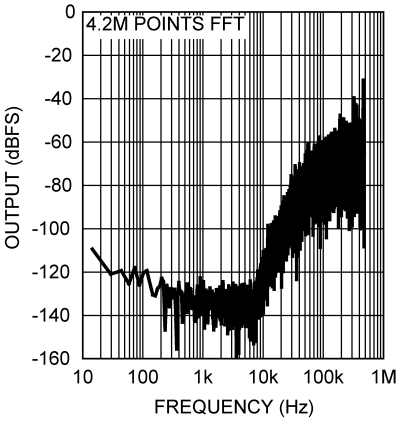

Figure 21.

Noise vs. Frequency
@ CLOCK = 1.2 MHz, 10 kHz Audio BW

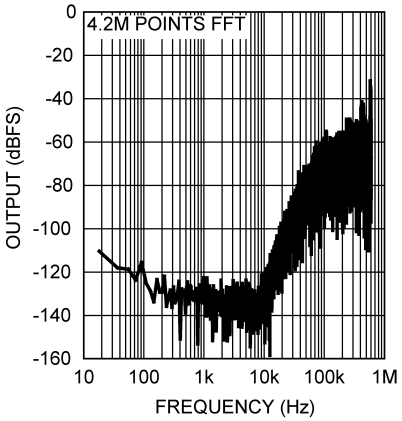

Figure 22.

Noise vs. Frequency
@ CLOCK = 1.92 MHz, 16 kHz Audio BW

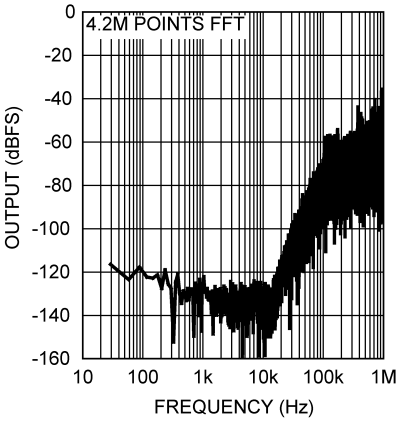

Figure 23.

Noise vs. Frequency
@ CLOCK = 2.4 MHz, 20 kHz Audio BW

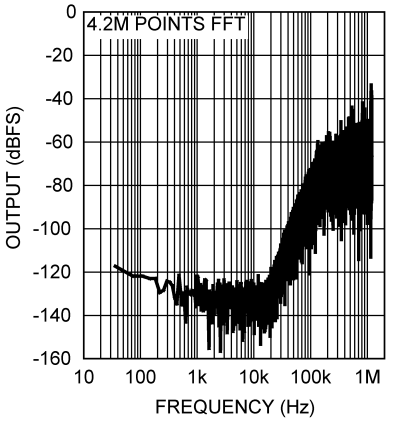

Figure 24.

PSRR vs. Frequency
@ CLOCK = 1.2 MHz

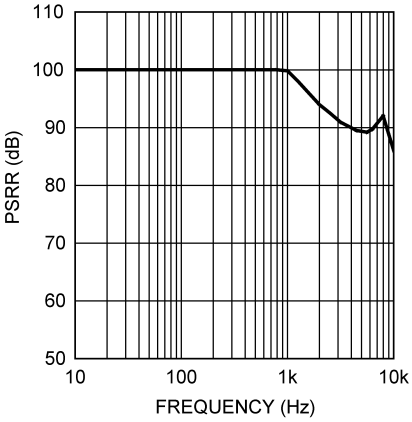

Figure 25.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, measurements are performed on an LMV1024 with V_{DD} = 1.8V, Clock Duty Cycle = 50% and a 100 nF capacitor is placed between V_{REF} and GND, T_J = 25°C.

PSRR vs. Frequency
@ CLOCK = 2.4 MHz

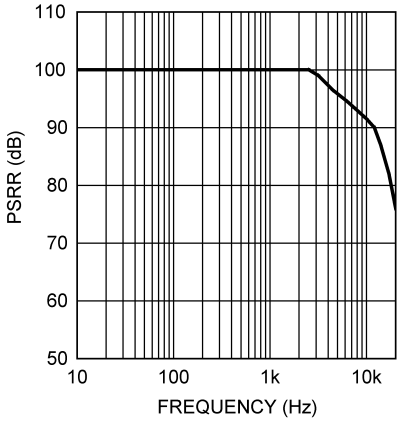

Figure 26.

Output vs. Input Amplitude
@ CLOCK = 408 kHz, 3.4 kHz Audio BW

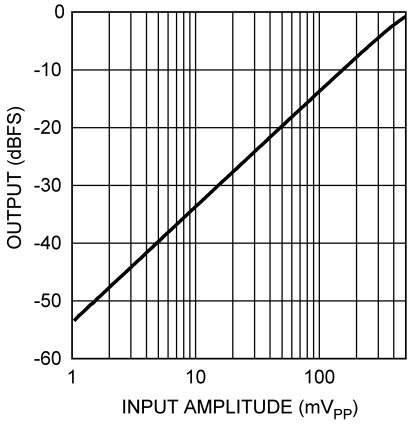

Figure 27.

Output vs. Input Amplitude
@ CLOCK = 960 kHz, 8 kHz Audio BW

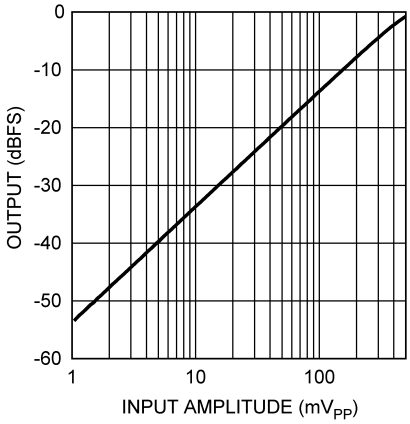

Figure 28.

Output vs. Input Amplitude
@ CLOCK = 1.2 MHz, 10 kHz Audio BW

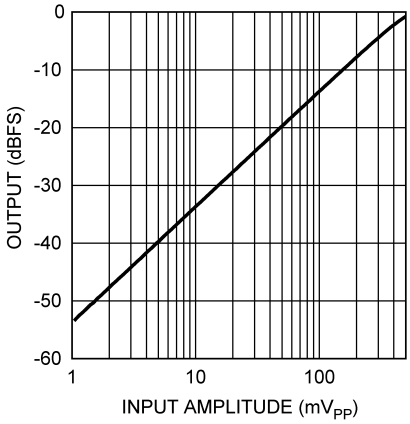

Figure 29.

Output vs. Input Amplitude
@ CLOCK = 1.92 MHz, 16 kHz Audio BW

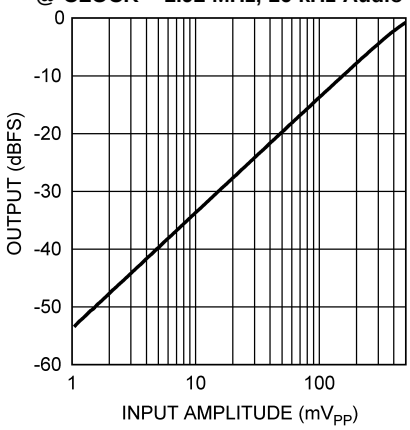

Figure 30.

Output vs. Input Amplitude
@ CLOCK = 2.4 MHz, 20 kHz Audio BW

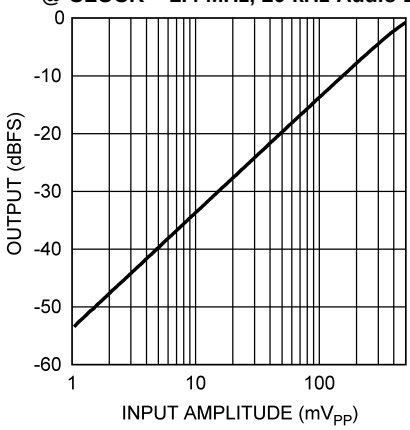

Figure 31.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, measurements are performed on an LMV1024 with V_{DD} = 1.8V, Clock Duty Cycle = 50% and a 100 nF capacitor is placed between V_{REF} and GND, T_J = 25°C.

Output vs. Frequency
@ CLOCK = 408 kHz, 3.4 kHz Audio BW

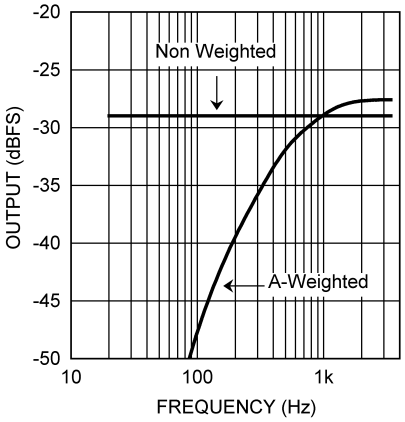

Figure 32.

Output vs. Frequency
@ CLOCK = 960 kHz, 8 kHz Audio BW

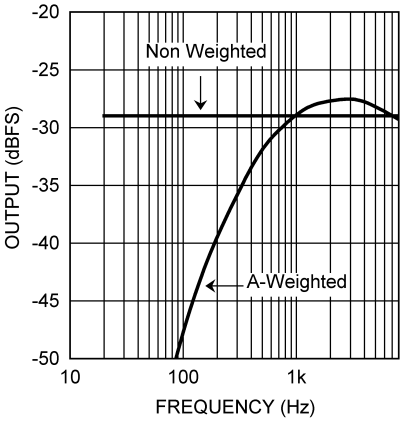

Figure 33.

Output vs. Frequency
@ CLOCK = 1.2 MHz, 10 kHz Audio BW

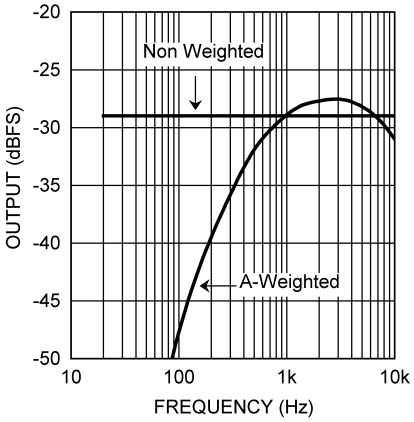

Figure 34.

Output vs. Frequency
@ CLOCK = 1.92 MHz, 16 kHz Audio BW

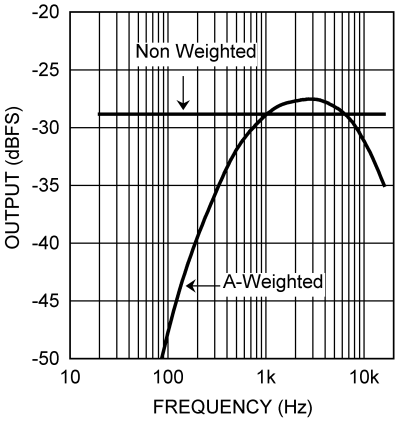

Figure 35.

Output vs. Frequency
@ CLOCK = 2.4 MHz, 20 kHz Audio BW

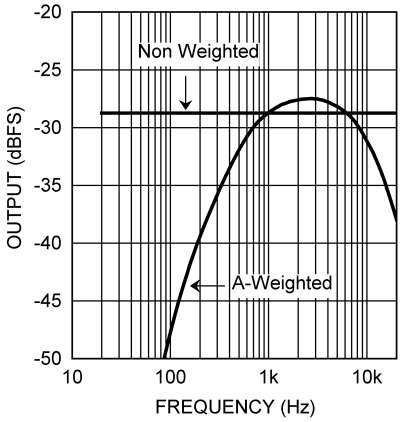

Figure 36.

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APPLICATION SECTION

The LMV1024/LMV1026 consist of a pre-amplifier and sigma delta converter for placement inside an electret condenser microphone (ECM). The output of the LMV1024/LMV1026 is a robust digital serial bit stream eliminating the sensitive low-level analog signals of conventional JFET microphones. This application section describes, among others, a typical application, a sensitivity comparison between different ECM types, stereo operation and layout recommendations on the ECM PCBs.

TYPICAL APPLICATION

Figure 37 depicts a typical application, where the LMV1024 or LMV1026 is built inside the ECM canister. This ECM can be directly connected to a DSP in a digital audio system, like a baseband chip in a cell phone. Connecting is easy because of the digital LMV1024/LMV1026 interface. A digital filter in the DSP or Baseband decimates the audio signal.

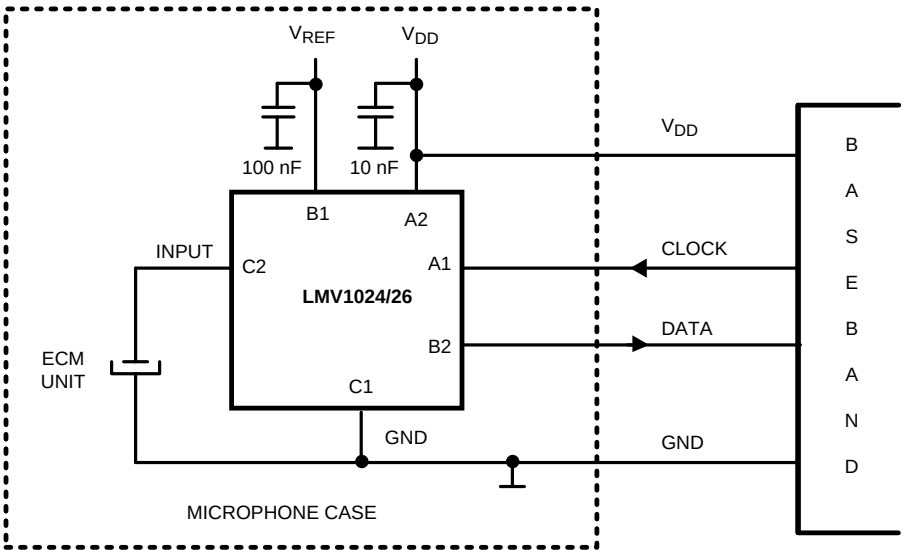

Figure 37. Typical Application

BUILT-IN PRE-AMPLIFIER / ADC

The LMV1024/LMV1026 are offered in a space saving small 6-bump DSBGA package in order to fit inside small ECM canisters. The LMV1024 or LMV1026 IC is placed on the PCB. This PCB forms the bottom of the microphone, which is placed in the cell phone.

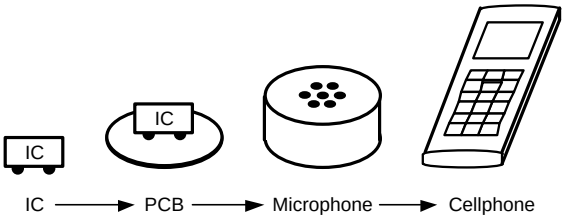

Figure 38. Built-in Pre-Amplifier / ADC

Figure 39 depicts a cross section of a microphone with the IC inside the ECM canister. The PCB of the microphone has 4 pads that connects V_{DD}, Ground, DATA and the CLOCK.

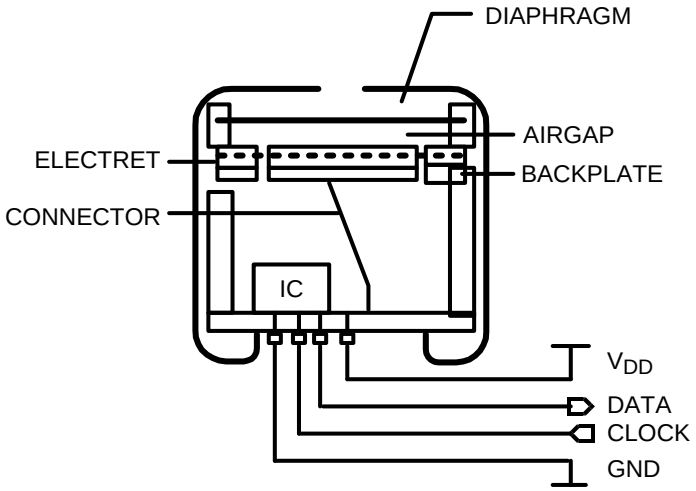

Figure 39. Cross section of a Microphone

A-WEIGHTED FILTER

The human ear has a frequency range from about 20 Hz to 20 kHz. Within this range the sensitivity of the human ear is not equal for each frequency. In order to approach a natural hearing response, weighting filters are introduced. One of these filters is the A-weighted filter. The A-weighted filter is commonly used in signal-to-noise ratio measurements, where sound is compared to device noise. The filter improves the correlation of the measured data to the signal-to-noise ratio perceived by the human ear.

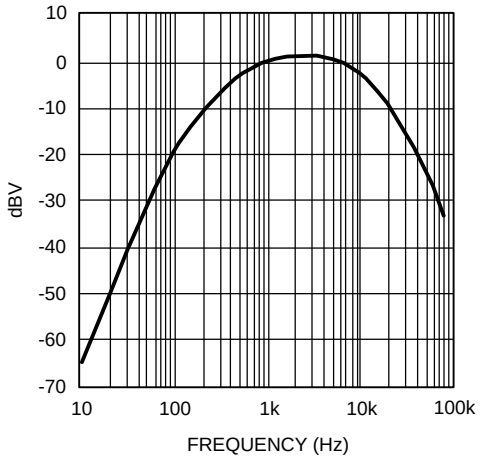

Figure 40. A-weighted Filter

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SENSITIVITY

Sensitivity is a measure for the transfer from the applied acoustic signal to the output of the microphone. Conventional JFET microphones and microphones with built-in gain have a sensitivity that is expressed in dB(V/Pa), where 0dB = 1V/Pa. A certain pressure on the electret of the microphone gives a certain voltage at the output of the microphone. Since the LMV1024 microphone has a digital output, the sensitivity will be stated in dB(Full Scale/Pascal) or dB(FS/Pa) as opposed to conventional microphones. This section compares the various microphone types and their sensitivity. Examples are given to calculate the resulting output for a given sound pressure.

Sound Pressure Level

The volume of sound applied to a microphone is usually stated as a sound pressure in dB SPL. This unity of dB SPL refers to the threshold of hearing of the human ear. The sound pressure in decibels is defined by:

$SPL = 20 \log (P_M/P_O)$

where

- SPL is the Sound Pressure in dB
- $SPLP_M$ is the measured absolute sound pressure
- PaP_O is the threshold of hearing (20 µPa) (1)

In order to calculate the resulting output voltage of the electret element for a given sound pressure in dB SPL, the absolute sound pressure P_M must be known. This is the absolute sound pressure in decibels referred to 1 Pa instead of 20 µPa. The absolute sound pressure P_M in dBPa is given by:

$P_M = SPL\ (dB\ SPL) + P_O\ (dBPa) P_M = SPL + 20*\log\ 20\ \mu Pa P_M = SPL - 94\ dB$ (2)

JFET Microphone

Translation from the absolute sound pressure level to a voltage can be done when the electrets sensitivity is known. A typical electret element has a sensitivity of −44 dB(V/Pa). This is also the typical sensitivity number for the JFET microphone, since a JFET usually has a gain of about 1x (0 dB). A block diagram of a microphone with a JFET is given in Figure 41.

Example: Busy traffic has a Sound Pressure of 70 dB SPL.

Microphone Output = SPL + C + S

where

- SPL is the Sound Pressure in dB
- SPLC is the dB SPL to dBPa conversion (−94 dB)S is the Sensitivity in dB(V/Pa)
- Microphone Output = 70 – 94 – 44 = −68 dBVThis is equivalent to 1.13 mV_{PP}. (3)

The analog output signal is so low that it can easily be distorted by interference from outside the microphone. Additional gain is desirable to make the signal less sensitive to interference.

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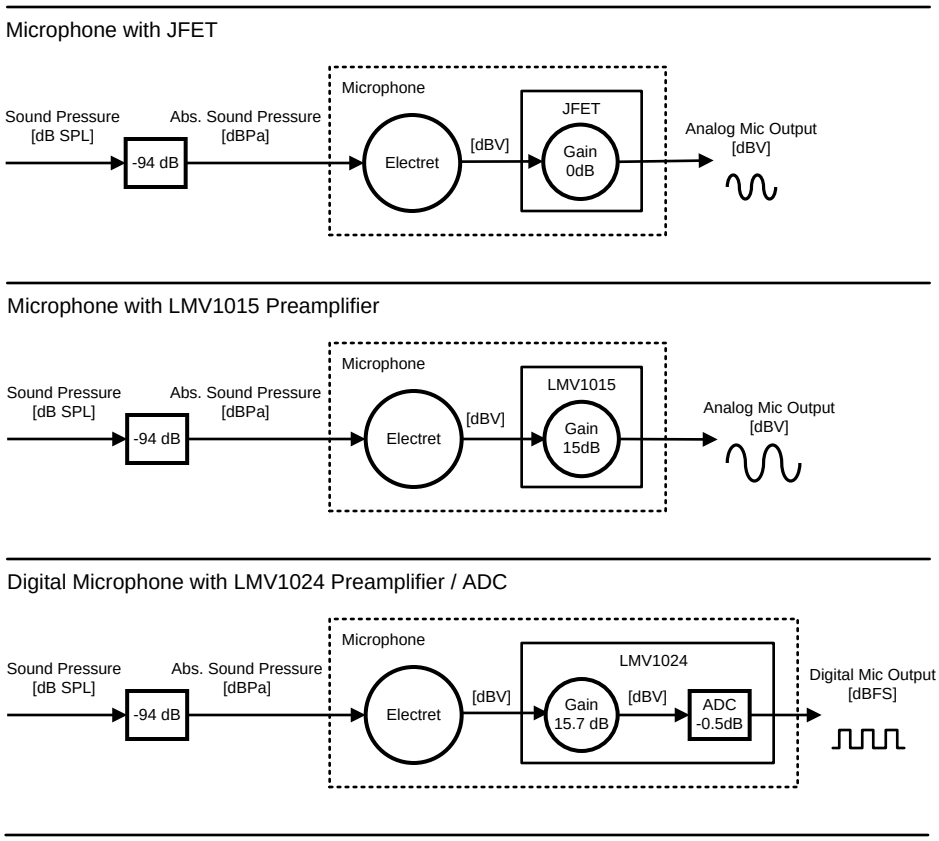

Figure 41. Microphone Sensitivity

Microphone with Additional Gain

When gain is added to the electret element, the analog signal becomes larger and therefore more robust. This can be accomplished by using a pre-amplifier with a higher gain then the JFET. The sensitivity of the microphone consists of the sensitivity of the electret plus the gain of the pre-amplifier. When choosing TI's LMV1015-15 for instance, a gain of 15 dB is added by the pre-amplifier. This results in a sensitivity of −29 dB(V/Pa) with a typical electret element of −44 dB(V/Pa). TI has a wide range of pre-amplifiers with different gain factors, which can be used to replace the JFET inside the microphone canister. Please visit www.ti.com for more information on the LMV1015 and LMV1032 pre-amplifier series. A block diagram with the LMV1015 pre-amplifier inside an ECM is given in Figure 41.

When taking the same example of busy traffic (70 dB SPL), the output voltage of the microphone with the LMV1015 is:

Microphone Output = SP + C + S

where

- SP is the Sound Pressure in dB
- SPLC is the dB SPL to dBPa conversion
- (−94 dB)S is the Sensitivity in dB(V/Pa)
- Microphone output = 70 - 94 - 29 = −53 dBV. (4)

This is equivalent to 6.33 mV_{PP}

The pre-amplifier with additional gain reduces the impact of noise on the wiring / traces from the microphone to the baseband chip significantly. To minimize interference ultimately, an Analog-to-Digital converter is integrated in both the LMV1024/LMV1026, realizing a digital interface between the microphone and the baseband.

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Digital Microphone

By integrating the Analog-to-Digital converter (ADC) in the LMV1024/LMV1026 all analog signals are kept within the “shielded” microphone canister. The output is a digital interface that is robust and insensitive to interference and noise from outside the canister. The output is expressed in dBFS and therefore the sensitivity is also stated in dB(FS/Pa) instead of dB(V/Pa). To calculate the digital output (Data) in dBFS the following equation can be written for the LMV1024/LMV1026:

$$\text{Digital Output} = 10 \text{ LOG} \left[\frac{P_{INPUT}}{P_{REF}} \right] + A$$

where

- P_{REF} is the reference power, which is defined as the maximum allowed input power (Full Scale).
- P_{INPUT} is the applied power on the input pin and “A” is the gain of the pre-amplifier in decibels. (5)

Written into voltages, the equation is:

$$\text{Digital Output} = 20 \text{ LOG} \left[\frac{V_{INPUT}}{V_{REF}} \right] + A \quad (6)$$

Or in decibels:

Digital Output (dBFS) = Input (dBV) - Reference (dB) + A

where

- Input = 20 Log
- V_{INPUT} (V_{RMS})Ref = 20 Log
- V_{REF} (V_{RMS})A is the Gain (dB) (7)

For the LMV1024/LMV1026 the reference voltage V_{REF} is $1.5V_P$ (1.06 V_{RMS}) and the Gain A is 15.7 dB. These parameters are fixed inside the device. Knowing this, Equation 6 can be simplified:

Digital Output (dBFS) = V_{INPUT} (dBV) - 0.5 + 15.7Digital Output (dBFS) = V_{INPUT} (dBV) + 15.2 (8)

The sensitivity of the digital microphone is the sensitivity of a conventional microphone plus the input to output transfer of the LMV1024. The sensitivity of a typical digital microphone is therefore:

−44 + 15.2 = −28.8 dB(FS/Pa). (9)

Digital Output = SP + C + S

where

- SP is the Sound Pressure in dB
- SPLC is the dB SPL to dBPa conversion
- (−94 dB)S is the Sensitivity in dB(V/Pa) (10)

Taking the example of busy traffic (70 dB SPL) again results in the following digital output (dBFS):

Digital Output (dBFS) = SP - C + SDigital Output (dBFS) = 70 - 94 - 28.8 = −52.8 dBFS (11)

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ANALOG-TO-DIGITAL CONVERTER

The ADC used in the LMV1024/LMV1026 is an one bit sigma delta converter with a Pulse Density Modulated output signal (PDM). The output of this ADC can be either High (one) or Low (zero). Assume that the LMV1024/LMV1026 input is at the minimum level. In that case the DATA output will produce almost only “zeros”. When the input increases, the amount of “ones” increases too. At mid-point, where the input is 0V, the number of “zeros” will equal the number of “ones”. At the time that the input approaches the maximum level, the DATA output produces a majority of “ones”. Figure 42 shows the resulting DATA output as function of the input.

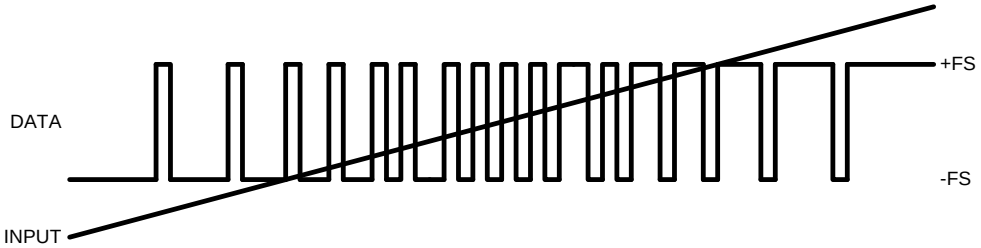

Figure 42. DATA Output versus Input Amplitude

An important characteristic of the sigma delta converter is that the noise is shifted out of the band to frequencies above the band of interest. The band that can be used (Audio Bandwidth) relates directly the applied clock frequency. Table 1 shows the relation between the Clock Frequency and a couple of common Audio Bandwidths.

Table 1. Audio Bandwidth vs. Clock Frequency

Clock Frequency	Audio Bandwidth
408 kHz	3.4 kHz
960 kHz	8 kHz
1.2 MHz	10 kHz
1.92 MHz	16 kHz
2.4 MHz	20 kHz

The high corner of the band of interest (knee) is determined by the clock frequency divided by 2 times the OSR. The factor of two comes from the Nyquist theorem. The over sampling ratio (OSR) of this particular ADC is chosen at 60. This sets the high corner of the band at the clock frequency divided by 120. For instance when a bandwidth of 10 kHz is desired, the clock frequency needs to be 1.2 MHz or higher. Figure 43 depicts the noise shaping effect in a frequency spectrum plot, where a 1 kHz signal is applied.

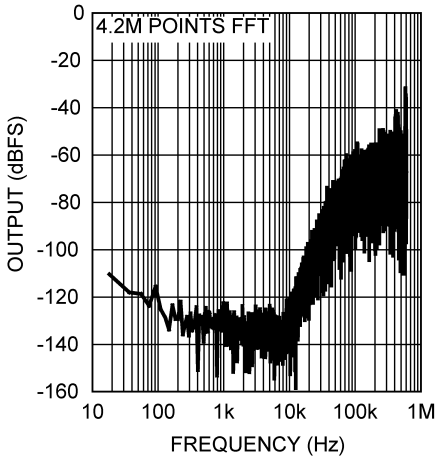

Figure 43. Frequency Spectrum

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To eliminate the noise above the band of interest a low pass decimation filter is implemented in the baseband chip or DSP. The resulting frequency spectrum contains only the frequency components left within the band of interest. Figure 44 depicts the frequency spectrum after filtering.

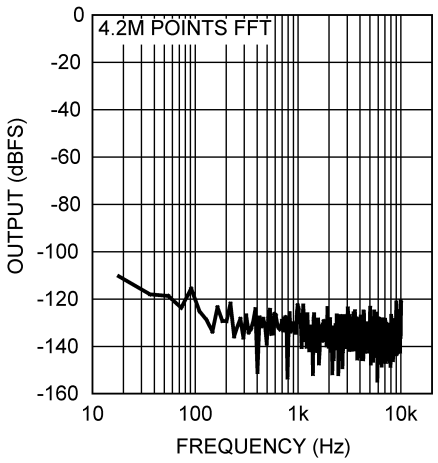

Figure 44. Frequency Spectrum after Filtering

STEREO OPERATION

The LMV1024 and the LMV1026 are designed to operate together in a stereo solution with two microphones. One microphone will have a LMV1024 built-in and the other will have a LMV1026 built-in. These two microphones share the same interface lines to minimize wiring (Figure 45).

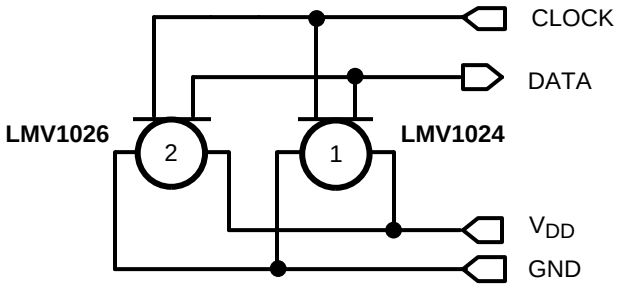

Figure 45. Stereo Application

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Both microphones produce valid data in only one half of a clock cycle to allow the two microphones to operate on the same I/O lines (Data and Clock). To avoid overlap between the drivers of the microphones, one microphone always goes into a high impedance state before the second microphone starts driving the data-line. The LMV1024 is positive edge triggered while the LMV1026 is negative edge triggered. The timing between the two microphones is shown in Figure 46. For exact timing values, please see the Electrical Characteristics table.

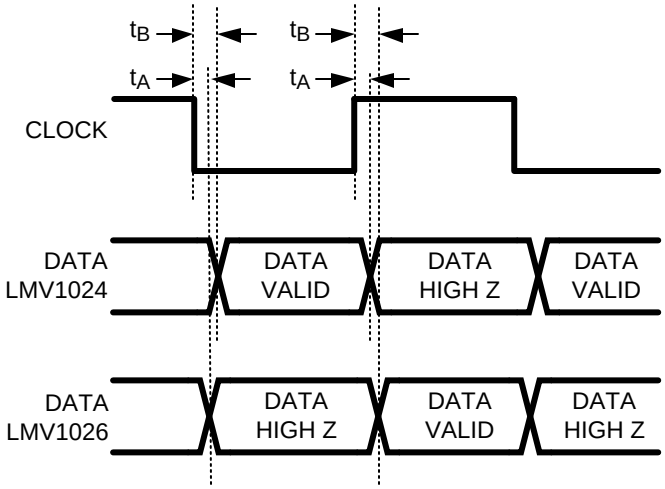

Figure 46. Timing

LAYOUT CONSIDERATIONS

To obtain the best possible performance from the microphone, special care needs to be taken for the design of the PCB. Especially the V_{IN} trace is very sensitive as it is connected to the high impedance electret element. It is essential to isolate and shield the V_{IN} trace as much as possible from the digital signal traces (DATA and CLOCK). This needs to be done to avoid any switching noise coupling directly into the input of the IC. An example of a PCB layout is given in Figure 47. The microphone PCB has two capacitors. One capacitor (100 nF) is connected to the reference pin of the LMV1024/LMV1026. The other capacitor (10 nF) is used as decoupling for high frequencies on the supply. No capacitors should be placed on the data output of the LMV1024/LMV1026 since it will only load the output driver and would degrade the performance. This is opposite to the regular analog phantom biased microphones, where capacitors are needed to improve RFI.

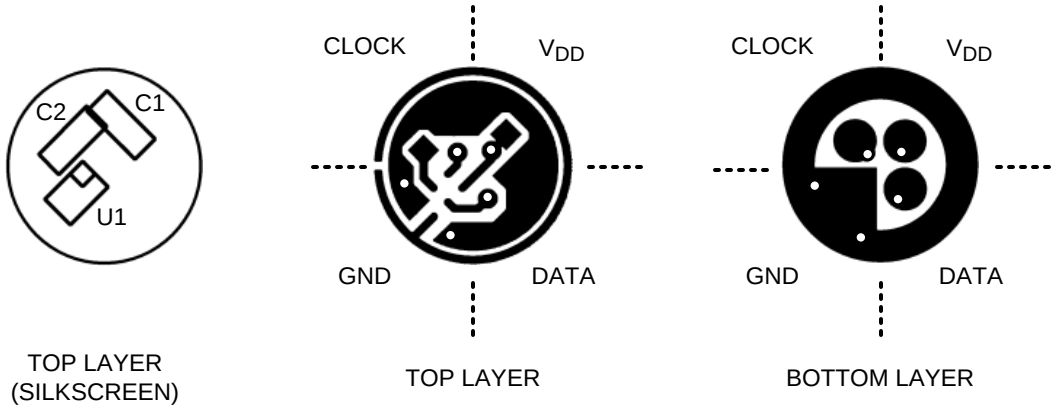

Figure 47. PCB Layout

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REVISION HISTORY

Changes from Revision B (April 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	20

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