ADC128S102 8-Channel, 500 ksps to 1 Msps, 12-Bit A/D Converter

Check for Samples: ADC128S102

FEATURES

- **Eight Input Channels**
- **Variable Power Management**
- **Independent Analog and Digital Supplies**
- **SPI™/ QSPI™/ MICROWIRE™/DSP Compatible**
- **Packaged in 16-Lead TSSOP**

APPLICATIONS

- **Automotive Navigation**
- **Portable Systems**
- **Medical Instruments**
- **Mobile Communications**
- **Instrumentation and Control Systems**

KEY SPECIFICATIONS

- **Conversion Rate 500 ksps to 1 MSPS**
- **DNL (V_A = V_D = 5.0 V) +1.5 / −0.9**
- **LSB (max) INL (V_A = V_D = 5.0 V) ±1.2 LSB (max)**
- **Power Consumption**
  - **3V Supply 2.3 mW (typ)**
  - **5V Supply 10.7 mW (typ)**

DESCRIPTION

The ADC128S102 is a low-power, eight-channel CMOS 12-bit analog-to-digital converter specified for conversion throughput rates of 500 ksps to 1 MSPS. The converter is based on a successive-approximation register architecture with an internal track-and-hold circuit. It can be configured to accept up to eight input signals at inputs IN0 through IN7.

The output serial data is straight binary and is compatible with several standards, such as SPI™, QSPI™, MICROWIRE™, and many common DSP serial interfaces.

The ADC128S102 may be operated with independent analog and digital supplies. The analog supply (V_A) can range from +2.7V to +5.25V, and the digital supply (V_D) can range from +2.7V to V_A. Normal power consumption using a +3V or +5V supply is 2.3 mW and 10.7 mW, respectively. The power-down feature reduces the power consumption to 0.06 µW using a +3V supply and 0.25 µW using a +5V supply.

The ADC128S102 is packaged in a 16-lead TSSOP package. Operation over the extended industrial temperature range of −40°C to +105°C is ensured.

Connection Diagram

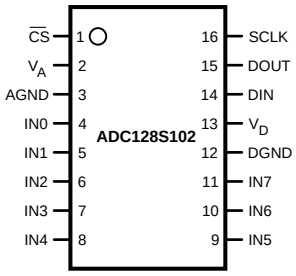
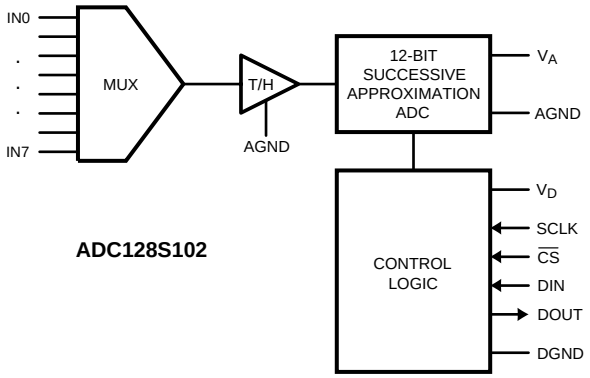


Figure 1. TSSOP Package
See Package Number PW0016A

Block Diagram



Pin Descriptions

Pin No.	Name	Description
ANALOG I/O		
4 - 11	IN0 to IN7	Analog inputs. These signals can range from 0V to V_{REF}.
DIGITAL I/O		
16	SCLK	Digital clock input. The ensured performance range of frequencies for this input is 8 MHz to 16 MHz. This clock directly controls the conversion and readout processes.
15	DOUT	Digital data output. The output samples are clocked out of this pin on the falling edges of the SCLK pin.
14	DIN	Digital data input. The ADC128S102's Control Register is loaded through this pin on rising edges of the SCLK pin.
1	CS	Chip select. On the falling edge of $\overline{CS}$, a conversion process begins. Conversions continue as long as $\overline{CS}$ is held low.
POWER SUPPLY		
2	V_A	Positive analog supply pin. This voltage is also used as the reference voltage. This pin should be connected to a quiet +2.7V to +5.25V source and bypassed to GND with 1 µF and 0.1 µF monolithic ceramic capacitors located within 1 cm of the power pin.
13	V_D	Positive digital supply pin. This pin should be connected to a +2.7V to V_A supply, and bypassed to GND with a 0.1 µF monolithic ceramic capacitor located within 1 cm of the power pin.
3	AGND	The ground return for the analog supply and signals.
12	DGND	The ground return for the digital supply and signals.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

Analog Supply Voltage V_A		−0.3V to 6.5V
Digital Supply Voltage V_D		−0.3V to V_A + 0.3V, max 6.5V
Voltage on Any Pin to GND		−0.3V to V_A +0.3V
Input Current at Any Pin (3)		±10 mA
Package Input Current(3)		±20 mA
Power Dissipation at T_A = 25°C		See (4)
ESD Susceptibility (5)	Human Body Model	2500V
	Machine Model	250V
For soldering specifications: see product folder at www.ti.com and http://www.ti.com/lit/SNOA549		
Junction Temperature		+150°C
Storage Temperature		−65°C to +150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(3) When the input voltage at any pin exceeds the power supplies (that is, V_{IN} < AGND or V_{IN} > V_A or V_D), the current at that pin should be limited to 10 mA. The 20 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 10 mA to two.
(4) The absolute maximum junction temperature ($T_J$max) for this device is 150°C. The maximum allowable power dissipation is dictated by $T_J$max, the junction-to-ambient thermal resistance (θ_{JA}), and the ambient temperature (T_A), and can be calculated using the formula $P_D MAX = (T_J max - T_A)/\theta_{JA}$. In the 16-pin TSSOP, θ_{JA} is 96°C/W, so P_DMAX = 1,200 mW at 25°C and 625 mW at the maximum operating ambient temperature of 105°C. Note that the power consumption of this device under normal operation is a maximum of 12 mW. The values for maximum power dissipation listed above will be reached only when the ADC128S102 is operated in a severe fault condition (e.g. when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Obviously, such conditions should always be avoided.
(5) Human body model is 100 pF capacitor discharged through a 1.5 kΩ resistor. Machine model is 220 pF discharged through ZERO ohms

Operating Ratings (1)(2)

Operating Temperature	−40°C ≤ T_A ≤ +105°C
V_A Supply Voltage	+2.7V to +5.25V
V_D Supply Voltage	+2.7V to V_A
Digital Input Voltage	0V to V_A
Analog Input Voltage	0V to V_A
Clock Frequency	8 MHz to 16 MHz

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) All voltages are measured with respect to GND = 0V, unless otherwise specified.

Package Thermal Resistance

Package	**θ_{JA}**
16-lead TSSOP on 4-layer, 2 oz. PCB	96°C / W

ADC128S102 Converter Electrical Characteristics (1)

The following specifications apply for AGND = DGND = 0V, f_{SCLK} = 8 MHz to 16 MHz, f_{SAMPLE} = 500 ksps to 1 MSPS, C_L = 50pF, unless otherwise noted. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}**: all other limits T_A = 25°C.

Parameter		Test Conditions	Typical	Limits (2)	Units
STATIC CONVERTER CHARACTERISTICS					
	Resolution with No Missing Codes			**12**	Bits
INL	Integral Non-Linearity (End Point Method)	$V_A = V_D$ = +3.0V	±0.4	**±1**	LSB (max)
		$V_A = V_D$ = +5.0V	±0.5	**±1.2**	LSB (max)
DNL	Differential Non-Linearity	$V_A = V_D$ = +3.0V	+0.4	**+0.9**	LSB (max)
			−0.2	**−0.7**	LSB (min)
		$V_A = V_D$ = +5.0V	+0.7	**+1.5**	LSB (max)
			−0.4	**−0.9**	LSB (min)
V_{OFF}	Offset Error	$V_A = V_D$ = +3.0V	+0.8	**±2.3**	LSB (max)
		$V_A = V_D$ = +5.0V	+1.1	**±2.3**	LSB (max)
OEM	Offset Error Match	$V_A = V_D$ = +3.0V	±0.1	**±1.5**	LSB (max)
		$V_A = V_D$ = +5.0V	±0.3	**±1.5**	LSB (max)
FSE	Full Scale Error	$V_A = V_D$ = +3.0V	+0.8	**±2.0**	LSB (max)
		$V_A = V_D$ = +5.0V	+0.3	**±2.0**	LSB (max)
FSEM	Full Scale Error Match	$V_A = V_D$ = +3.0V	±0.1	**±1.5**	LSB (max)
		$V_A = V_D$ = +5.0V	±0.3	**±1.5**	LSB (max)
DYNAMIC CONVERTER CHARACTERISTICS					
FPBW	Full Power Bandwidth (−3dB)	$V_A = V_D$ = +3.0V	8		MHz
		$V_A = V_D$ = +5.0V	11		MHz
SINAD	Signal-to-Noise Plus Distortion Ratio	$V_A = V_D$ = +3.0V, f_{IN} = 40.2 kHz, −0.02 dBFS	73	**70**	dB (min)
		$V_A = V_D$ = +5.0V, f_{IN} = 40.2 kHz, −0.02 dBFS	73	**70**	dB (min)
SNR	Signal-to-Noise Ratio	$V_A = V_D$ = +3.0V, f_{IN} = 40.2 kHz, −0.02 dBFS	73	**70.8**	dB (min)
		$V_A = V_D$ = +5.0V, f_{IN} = 40.2 kHz, −0.02 dBFS	73	**70.8**	dB (min)
THD	Total Harmonic Distortion	$V_A = V_D$ = +3.0V, f_{IN} = 40.2 kHz, −0.02 dBFS	−88	**−74**	dB (max)
		$V_A = V_D$ = +5.0V, f_{IN} = 40.2 kHz, −0.02 dBFS	−90	**−74**	dB (max)
SFDR	Spurious-Free Dynamic Range	$V_A = V_D$ = +3.0V, f_{IN} = 40.2 kHz, −0.02 dBFS	91	**75**	dB (min)
		$V_A = V_D$ = +5.0V, f_{IN} = 40.2 kHz, −0.02 dBFS	92	**75**	dB (min)
ENOB	Effective Number of Bits	$V_A = V_D$ = +3.0V, f_{IN} = 40.2 kHz	11.8	**11.3**	Bits (min)
		$V_A = V_D$ = +5.0V, f_{IN} = 40.2 kHz, −0.02 dBFS	11.8	**11.3**	Bits (min)
ISO	Channel-to-Channel Isolation	$V_A = V_D$ = +3.0V, f_{IN} = 20 kHz	82		dB
		$V_A = V_D$ = +5.0V, f_{IN} = 20 kHz, −0.02 dBFS	84		dB

(1) Data sheet min/max specification limits are ensured by design, test, or statistical analysis.
(2) Tested limits are specified to TI's AOQL (Average Outgoing Quality Level).

ADC128S102 Converter Electrical Characteristics (1) (continued)

The following specifications apply for AGND = DGND = 0V, f_{SCLK} = 8 MHz to 16 MHz, f_{SAMPLE} = 500 ksps to 1 MSPS, C_L = 50pF, unless otherwise noted. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}**: all other limits T_A = 25°C.

Parameter		Test Conditions	Typical	Limits (2)	Units
IMD	Intermodulation Distortion, Second Order Terms	$V_A = V_D$ = +3.0V, f_a = 19.5 kHz, f_b = 20.5 kHz	−89		dB
		$V_A = V_D$ = +5.0V, f_a = 19.5 kHz, f_b = 20.5 kHz	−91		dB
	Intermodulation Distortion, Third Order Terms	$V_A = V_D$ = +3.0V, f_a = 19.5 kHz, f_b = 20.5 kHz	−88		dB
		$V_A = V_D$ = +5.0V, f_a = 19.5 kHz, f_b = 20.5 kHz	−88		dB
ANALOG INPUT CHARACTERISTICS					
V_{IN}	Input Range		0 to V_A		V
I_{DCL}	DC Leakage Current			**±1**	µA (max)
C_{INA}	Input Capacitance	Track Mode	33		pF
		Hold Mode	3		pF
DIGITAL INPUT CHARACTERISTICS					
V_{IH}	Input High Voltage	$V_A = V_D$ = +2.7V to +3.6V		**2.1**	V (min)
		$V_A = V_D$ = +4.75V to +5.25V		**2.4**	V (min)
V_{IL}	Input Low Voltage	$V_A = V_D$ = +2.7V to +5.25V		**0.8**	V (max)
I_{IN}	Input Current	V_{IN} = 0V or V_D	±0.01	**±1**	µA (max)
C_{IND}	Digital Input Capacitance		2	**4**	pF (max)
DIGITAL OUTPUT CHARACTERISTICS					
V_{OH}	Output High Voltage	I_{SOURCE} = 200 µA, $V_A = V_D$ = +2.7V to +5.25V		**V_D − 0.5**	V (min)
V_{OL}	Output Low Voltage	I_{SINK} = 200 µA to 1.0 mA, $V_A = V_D$ = +2.7V to +5.25V		**0.4**	V (max)
I_{OZH}, I_{OZL}	Hi-Impedance Output Leakage Current	$V_A = V_D$ = +2.7V to +5.25V		**±1**	µA (max)
C_{OUT}	Hi-Impedance Output Capacitance (3)		2	**4**	pF (max)
	Output Coding		Straight (Natural) Binary		
POWER SUPPLY CHARACTERISTICS (C_L = 10 pF)					
V_A, V_D	Analog and Digital Supply Voltages	$V_A \geq V_D$		**2.7**	V (min)
				5.25	V (max)
$I_A + I_D$	Total Supply Current Normal Mode ($\overline{CS}$ low)	$V_A = V_D$ = +2.7V to +3.6V, f_{SAMPLE} = 1 MSPS, f_{IN} = 40 kHz	0.76	**1.5**	mA (max)
		$V_A = V_D$ = +4.75V to +5.25V, f_{SAMPLE} = 1 MSPS, f_{IN} = 40 kHz	2.13	**3.1**	mA (max)
	Total Supply Current Shutdown Mode ($\overline{CS}$ high)	$V_A = V_D$ = +2.7V to +3.6V, f_{SCLK} = 0 ksps	20		nA
		$V_A = V_D$ = +4.75V to +5.25V, f_{SCLK} = 0 ksps	50		nA
P_C	Power Consumption Normal Mode ($\overline{CS}$ low)	$V_A = V_D$ = +3.0V f_{SAMPLE} = 1 MSPS, f_{IN} = 40 kHz	2.3	**4.5**	mW (max)
		$V_A = V_D$ = +5.0V f_{SAMPLE} = 1 MSPS, f_{IN} = 40 kHz	10.7	**15.5**	mW (max)
	Power Consumption Shutdown Mode ($\overline{CS}$ high)	$V_A = V_D$ = +3.0V f_{SCLK} = 0 ksps	0.06		µW
		$V_A = V_D$ = +5.0V f_{SCLK} = 0 ksps	0.25		µW

(3) Data sheet min/max specification limits are ensured by design, test, or statistical analysis.

ADC128S102 Converter Electrical Characteristics (1) (continued)

The following specifications apply for AGND = DGND = 0V, f_{SCLK} = 8 MHz to 16 MHz, f_{SAMPLE} = 500 ksps to 1 MSPS, C_L = 50pF, unless otherwise noted. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}**: all other limits T_A = 25°C.

Parameter		Test Conditions	Typical	Limits (2)	Units
AC ELECTRICAL CHARACTERISTICS					
f_{SCLK}MIN	Minimum Clock Frequency	$V_A = V_D$ = +2.7V to +5.25V	0.8	**8**	MHz (min)
f_{SCLK}	Maximum Clock Frequency	$V_A = V_D$ = +2.7V to +5.25V		**16**	MHz (max)
f_S	Sample Rate Continuous Mode	$V_A = V_D$ = +2.7V to +5.25V	50	**500**	ksps (min)
				1	MSPS (max)
$t_{CONVERT}$	Conversion (Hold) Time	$V_A = V_D$ = +2.7V to +5.25V		**13**	SCLK cycles
DC	SCLK Duty Cycle	$V_A = V_D$ = +2.7V to +5.25V	30	**40**	% (min)
			70	**60**	% (max)
t_{ACQ}	Acquisition (Track) Time	$V_A = V_D$ = +2.7V to +5.25V		**3**	SCLK cycles
	Throughput Time	Acquisition Time + Conversion Time $V_A = V_D$ = +2.7V to +5.25V		**16**	SCLK cycles
t_{AD}	Aperture Delay	$V_A = V_D$ = +2.7V to +5.25V	4		ns

ADC128S102 Timing Specifications

The following specifications apply for $V_A = V_D$ = +2.7V to +5.25V, AGND = DGND = 0V, f_{SCLK} = 8 MHz to 16 MHz, f_{SAMPLE} = 500 ksps to 1 MSPS, and C_L = 50pF. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}**: all other limits T_A = 25°C.

Parameter		Test Conditions	Typical	Limits (1)	Units
t_{CSH}	$\overline{CS}$ Hold Time after SCLK Rising Edge		0	**10**	ns (min)
t_{CSS}	$\overline{CS}$ Setup Time prior to SCLK Rising Edge		4.5	**10**	ns (min)
t_{EN}	$\overline{CS}$ Falling Edge to DOUT enabled		5	**30**	ns (max)
t_{DACC}	DOUT Access Time after SCLK Falling Edge		17	**27**	ns (max)
t_{DHLD}	DOUT Hold Time after SCLK Falling Edge		4		ns (typ)
t_{DS}	DIN Setup Time prior to SCLK Rising Edge		3	**10**	ns (min)
t_{DH}	DIN Hold Time after SCLK Rising Edge		3	**10**	ns (min)
t_{CH}	SCLK High Time			**0.4 x t_{SCLK}**	ns (min)
t_{CL}	SCLK Low Time			**0.4 x t_{SCLK}**	ns (min)
t_{DIS}	$\overline{CS}$ Rising Edge to DOUT High-Impedance	DOUT falling	2.4	**20**	ns (max)
		DOUT rising	0.9	**20**	ns (max)

(1) Tested limits are specified to TI's AOQL (Average Outgoing Quality Level).

TIMING DIAGRAMS

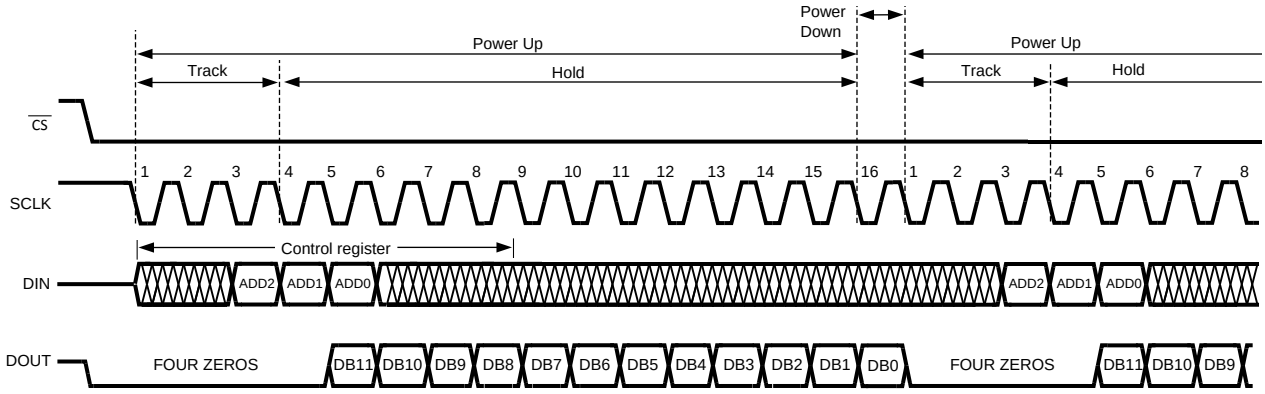


Figure 2. ADC128S102 Operational Timing Diagram

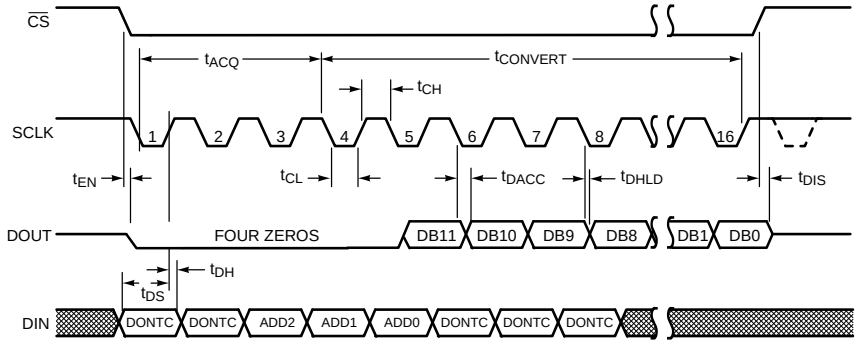


Figure 3. ADC128S102 Serial Timing Diagram

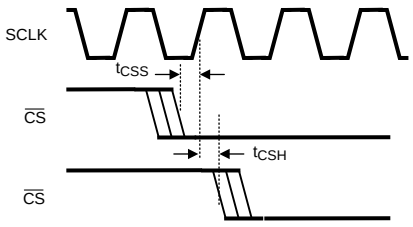


Figure 4. SCLK and $\overline{CS}$ Timing Parameters

Specification Definitions

ACQUISITION TIME is the time required for the ADC to acquire the input voltage. During this time, the hold capacitor is charged by the input voltage.

APERTURE DELAY is the time between the fourth falling edge of SCLK and the time when the input signal is internally acquired or held for conversion.

CONVERSION TIME is the time required, after the input voltage is acquired, for the ADC to convert the input voltage to a digital word.

CHANNEL-TO-CHANNEL ISOLATION is resistance to coupling of energy from one channel into another channel.

CROSSTALK is the coupling of energy from one channel into another channel. This is similar to Channel-to-Channel Isolation, except for the sign of the data.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB.

DUTY CYCLE is the ratio of the time that a repetitive digital waveform is high to the total time of one period. The specification here refers to the SCLK.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and Distortion or SINAD. ENOB is defined as (SINAD - 1.76) / 6.02 and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

FULL POWER BANDWIDTH is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input.

FULL SCALE ERROR (FSE) is a measure of how far the last code transition is from the ideal 1½ LSB below V_{REF^+} and is defined as:

$$V_{FSE} = V_{max} + 1.5\ LSB - V_{REF^+} \quad (1)$$

where V_{max} is the voltage at which the transition to the maximum code occurs. FSE can be expressed in Volts, LSB or percent of full scale range.

GAIN ERROR is the deviation of the last code transition (111...110) to (111...111) from the ideal (V_{REF} - 1.5 LSB), after adjusting for offset error.

INTEGRAL NON-LINEARITY (INL) is a measure of the deviation of each individual code from a line drawn from negative full scale (½ LSB below the first code transition) through positive full scale (½ LSB above the last code transition). The deviation of any given code from this straight line is measured from the center of that code value.

INTERMODULATION DISTORTION (IMD) is the creation of additional spectral components as a result of two sinusoidal frequencies being applied to an individual ADC input at the same time. It is defined as the ratio of the power in both the second or the third order intermodulation products to the power in one of the original frequencies. Second order products are $f_a \pm f_b$, where f_a and f_b are the two sine wave input frequencies. Third order products are ($2f_a \pm f_b$) and ($f_a \pm 2f_b$). IMD is usually expressed in dB.

MISSING CODES are those output codes that will never appear at the ADC outputs. These codes cannot be reached with any input value. The ADC128S102 is ensured not to have any missing codes.

OFFSET ERROR is the deviation of the first code transition (000...000) to (000...001) from the ideal (i.e. GND + 0.5 LSB).

SIGNAL TO NOISE RATIO (SNR) is the ratio, expressed in dB, of the rms value of the input signal to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including d.c. or the harmonics included in THD.

SIGNAL TO NOISE PLUS DISTORTION (S/N+D or SINAD) Is the ratio, expressed in dB, of the rms value of the input signal to the rms value of all of the other spectral components below half the clock frequency, including harmonics but excluding d.c.

SPURIOUS FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the desired signal amplitude to the amplitude of the peak spurious spectral component, where a spurious spectral component is any signal present in the output spectrum that is not present at the input and may or may not be a harmonic.

TOTAL HARMONIC DISTORTION (THD) is the ratio, expressed in dBc, of the rms total of the first five harmonic components at the output to the rms level of the input signal frequency as seen at the output. THD is calculated as:

$$THD = 20 \bullet \log_{10} \sqrt{\frac{A_{f2}^2 + \cdots + A_{f10}^2}{A_{f1}^2}} \quad (2)$$

where A_{f1} is the RMS power of the input frequency at the output and A_{f2} through A_{f10} are the RMS power in the first 9 harmonic frequencies.

THROUGHPUT TIME is the minimum time required between the start of two successive conversions. It is the acquisition time plus the conversion and read out times. In the case of the ADC128S102, this is 16 SCLK periods.

Typical Performance Characteristics

T_A = +25°C, f_{SAMPLE} = 1 MSPS, f_{SCLK} = 16 MHz, f_{IN} = 40.2 kHz unless otherwise stated.

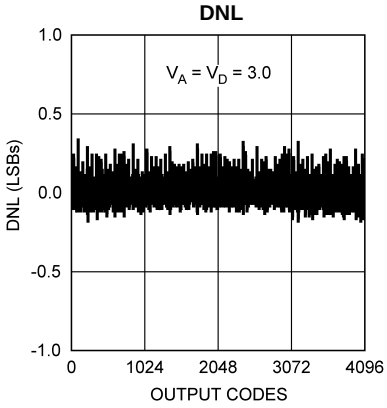


Figure 5.

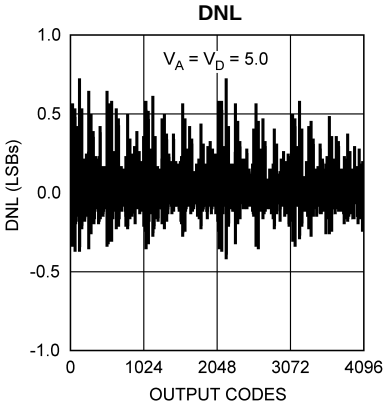


Figure 6.

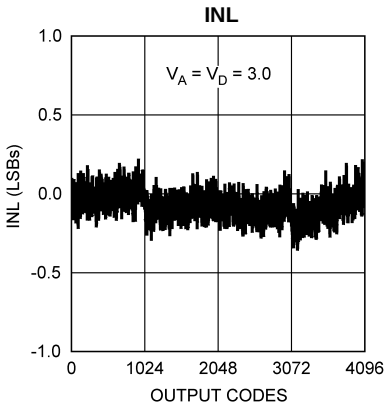


Figure 7.

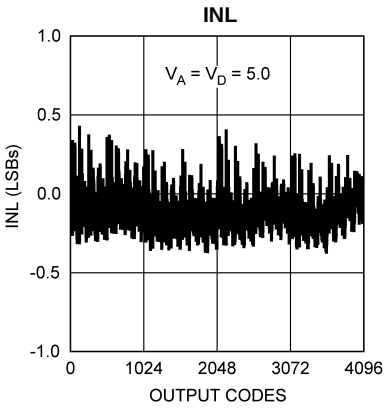


Figure 8.

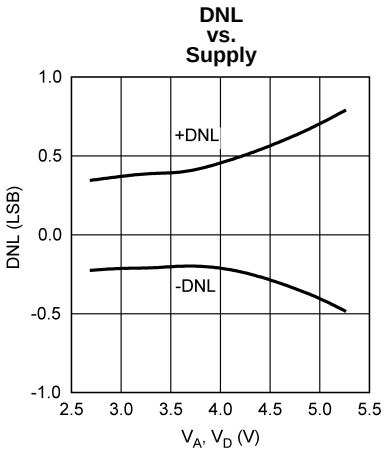


Figure 9.

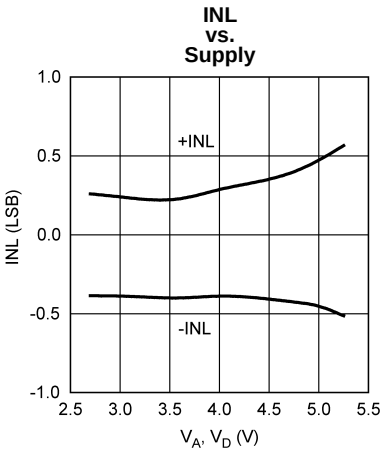


Figure 10.

Typical Performance Characteristics (continued)

T_A = +25°C, f_{SAMPLE} = 1 MSPS, f_{SCLK} = 16 MHz, f_{IN} = 40.2 kHz unless otherwise stated.

SNR vs. Supply

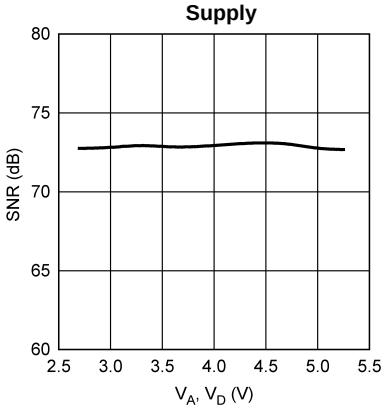


Figure 11.

THD vs. Supply

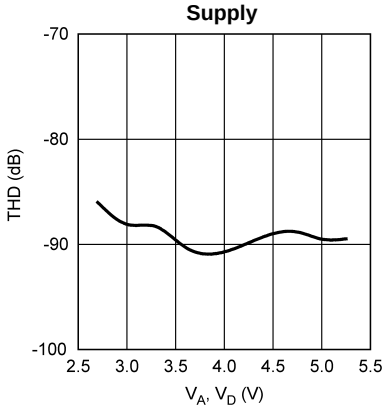


Figure 12.

ENOB vs. Supply

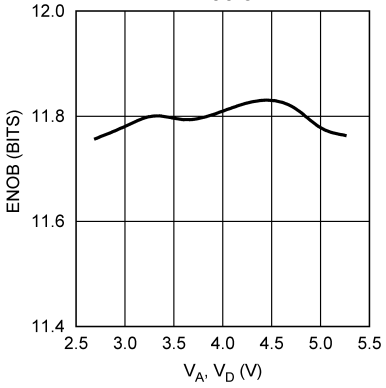


Figure 13.

DNL vs. V_D with V_A = 5.0 V

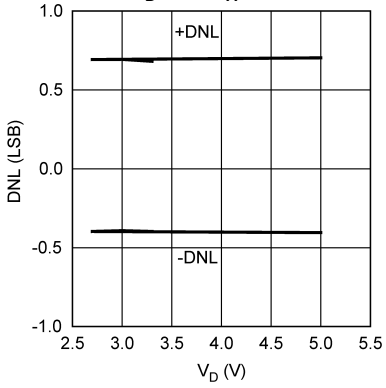


Figure 14.

INL vs. V_D with V_A = 5.0 V

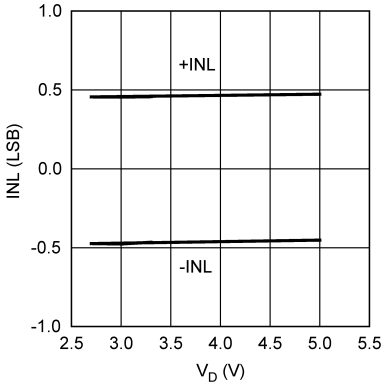


Figure 15.

DNL vs. SCLK Duty Cycle

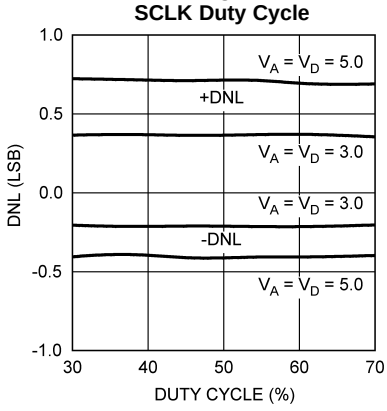


Figure 16.

Typical Performance Characteristics (continued)

T_A = +25°C, f_{SAMPLE} = 1 MSPS, f_{SCLK} = 16 MHz, f_{IN} = 40.2 kHz unless otherwise stated.

INL vs. SCLK Duty Cycle

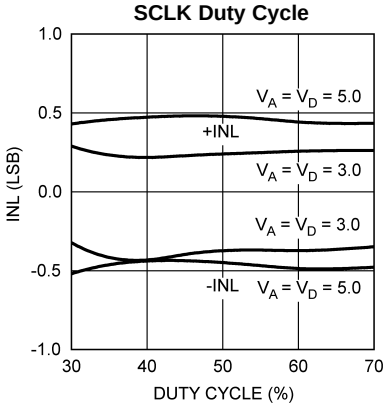


Figure 17.

SNR vs. SCLK Duty Cycle

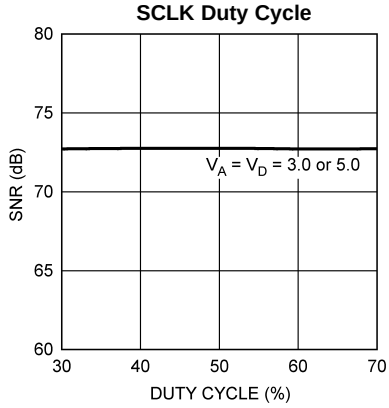


Figure 18.

THD vs. SCLK Duty Cycle

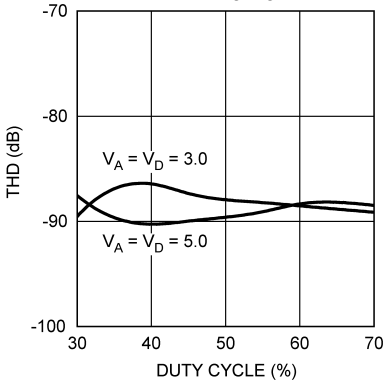


Figure 19.

ENOB vs. SCLK Duty Cycle

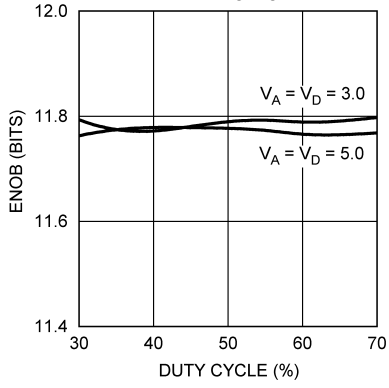


Figure 20.

DNL vs. SCLK

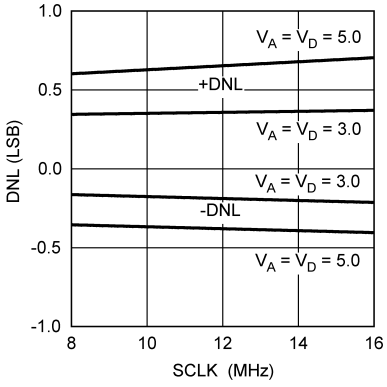


Figure 21.

INL vs. SCLK

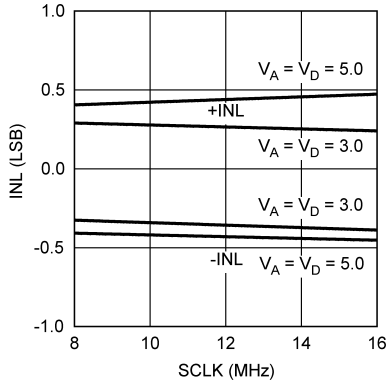


Figure 22.

Typical Performance Characteristics (continued)

T_A = +25°C, f_{SAMPLE} = 1 MSPS, f_{SCLK} = 16 MHz, f_{IN} = 40.2 kHz unless otherwise stated.

SNR vs. SCLK

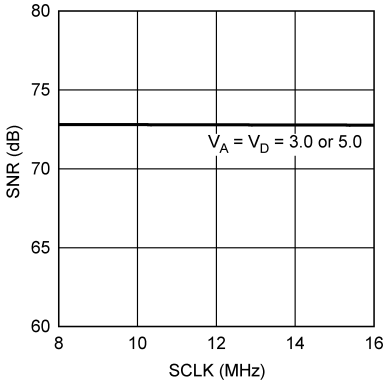


Figure 23.

THD vs. SCLK

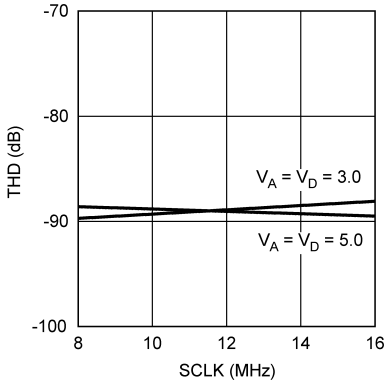


Figure 24.

ENOB vs. SCLK

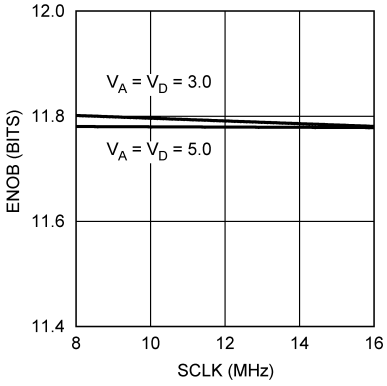


Figure 25.

DNL vs. Temperature

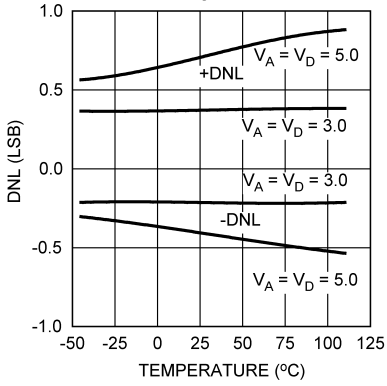


Figure 26.

INL vs. Temperature

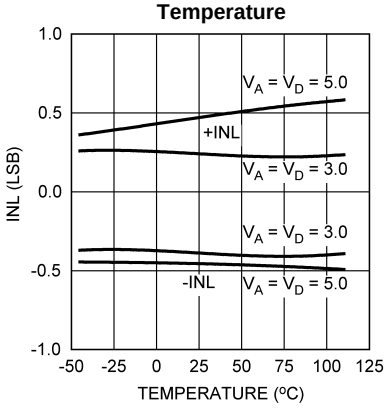


Figure 27.

SNR vs. Temperature

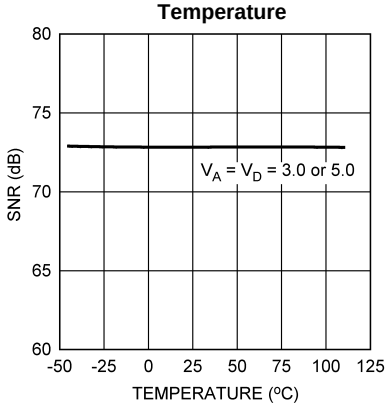


Figure 28.

Typical Performance Characteristics (continued)

T_A = +25°C, f_{SAMPLE} = 1 MSPS, f_{SCLK} = 16 MHz, f_{IN} = 40.2 kHz unless otherwise stated.

THD vs. Temperature

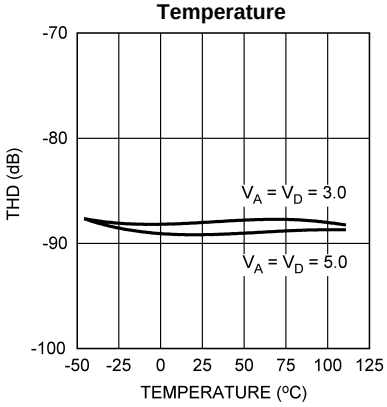


Figure 29.

ENOB vs. Temperature

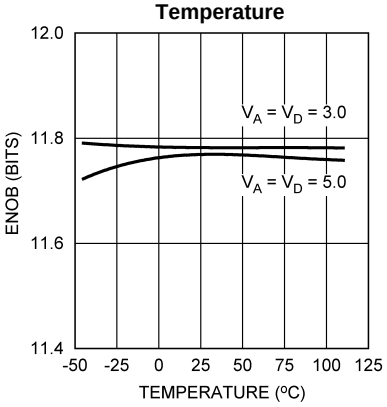


Figure 30.

SNR vs. Input Frequency

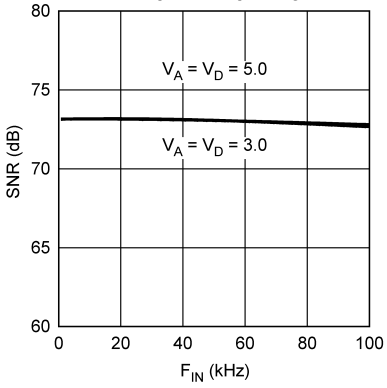


Figure 31.

THD vs. Input Frequency

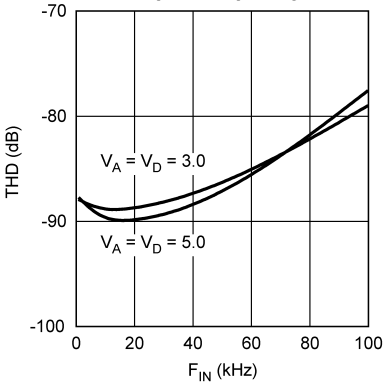


Figure 32.

ENOB vs. Input Frequency

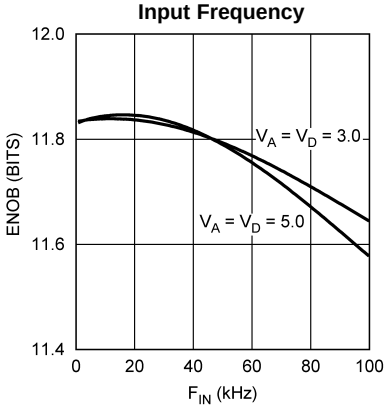


Figure 33.

Power Consumption vs. SCLK

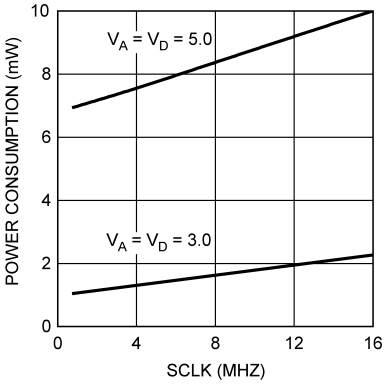


Figure 34.

FUNCTIONAL DESCRIPTION

The ADC128S102 is a successive-approximation analog-to-digital converter designed around a charge-redistribution digital-to-analog converter.

ADC128S102 OPERATION

Simplified schematics of the ADC128S102 in both track and hold operation are shown in Figure 35 and Figure 36 respectively. In Figure 35, the ADC128S102 is in track mode: switch SW1 connects the sampling capacitor to one of eight analog input channels through the multiplexer, and SW2 balances the comparator inputs. The ADC128S102 is in this state for the first three SCLK cycles after $\overline{CS}$ is brought low.

Figure 36 shows the ADC128S102 in hold mode: switch SW1 connects the sampling capacitor to ground, maintaining the sampled voltage, and switch SW2 unbalances the comparator. The control logic then instructs the charge-redistribution DAC to add or subtract fixed amounts of charge to or from the sampling capacitor until the comparator is balanced. When the comparator is balanced, the digital word supplied to the DAC is the digital representation of the analog input voltage. The ADC128S102 is in this state for the last thirteen SCLK cycles after $\overline{CS}$ is brought low.

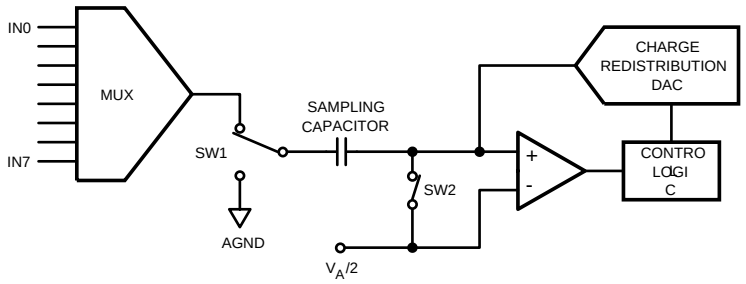


Figure 35. ADC128S102 in Track Mode

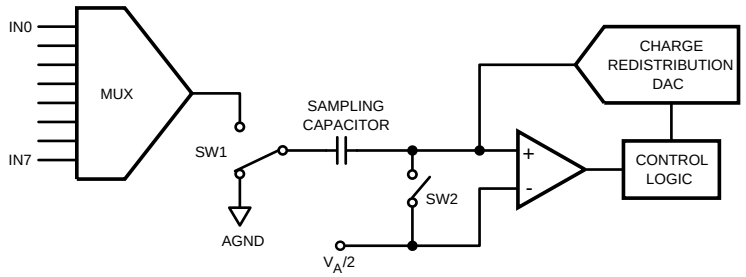


Figure 36. ADC128S102 in Hold Mode

SERIAL INTERFACE

An operational timing diagram and a serial interface timing diagram for the ADC128S102 are shown in the Timing Diagrams section. $\overline{CS}$, chip select, initiates conversions and frames the serial data transfers. SCLK (serial clock) controls both the conversion process and the timing of serial data. DOUT is the serial data output pin, where a conversion result is sent as a serial data stream, MSB first. Data to be written to the ADC128S102's Control Register is placed on DIN, the serial data input pin. New data is written to DIN with each conversion.

A serial frame is initiated on the falling edge of $\overline{CS}$ and ends on the rising edge of $\overline{CS}$. Each frame must contain an integer multiple of 16 rising SCLK edges. The ADC's DOUT pin is in a high impedance state when $\overline{CS}$ is high and is active when $\overline{CS}$ is low. Thus, $\overline{CS}$ acts as an output enable. Similarly, SCLK is internally gated off when $\overline{CS}$ is brought high.

During the first 3 cycles of SCLK, the ADC is in the track mode, acquiring the input voltage. For the next 13 SCLK cycles the conversion is accomplished and the data is clocked out. SCLK falling edges 1 through 4 clock out leading zeros while falling edges 5 through 16 clock out the conversion result, MSB first. If there is more than one conversion in a frame (continuous conversion mode), the ADC will re-enter the track mode on the falling edge of SCLK after the N*16th rising edge of SCLK and re-enter the hold/convert mode on the N*16+4th falling edge of SCLK. "N" is an integer value.

The ADC128S102 enters track mode under three different conditions. In Figure 2, $\overline{CS}$ goes low with SCLK high and the ADC enters track mode on the first falling edge of SCLK. In the second condition, $\overline{CS}$ goes low with SCLK low. Under this condition, the ADC automatically enters track mode and the falling edge of $\overline{CS}$ is seen as the first falling edge of SCLK. In the third condition, $\overline{CS}$ and SCLK go low simultaneously and the ADC enters track mode. While there is no timing restriction with respect to the rising edges of $\overline{CS}$ and SCLK, see Figure 4 for setup and hold time requirements for the falling edge of $\overline{CS}$ with respect to the rising edge of SCLK.

While a conversion is in progress, the address of the next input for conversion is clocked into a control register through the DIN pin on the first 8 rising edges of SCLK after the fall of $\overline{CS}$. See Table 1, Table 2, and Table 3.

There is no need to incorporate a power-up delay or dummy conversions as the ADC128S102 is able to acquire the input signal to full resolution in the first conversion immediately following power-up. The first conversion result after power-up will be that of IN0.

Table 1. Control Register Bits

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DONTC	**DONTC**	**ADD2**	**ADD1**	**ADD0**	**DONTC**	**DONTC**	**DONTC**

Table 2. Control Register Bit Descriptions

Bit No:	Symbol:	Description
7, 6, 2, 1, 0	DONTC	Don't care. The values of these bits do not affect the device.
5	ADD2	These three bits determine which input channel will be sampled and converted at the next conversion cycle. The mapping between codes and channels is shown in Table 3.
4	ADD1	
3	ADD0	

Table 3. Input Channel Selection

ADD2	ADD1	ADD0	Input Channel
0	0	0	IN0 (Default)
0	0	1	IN1
0	1	0	IN2
0	1	1	IN3
1	0	0	IN4
1	0	1	IN5
1	1	0	IN6
1	1	1	IN7

ADC128S102 TRANSFER FUNCTION

The output format of the ADC128S102 is straight binary. Code transitions occur midway between successive integer LSB values. The LSB width for the ADC128S102 is V_A / 4096. The ideal transfer characteristic is shown in Figure 37. The transition from an output code of 0000 0000 0000 to a code of 0000 0000 0001 is at 1/2 LSB, or a voltage of V_A / 8192. Other code transitions occur at steps of one LSB.

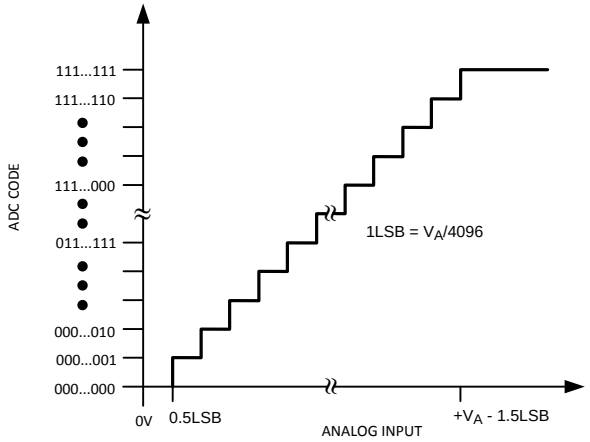


Figure 37. Ideal Transfer Characteristic

ANALOG INPUTS

An equivalent circuit for one of the ADC128S102's input channels is shown in Figure 38. Diodes D1 and D2 provide ESD protection for the analog inputs. The operating range for the analog inputs is 0 V to V_A. Going beyond this range will cause the ESD diodes to conduct and result in erratic operation.

The capacitor C1 in Figure 38 has a typical value of 3 pF and is mainly the package pin capacitance. Resistor R1 is the on resistance of the multiplexer and track / hold switch and is typically 500 ohms. Capacitor C2 is the ADC128S102 sampling capacitor, and is typically 30 pF. The ADC128S102 will deliver best performance when driven by a low-impedance source (less than 100 ohms). This is especially important when using the ADC128S102 to sample dynamic signals. Also important when sampling dynamic signals is a band-pass or low-pass filter which reduces harmonics and noise in the input. These filters are often referred to as anti-aliasing filters.

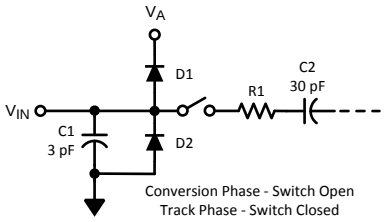


Figure 38. Equivalent Input Circuit

DIGITAL INPUTS AND OUTPUTS

The ADC128S102's digital inputs (SCLK, $\overline{CS}$, and DIN) have an operating range of 0 V to V_A. They are not prone to latch-up and may be asserted before the digital supply (V_D) without any risk. The digital output (DOUT) operating range is controlled by V_D. The output high voltage is V_D - 0.5V (min) while the output low voltage is 0.4V (max).

Applications Information

TYPICAL APPLICATION CIRCUIT

A typical application is shown in Figure 39. The split analog and digital supply pins are both powered in this example by the TI LP2950 low-dropout voltage regulator. The analog supply is bypassed with a capacitor network located close to the ADC128S102. The digital supply is separated from the analog supply by an isolation resistor and bypassed with additional capacitors. The ADC128S102 uses the analog supply (V_A) as its reference voltage, so it is very important that V_A be kept as clean as possible. Due to the low power requirements of the ADC128S102, it is also possible to use a precision reference as a power supply.

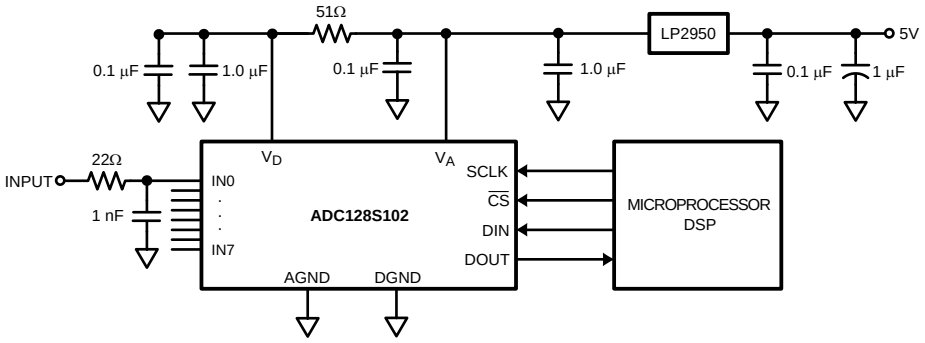


Figure 39. Typical Application Circuit

POWER SUPPLY CONSIDERATIONS

There are three major power supply concerns with this product: power supply sequencing, power management, and the effect of digital supply noise on the analog supply.

Power Supply Sequence

The ADC128S102 is a dual-supply device. The two supply pins share ESD resources, so care must be exercised to ensure that the power is applied in the correct sequence. To avoid turning on the ESD diodes, the digital supply (V_D) cannot exceed the analog supply (V_A) by more than 300 mV. Therefore, V_A must ramp up before or concurrently with V_D.

Power Management

The ADC128S102 is fully powered-up whenever $\overline{CS}$ is low and fully powered-down whenever $\overline{CS}$ is high, with one exception. If operating in continuous conversion mode, the ADC128S102 automatically enters power-down mode between SCLK's 16th falling edge of a conversion and SCLK's 1st falling edge of the subsequent conversion (see Figure 2).

In continuous conversion mode, the ADC128S102 can perform multiple conversions back to back. Each conversion requires 16 SCLK cycles and the ADC128S102 will perform conversions continuously as long as $\overline{CS}$ is held low. Continuous mode offers maximum throughput.

In burst mode, the user may trade off throughput for power consumption by performing fewer conversions per unit time. This means spending more time in power-down mode and less time in normal mode. By utilizing this technique, the user can achieve very low sample rates while still utilizing an SCLK frequency within the electrical specifications. The Power Consumption vs. SCLK curve in the Typical Performance Characteristics section shows the typical power consumption of the ADC128S102. To calculate the power consumption (P_C), simply multiply the fraction of time spent in the normal mode (t_N) by the normal mode power consumption (P_N), and add the fraction of time spent in shutdown mode (t_S) multiplied by the shutdown mode power consumption (P_S) as shown in Equation 3.

$$P_C = \frac{t_N}{t_N + t_S} \times P_N + \frac{t_S}{t_N + t_S} \times P_S \quad (3)$$

Power Supply Noise Considerations

The charging of any output load capacitance requires current from the digital supply, V_D. The current pulses required from the supply to charge the output capacitance will cause voltage variations on the digital supply. If these variations are large enough, they could degrade SNR and SINAD performance of the ADC. Furthermore, if the analog and digital supplies are tied directly together, the noise on the digital supply will be coupled directly into the analog supply, causing greater performance degradation than would noise on the digital supply alone. Similarly, discharging the output capacitance when the digital output goes from a logic high to a logic low will dump current into the die substrate, which is resistive. Load discharge currents will cause "ground bounce" noise in the substrate that will degrade noise performance if that current is large enough. The larger the output capacitance, the more current flows through the die substrate and the greater the noise coupled into the analog channel.

The first solution to keeping digital noise out of the analog supply is to decouple the analog and digital supplies from each other or use separate supplies for them. To keep noise out of the digital supply, keep the output load capacitance as small as practical. If the load capacitance is greater than 50 pF, use a 100 Ω series resistor at the ADC output, located as close to the ADC output pin as practical. This will limit the charge and discharge current of the output capacitance and improve noise performance. Since the series resistor and the load capacitance form a low frequency pole, verify signal integrity once the series resistor has been added.

LAYOUT AND GROUNDING

Capacitive coupling between the noisy digital circuitry and the sensitive analog circuitry can lead to poor performance. The solution is to keep the analog circuitry separated from the digital circuitry and the clock line as short as possible.

Digital circuits create substantial supply and ground current transients. The logic noise generated could have significant impact upon system noise performance. To avoid performance degradation of the ADC128S102 due to supply noise, do not use the same supply for the ADC128S102 that is used for digital logic.

Generally, analog and digital lines should cross each other at 90° to avoid crosstalk. However, to maximize accuracy in high resolution systems, avoid crossing analog and digital lines altogether. It is important to keep clock lines as short as possible and isolated from ALL other lines, including other digital lines. In addition, the clock line should also be treated as a transmission line and be properly terminated.

The analog input should be isolated from noisy signal traces to avoid coupling of spurious signals into the input. Any external component (e.g., a filter capacitor) connected between the converter's input pins and ground or to the reference input pin and ground should be connected to a very clean point in the ground plane.

We recommend the use of a single, uniform ground plane and the use of split power planes. The power planes should be located within the same board layer. All analog circuitry (input amplifiers, filters, reference components, etc.) should be placed over the analog power plane. All digital circuitry and I/O lines should be placed over the digital power plane. Furthermore, all components in the reference circuitry and the input signal chain that are connected to ground should be connected together with short traces and enter the analog ground plane at a single, quiet point.

REVISION HISTORY

Changes from Revision D (March 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	18

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
ADC128S102CIMT	ACTIVE	TSSOP	PW	16	92	TBD	Call TI	Call TI	-40 to 105	128S102 CIMT	Samples
ADC128S102CIMT/NOPB	ACTIVE	TSSOP	PW	16	92	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 105	128S102 CIMT	Samples
ADC128S102CIMTX	ACTIVE	TSSOP	PW	16	2500	TBD	Call TI	Call TI	-40 to 105	128S102 CIMT	Samples
ADC128S102CIMTX/NOPB	ACTIVE	TSSOP	PW	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 105	128S102 CIMT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

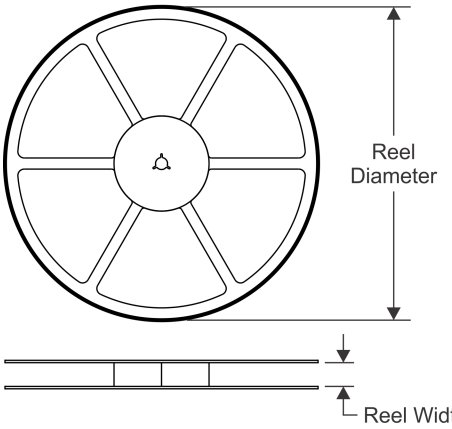
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

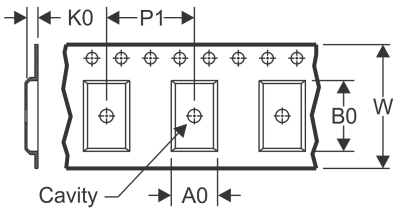
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

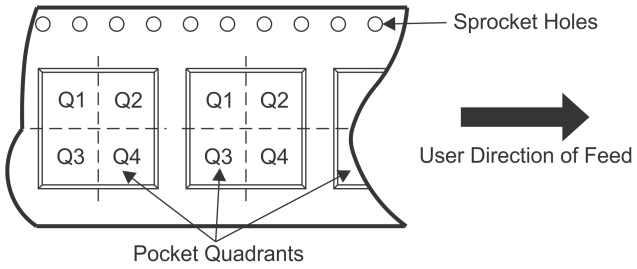


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

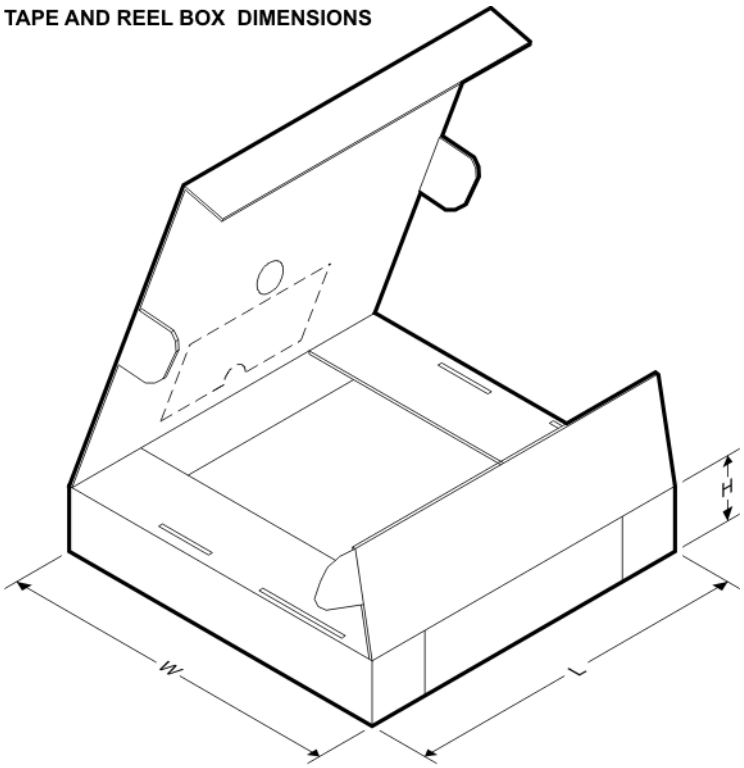
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADC128S102CIMTX	TSSOP	PW	16	2500	330.0	12.4	6.95	8.3	1.6	8.0	12.0	Q1
ADC128S102CIMTX/NOPB	TSSOP	PW	16	2500	330.0	12.4	6.95	8.3	1.6	8.0	12.0	Q1

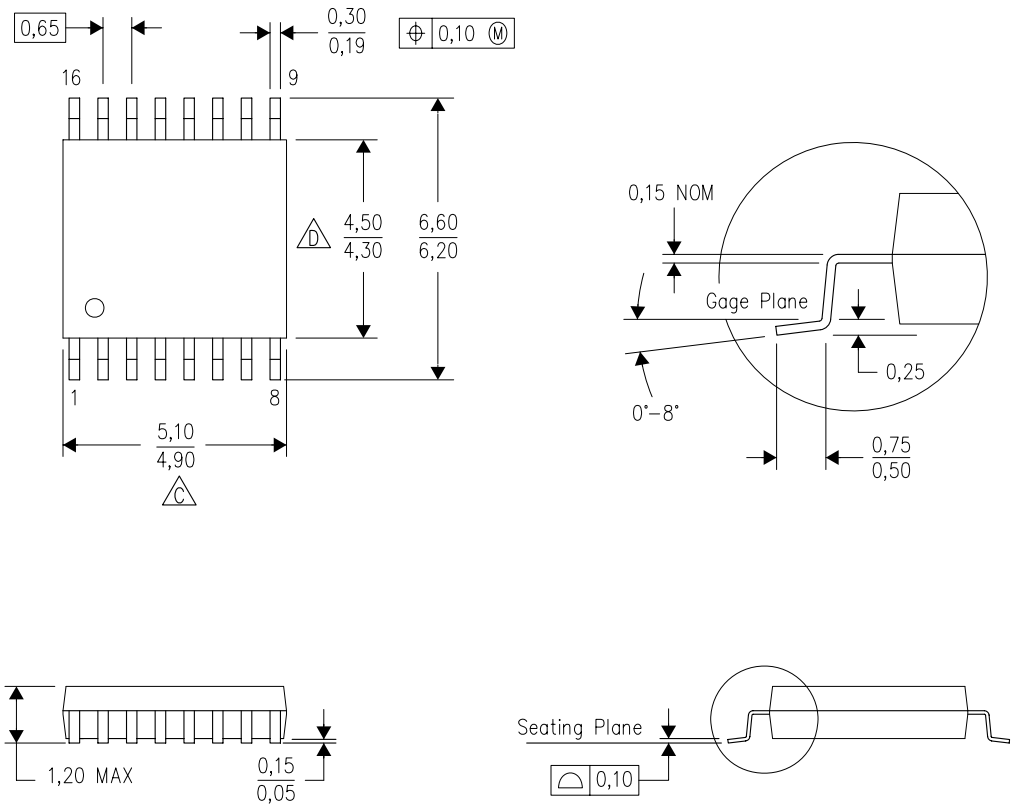
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADC128S102CIMTX	TSSOP	PW	16	2500	349.0	337.0	45.0
ADC128S102CIMTX/NOPB	TSSOP	PW	16	2500	349.0	337.0	45.0

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



4040064–4/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265