LM48560 Boomer™ Audio Power Amplifier Series High Voltage Class H Ceramic Speaker Driver with Automatic Level Control

Check for Samples: LM48560

FEATURES

- **Class H Topology**
- **Integrated Boost Converter**
- **Bridge-Tied Load (BTL) Output**
- **Selectable Differential Inputs**
- **Selectable Control Interfaces**
  - **(Hardware or Software mode)**
- **I^2C Programmable ALC**
- **Low Supply Current**
- **Minimum External Components**
- **Micro-Power Shutdown**
- **Available in Space-Saving DSBGA Package**

APPLICATIONS

- **Touch screen Smart Phones**
- **Tablet PCs**
- **Portable Electronic Devices**
- **MP3 Players**

KEY SPECIFICATIONS

- **Output Voltage at V_{DD} = 3.6V, R_L = 1.5µF+10Ω, THD+N ≤ 1%**
  - **$30V_{P-P}$ (Typ)**
- **Quiescent Power Supply Current at 3.6V (ALC Enabled)**
  - **4mA (Typ)**
- **Power Dissipation at $25V_{P-P}$, 1W (Typ)**
- **Shutdown Current, 0.1µA (Typ)**

DESCRIPTION

The LM48560 is a high voltage, high efficiency, Class H driver for ceramic speakers and piezo actuators. The LM48560's Class H architecture offers significant power savings compared to traditional Class AB amplifiers. The device provides $30V_{P-P}$ output drive while consuming just 4mA of quiescent current from a 3.6V supply.

The LM48560 features TI's unique automatic level control (ALC) that provides output limiter functionality. The LM48560 features two fully differential inputs with separate gain settings, and a selectable control interface. In software control mode, the gain control and device modes are configured through the I^2C interface. In hardware control mode, the gain and input mux are configured through a pair of logic inputs.

The LM48560 has a low power shutdown mode that reduces quiescent current consumption to 0.1µA. The LM48560 is a available in an ultra-small 16–bump DSBGA package (1.97mm x 1.97mm).

Typical Application

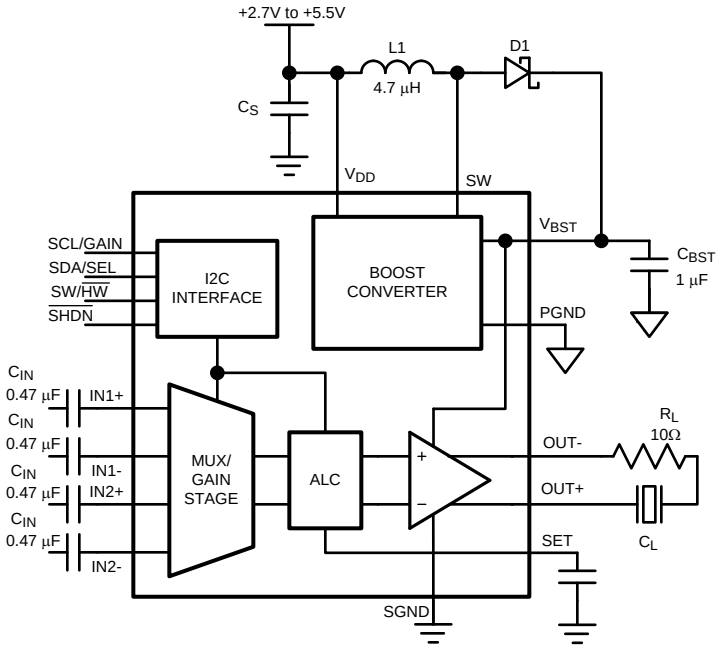


Figure 1. Typical Application Circuit

Connection Diagram

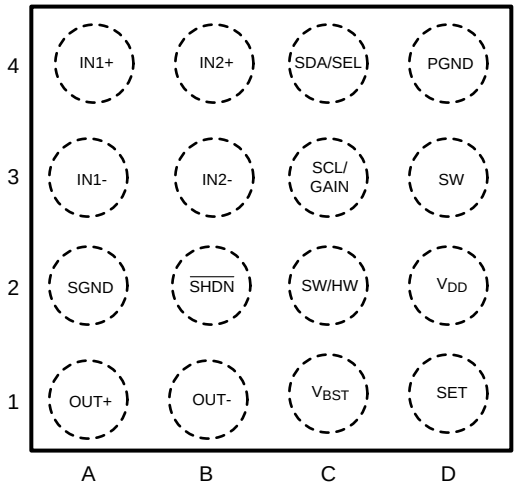


Figure 2. DSBGA Package
1.97mm x 1.97mm x 0.6mm
Top View
See Package Number YZR0016

BUMP DESCRIPTIONS

Bump	Name	Description
A1	OUT+	Amplifier Non-Inverting Output
A2	SGND	Amplifier Ground
A3	IN1–	Amplifier Inverting Input 1
A4	IN1+	Amplifier Non-Inverting Input 1
B1	OUT-	Amplifier Inverting Output
B2	$\overline{SHDN}$	Active Low Shutdown. Connect $\overline{SHDN}$ to GND to disable device. Connect $\overline{SHDN}$ to V_{DD} for normal operation
B3	IN2–	Amplifier Inverting Input 2
B4	IN2+	Amplifier Non-Inverting Input 2
C1	V_{BST}	Boost Converter Output
C2	SW/$\overline{HW}$	Mode Selection Control: SW/$\overline{HW}$ = 0 → Hardware Mode SW/$\overline{HW}$ = 1 → Software Mode
C3	SCL/GAIN	I^2C Serial Clock Input (Software Mode) Gain Select Input (Hardware Mode) see (Table 2)
C4	SDA/SEL	I^2C Serial Data Input (Software Mode) Amplifier Input Select (Hardware Mode) see (Table 2)
D1	SET	ALC Timing Input
D2	V_{DD}	Power Supply
D3	SW	Boost Converter Switching Node
D4	PGND	Boost Converter Ground

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

Supply Voltage(1)		6V
SW Voltage		25V
V_{BST} Voltage		21V
Input Voltage		−0.3V to V_{DD} + 0.3V
Power Dissipation(3)		Internally limited
ESD Rating, Human Body Model(4)		2kV
ESD Rating	Machine Model(5)	100V
	Charge Device Model(6)	500V
Storage Temperature		−65°C to + 150°C
Junction Temperature		150°C
Thermal Resistance	θ_{JA} (TLA16Z1A)	55 °C/W
Soldering Information	See AN-1112 (SNVA009) "DSBGA Wafer Level Chip Scale Package."	

(1) "*Absolute Maximum Ratings*" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the *Absolute Maximum Ratings* or other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. The *Recommended Operating Conditions* indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.

(2) The *Electrical Characteristics* tables list ensured specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics Conditions* and/or Notes. Typical specifications are estimations only and are not ensured.

(3) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$ or the given in *Absolute Maximum Ratings*, whichever is lower.

(4) Human body model, applicable std. JESD22-A114C.

(5) Machine model, applicable std. JESD22-A115-A.

(6) Charge device model, applicable std. JESD22-C101-C.

Operating Ratings

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$	$-40°C \le T_A \le +85°C$
Supply Voltage	V_{DD}	$2.7V \le V_{DD} \le 5.5V$

Electrical Characteristics V_{DD} = 3.6V(1)(2)

The following specifications apply for R_L = 1.5µF + 10Ω, C_{BST} = 1µF, C_{IN} = 0.47µF, C_{SET} = 100nF, A_V = 24dB unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM48560			Units (Limits)
			Min (3)	Typ (4)	Max (3)	
V_{DD}	Supply Voltage Range		2.7		5.5	V
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, R_L = ∞				
		ALC Enabled		4	6	mA
		ALC Disabled		3.6		mA
P_D	Power Consumption	V_{OUT} = 25V_{P-P}, f = 1kHz		1		W
I_{SD}	Shutdown Current	Software Mode		2.5	4.4	µA
		Hardware Mode		0.1	2	µA
T_{WU}	Wake-up Time	From Shutdown		15		ms
V_{OS}	Differential Output Offset Voltage	A_V = 24V		10	90	mV
		A_V = 0dB (Boost Disabled)		5	20	mV
A_V	Gain (Hardware Mode)	IN1 GAIN = 0 GAIN = 1	 0.5 5.5	 0 6	 0.5 6.5	 dB dB
		IN2 GAIN = 0 GAIN = 1	 23.5 29.5	 24 30	 24.5 30.5	 dB dB
	Gain (Software Mode)	Boost Disabled GAIN1 = 0, GAIN0 = 0 GAIN1 = 0, GAIN0 = 1 GAIN1 = 1, GAIN0 = 0 GAIN1 = 1, GAIN0 = 1	 –0.5 5.5 11.5 17.5	 0 6 12 18	 0.5 6.5 12.5 18.5	 dB dB dB dB
		Boost Enabled GAIN1 = 0, GAIN0 = 0 GAIN1 = 0, GAIN0 = 1 GAIN1 = 1, GAIN0 = 0 GAIN1 = 1, GAIN0 = 1	 20.5 23.5 26.5 29.5	 21 24 27 30	 21.5 24.5 27.5 30.5	 dB dB dB dB
	Gain Step Size (Software Mode)			3		dB
R_{IN}	Input Resistance	A_V = 0dB A_V = 30dB	46 46	50 50	58 58	kΩ kΩ
V_{OUT}	Output Voltage	THD+N = 1%				
		f = 200Hz f = 1kHz	 25	30 30		V_{P-P} V_{P-P}
THD+N	Total Harmonic Distortion + Noise	V_{OUT} = 18V_{P-P}, f = 1kHz		0.08		%
PSRR	Power Supply Rejection Ratio (Figure 3)	V_{DD} = 3.6V + 200mV_{P-P} sine, Inputs = AC GND				
		f_{RIPPLE} = 217Hz	55	78		dB
		f_{RIPPLE} = 1kHz		76		dB

(1) "*Absolute Maximum Ratings*" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the *Absolute Maximum Ratings* or other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. The *Recommended Operating Conditions* indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.

(2) The *Electrical Characteristics* tables list ensured specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics Conditions* and/or Notes. Typical specifications are estimations only and are not ensured.

(3) Datasheet min/max specification limits are ensured by design, test, or statistical analysis.

(4) Typical values represent most likely parametric norms at T_A = +25ºC, and at the *Recommended Operation Conditions* at the time of product characterization and are not ensured.

Electrical Characteristics V_{DD} = 3.6V[1][2] (continued)

The following specifications apply for R_L = 1.5µF + 10Ω, C_{BST} = 1µF, C_{IN} = 0.47µF, C_{SET} = 100nF, A_V = 24dB unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM48560			Units (Limits)
			Min (3)	Typ (4)	Max (3)	
CMRR	Common Mode Rejection Ratio (Figure 4)	V_{CM} = 200mV_{P-P} sine				
		f_{RIPPLE} = 217Hz		68		dB
		f_{RIPPLE} = 1kHz		78		dB
SNR	Signal-to-Noise-Ratio	Boost Disabled, A-weighted		107		dB
		Boost Enabled A-weighted		98		dB
ε_{OS}	Output Noise	A-weighted A_V = 24dB A_V = 0dB (Boost Disabled)		134 16		μV_{RMS} μV_{RMS}
T_A	Attack Time	ATK1:ATK0 = 00, C_{SET} = 100nF		0.83		ms
T_R	Release time	RLT1:RLT0 = 00, C_{SET} = 100nF		0.5		s
f_{SW}	Boost Converter Switching Frequency			2		MHz
I_{LIMIT}	Boost Converter Current Limit			1.5		A
V_{IH}	Logic High Input Threshold	$\overline{SHDN}$	1.4			V
V_{IL}	Logic Low Input Threshold	$\overline{SHDN}$			0.5	V
I_{IN}	Input Leakage Current	$\overline{SHDN}$		0.1	0.2	µA

I^2C Interface Characteristics[1][2]

The following specifications apply for R_{PU} = 1kΩ to V_{DD}, SW/$\overline{HW}$ = 1 (Software Mode) unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM48560			Units (Limits)
			Min (3)	Typ (4)	Max (3)	
V_{IH}	Logic Input High Threshold	SDA, SCL	1.1			V
V_{IL}	Logic Input Low Threshold	SDA, SCL			0.5	V
	SCL Frequency				400	kHz
t_1	SCL Period		2.5			µs
t_2	SDA Setup Time		250			ns
t_3	SDA Stable Time		250			ns
t_4	Start Condition Time		250			ns
t_5	Stop Condition Time		250			ns

(1) "*Absolute Maximum Ratings*" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the *Absolute Maximum Ratings* or other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. The *Recommended Operating Conditions* indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.

(2) The *Electrical Characteristics* tables list ensured specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics Conditions* and/or Notes. Typical specifications are estimations only and are not ensured.

(3) Typical values represent most likely parametric norms at T_A = +25ºC, and at the *Recommended Operation Conditions* at the time of product characterization and are not ensured.

(4) Charge device model, applicable std. JESD22-C101-C.

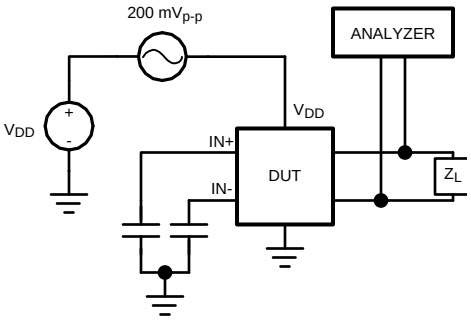


Figure 3. PSRR Test Circuit

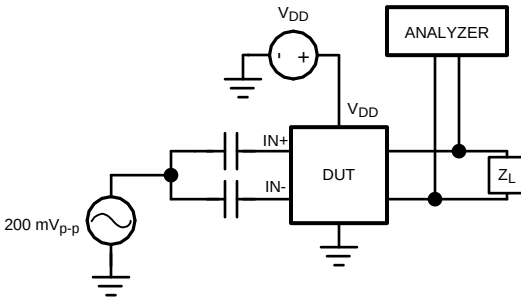


Figure 4. CMRR Test Circuit

Typical Performance Characteristics

All typical performance curves are taken with conditions seen in Figure 1 (Typical Application Circuit), unless otherwise specified.

THD+N vs FREQUENCY
C_L = 0.6µF, V_{DD} = 3.6V, Boosted, A_V = 24dB

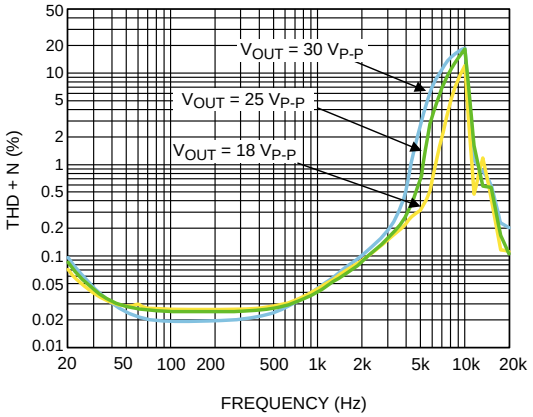


Figure 5.

THD+N vs FREQUENCY
C_L = 1.0µF, V_{DD} = 3.6V, Boosted, A_V = 24dB

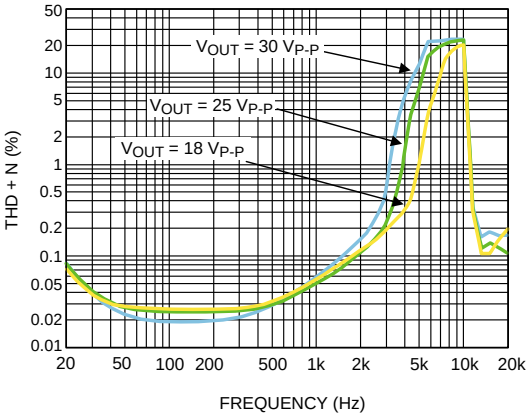


Figure 6.

THD+N vs FREQUENCY
C_L = 1.5µF, V_{DD} = 3.6V, Boosted, A_V = 24dB

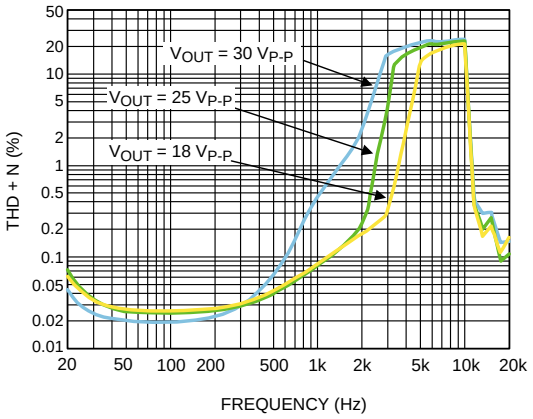


Figure 7.

THD+N vs FREQUENCY
V_{DD} = 3.6V, C_L = 0.6µF, V_{OUT} = 5V_{P-P}
Unboosted, A_V = 0dB

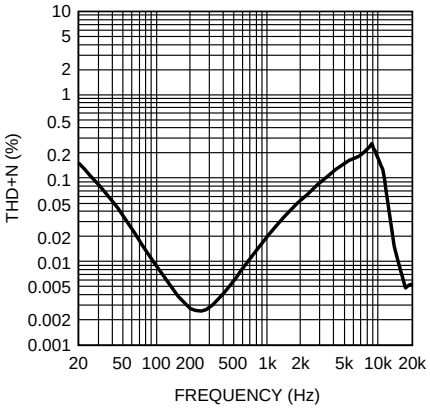


Figure 8.

THD+N vs FREQUENCY
V_{DD} = 3.6V, C_L = 1µF, V_{OUT} = 5V_{P-P}
Unboosted , A_V = 0dB

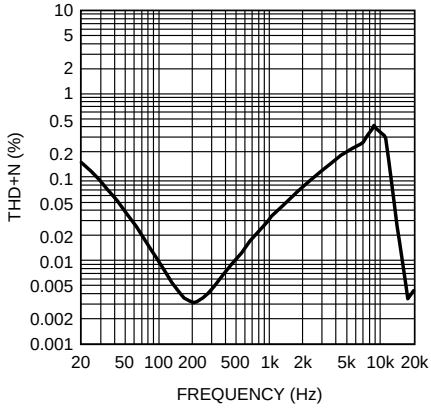


Figure 9.

THD+N vs FREQUENCY
V_{DD} = 3.6V, C_L = 1.5µF, V_{OUT} = 5V_{P-P}
Unboosted, A_V = 0dB

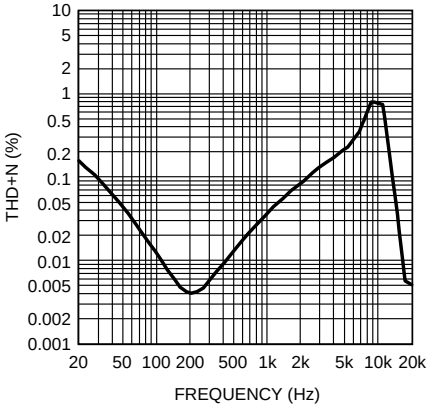


Figure 10.

Typical Performance Characteristics (continued)

All typical performance curves are taken with conditions seen in Figure 1 (Typical Application Circuit), unless otherwise specified.

OUTPUT VOLTAGE vs FREQUENCY
C_L = 1.5µF, THD+N ≤ 1%, Boosted

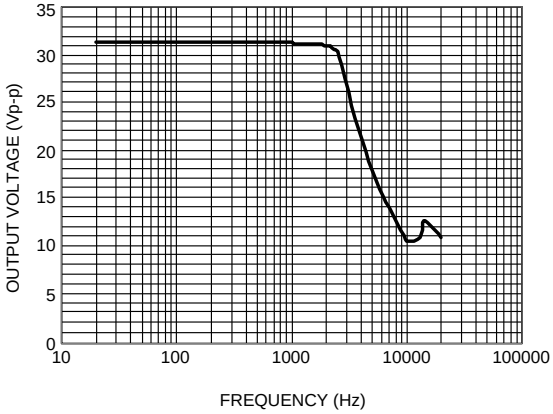


Figure 11.

OUTPUT VOLTAGE vs FREQUENCY
C_L = 1.5µF, THD+N ≤ 1%, Unboosted

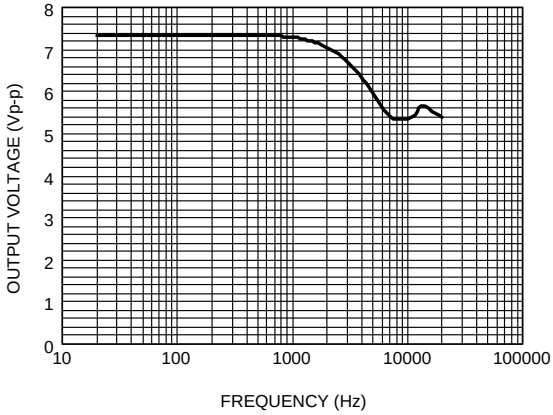


Figure 12.

THD+N vs OUTPUT VOLTAGE
C_L = 0.6µF, V_{DD} = 3.6V, Boosted, A_V = 24dB

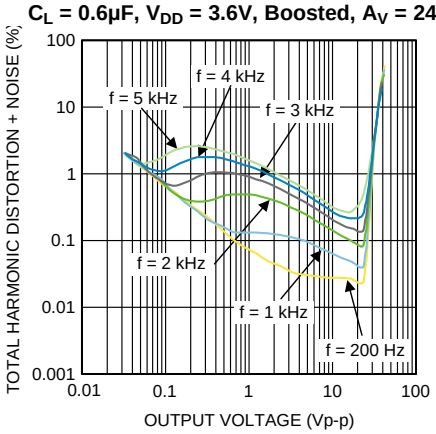


Figure 13.

THD+N vs OUTPUT VOLTAGE
C_L = 1.0µF, V_{DD} = 3.6V, Boosted, A_V = 24dB

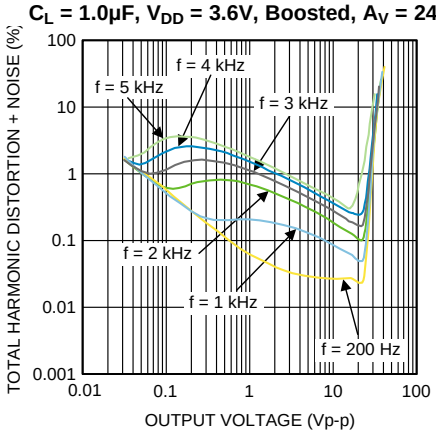


Figure 14.

THD+N vs OUTPUT VOLTAGE
C_L = 1.5µF, V_{DD} = 3.6V, Boosted, A_V = 24dB

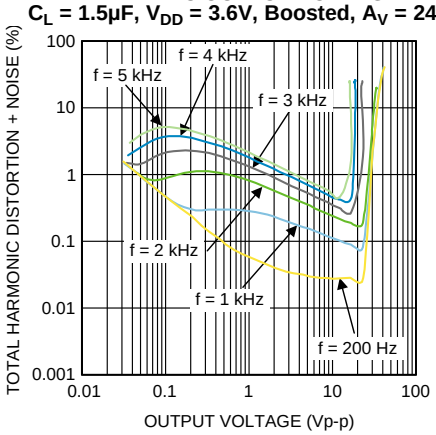


Figure 15.

THD+N vs OUTPUT VOLTAGE
C_L = 1.5µF, V_{DD} = 3.6V, Unboosted, A_V = 0dB

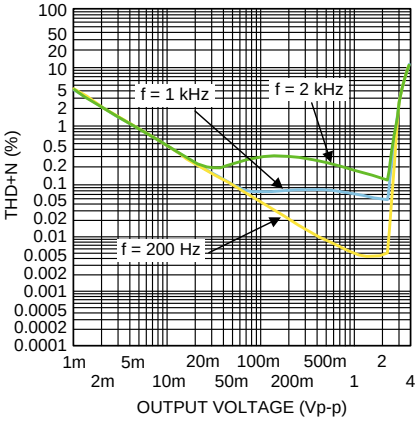


Figure 16.

Typical Performance Characteristics (continued)

All typical performance curves are taken with conditions seen in Figure 1 (Typical Application Circuit), unless otherwise specified.

INPUT VOLTAGE vs OUTPUT VOLTAGE
ALC Enabled, A_V = 21dB, V_{DD} = 3.6V

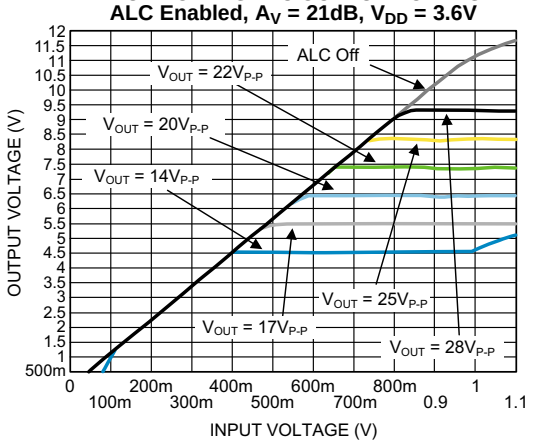


Figure 17.

SUPPLY CURRENT vs SUPPLY VOLTAGE
R_L = ∞

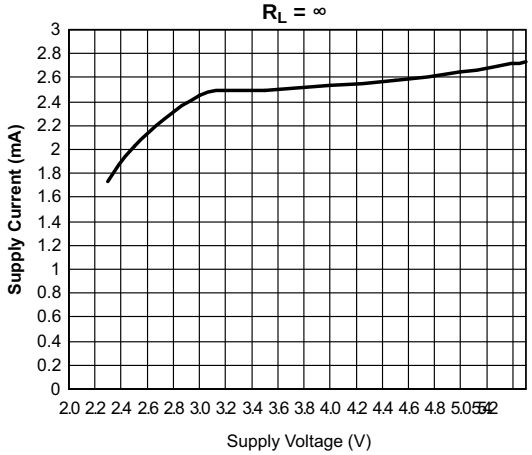


Figure 18.

TOTAL POWER CONSUMPTION vs OUTPUT VOLTAGE
V_{DD} = 3.6V, C_L = 0.6µF

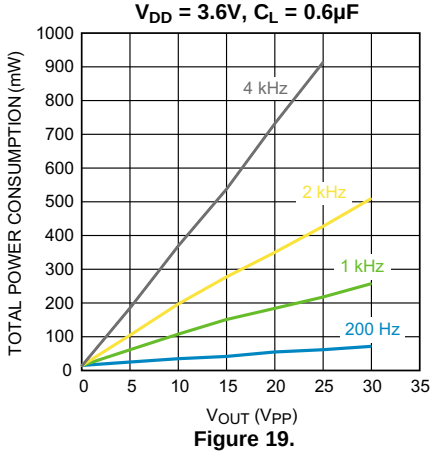


Figure 19.

TOTAL POWER CONSUMPTION vs OUTPUT VOLTAGE
V_{DD} = 3.6V, C_L = 1.0µF

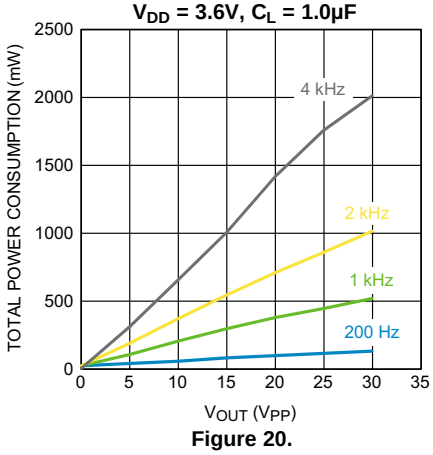


Figure 20.

TOTAL POWER CONSUMPTION vs OUTPUT VOLTAGE
V_{DD} = 3.6V, C_L = 1.5µF

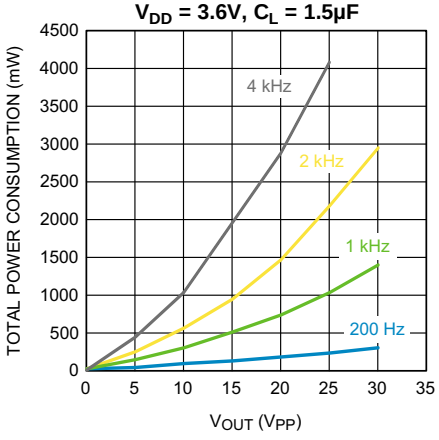


Figure 21.

COMMON MODE REJECTION RATIO vs FREQUENCY
V_{CM}= 200mV$_{P-P}$, C_{IN} = 10µF, V_{DD} = 3.6V, C_L = 1.5µF

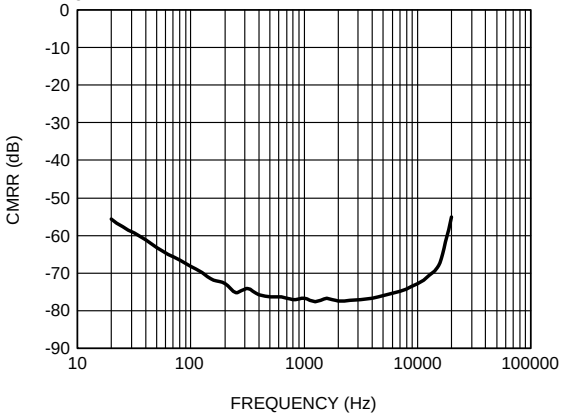


Figure 22.

Typical Performance Characteristics (continued)

All typical performance curves are taken with conditions seen in Figure 1 (Typical Application Circuit), unless otherwise specified.

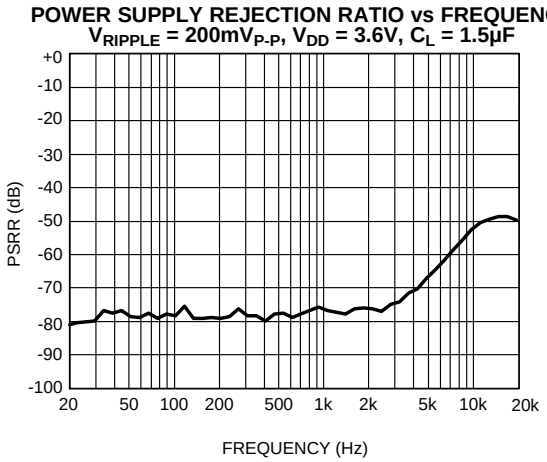


Figure 23.

APPLICATION INFORMATION

READ/WRITE I²C COMPATIBLE INTERFACE

The LM48560 is controlled through an I²C compatible serial interface that consists of a serial data line (SDA) and a serial clock (SCL). The clock line is uni-directional. The data line is bi-directional (open drain). The LM48560 and the master can communicate at clock rates up to 400kHz. Figure 24 shows the I²C interface timing diagram. Data on the SDA line must be stable during the HIGH period of SCL. The LM48560 is a transmit/receive slave-only device, reliant upon the master to generate the SCL signal. Each transmission sequence is framed by a START condition and a STOP condition Figure 25. Each data word, device address and data, transmitted over the bus is 8 bits long and is always followed by an acknowledge pulse Figure 26. The LM48560 device address is 1101111.

I²C BUS FORMAT

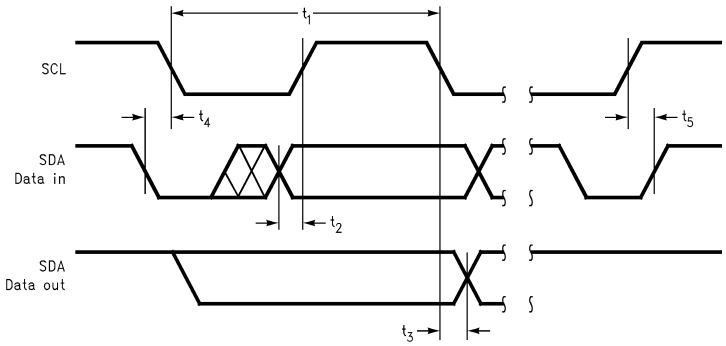


Figure 24. I²C Timing Diagram

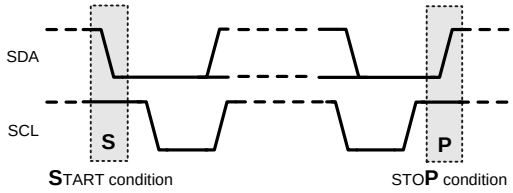


Figure 25. Start and Stop Diagram

WRITE SEQUENCE

The example write sequence is shown in Figure 26. The START signal, the transition of SDA from HIGH to LOW while SDA is HIGH, is generated, altering all devices on the bus that a device address is being written to the bus.

The 7-bit device address is written to the bus, most significant bit (MSB) first, followed by the R/$\overline{W}$ bit (R/$\overline{W}$ = 0 indicating the master is writing to the LM48560). The data is latched in on the rising edge of the clock. Each address bit must be stable while SDA is HIGH. After the R/$\overline{W}$ bit is transmitted, the master device releases SDA, during which time, an acknowledge clock pulse is generated by the slave device. If the LM48560 receives the correct address, the device pulls the SDA line low, generating and acknowledge bit (ACK).

Once the master device registers the ACK bit, the 8-bit register address word is sent, MSB first. Each data bit should be stable while SCL is HIGH. After the 8-bit register address is sent, the LM48560 sends another ACK bit. Upon receipt of the acknowledge, the 8-bit register data is sent, MSB first. The register data word is followed by an ACK, upon receipt of which, the master issues a STOP bit, allowing SDA to go high while SDA is high.

Figure 26. Example I²C Write Cycle

READ SEQUENCE

The example read sequence is shown in Figure 27. The START signal, the transition of SDA from HIGH to LOW while SDA is HIGH, is generated, altering all devices on the bus that a device address is being written to the bus.

The 7-bit device address is written to the bus, followed by the R/$\overline{W}$ = 1 (R/$\overline{W}$ = 1 indicating the master wants to read data from the LM48560). After the R/$\overline{W}$ bit is transmitted, the master device releases SDA, during which time, an acknowledge clock pulse is generated by the slave device. If the LM48560 receives the correct address, the device pulls the SDA line low, generating and acknowledge bit (ACK). Once the master device registers the ACK bit, the 8-bit register address word is sent, MSB first, followed by an ACK and selected register data from the LM48560. The register data is sent MSB first. Following the acknowledgement of the register data word [7:0], the master issues a STOP bit, allowing SDA to go high while SDA is high.

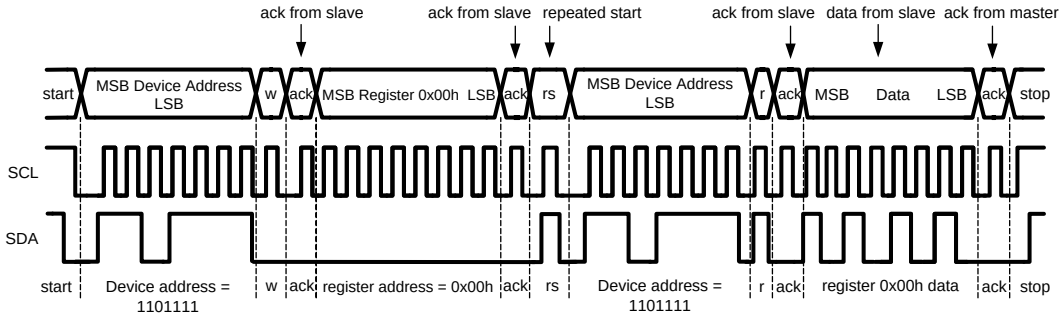


Figure 27. Example I²C Read Cycle

Table 1. Device Address

	B7	B6	B5	B4	B3	B2	B1	B0 (R/$\overline{W}$)
Device Address	1	1	0	1	1	1	1	0

Table 2. Mode Selection

SW/HW	SDA/SEL	SCL/GAIN	MODE
0	0 (Boost Disabled)	0	IN1, A_V = 0
		1	IN1, A_V = 6
	1 (Boost Enabled)	0	IN2, A_V = 24
		1	IN2, A_V = 30
1	X	X	I²C Mode

Table 3. I²C Control Registers

REGISTER ADDRESS	Register Name	B7	B6	B5	B4	B3	B2	B1	B0
0x00h	SHUTDOWN CONTROL	X	X	X	X	TURN_ON	IN_SEL	BOOST_EN	$\overline{SHDN}$
0x01h	NO CLIP CONTROL	X	RLT1	RLT0	ATK1	ATK0	PLEV2	PLEV1	PLEV0
0x02h	GAIN CONTROL	X	X	X	X	X	X	GAIN1	GAIN0
0x03h	TEST MODE	X	X	X	X	X	X	X	X

Table 4. Shutdown Control Register

BIT	NAME	VALUE	DESCRIPTION
B7:B4	UNUSED	X	Unused, set to 0
B3	TURN_ON	0	Normal turn on time, t_{WU} = 15ms
		1	Fast turn on time, t_{WU} = 5ms
B2	IN_SEL	0	Input 1 selected
		1	Input 2 selected
B1	BOOST_EN	0	Boost disabled
		1	Boost enabled
B0	$\overline{SHDN}$	0	Device shutdown
		1	Device enabled

Table 5. No Clip Control Register

BIT	NAME	VALUE			DESCRIPTION
B7	UNUSED	X			Unused, set to 0
B6:B5	RLT1 (B6) RLT0 (B5)	B6	B5		Sets Release Time based on C_{SET}. See RELEASE TIME section.
		0	0		T_R = 0.5s
		0	1		T_R = 0.38s
		1	0		T_R = 0.21s
		1	1		T_R = 0.17s
B4:B3	ATK1 (B4) ATK0 (B3)	B4	B3		Sets Attack Time based on C_{SET}. See ATTACK TIME section.
		0	0		T_A = 0.83ms
		0	1		T_A = 1.2ms
		1	0		T_A = 1.5ms
		1	1		T_A = 2.2ms
B2:B0	PLEV2 (B2) PLEV1 (B1) PLEV0 (B0)	B2	B1	B0	Sets output voltage limit level.
		0	0	0	Voltage Limit disabled
		0	0	1	$V_{TH(VLIM)}$ = 14V_{P-P}
		0	1	0	$V_{TH(VLIM)}$ = 17V_{P-P}
		0	1	1	$V_{TH(VLIM)}$ = 20V_{P-P}
		1	0	0	$V_{TH(VLIM)}$ = 22V_{P-P}
		1	0	1	$V_{TH(VLIM)}$ = 25V_{P-P}
		1	1	0	$V_{TH(VLIM)}$ = 28V_{P-P}
		1	1	1	Voltage Limit disabled

Table 6. Gain Control Register

BIT	NAME	VALUE		DESCRIPTION
B7:B2	UNUSED	X		Unused, set to 0
B1:B0	GAIN1(B1) GAIN0 (B0)	B1	B0	Sets amplifier gain. Boost disabled (BOOST_EN = 0)
		0	0	0dB
		0	1	6dB
		1	0	12dB
		1	1	18dB

Table 6. Gain Control Register (continued)

BIT	NAME	VALUE		DESCRIPTION
B1:B0	GAIN1(B1) GAIN0 (B0)	B1	B0	Sets amplifier gain. Boost enabled (BOOST_EN = 1)
		0	0	21dB
		0	1	24dB
		1	0	27dB
		1	1	30dB

GENERAL AMPLIFIER FUNCTION

The LM48560 is a fully differential, Class H piezo driver for ceramic speakers and haptic actuators. The integrated, high efficiency boost converter dynamically adjusts the amplifier's supply voltage based on the output signal, increasing headroom and improving efficiency compared to a conventional Class AB driver. The fully differential amplifier takes advantage of the increased headroom and bridge-tied load (BTL) architecture, delivering significantly more voltage than a single-ended amplifier.

CLASS H OPERATION

Class H is a modification of another amplifier class (typically Class B or Class AB) to increase efficiency and reduce power dissipation. To decrease power dissipation, Class H uses a tracking power supply that monitors the output signal and adjusts the supply accordingly. When the amplifier output is below $3V_{P-P}$, the nominal boost voltage is 6V. As the amplifier output increases above $3V_{P-P}$, the boost voltage tracks the amplifier output as shown in Figure 28. When the amplifier output falls below $3V_{P-P}$, the boost converter returns to its nominal output voltage. Power dissipation is greatly reduced compared to conventional Class AB drivers.

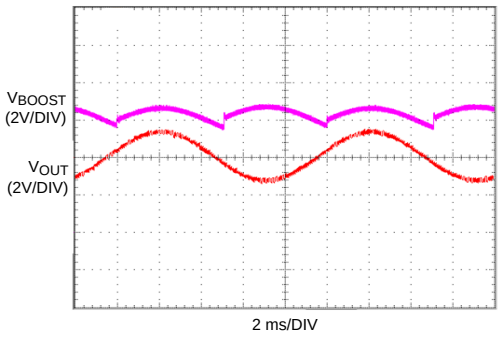


Figure 28. Class H Operation

DIFFERENTIAL AMPLIFIER EXPLANATION

The LM48560 features a fully differential amplifier. A differential amplifier amplifies the difference between the two input signals. A major benefit of the fully differential amplifier is the improved common mode rejection ratio (CMRR) over single ended input amplifiers. The increased CMRR of the differential amplifier reduces sensitivity to ground offset related noise injection, especially important in noisy systems.

AUTOMATIC LEVEL CONTROL (ALC)

The ALC is available in software mode only, and only in boosted mode. In hardware mode ALC is always disabled. The ALC limits the peak output voltage to the programmed value. Consequently, it limits the peak boost voltage, as this is derived from the output voltage. The ALC is continuous, in that it provides a continuous adjustment of the voltage gain in order to limit the output voltage to the programmed value. The available gain adjustment range is typically 8dB. When the input amplitude is further increased beyond the ALC attenuation range, the output will again increase. This is illustrated in the Typical Performance Graphs, as seen on the $14V_{PP}$ plot in the Input voltage vs Output Voltage curve. The attack and decay of the ALC is programmed by software and works in conjunction with the external capacitor C_{SET}. Typically C_{SET} is 0.1µF, although it can be changed from 0.1µF to 4.7µF to select other ranges of attack and decay time.

ATTACK TIME

Attack time (t_{ATK}) is the time it takes for the gain to be reduced by 6dB once the audio signal exceeds the ALC threshold. Fast attack times allow the ALC to react quickly and prevent transients such as symbol crashes from being distorted. However, fast attack times can lead to volume pumping, where the gain reduction and release becomes noticeable, as the ALC cycles quickly. Slower attack times cause the ALC to ignore the fast transients, and instead act upon longer, louder passages. Selecting an attack time that is too slow can lead to increased distortion in the case of the No Clip function, and possible output overload conditions in the case of the Voltage limiter. The attack time is set by a combination of the value of C_{SET} and the attack time coefficient as given by Equation 1:

$$t_{ATK} = 20k\Omega C_{SET} / \alpha_{ATK} \quad (1)$$

Where α_{ATK} is the attack time coefficient (Table 7) set by bits B4:B3 in the Voltage Limit Control Register. The attack time coefficient allows the user to set a nominal attack time. The internal 20kΩ resistor is subject to temperature change, and it has tolerance between -11% to +20%.

Table 7. Attack Time Coefficient

B4	B3	α_{ATK}
0	0	2.4
0	1	1.7
1	0	1.3
1	1	0.9

RELEASE TIME

Release time (t_{RL}) is the time it takes for the gain to return from 6dB to its normal level once the audio signal returns below the ALC threshold. A fast release time allows the ALC to react quickly to transients, preserving the original dynamics of the audio source. However, similar to a fast attack time, a fast release time contributes to volume pumping. A slow release time reduces the effect of volume pumping. The release time is set by a combination of the value of C_{SET} and release time coefficient as given by Equation 2:

$$t_{RL} = 20M\Omega C_{SET} / \alpha_{RL} \quad (s) \quad (2)$$

where α_{RL} is the release time coefficient (Table 8) set by bits B6:B5 in the No Clip Control Register. The release time coefficient allows the user to set a nominal release time. The internal 20MΩ is subject to temperature change, and it has tolerance between -11% to +20%.

Table 8. Release Time Coefficient

B6	B5	α_{RL}
0	0	4
0	1	5.3
1	0	9.5
1	1	11.8

BOOST CONVERTER

The LM48560 features an integrated boost converter with a dynamic output control. The device monitors the output signal of the amplifier, and adjusts the output voltage of the boost converter to maintain sufficient headroom while improving efficiency.

SOFTWARE/HARDWARE MODE

Device operation in hardware or software mode is determined by the state of the SW/$\overline{HW}$ pin. Connect SW/$\overline{HW}$ to ground for hardware mode, and connect to V_{DD} for software mode.

SW/$\overline{HW}$	SDA/SEL	SCL/GAIN	MODE
0	0 (Boost Disabled)	0	IN1, Av = 0
		1	IN1, Av = 6
	1 (Boost Enabled)	0	IN2, Av = 24
		1	IN2, Av = 30
1	SDA	SCL	I^2C Mode

GAIN SETTING

The LM48560 features four internally configured gain settings 0db, 6dB, and 30dB. The device gain is selected through a single pin (GAIN). The gain settings are shown in Table 9.

Table 9. Gain Setting

GAIN	GAIN SETTING IN1	GAIN SETTING IN2
0	0dB	24dB
1	6dB	30dB

SHUTDOWN FUNCTION

The LM48560 features a low current shutdown mode. Set $\overline{SD}$ = GND to disable the amplifier and boost converter and reduce supply current to 0.01µA.

SINGLE-ENDED INPUT CONFIGURATION

The LM48560 is compatible with single-ended sources. When configured for single-ended inputs, input capacitors must be used to block and DC component at the input of the device. Figure 29 shows the typical single-ended applications circuit.

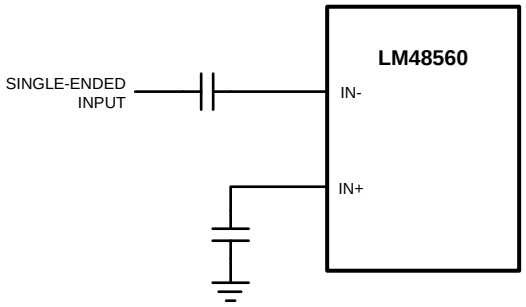


Figure 29. Single-Ended Input Configuration

PROPER SELECTION OF EXTERNAL COMPONENTS

ALC Timing (C_{SET}) Capacitor Selection

The recommended range value of C_{SET} is between .01µF to 1µF. Lowering the value below .01µF can increase the attack time but LM48560 ALC ability to regulate its output can be disrupted and approaches the hard limiter circuit. This in turn increases the THD+N and audio quality will be severely affected.

Power Selection of External Components

Proper power supply bypassing is critical for low noise performance and high PSRR. Place the supply bypass capacitors as close to the device as possible. Place a 1µF ceramic capacitor from V_{DD} to GND. Additional bulk capacitance may be added as required.

Boost Converter Capacitor Selection

The LM48560 boost converter requires three external capacitors for proper operation: a 1µF supply bypass capacitor, and 1µF + 100pF output reservoir capacitors. Place the supply bypass capacitor as close to V_{DD} as possible. Place the reservoir capacitors as close to VBST and VAMP as possible. Low ESR surface-mount multi-layer ceramic capacitors with X7R or X5R temperature characteristics are recommended. Select output capacitors with voltage rating of 25V or higher. Tantalum, OS-CON and aluminum electrolytic capacitors are not recommended. See Table 10 for suggested capacitor manufacturers.

Inductor Selection

The LM48560 boost converter is designed for use with a 4.7µH inductor. Choose an inductor with a saturation current rating greater than the maximum operating peak current of the LM48560 (> 1A). This ensures that the inductor does not saturate, preventing excess efficiency loss, over heating and possible damage to the inductor. Additionally, choose an inductor with the lowest possible DCR (series resistance) to further minimize efficiency losses.

Diode Selection

Use a Schottkey diode as shown in Figure 1. A 20V diode such as the NSR0520V2T1G from On Semiconductor is recommended. The NSR0520V2T1G is designed to handle a maximum average current of 500mA.

PCB LAYOUT GUIDELINES

Minimize trace impedance of the power, ground and all output traces for optimum performance. Voltage loss due to trace resistance between the LM48560 and the load results in decreased output power and efficiency. Trace resistance between the power supply and ground has the same effect as a poorly regulated supply, increased ripple and reduced peak output power. Use wide traces for power supply inputs and amplifier outputs to minimize losses due to trace resistance, as well as route heat away from the device. Proper grounding improves audio performance, minimizes crosstalk between channels and prevents switching noise from interfering with the audio signal. Use of power and ground planes is recommended.

Place all digital components and route digital signal traces as far as possible from analog components and traces. Do not run digital and analog traces in parallel on the same PCB layer. If digital and analog signal lines must cross either over or under each other, ensure that they cross in a perpendicular fashion.

DEMO BOARD USER GUIDE

Quick Start Guide (Hardware Mode):

1. Short pins 1 (VDD) and 2 of JU1 for normal operation.
2. Short pins 2 and 3(GND) of JU7 to set the device in hardware mode.
3. Short pins 2 and 3 (GND) of JU3 to select IN1.
4. Short pins 2 and 3 (GND) of JU2 for 0dB gain.
5. Connect a power supply (2.7V-5.5V) and ground reference respectively to the VDD and GND headers on the demo board.
6. Connect a differential audio input to IN1+ and IN2-
7. Power on the board and observe the output on OUT+ and OUT-

Quick Start Guide (Software Mode):

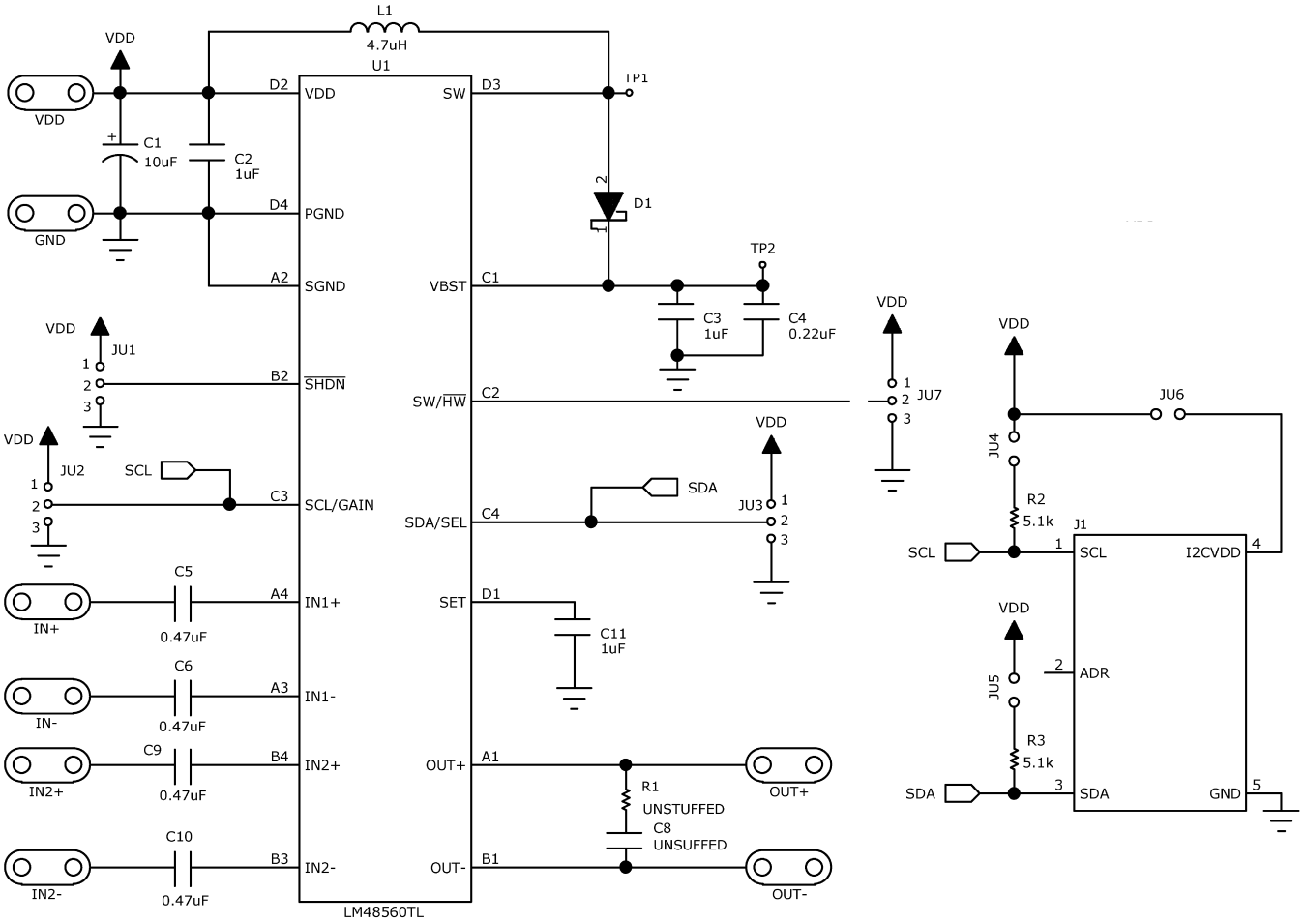
1. Short pins 1 (VDD) and 2 of JU1 for normal operation.
2. Short pins 1 (VDD) and 2 of JU7 to set the device in software mode.
3. Short pins 1 (VDD) and 2 of JU3 to select IN2.
4. Short pins 2 and 3 (GND) of JU2 for 24dB gain.
5. Connect a power supply (2.7V-5.5V) and ground reference respectively to the VDD and GND headers on the demo board.
6. Connect a differential audio input to IN1+ and IN2-
7. Connect the USB/I2C board to the LM48560 demo board.
8. Connect the USB/I2C board to a PC
9. Turn on the power supply
10. Launch the LM48560 software GUI
11. Verify that the bottom left corner of the GUI reads "USB Connected ALL ACK(1)"
12. Select the following:
    (a) INPUT SELECT = INPUT 1
    (b) BOOST = ON
    (c) TURN ON TIME = NORMAL
    (d) GAIN = 0dB

(1) If the GUI reads "USB I/O error NAK" the device has not been acknowledged, please double check your connections.

Table 10. Header Functionality

Designator	Function	Notes
VDD	VDD	Power Supply
GND	GND	Ground reference
OUT+	OUTPUT	Positive output terminal
OUT-	OUTPUT	Negative output terminal
IN1+	INPUT 1	Positive input terminal 1
IN1-	INPUT 1	Negative input terminal 1
IN2+	INPUT 2	Positive input terminal 2
IN2-	INPUT 2	Negative input terminal 2
JU1	Shutdown	Short pin 1 (VDD) and pin 2 for normal operation Short pin 2 and pin 3 (GND) for device shutdown
JU2	SCL/Gain Select	Hardware mode: Short pin 2 to pin 1 (VDD) for higher gain. Short pin 2 to pin 3(GND) for lower gain. (See Table 9) Software mode: Keep pins 1-3 open. Pin 2 = SCL for I2C communication
JU3	SDA/Input Select	Hardware mode: Short pin 2 to pin 1 (VDD) to select IN2. Short pin 2 to pin 3 (GND) to select IN1. (See Table 9) Software mode: Keep pins 1-3 open. Pin 2 = SCL for I2C communication
JU4	SCL Pullup	Short JU4 to connect pullup resistor to VDD. Open to use external I2C supply voltage
JU5	SDA pullup	Short JU5 to connect pullup resistor to VDD. Open to use external I2C supply voltage
JU6	I2C VDD	Short JU6 to use VDD as I2C VDD. Open to use external I2C supply voltage
JU7	SW/HW	Software Mode: Short pins 1 (VDD) and 2 Hardware Mode: Short pins 2 and 3(GND)

Demo Board Schematic



PC Board Layout

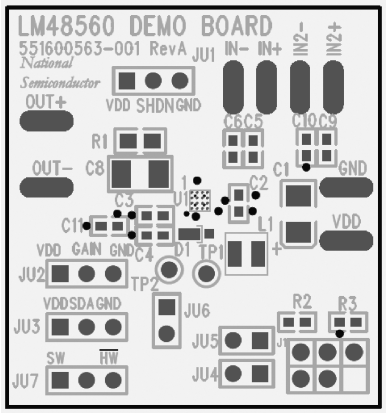


Figure 30. Top Silk Screen

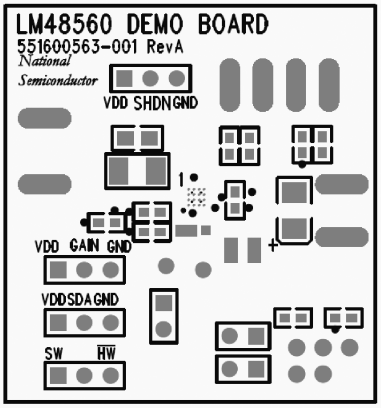


Figure 31. Solder Mask Top

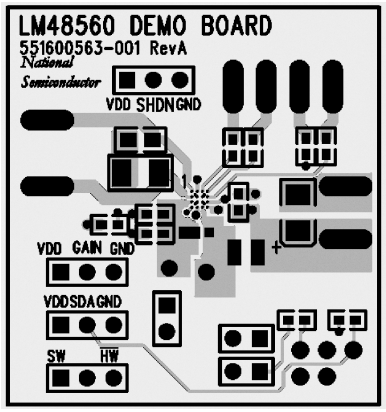


Figure 32. Top Layer

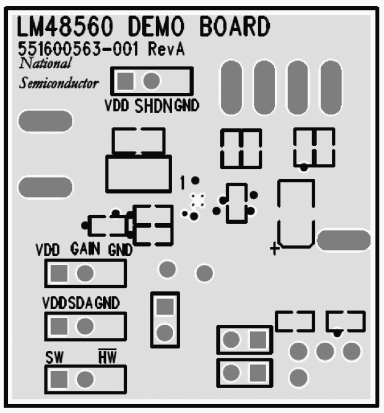


Figure 33. Layer 2

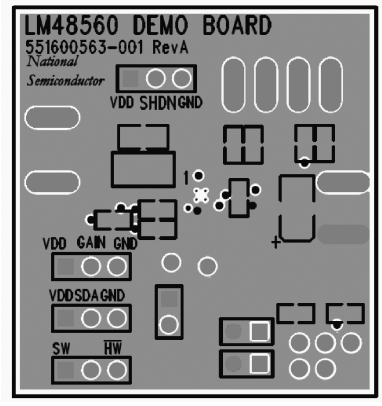


Figure 34. Layer 3

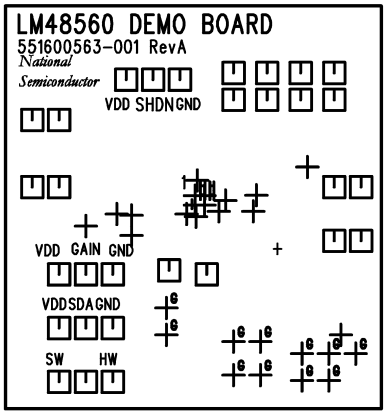


Figure 35. Drill Drawing

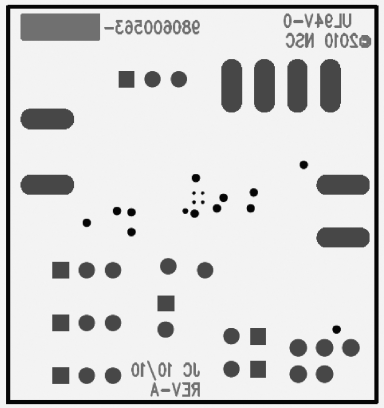


Figure 36. Silk Bottom

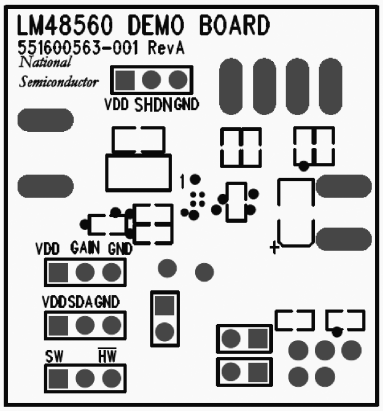


Figure 37. Solder Mask Bottom

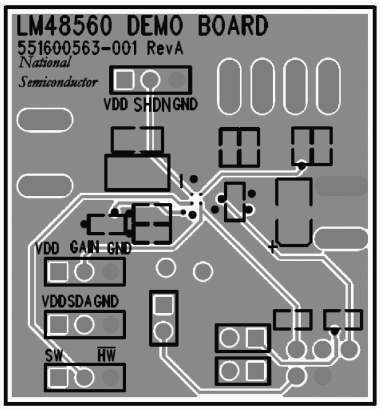


Figure 38. Bottom Layer

Revision History

Rev	Date	Description
1.0	08/16/11	Initial WEB released.
1.01	09/21/11	Input edits under CLASS H OPERATION.
1.02	11/01/11	Edited curves 30150753, 54, 55, 56, and Figure 26 (I^2C Read Cycle).
1.03	11/10/11	Edited Figure 26.
1.04	07/25/12	Input texts/limits edits in the EC table.
1.05	08/22/12	Edited Table 7 and Table 8.
E	05/02/2013	Changed layout of National Data Sheet to TI format.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM48560TL/NOPB	ACTIVE	DSBGA	YZR	16	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		GO5	Samples
LM48560TLX/NOPB	ACTIVE	DSBGA	YZR	16	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		GO5	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

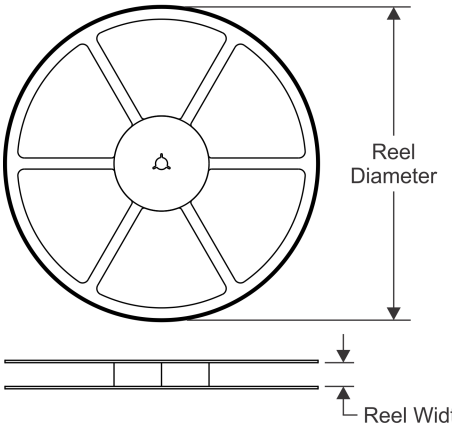
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

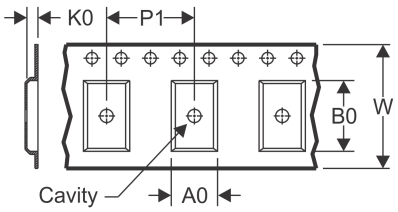
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

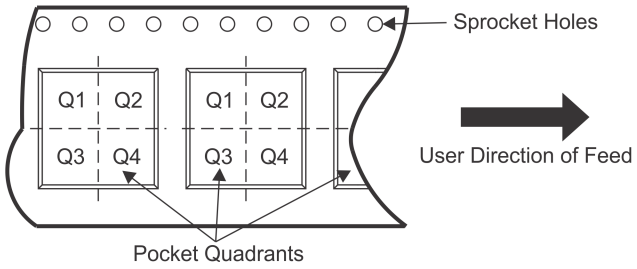


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

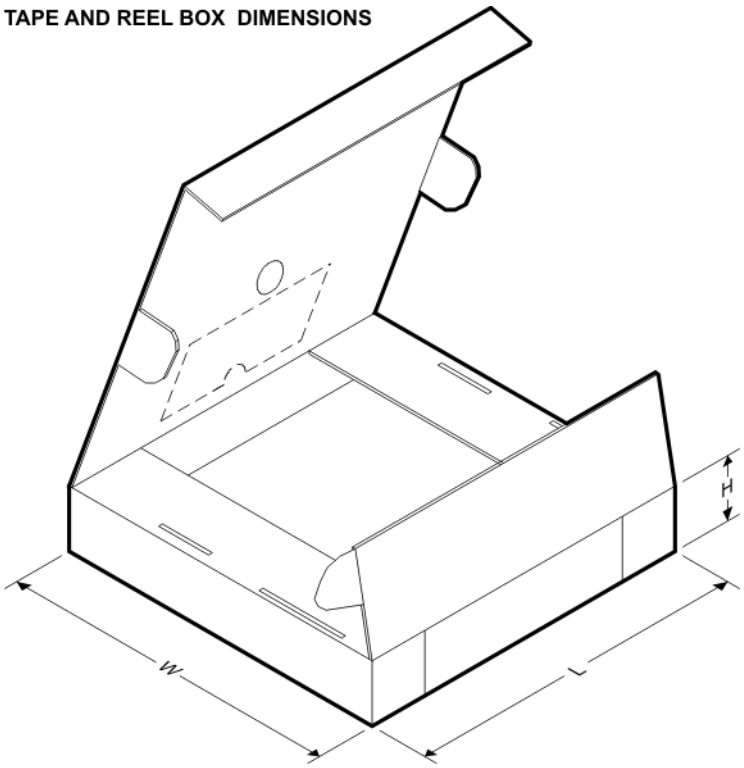
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM48560TL/NOPB	DSBGA	YZR	16	250	178.0	8.4	2.08	2.08	0.76	4.0	8.0	Q1
LM48560TLX/NOPB	DSBGA	YZR	16	3000	178.0	8.4	2.08	2.08	0.76	4.0	8.0	Q1

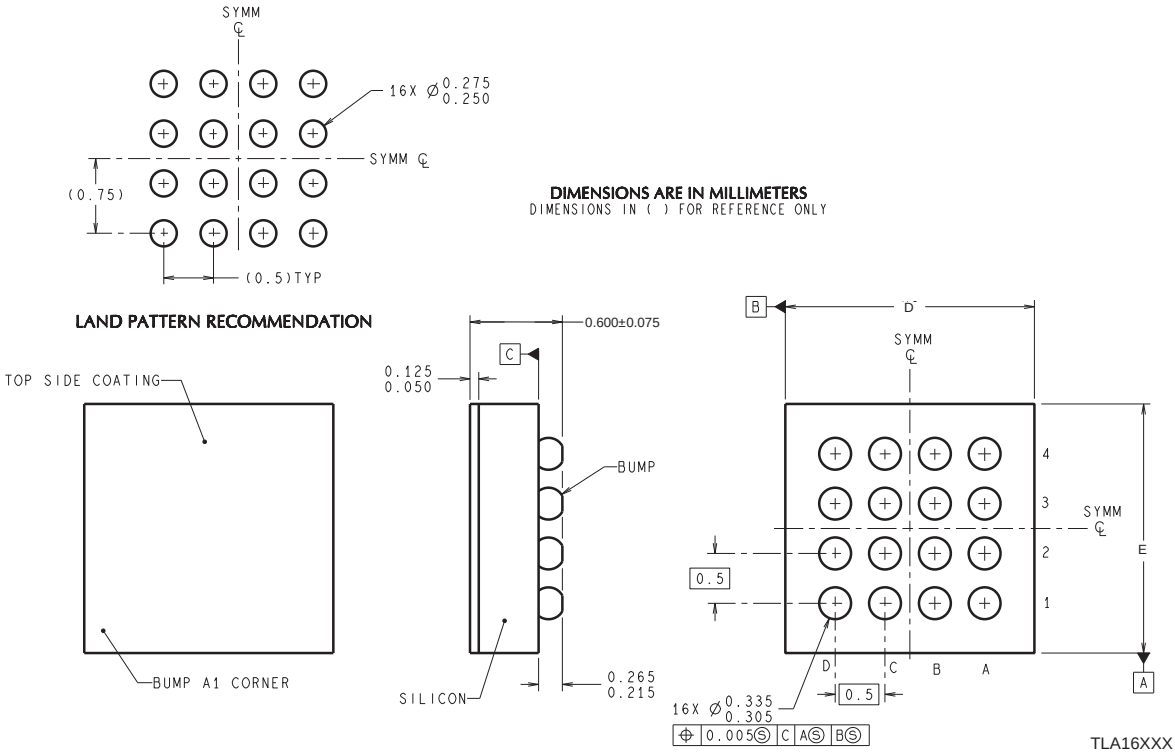
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM48560TL/NOPB	DSBGA	YZR	16	250	210.0	185.0	35.0
LM48560TLX/NOPB	DSBGA	YZR	16	3000	210.0	185.0	35.0

YZR0016



D: Max = 1.99 mm, Min = 1.93 mm

E: Max = 1.99 mm, Min = 1.93 mm

4215051/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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