LM98640 Dual Channel, 14-Bit, 40 MSPS Analog Front End with LVDS Output

Check for Samples: LM98640

FEATURES

- **Seialized LVDS Outputs**
- **LVDS Input Clock**
- **CDS or S/H Processing for CCD or CIS Sensors**
- **Programmable Analog Gain for Each Channel**
- **Programmable Analog Offset Correction**
- **Programmable Input Clamp Voltage**
- **Programmable Sampling Edge up to 1/64th Pixel Period**

KEY SPECIFICATIONS

- **Input Level: 2.85 Volts**
- **ADC Resolution: 14 Bit**
- **ADC Sampling Rate: 5 MSPS to 40 MSPS**
- **INL @ 15 MHz: ±3.5 LSB**
- **CDS or S/H Gain: 0 dB or 6 dB**
- **PGA Gain Steps: 256 Steps**
- **PGA Gain Range: -3 dB to 18 dB**
- **Coarse DAC Resolution: ±8 Bits**
- **Coarse DAC Range: ±250 mV**
- **Fine DAC Resolution: ±8 Bits**
- **Fine DAC Range: ±5 mV**
- **Noise Floor: -79 dB**
- **Crosstalk: -80dB**
- **Power Consumption**
- **PGA 1-4x Gain:**
  - **125 mW per Channel (15 MSPS)**
  - **140 mW per Channel (25 MSPS)**
- **PGA 1-8x Gain:**
  - **125 mW per Channel (15 MSPS)**
  - **178 mW per Channel (40 MSPS)**
- **Supply Voltages:**
  - **3.3V Nominal (3.15V to 3.45V Range)**
  - **1.8V Nominal (1.7V to 1.9V Range)**

APPLICATIONS

- **Focal Plane Electronics**
- **Imaging Attitude Control Systems**
- **Assembly Line Vision Systems**
- **Factory Automation Vision Systems**
- **High-speed Document Scanner**
- **Multi- Function Peripherals**

DESCRIPTION

The LM98640 is a fully integrated, high performance 14-bit, 5 MSPS to 40 MSPS signal processing solution for image processing applications. The Serial LVDS Output format performs well during ionizing doses, preventing data loss. The LM98640 has an adaptive power scaling feature to optimize power consumption based on the operating frequency and amount of gain required. High-speed signal throughput is achieved with an innovative architecture utilizing Correlated Double Sampling (CDS), typically employed with CCD arrays, or Sample and Hold (S/H) inputs (for Contact Image Sensors and CMOS image sensors). The sampling edges are programmable to a resolution of 1/64th of a pixel period. Both the CDS and S/H have a programmable gain of either 0 dB or 6 dB. The signal paths utilize two ±8 bit offset correction DACs for coarse and fine offset correction, and 8 bit Programmable Gain Amplifiers (PGA) for each channel. The PGA and offset DAC are programmed independently allowing unique values of gain and offset for each input. The signals are then routed to two on chip 14-bit 40 MHz high performance analog-to-digital converters (ADC). The fully differential processing channel provides exceptional noise immunity, having a very low noise floor of -79 dB with a gain of 1x. The 14-bit ADCs have excellent dynamic performance making the LM98640 transparent in the image reproduction chain.

LM98640 Overall Chip Block Diagram

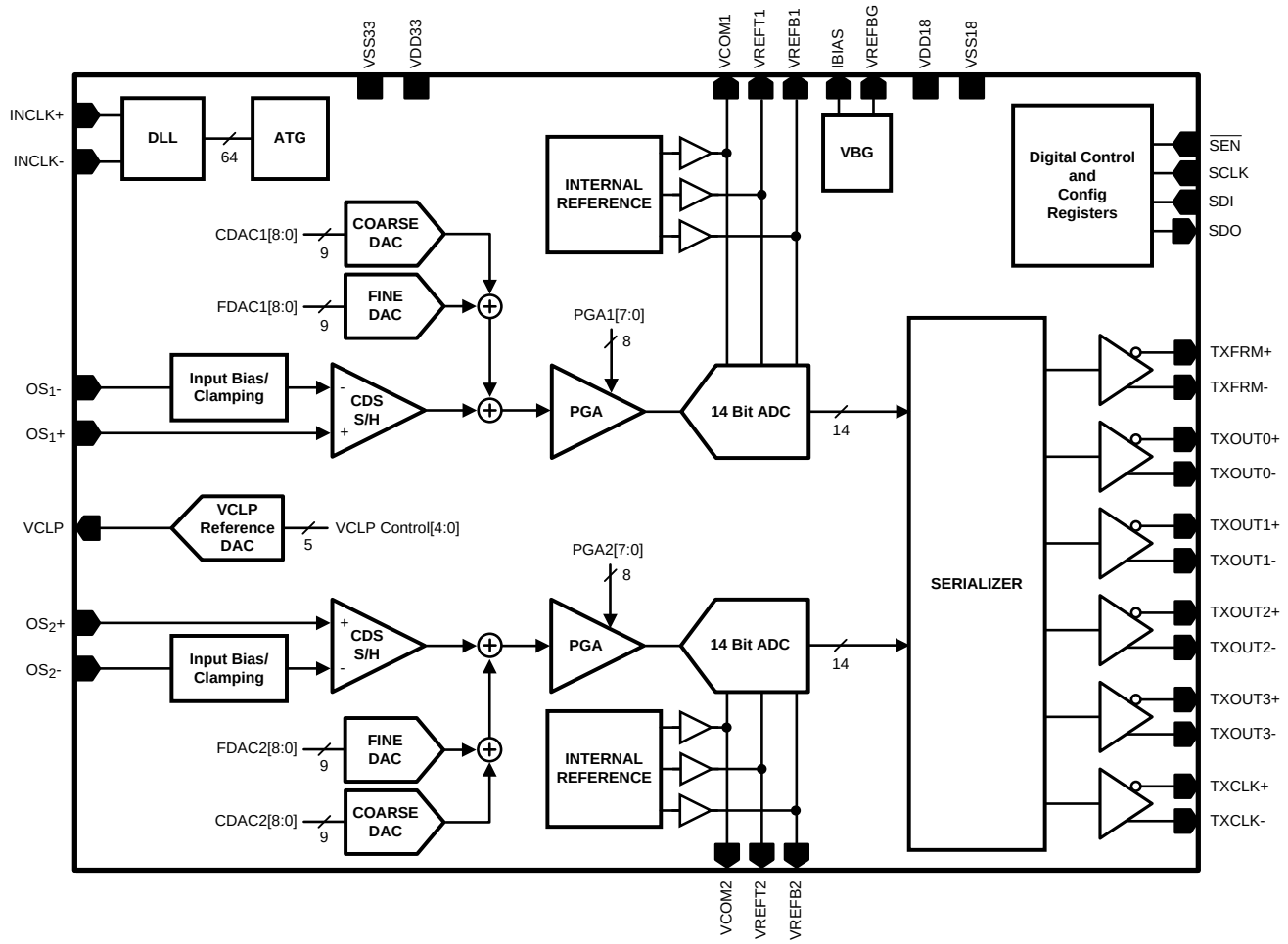


Figure 1. Chip Block Diagram

LM98640 Pin Out Diagram

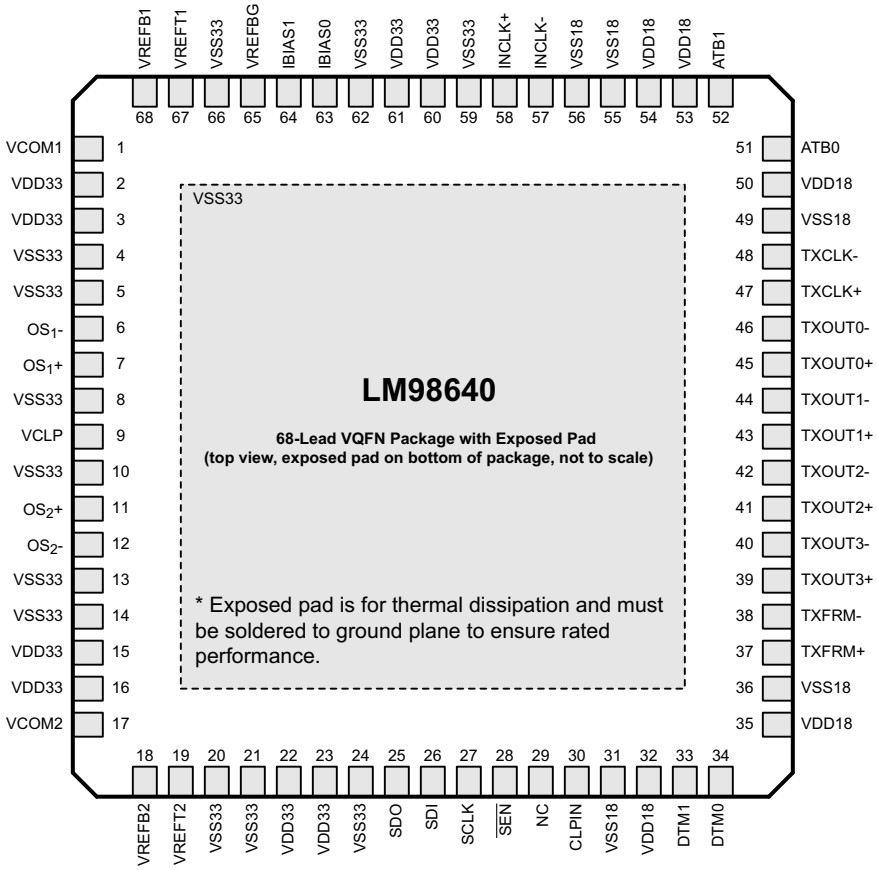


Figure 2. LM98640 Pin Out Diagram
VQFN Package
See Package Number NKE0068A

System Block Diagram

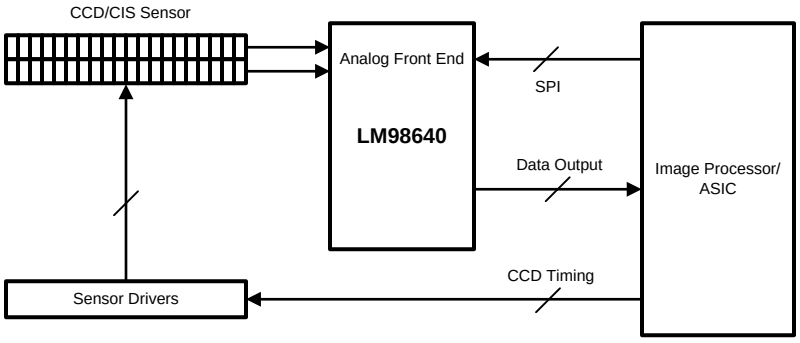


Figure 3. TYPICAL CCD SYSTEM

Typical Application Diagram

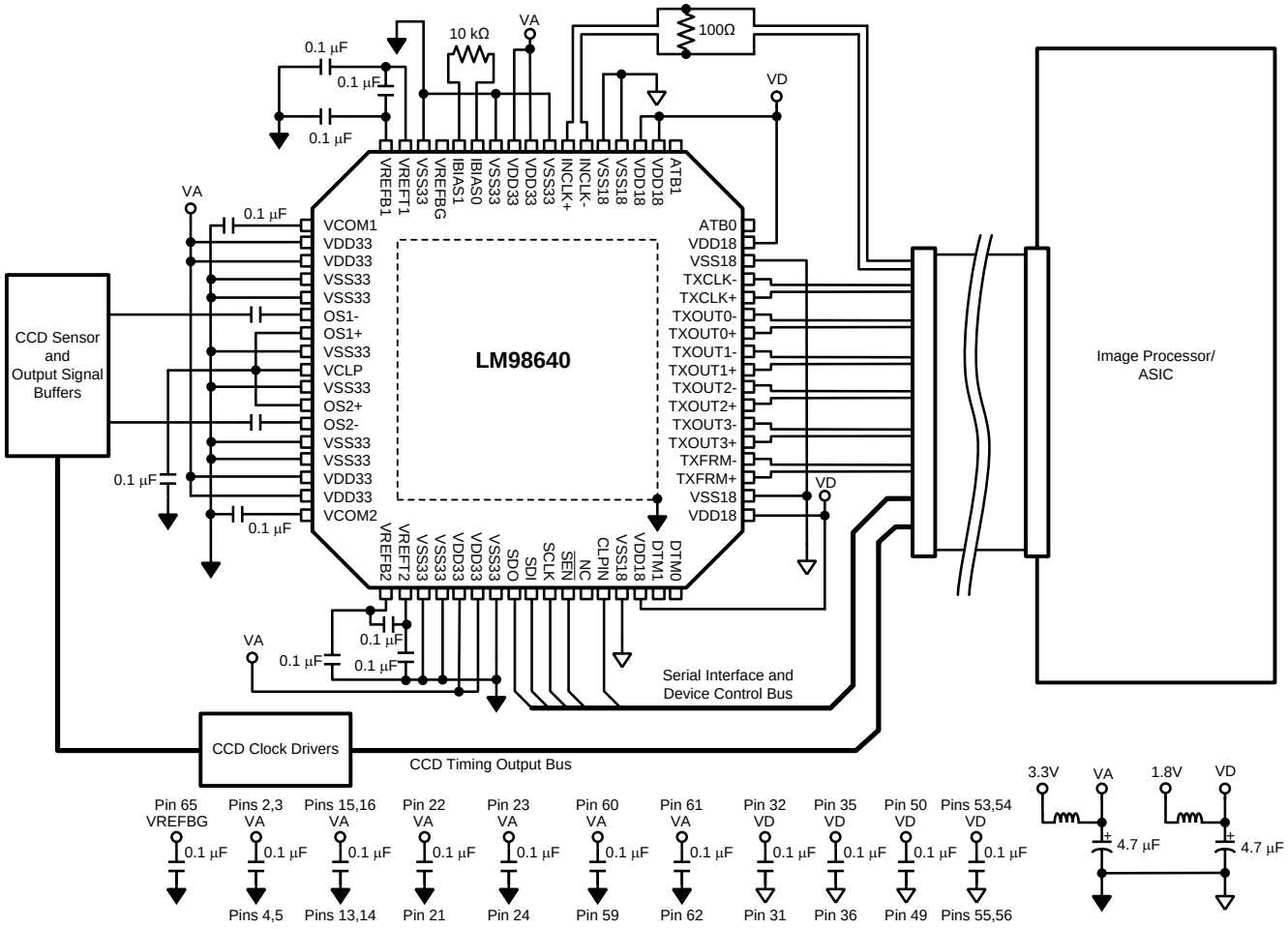


Figure 4. Typical Sample/Hold Mode Application Diagram

PIN DESCRIPTIONS

Pin	Name	I/O[1]	Typ	Res	Description
1	VCOM1	O	A		Common mode of ADC reference. Bypass with 0.1 µF capacitor to VSS33.
2	VDD33		P		Analog power supply. Decouple with minimum 0.1 µF capacitor to VSS33 plane.
3	VDD33		P		Analog power supply. Decouple with minimum 0.1 µF capacitor to VSS33 plane.
4	VSS33		P		Analog supply return.
5	VSS33		P		Analog supply return.
6	OS1-	I	A		Analog input signal.
7	OS1+	I	A		Sample/Hold Mode Reference Level. Bypassed with a 0.1 µF to ground in CDS mode.
8	VSS33		P		Analog supply return.
9	VCLP	O	A		Programmable Clamp Voltage output. Normally bypassed with a 0.1 µF capacitor to VSS33.
10	VSS33		P		Analog supply return.
11	OS2+	I	A		Sample/Hold Mode Reference Level. Bypassed with a 0.1 µF to ground in CDS mode.
12	OS2-	I	A		Analog input signal.
13	VSS33		P		Analog supply return.
14	VSS33		P		Analog supply return.
15	VDD33		P		Analog power supply. Decouple with minimum 0.1 µF capacitor to VSS33 plane.
16	VDD33		P		Analog power supply. Decouple with minimum 0.1 µF capacitor to VSS33 plane.
17	VCOM2	O	A		Common mode of ADC reference. Bypass with 0.1 µF capacitor to ground.
18	VREFB2	O	A		Bottom of ADC reference. Bypass with a 0.1 µF capacitor to ground.
19	VREFT2	O	A		Top of ADC reference. Bypass with a 0.1 µF capacitor to ground.
20	VSS33		P		Analog supply return.
21	VSS33		P		Analog supply return.
22	VDD33		P		Analog power supply. Decouple with minimum 0.1 µF capacitor to VSS33 plane.
23	VDD33		P		Analog power supply. Decouple with minimum 0.1 µF capacitor to VSS33 plane.
24	VSS33		P		Analog supply return.
25	SDO	O	D		Serial Interface Data Output. (Tri-State when $\overline{SEN}$ is high)
26	SDI	I	D		Serial Interface Data Input. (Tri-State when $\overline{SEN}$ is high)
27	SCLK	I	D	PD	Serial Interface shift register clock. (Tri-State when $\overline{SEN}$ is high)
28	$\overline{SEN}$	I	D	PU	Active-low chip enable for the Serial Interface.
29	NC				No Connection. Can be connected to VSS18.
30	CLPIN	I	D		Input clamp signal.
31	VSS18		P		Digital supply return.
32	VDD18		P		Digital power supply. Decouple with minimum 0.1 µF capacitor to VSS18 plane.
33	DTM1	O	D		Digital Timing Monitor. If not used, can be connected to VDD18 through a 10kΩ resistor.
34	DTM0	O	D		Digital Timing Monitor. If not used, can be connected to VDD18 through a 10 kΩ resistor.
35	VDD18		P		Digital power supply. Decouple with minimum 0.1 µF capacitor to VSS18 plane.
36	VSS18		P		Digital supply return.
37	TXFRM+	O	D		LVDS Frame+
38	TXFRM-	O	D		LVDS Frame-
39	TXOUT3+	O	D		LVDS Data Out3+
40	TXOUT3-	O	D		LVDS Data Out3-
41	TXOUT2+	O	D		LVDS Data Out2+
42	TXOUT2-	O	D		LVDS Data Out2-
43	TXOUT1+	O	D		LVDS Data Out1+
44	TXOUT1-	O	D		LVDS Data Out1-
45	TXOUT0+	O	D		LVDS Data Out0+

(1) (I=Input), (O=Output), (IO=Bi-directional), (P=Power), (D=Digital), (A=Analog), (PU=Pull Up with an internal resistor), (PD=Pull Down with an internal resistor.).

PIN DESCRIPTIONS (continued)

Pin	Name	I/O[1]	Typ	Res	Description
46	TXOUT0-	O	D		LVDS Data Out0-
47	TXCLK+	O	D		LVDS Clock+
48	TXCLK-	O	D		LVDS Clock-
49	VSS18		P		Digital supply return.
50	VDD18		P		Digital power supply. Decouple with minimum 0.1 µF capacitor to VSS18 plane.
51	ATB0	O	A		Analog Test Bus. If not used, can be connected to VSS18 through a 10 kΩ resistor.
52	ATB1	O	A		Analog Test Bus. If not used, can be connected to VSS18 through a 10 kΩ resistor.
53	VDD18		P		Digital power supply. Decouple with minimum 0.1 µF capacitor to VSS18 plane.
54	VDD18		P		Digital power supply. Decouple with minimum 0.1 µF capacitor to VSS18 plane.
55	VSS18		P		Digital supply return.
56	VSS18		P		Digital supply return.
57	INCLK-	I	D		Clock Input. Inverting input for LVDS clocks.
58	INCLK+	I	D		Clock Input. Non-Inverting input for LVDS clocks.
59	VSS33		P		Analog supply return.
60	VDD33		P		Analog power supply. Decouple with minimum 0.1 µF capacitor to VSS33 plane.
61	VDD33		P		Analog power supply. Decouple with minimum 0.1 µF capacitor to VSS33 plane.
62	VSS33		P		Analog supply return.
63	IBIAS0	I	A		Connect with external 10 kΩ 1% resistor to IBIAS1 pin.
64	IBIAS1	I	A		Connect with external 10 kΩ 1% resistor to IBIAS0 pin.
65	VREFBG	O	A		Band gap reference output. Bypass with a 0.1 µF capacitor to VSS33. Can be overdriven with external voltage source.
66	VSS33		P		Analog supply return.
67	VREFT1	O	A		Top of ADC reference. Bypass with a 0.1 µF capacitor to VSS33.
68	VREFB1	O	A		Bottom of ADC reference. Bypass with a 0.1 µF capacitor to VSS33.
	Exp Pad		P		Exposed pad must be soldered to ground plane to ensure rated performance.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Absolute Maximum Ratings(1)(2)

Supply Voltage (VDD33)		4.2V
Supply Voltage (VDD18)		2.35V
Voltage on any VDD33 Input Pin (Not to exceed 4.2V)		-0.3V to (VDD33 + 0.3V)
Voltage on any VDD33 Output Pin (Not to exceed 4.2V)		-0.3V to (VDD33 + 0.3V)
Voltage on any VDD18 Input Pin (Not to exceed 2.35V)		-0.3V to (VDD18 + 0.3V)
Voltage on any VDD18 Output Pin (Not to exceed 2.35V)		-0.3V to (VDD18 + 0.3V)
Input Current at any pin other than Supply Pins(3)		±25 mA
Package Input Current (except Supply Pins)(3)		±50 mA
Maximum Junction Temperature (TA)		150°C
Thermal Resistance(4)	(θ_{JA}) @ 225 LFPB	16.7°C/W
	(θ_{JA}) @ 0 LFPB	22.5°C/W
ESD Rating(5)	Human Body Model	4000V
	Machine Model	200V
	Charged Device Model	750V
Storage Temperature		-65°C to +150°C
Soldering process must comply with Texas Instruments Reflow Temperature Profile specifications. Refer to SNOA549(6)		

(1) All voltages are measured with respect to VSS = 0V, unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions. Operation of the device beyond the Operating Ratings is not recommended.
(3) When the input voltage (V_{IN}) at any pin exceeds the power supplies (V_{IN} < VSS or V_{IN} > VDD33), the current at that pin should be limited to 25 mA. The 50 mA maximum package input current rating limits the number of pins that can simultaneously safely exceed the power supplies with an input current of 25 mA to two.
(4) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA} and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} – T_A)/\theta_{JA}$. The values for maximum power dissipation listed above will be reached only when the device is operated in a severe fault condition (e.g. when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Such conditions should always be avoided.
(5) Human body model is 100 pF capacitor discharged through a 1.5 kΩ resistor. Machine model is 220 pF discharged through 0Ω.
(6) Reflow temperature profiles are different for lead-free and non-lead-free packages.

Operating Ratings(1)(2)

Operating Temperature Range	$0°C \le T_A \le +70°C$
VDD33	+3.15V to +3.45V
VDD18	+1.7V to +1.9V
| VSS33 - VSS18 |	≤100 mV

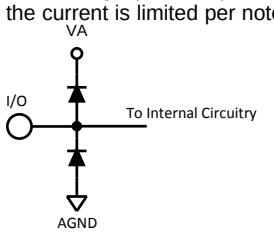
(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions. Operation of the device beyond the Operating Ratings is not recommended.
(2) All voltages are measured with respect to VSS = 0V, unless otherwise specified.

LM98640 Electrical Characteristics(1)

The following specifications apply for VDD33 = 3.3V, VDD18 = 1.8V, C_L = 10 pF, and f_{INCLK} = 40 MHz unless otherwise specified. **Boldface limits apply for TA = TMIN to TMAX; all other limits TA = 25°C.**

Symbol	Parameter	Conditions	Typical(2)	Min	Max	Units
CMOS Digital Input DC Specifications (SCLK, $\overline{SEN}$, SDI, CLPIN)						
V_{IH}	Logical “1” Input Voltage			**2.0**		V
V_{IL}	Logical “0” Input Voltage				**0.8**	V
I_{IH}	Logical “1” Input Current V_{IH} = VDD33	CLPIN	40		**46**	µA
		SCLK, SDI	40		**300**	nA
		$\overline{SEN}$	24		**30**	µA
I_{IL}	Logical “0” Input Current V_{IL} = VSS	CLPIN	-85	**-300**		nA
		SCLK, SDI	-50	**-300**		nA
		$\overline{SEN}$	-65	**-75**		µA
CMOS Digital Output DC Specifications (SDO)						
V_{OH}	Logical "1" Output Voltage	I_{OUT} = -0.5mA	1.93	**1.8**		V
V_{OL}	Logical "0" Output Voltage	I_{OUT} = 1.6mA	0.05		**0.2**	V
I_{OH}	Output Leakage Current	$V_{OUT} = V_{DD}$	20		**50**	nA
I_{OL}	Output Leakage Current	$V_{OUT} = V_{SS}$	-20	**-50**		nA
LVDS Clock Receiver DC Specifications (INCLK+ and INCLK- Pins)						
V_{IHL}	Differential LVDS Clock	R_L = 100Ω	100		**250**	mV
	High Threshold Voltage	V_{CM} (LVDS Input Common Mode Voltage) = 1.25V				
V_{ILL}	Differential LVDS Clock	RL = 100Ω	-100			mV
	Low Threshold Voltage	V_{CM} (LVDS Input Common Mode Voltage) = 1.25V		**-250**		
LVDS Output DC Specifications						
V_{OD}	Differential Output Voltage	LVDS Output Modes = 0000 x100 R_L = 100Ω	275			mV
V_{OS}	LVDS Output Offset Voltage		1.19			V
V_{OD}	Differential Output Voltage	LVDS Output Modes = 0000 x101 R_L = 100Ω	325			mV
V_{OS}	LVDS Output Offset Voltage		1.19			V
V_{OD}	Differential Output Voltage	LVDS Output Modes = 0000 x110 R_L = 100Ω	377			mV
V_{OS}	LVDS Output Offset Voltage		1.1			V
V_{OD}	Differential Output Voltage	LVDS Output Modes = 0000 x111 R_L = 100Ω	425	**350**	**590**	mV
V_{OS}	LVDS Output Offset Voltage		1.1	**0.95**	**1.2**	V
I_{OH}	LVDS Output Leakage Current		4.25		**5**	µA
I_{OL}	LVDS Output Leakage Current		-4.29	**-5**		µA
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V, R_L = 100Ω	40		**50**	mA
I_{IHL}	Diffferential LVDS Clock Input Current	V_{IH} = VDD33	23		**36**	µA
I_{ILL}	Diffferential LVDS Clock Input Current	V_{IL} = VSS	-34	**-49**		µA

(1) The analog inputs are protected as shown below. Input voltage magnitudes beyond the supply rails will not damage the device, provided the current is limited per note 3. However, input errors will be generated If the input goes above VDD33 and below VSS.



(2) Typical figures are at T_A = 25°C, and represent most likely parametric norms at the time of product characterization. The typical specifications are not ensured.

LM98640 Electrical Characteristics[1] (continued)

The following specifications apply for VDD33 = 3.3V, VDD18 = 1.8V, C_L = 10 pF, and f_{INCLK} = 40 MHz unless otherwise specified. **Boldface limits apply for TA = TMIN to TMAX; all other limits TA = 25°C.**

Symbol	Parameter	Conditions	Typical[2]	Min	Max	Units
Power Supply Specifications						
IA		Powerdown Control Reg = 0x00 (see Power Trimming section for PGA and ADC Power Trimming register settings)				
		5 MHz	51.5			mA
		15 MHz	61.3			
		25 MHz	69.6			
		40 MHz	87.6			
	VDD33 Analog Supply Current **Dual Channel** Power optimized for **PGA Gain = 1-8x**	Powerdown Control Reg = 0x00 (see Power Trimming section for PGA and ADC Power Trimming register settings)				
		5 MHz	51.5			mA
		15 MHz	61.3			
		25 MHz	72.9			
		40 MHz	91.3		**103**	
		Powerdown Control Reg = 0x15 (CH1 PD) or = 0x2A (CH2 PD) (see Power Trimming section for PGA and ADC Power Trimming register settings)				
		5 MHz	29.5			mA
		15 MHz	36.1			
		25 MHz	42			
		40 MHz	53.7			
	VDD33 Analog Supply Current **Single Channel** Power optimized for **PGA Gain = 1-8x**	Powerdown Control Reg = 0x15 (CH1 PD) or = 0x2A (CH2 PD) (see Power Trimming section for PGA and ADC Power Trimming register settings)				
		5 MHz	29.5			mA
		15 MHz	36.1			
		25 MHz	43.8			
		40 MHz	55.6		**64**	
	VDD33 Analog Supply Current **Powerdown**	Powerdown Control Reg = 0x80	2.85		**3.85**	mA
ID	VDD18 Digital Supply Current **LVDS Quad Lane Mode** LVDS Output Mode Reg = 0x0E	5 MHz	36			mA
		15 MHz	39			
		25 MHz	42			
		40 MHz	45			
	VDD18 Digital Supply Current	5 MHz	23.5			mA
		15 MHz	25.5			
		25 MHz	27.5			
		40 MHz	30.5		**37**	
	VDD18 Digital Supply Current **Powerdown**	Powerdown Control Reg = 0x80	1.2		**3.0**	mA

LM98640 Electrical Characteristics[1] (continued)

The following specifications apply for VDD33 = 3.3V, VDD18 = 1.8V, C_L = 10 pF, and f_{INCLK} = 40 MHz unless otherwise specified. **Boldface limits apply for TA = TMIN to TMAX; all other limits TA = 25°C.**

Symbol	Parameter	Conditions	Typical[2]	Min	Max	Units
PWR	Average Power Dissipation Power optimized for PGA Gain = 1-4x Dual Channel LVDS Dual Lane Mode	5 MHz	212			mW
		15 MHz	250			
		25 MHz	280			
		40 MHz	345		**390**	
	Average Power Dissipation Power optimized for PGA Gain = 1-8x Dual Channel LVDS Dual Lane Mode	5 MHz	212			mW
		15 MHz	250			
		25 MHz	290			
		40MHz	356		**407**	
PSRR	Dynamic Power Supply Rejection Ratio CDS Gain = 1x PGA Gain = 1x[3]	200 mVpp, 200 KHz	-72.3			dB
		200 mVpp, 500 KHz	-72			
		200 mVpp, 1 MHz	-71			
		200 mVpp, 1.5 MHz	-68			
		200 mVpp, 2 MHz	-66			
Internal Reference Specifications						
V_{REFBG}	Reference Voltage	See[4]	1.218			V
	Reference Tolerance (chip to chip)	See[5]	±2			%
R_{REFBG}	Reference Impedance	See[5]	20			kΩ
V_{REFTC}	Temperature Coefficient	25°C to 125°C	80			ppm/°C
		-55°C to 25°C	50			
Input Sampling Circuit Specifications						
V_{IN}	Input Voltage Level	CDS Gain=1x, PGA Gain=1x			**2**	Vp-p
		CDS Gain=2x, PGA Gain=1x			**1**	
		CDS Gain=1x, PGA Gain=0.7x	2.85			
V_{RESET}	Reset Feed Through		500			mV
I_{IN_SH}	Sample and Hold Mode Input Leakage Current[5]	CDS Gain = 1x	384			µA
		OS_X = VDD33 (OS_X = VSS)				
		CDS Gain = 2x	-475			µA
		OS_X = VDD33 (OS_X = VSS)				
C_{SH}	Sample/Hold Mode	CDS Gain = 1x	4			pF
	Equivalent Input Capacitance					
	(see Figure 22)[5]	CDS Gain = 2x	8			pF
I_{IN_CDS}	CDS Mode	OS_X = VDD33 (OS_X = VSS)	300			nA
	Input Leakage Current[5]					
R_{CLPIN}	CLPIN Switch Resistance		16			Ω
	(OS_X to VCLP Node in Figure 19)[5]					

(3) Dynamic Power Supply Rejection Ratio is performed by injecting a 200 mVpp sine wave ac coupled to the analog supply pin. The LM98640's inputs are left floating in CDS mode and an FFT is captured. The spur specified by the injected signal is recorded.
(4) This Parameter is specified by design and/or characterization and is not tested.
(5) This Parameter is specified by design and/or characterization and is not tested.

LM98640 Electrical Characteristics[1] (continued)

The following specifications apply for VDD33 = 3.3V, VDD18 = 1.8V, C_L = 10 pF, and f_{INCLK} = 40 MHz unless otherwise specified. **Boldface limits apply for TA = TMIN to TMAX; all other limits TA = 25°C.**

Symbol	Parameter	Conditions	Typical[2]	Min	Max	Units
VCLP Reference Circuit Specification						
	VCLP DAC Resolution		5	**5**		Bits
	VCLP DAC Step Size		98	**96**	**102**	mV
V_{VCLP}	VCLP DAC Voltage Min Output	VCLP Control Register = 0110 0000	224	**194**	**298**	mV
	VCLP DAC Voltage Max Output	VCLP Control Register = 0111 1101	3.07	**2.99**	**3.11**	V
I_{SC}	VCLP DAC Short Circuit Output Current	VCLP Control Register = 011x xxxx	33			mA
Coarse Analog Offset DAC Specifications						
	Resolution		±8			Bits
	Offset Adjustment Range Referred to AFE Input CDS Gain = 1x	Minimum DAC Code = 0x000	-262			mV
		Maximum DAC Code = 0x1FF	263			
	Offset Adjustment Range Referred to AFE Input CDS Gain = 2x	Minimum DAC Code = 0x000	-131			mV
		Maximum DAC Code = 0x1FF	131			
	Offset Adjustment Range Referred to AFE Output	Minimum DAC Code = 0x000	-2146			LSB
		Maximum DAC Code = 0x1FF	2154			
	DAC Step Size CDS Gain = 1x	Input Referred	1			mV
	DAC Step Size CDS Gain = 1x	Output Referred	8			LSB
DNL	Differential Non-Linearity	CDS Gain = 1x or 2x 40 MHz	±0.97			LSB
INL	Integral Non-Linearity	CDS Gain = 1x or 2x 40 MHz	±1.5			LSB
Fine Analog Offset DAC Specifications						
	Resolution		±8			Bits
	Offset Adjustment Range Referred to AFE Input CDS Gain = 1x	Minimum DAC Code = 0x000	-4.6			mV
		Maximum DAC Code = 0x1FF	5.3			
	Offset Adjustment Range Referred to AFE Input CDS Gain = 2x	Minimum DAC Code = 0x000	-2.3			mV
		Maximum DAC Code = 0x1FF	2.6			
	Offset Adjustment Range Referred to AFE Output	Minimum DAC Code = 0x000	-38			LSB
		Maximum DAC Code = 0x1FF	43			
	DAC Step Size CDS Gain = 1x	Input Referred	20			uV
	DAC Step Size CDS Gain = 1x	Output Referred	0.16			LSB
DNL	Differential Non-Linearity		±1			LSB
INL	Integral Non-Linearity		±2.2			LSB

LM98640 Electrical Characteristics[1] (continued)

The following specifications apply for VDD33 = 3.3V, VDD18 = 1.8V, C_L = 10 pF, and f_{INCLK} = 40 MHz unless otherwise specified. **Boldface limits apply for TA = TMIN to TMAX; all other limits TA = 25°C.**

Symbol	Parameter	Conditions	Typical[2]	Min	Max	Units
PGA Specifications						
	Gain Resolution				**8**	Bits
	Monotonicity	See[6]				
	Maximum Gain	CDS Gain = 1x	8.3	**7.92**		V/V
		CDS Gain = 1x	18.4	**17.99**		dB
	Minimum Gain	CDS Gain = 1x	0.64		**.7**	V/V
		CDS Gain = 1x	-3.8		**-3.10**	dB
	PGA Function	Gain (V/V) = (180/(277-PGA Code))				
		Gain (dB) = 20LOG10(180/(277-PGA Code))				
	Channel Matching	Minimum PGA Gain	99.0	**95.2**		%
		Maximum PGA Gain	99.0	**95.2**		%
ADC Specifications						
V_{REFT}	Top of Reference		2.0			V
V_{REFB}	Bottom of Reference		1.0			V
V_{REFT} - V_{REFB}	Differential Reference Voltage		1.0			V
	Overrange Output Code		16383	**16383**		Code
	Underrange Output Code		0		**0**	Code
Full Channel Performance Specifications						
DNL	Differential Non-Linearity	5 MHz	0.78	**-1.03**	**1.53**	LSB
		5 MHz CDS	1.0			
		15 MHz	0.78			
		25 MHz	0.78			
		40 MHz	0.78			
INL	Integral Non-Linearity	5 MHz	1.7	**−5.38**	**4.38**	LSB
		5 MHz CDS	1.7			
		15 MHz	1.9			
		25 MHz	2.4			
		40 MHz	6.0			
Noise	Noise Floor CDS Gain = 1x PGA Gain = FE	5 MHz	-66.0			dB
		15 MHz	-66.0			dB
		25 MHz	-66.0			dB
		40 MHz	-66.0			dB
	Noise Floor CDS Gain = 1x PGA Gain = FE	5 MHz	8.20			LSB
		15 MHz	8.20			LSB
		25 MHz	8.20			LSB
		40 MHz	8.20			LSB
	Noise Floor CDS Gain = 1x PGA Gain = 61	5 MHz	-79			dB
		15 MHz	-79			dB
		25 MHz	-79			dB
		40 MHz	-79			dB
	Noise Floor CDS Gain = 1x PGA Gain = 61	5 MHz	1.8			LSB
		15 MHz	1.8			LSB
		25 MHz	1.8			LSB
		40 MHz	1.8			LSB

(6) This Parameter is specified by design and/or characterization and is not tested.

LM98640 Electrical Characteristics[1] (continued)

The following specifications apply for VDD33 = 3.3V, VDD18 = 1.8V, C_L = 10 pF, and f_{INCLK} = 40 MHz unless otherwise specified. **Boldface limits apply for TA = TMIN to TMAX; all other limits TA = 25°C.**

Symbol	Parameter	Conditions	Typical[2]	Min	Max	Units
	Channel to Channel Crosstalk	5 MHz	-79			dB
		15 MHz	-86			
		25 MHz	-79			
		40 MHz	-76			
BMD	CDS Mode Bimodal Offset CDS Gain = 1x PGA Gain = 8x	5 MHz	2.2			mV
		15 MHz	2.1			
		25 MHz	2.2			
		40 MHz	2.3			
	CDS Mode Bimodal Offset CDS Gain = 1x PGA Gain = 1x	5 MHz	0.35			mV
		15 MHz	0.29			
		25 MHz	0.33			
		40 MHz	0.4			
SNR	Signal-to-Noise Ratio	5 MHz	67.4			dB
		15 MHz	68.0			dB
		25 MHz	68.5			dB
		40 MHz	68.5			dB
THD	Total Harmonic Distortion	5 MHz	-71.4			dB
		15 MHz	-75.1			dB
		25 MHz	-68.9			dB
		40 MHz	-62.0			dB
SFDR	Spurious-Free Dynamic Range	5 MHz	71.5			dB
		15 MHz	76.0			dB
		25 MHz	69.0			dB
		40 MHz	62.0			dB
SINAD	Signal-to-Noise Plus Distortion Ratio	5 MHz	67.0			dB
		15 MHz	68.0			dB
		25 MHz	66.0			dB
		40 MHz	61.0			dB
ENOB	Effective Number of Bits	5 MHz	10.8			Bits
		15 MHz	11.0			Bits
		25 MHz	10.7			Bits
		40 MHz	9.8			Bits

AC Timing Specifications

The following specifications apply for VDD33 = 3.3V, VDD18 = 1.8V, C_L = 10pF, and f_{INCLK} = 15 MHz unless otherwise specified. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}; all other limits T_A = 25°C.**

Symbol	Parameter	Conditions	Typical(1)	Min	Max	Units
Input Clock Timing Specifications						
f_{INCLK}	Input Clock Frequency	INCLK = ADCCLK (ADC Rate Clock)		**5**	**40**	MHz
T_{dc}	Input Clock Duty Cycle		50/50	**40/60**	**60/40**	%
Full Channel Latency Specifications						
t_{LAT}	Pipeline Latency	See(2)			**10**	T_{ADC}
LVDS Output Timing Specifications						
t_{DOD}	Data Output Delay	f_{INCLK} = 40 MHz INCLK = ADCCLK (ADC Rate Clock) LVDS Output Specifications not tested in production. Min/Max ensured by design, characterization and statistical analysis.	6.44			ns
t_{DSO}	Dual Lane Mode Odd Data Setup		0.69			ns
t_{DSE}	Dual Lane Mode Even Data Setup		0.89			ns
t_{QSR}	Quad Lane Mode Data to Rising Clock Setup		0.63			ns
t_{QHF}	Quad Lane Mode Falling Clock to Data Hold		0.53			ns
Serial Interface Timing Specifications						
f_{SCLK}	Input Clock Frequency	$f_{SCLK} <= f_{INCLK}$ INCLK = ADCCLK (ADC Rate Clock)		**1**	**20**	MHz
	SCLK Duty Cycle		50/50	**40/60**	**60/40**	ns
t_{IH}	Input Hold Time		1	**2.5**		ns
t_{IS}	Input Setup Time		1	**2.5**		ns
t_{SENSC}	SCLK Start Time After $\overline{SEN}$ Low		1	**1.5**		ns
t_{SCSEN}	$\overline{SEN}$ High after last SCLK Rising Edge		2	**2.5**		ns
t_{SENW}	$\overline{SEN}$ Pulse Width		6	**8**		ns
t_{OD}	Output Delay Time		10.54		**11.6**	ns
t_{HZ}	Data Output to High Z		1.2		**1.23**	T_{SCLK}

(1) Typical figures are at T_A = 25°C, and represent most likely parametric norms at the time of product characterization. The typical specifications are not ensured.
(2) This Parameter is specified by design and/or characterization and is not tested.

Typical Performance Characteristics

T_A = 25°C, F_S = 15 MHz, PGA Gain = 1x, CDS Gain = 1x, Dual Lane Output Mode, F_{IN} = 7.48 MHz unless otherwise stated.

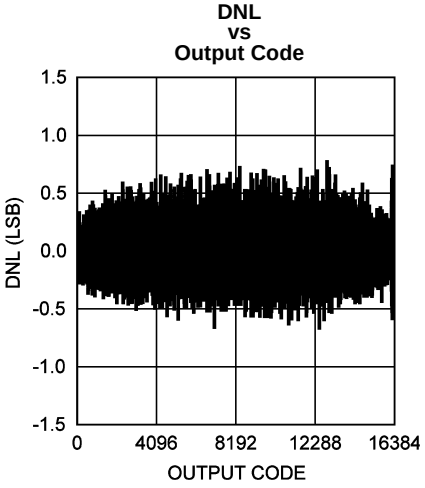


Figure 5.

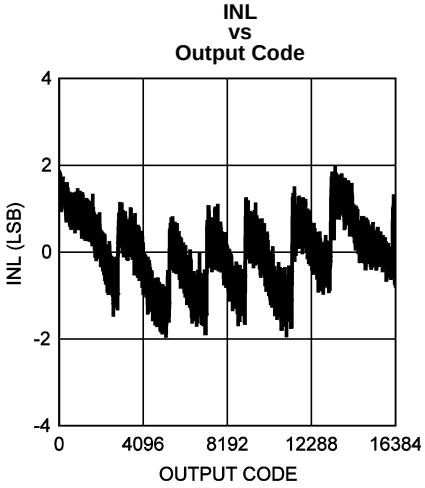


Figure 6.

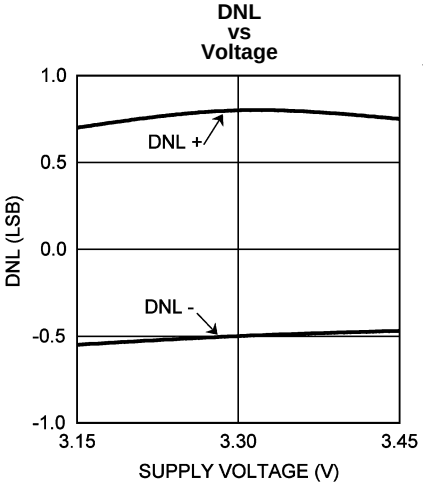


Figure 7.

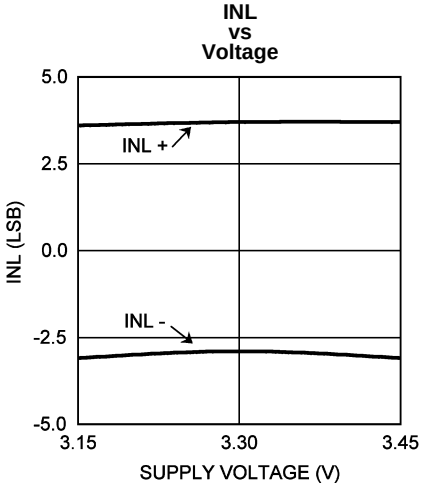


Figure 8.

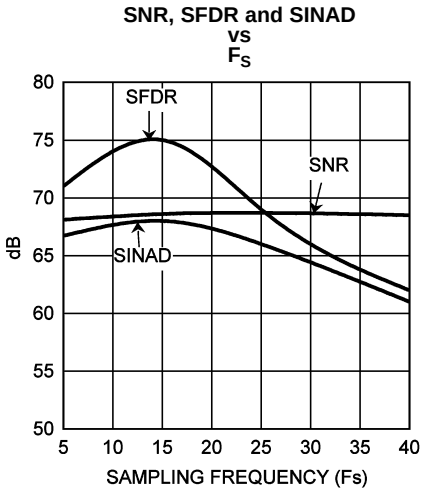


Figure 9.

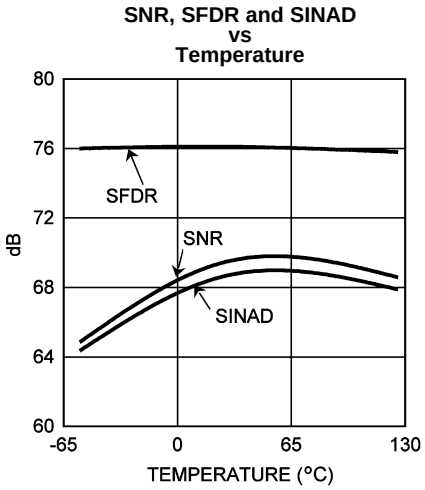


Figure 10.

Typical Performance Characteristics (continued)

T_A = 25°C, F_S = 15 MHz, PGA Gain = 1x, CDS Gain = 1x, Dual Lane Output Mode, F_{IN} = 7.48 MHz unless otherwise stated.

SNR, SFDR and SINAD vs Voltage

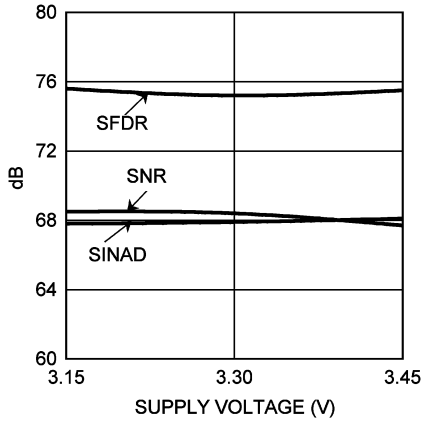


Figure 11.

THD and Noise vs F_S

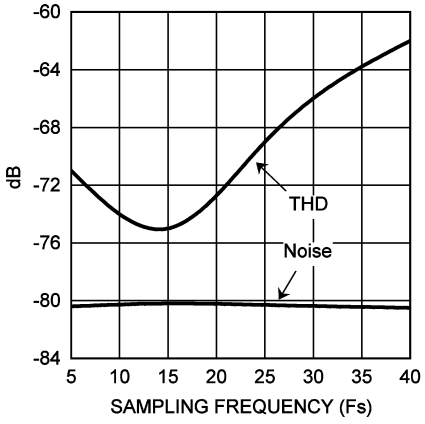


Figure 12.

THD and Noise vs Temperature

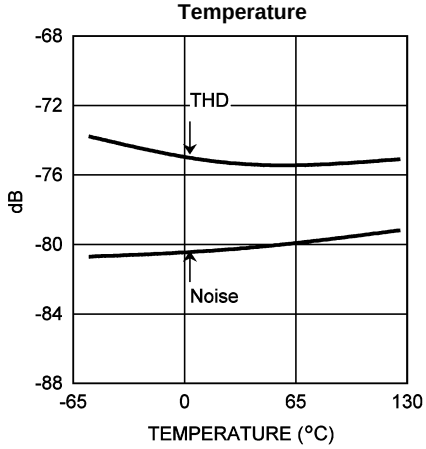


Figure 13.

THD and Noise vs Voltage

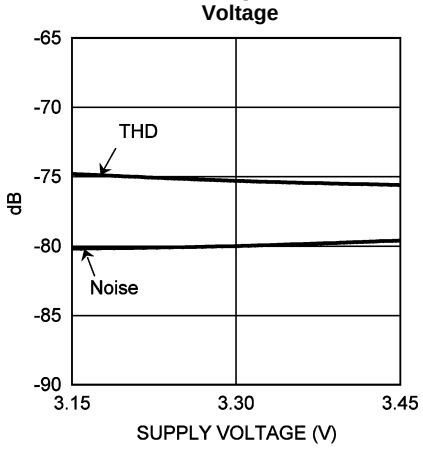


Figure 14.

Power vs F_S

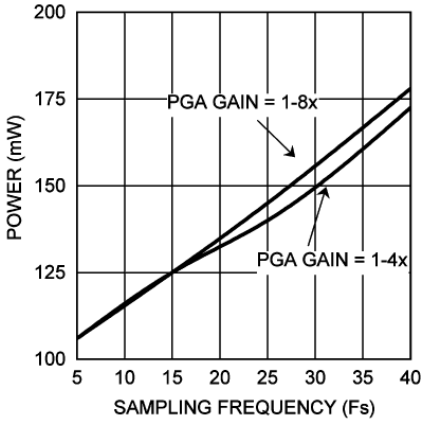


Figure 15.

Dynamic PSRR vs Power Supply Frequency

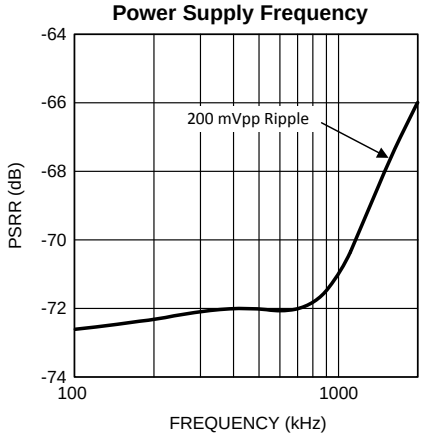


Figure 16.

SYSTEM OVERVIEW

Introduction

The LM98640 is a 14-bit, 5 MSPS to 40 MSPS, dual channel, complete Analog Front End (AFE) for digital imaging applications. The system block diagram of the LM98640, shown in Figure 4 highlights the main features of the device. Each input has its own Input Bias and Clamping Network and Correlated Double Sample (CDS) amplifier (which can also be configure to operate in Sample/Hold Mode). Two ±8-Bit Offset DACs apply independent coarse and fine offset correction for each channel. A -3 to 18 dB Programmable Gain Amplifier (PGA) applies independent gain correction for each channel. The signals are digitized using two independent on chip high performance 14-bit, 40 MHz analog-to-digital converters. The data is finally output using a unique Serial LVDS output format that prevents data loss during any ionizing doses.

Input Sampling Modes

The LM98640 provides two input sampling modes: Sample & Hold mode and Correlated Double Sample (CDS) mode. The following sections describe these two input sampling modes.

Sample & Hold Mode

In Sample/Hold mode, a Video Level signal and a Reference Level signal need to be presented to the LM98640. The Reference Level signal must be connected to the OS_X+ pin, and the Video Level signal connected to the OS_X- pin. The output code will then be OS_X+ minus OS_X-, or the difference between the Reference Level and Video Level. A minimum code represents zero deviation between the Reference and Video Levels and a maximum code represents a 2V deviation between the Reference and Video Levels with CDS and PGA gains of 1x.

The Reference Level signal can be either an external signal from the image sensor, or the VCLP pin can be externally connected to the OS_X+ pin. In order to fully utilize the range of the input circuitry it is desirable to cause the Black Level signal voltage to be as close to the Reference Level voltage as possible, resulting in a near zero scale output for Black Level pixels. The LM98640 provides several methods for ensuring the Black Level signal and Reference Level are matched, these are described in the Input Bias and Clamping section.

To place the LM98640 in Sample & Hold Mode from power up, first write the baseline configuration to the registers as shown in the Table 5 section. This configuration has Sample & Hold mode enabled by default. Next, the SAMPLE pulse must be properly positioned over the input signal using the CLAMP/SAMPLE Adjust.

Sample & Hold Mode Clamp/Sample Adjust

For accurate sampling of the input signals the LM98640 allows for full adjustment of the internal SAMPLE pulse to align it to the proper positions over the input signal. In Sample & Hold mode the SAMPLE pulse should be placed over the pixel output period of the image sensor. Only the Sample Start and Sample End Registers (0x22,0x23) need to be configured, the Clamp Start and Clamp End Registers (0x20,0x21) are not valid in Sample & Hold Mode. Internally the input clock is divided into 64 edges per clock period, the Sample Start and Sample End Registers correspond to the internal edge number the SAMPLE pulse will start and end. To adjust the SAMPLE pulse, first send the CLAMP and SAMPLE signals to the DTM pins by writing **10** to bits[4:3] of the Clock Monitor Register (0x09). This will allow the user to observe the SAMPLE pulse on pin DTM1 along with the image sensor output using an oscilloscope. Then, using the Sample Start and End Registers, adjust the SAMPLE pulse to align it over the Video Level portion of the image sensor output. To allow for settling and to reduce noise, the SAMPLE pulse should be made as wide as possible and fill the entire Video Level portion of the input signal.

Figure 17 shows some examples of an input waveform and where the SAMPLE pulse should be placed. Ideally the image sensor output would line up directly with the input clock at the AFE inputs, but due to trace delays in the system the image sensor output is delayed relative to the input clock. In the delayed image sensor waveform the Sample Start value is higher than the Sample End value. In this situation the SAMPLE pulse will start in one clock period and wraps around to the next. This allows the LM98640 to adjust for the delay in the image sensor waveform. Notice that edge zero of the internal clock does not line up with the rising edge of the input clock. This is due to internal delays of the clock signals. The amount of delay can be calculated from operating frequency using the following formula: t_{DCLK} = 6.0 ns + 3/64 * T_{INCLK}

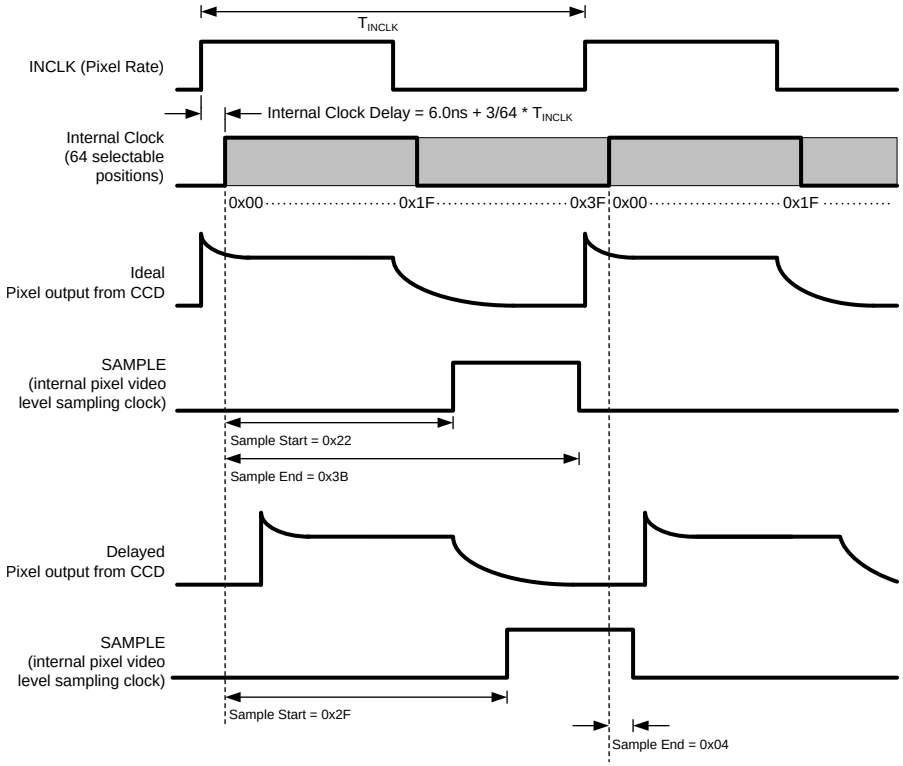


Figure 17. S/H Mode CLAMP/SAMPLE Adjust

CDS Mode

In CDS mode, both the Reference Level and Video Level are presented to the LM98640 on the OS_X- pin. The OS_X+ pin should be bypassed to ground with a 0.1 µF capacitor. The CLAMP pulse is then used to sample the Reference Level and the SAMPLE pulse is used to sample the Video Level. The output code will then be the Reference Level minus the Video Level, or the difference between the Reference Level and Video Level. A minimum code represents zero deviation between the Reference and Video Levels and a maximum code represents a 2V deviation between the Reference and Video Levels with CDS and PGA gains of 1x.

To place the LM98640 in CDS Mode from power up, first write the baseline configuration to the registers as shown in the Table 5 Section. Then ensure S/H mode is disabled by clearing bit[7] of the Sample & Hold Register (0x06), then enable CDS mode by setting bit[0] of the Main Configuration Register (0x00). Next the CLAMP and SAMPLE pulses need to be positioned correctly over the reference and video levels respectively using the CLAMP/SAMPLE Adjust.

CDS Mode Bimodal Offset

In CDS mode, the input sampling amplifier has two physical paths through which a particular pixel will be sampled. These two sampling paths are a requirement in the Correlated Double Sampling architecture. The sampling of the one pixel will travel the first path (arbitrarily called an even pixel), and the sampling of the next pixel will travel the second path (called an odd pixel). The sampling will continue in an even/odd/even/odd fashion for all pixels processed in a particular channel. Due to slight variances in the sampling paths (most commonly a difference in switched capacitor matching), the processing of identical pixels through the two different paths may result in a small offset in ADC output data between the two paths. To correct this, a simple digital offset can be applied in post processing to either the even pixel data or the odd pixel data. To simplify this action, the LM98640 will indicate (with the TXFRM signal) whether the pixel traveled the even path or the odd path. For all "Odd" pixels, the TXFRM signal is high for three TXCLK periods. For "Even" pixels, the TXFRM signal is high for two TXCLK periods. In Sample and Hold Mode there is only one sampling path, therefore there is no need to indicate an even or odd pixel. As a result, the TXFRM signal is the same for every pixel in Sample and Hold mode (i.e. high for three TXCLK periods).

CDS Mode CLAMP/SAMPLE Adjust

In CDS mode, the LM98640 utilizes two input networks, alternating between them every pixel, to increase throughput speeds. Because of this, there are two sets of CLAMP and SAMPLE pulses in Figure 18, one for even pixels and one for odd. Sample Start and Sample End Registers (0x22,0x23) along with the Clamp Start and Clamp End Registers (0x20,0x21) control both the even and odd CLAMP and SAMPLE pulses. To adjust the CLAMP and SAMPLE pulses, first send the $CLAMP_{ODD}$ and $SAMPLE_{ODD}$ signals to the DTM pins by writing **10** to bits[4:3] of the Clock Monitor Register (0x09). This will allow the user to observe the $CLAMP_{ODD}$ and $SAMPLE_{ODD}$ pulses on pins DTM0 and DTM1 along with the image sensor output using an oscilloscope. The CLAMP and SAMPLE pulses will only be shown for every other pixel because of the even odd architecture, but the positions of the even CLAMP and SAMPLE pulses will be identical to that of the odd CLAMP and SAMPLE. Then, using the Clamp Start/End and Sample Start/End registers, adjust the positions of the CLAMP and SAMPLE pulses to align them over the Reference and Video Levels of the input signal. To allow for settling and to reduce noise, the CLAMP and SAMPLE pulses should be made as wide as possible and placed near the far edge of their respective input levels.

The following figure shows some examples of input CCD waveforms and placement of the CLAMP and SAMPLE positions for each. Ideally the CCD output would line up directly with the input clock at the AFE inputs, but due to trace delays in the system the CCD output is delayed relative to the input clock. In the Delayed CCD waveform the Sample Start/End Register values are lower than the Clamp Start/End Register Values. In this situation the sample pulse is not generated until the next clock period, which allows it to be correctly placed in the Video Level of the input signal. Notice that edge zero of the internal clock does not line up with the rising edge of the input clock. This is due to internal delays of the clock signals. The amount of delay can be calculated from operating frequency using the following formula: $t_{DCLK} = 6.0\ ns + 3/64 * T_{INCLK}$

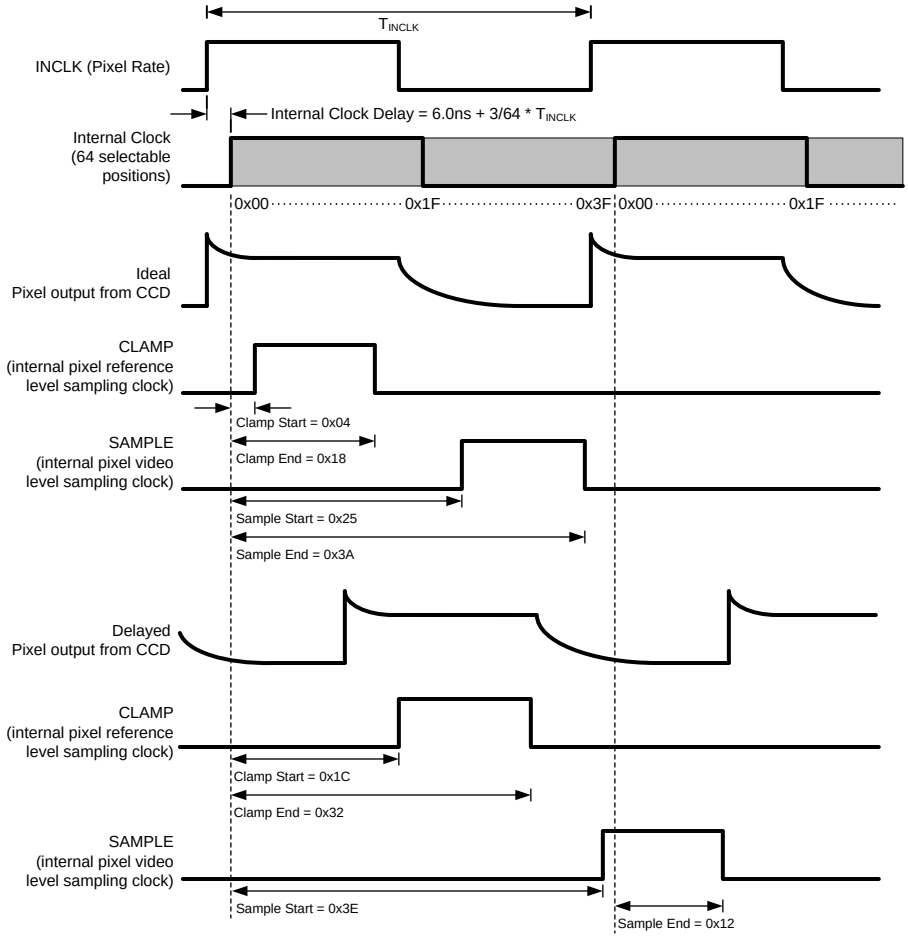


Figure 18. CDS Mode CLAMP/SAMPLE Adjust

Input Bias and Clamping

The inputs to the LM98640 are typically AC coupled and can be sampled in either Sample and Hold Mode (S/H Mode) or Correlated Double Sampling Mode (CDS Mode). The circuit of Figure 19 shows the input structure of the LM98640. The DC bias point for the LM98640 side of the AC coupling capacitor can to be set using an external DC bias resistor network, by using the CLPIN configuration, or by using the BITCLP configuration. A typical CCD waveform is shown in Figure 20. Also shown in Figure 20 is an internal signal “CLAMP” which can be used to “gate” the CLPIN signal so that it only occurs during the “pedestal” portion of the CCD pixel waveform.

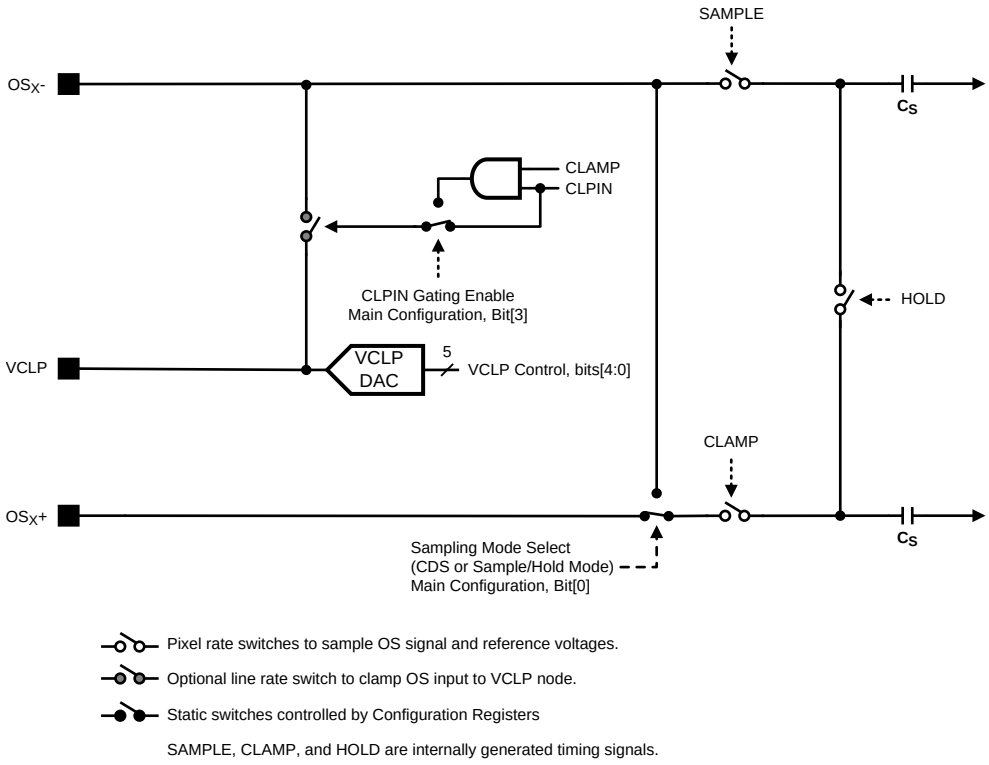


Figure 19. Input Structure Diagram

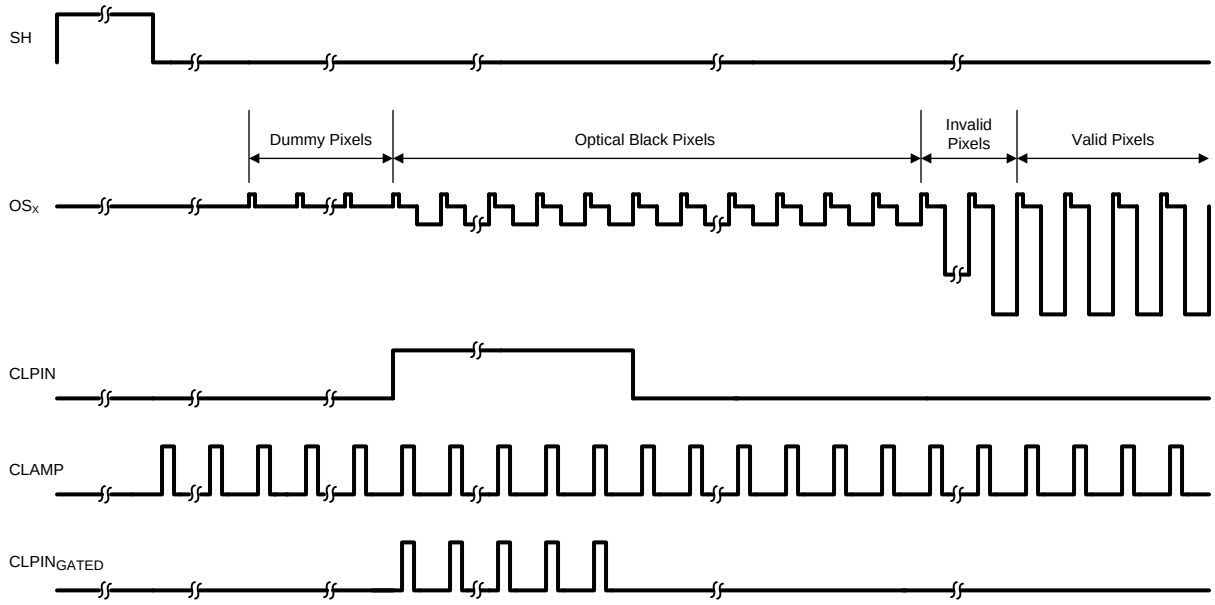


Figure 20. Typical CCD Waveform and LM98640 Input Clamp Signal (CLPIN)

Sample and Hold Mode Biasing

Proper DC biasing of the CCD waveform in Sample and Hold mode is critical for realizing optimal operating conditions. In Sample/Hold Mode, the DC bias point of the input pin is typically set by actuating the input clamp switch (see Figure 19) during optical black pixels which connects the input pins to the VCLP pin DC voltage. The signal controlling this switch is CLPIN. CLPIN is an external signal connected on the CLPIN pin.

Actuating the input clamp will force the average value of the CCD waveform to be centered around the VCLP DC voltage. During Optical Black Pixels, the CCD output has roughly three components. The first component of the pixel is a “Reset Noise” peak followed by the Reset (or Pedestal) Level voltage, then finally the Black Level voltage signal. Taking the average of these signal components will result in a final “clamped” DC bias point that is close to the Black Level signal voltage.

To provide a more precise DC bias point (i.e. a voltage closer to the Black Level voltage), the CLPIN pulse can be “gated” by the internally generated CLAMP clock. This resulting $CLPIN_{GATED}$ signal is the logical “AND” of the CLAMP and CLPIN signals as shown in Figure 20. By using the $CLPIN_{GATED}$ signal, the higher Reset Noise peak will not be included in the clamping period and only the Pedestal Level components of the CCD waveform will be centered around VCLP.

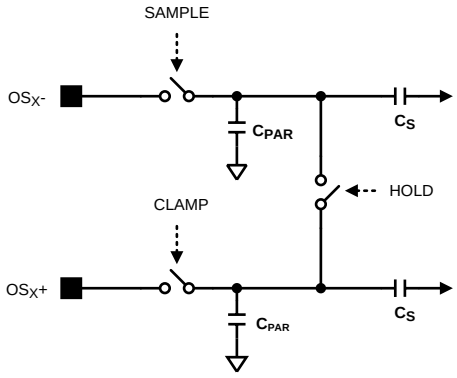


Figure 21. Sample and Hold Mode Simplified Input Diagram

In Sample and Hold Mode, the impedance of the analog input pins is dominated by the switched capacitance of the CDS/Sample and Hold amplifier. The amplifier switched capacitance, shown as C_S in Figure 21, and internal parasitic capacitances can be estimated by a single capacitor switched between the analog input and the VCLP reference pin for Sample and Hold mode. During each pixel cycle, the modeled capacitor, C_{SH}, is charged to the OS_X+ minus OS_X- voltage then discharged. The average input current at the OS_X- pin can be calculated knowing the input signal amplitude and the frequency of the pixel.

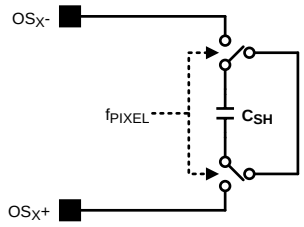


Figure 22. Equivalent Input Switched Capacitance S/H Mode

CDS Mode Biasing

Correlated Double Sampling mode does not require as precise a DC bias point as does Sample and Hold mode. This is due mainly to the nature of CDS itself, that is, the Video Signal voltage is referenced to the Reset Level voltage instead of the static DC VCLP voltage. The common mode voltage of these two points on the CCD waveform have little bearing on the resulting differential result. However, the DC bias point does need to be established to ensure the CCD waveform's common mode voltage is within rated operating ranges.

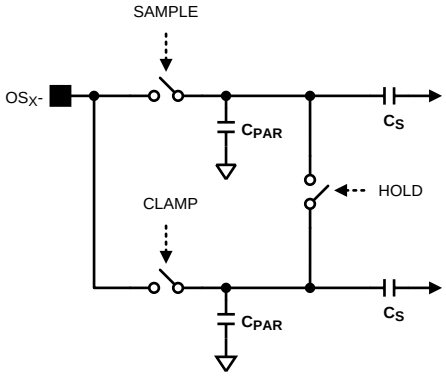


Figure 23. CDS Mode Simplified Input Diagram

The CDS mode biasing can be performed in the same way as described in the Sample and Hold Mode Biasing section, or, an external resistor divider can be placed across the OS_X- input to provide the DC bias voltage. In CDS Mode the OS_X+ pins should each be decoupled with 0.1 µF capacitors to ground.

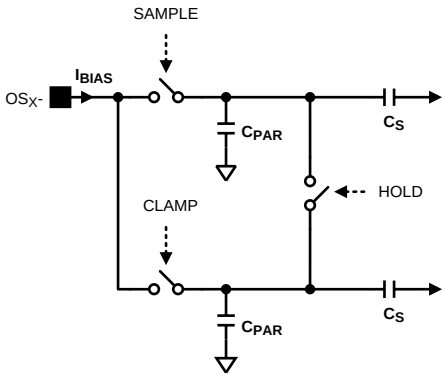


Figure 24. CDS Mode Input Bias Current

Unlike in Sample and Hold Mode, the input bias current in CDS Mode is relatively small. Due to the architecture of CDS switching, the average charge loss or gain on the input node is ideally zero over the duration of a pixel. This results in a much lower input bias current, whose main source is parasitic impedances and leakage currents. As a result of the lower input bias current in CDS Mode, maintaining the DC Bias point the input node over the length of a line will require a much smaller AC input coupling capacitor.

VCLP DAC

The VCLP pin can be used to provide the reference level for incoming signals in Sample and Hold Mode. The pin is driven by the VCLP DAC, the VCLP DAC has five bits and has an approximate range of 2.9V. The VCLP DAC is controlled by the VCLP Control Register (0x04), and programmable through the serial interface.

Programmable Gain

The LM98640 provides two independent gain stages. The first stage is in the input CDS/SH circuit. The second is in the form of a Programmable Gain Amplifier (PGA).

CDS/SH Stage Gain

The CDS/SH gain is programmable to either 0dB or 6dB gain. The load presented to the user in 6dB mode is roughly twice the switched load of 0dB mode. The CDS/SH gain settings affect both channels. The CDS/SH gain bit is located in bit 2 of the Main Configuration register, and programmable through the serial interface.

PGA Gain Plots

The PGA has an 8-bit resolution with a gain range of -3 dB to 18 dB. Figure 25 below shows a plot for the gain. Each channel has a independent PGA controlled by registers CH1 PGA and CH2 PGA, and programmable through the serial interface.

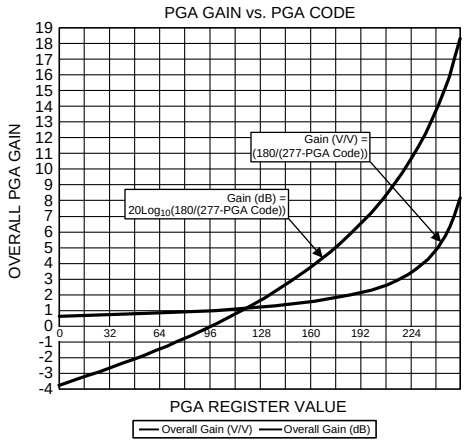


Figure 25. PGA Gain vs. PGA Gain Code

Programmable Analog Offset Correction

The LM98640 provides two analog DACs per channel to provide flexibility in offset control. Each channel has a Coarse DAC and Fine DAC which have ±8-bit resolutions (8–bit + Sign). The two DACs can be used independently or as Coarse/Fine configuration. The Coarse DAC provides a sufficient range with moderate step sizes, while the Fine DAC is for designs which need a finely tuned offset. The correction voltage is applied to the "Video" level for both Sample & Hold and CDS input modes. Because of the DACs location in the signal path, the correction range lowers as CDS gain increases, and the output referred correction steps and ranges increase with PGA gain. Table 1 provides the range and step size of each DAC.

Table 1. Analog Offset DAC Specifications

	CDS/SH Gain	Range(1)	Step Size(1)	Output ADC Codes
Coarse DAC	1x	±250 mV	1mV	±2048
	2x	±125 mV	500 µV	±2048
Fine DAC	1x	±5 mV	20 µV	±41
	2x	±2.5 mV	10 µV	±41

(1) Referred to Input

To use the Offset Correction DACs, the Coarse DAC and Fine DAC must be enabled using bits[6:5] of the Main Configuration Register (0x00). Then the desired correction value should be entered into the CDAC or FDAC register of the appropriate channel. The Offset Correction DACs use a signed binary format which is summarized in Table 2.

Table 2. Analog Offset Correction DAC Format

CDAC / FDAC Input Value	CDAC Correction (Codes)	FDAC Correction (Codes)
1 1111 1111	+2048	+41
1 0111 1111	+1024	+20
0 1111 1111	0	0
0 0111 1111	-1024	-20
0 0000 0000	-2048	-41

Analog-to-Digital Converter

The LM98640 has a 14bit Analog to Digital Converts (ADC) for each channel. Each ADC has maximum and minimum conversion rate of 40 MSPS and 5 MSPS per channel respectively. The DNL performance is +/-0.5LSB and +/-2LSB for INL for a 14bit out. The noise floor is -79dB at 2V with a programmable gain of 0dB. If an out of range pixel is presented to the ADC, the ADC will return to full compliance within two cycles of the pixel clock.

LVDS Output

LVDS Output Voltage

The LM98640 output data is presented in LVDS format. Table 3 shows the available LVDS differential output voltage (VOD) settings and its associated offset voltage (VOS).

Table 3. LVDS Differential Output Voltage Settings

VOD	VOS
250mV	1.2V
300mV	1.2V
350mV	1.1V
400mV	1.1V

LVDS Output Modes

The LM98640 has a unique serial LVDS output format to protect data transfer during ionizing doses. The format provides a buffer on either side of the data word, this is accomplished by clocking a 14-bit word using a 16-bit clock rate. In the event of an ionizing dose that affects the DLL the output clock period could fluctuate; with no buffer for the data word this fluctuation could cause the loss of one or more of the data word bits, but because the LM98640 provides the buffer the fluctuation does not cause any data loss. The data can also be sent out in two modes: Dual or Quad Lane. The following sections describe these two modes.

TXFRM Output

The LM98640 output includes a frame signal (TXFRM) that should be used to locate the beginning and end of a particular pixel's serial data word. The rising edge of TXFRM is coincident with the pixel's leading bit transition (TXOUT MSB). This TXFRM rising edge can be detected by the capturing FPGA or ASIC to mark the start of the serial data word.

In CDS mode, the input sampling amplifier has two physical paths through which a particular pixel will be sampled. These two sampling paths are a requirement in the Correlated Double Sampling architecture. The sampling of the one pixel will travel the first path (arbitrarily called an even pixel), and the sampling of the next pixel will travel the second path (called an odd pixel). The sampling will continue in an even/odd/even/odd fashion for all pixels processed in a particular channel. Due to slight variances in the sampling paths (most commonly a difference in switched capacitor matching), the processing of identical pixels through the two different paths may result in a small offset in ADC output data between the two paths. To correct this, a simple digital offset can be applied in post processing to either the even pixel data or the odd pixel data. To simplify this action, the LM98640 will indicate (with the TXFRM signal) whether the pixel traveled the even path or the odd path. For all "Odd" pixels, the TXFRM signal is high for three TXCLK periods. For "Even" pixels, the TXFRM signal is high for two TXCLK periods. In Sample and Hold Mode there is only one sampling path, therefore there is no need to indicate an even or odd pixel. As a result, the TXFRM signal is the same for every pixel in Sample and Hold mode (i.e. high for three TXCLK periods).

Output Mode 1 - Dual Lane

In Dual Lane mode each input channel has its own data output presented at 16X the pixel clock rate. A frame signal (TXFRM) is output at the pixel clock rate with the rising edge occurring coincident with the transition of the MSB of the data. In Sample/Hold Modes of operation, the falling edge is coincident with the transition of bit 7 of the data. In CDS Mode, the falling edge of TXFRM toggles between the transition of bit 9 and bit 7 of the data. A differential clock is also output with transitions aligned with the center of the data eye. Data rates for Dual Lane mode range from 80 Mbps, with a 5 MHz clock, up to 640 Mbps, with a 40 MHz clock.

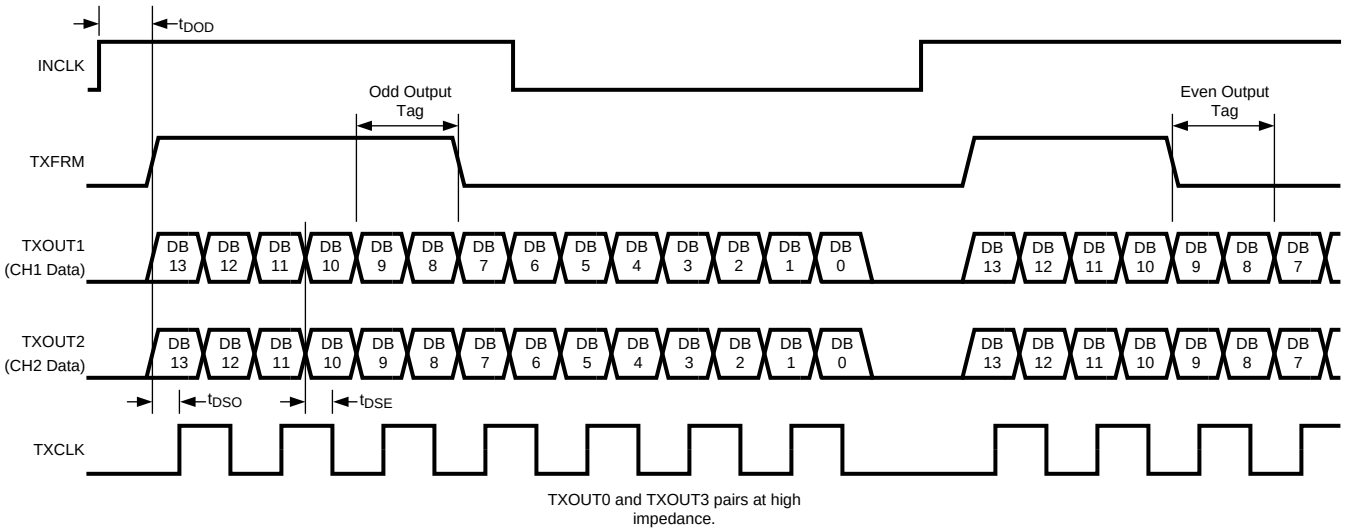


Figure 26. Dual Lane LVDS Output Timing Diagram

Output Mode 2 - Quad Lane

In Quad Lane mode each input channel is split into two data lanes which are presented at 8X the pixel rate. The MSBs (bits 13 through 7) will be presented to one channel while the LSBs (bits 6 through 0) will be presented to the other. A frame signal is run at the pixel clock rate with the rising edge coincident with the transition of the MSB of the data and the falling edge coincident with the transition of bits 10 and 3 of the data lanes for an odd output value, and coincident with the transition of bits 11 and 4 for a even output value. A differential clock is also output with rising edge transitions aligned within each data eye. Data rates for Quad Lane mode range from 40 Mbps, with a 5 MHz clock, up to 320 Mbps, with a 40 MHz clock.

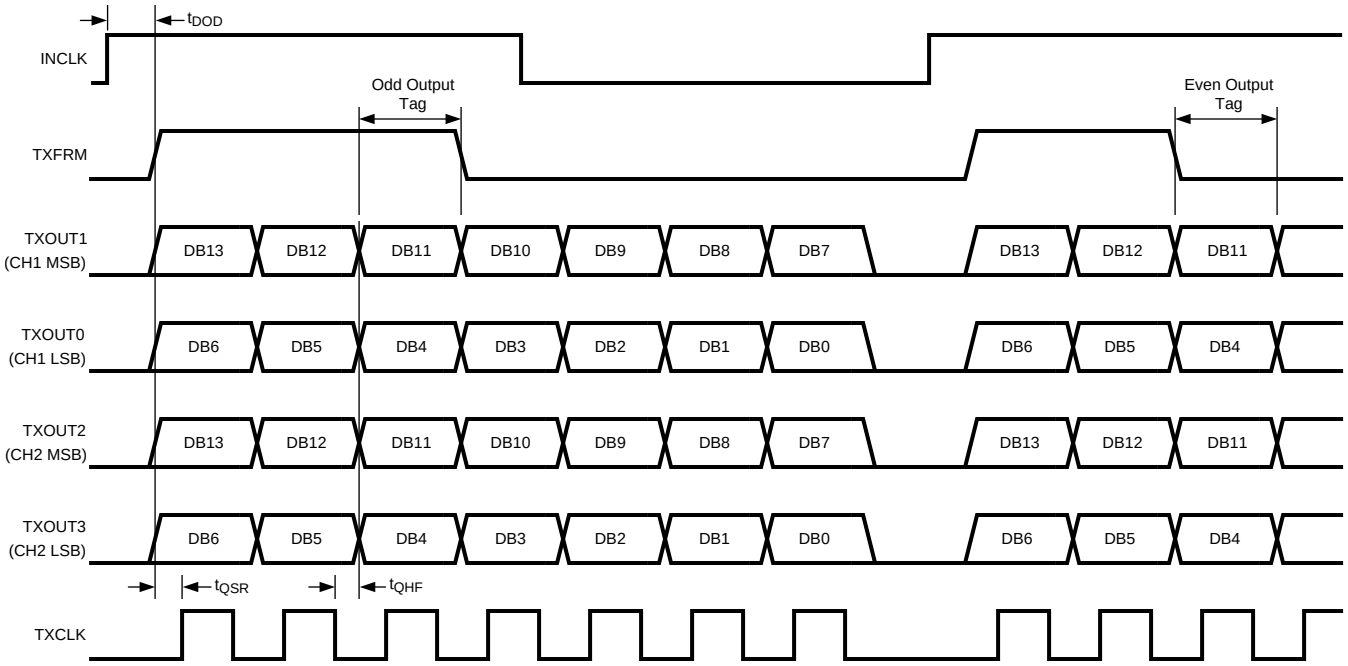


Figure 27. Quad Lane LVDS Data Output Timing Diagram

LVDS Test Modes

The LVDS test modes present programmable data patterns to the input of the LVDS serializer block. The type of pattern is selectable through the Test Pattern Control register. Once the LVDS test mode is enabled the patterns are output indefinitely. Table 4 below shows the available test pattern modes.

Table 4. Test Pattern Modes

Test Pattern Control[6:4]	Test Mode
000	Fixed Code
001	Horizontal Gradient
010	Vertical Gradient
011	Lattice Pattern
100	Strip Pattern
101	LVDS Test Pattern (Synchronous)
110	LVDS Test Pattern (Asynchronous)
111	Reserved

Each pattern consists of a Start Period and Valid Pixel region. During the Start Period the output is the minimum code (0x0000). The Valid Pixel region contains the selected Test Pattern Mode output. The length (in pixels) of the Start period is set using the Test Pattern Start register, and the width of the Valid Pixel region is set using the Test Pattern Width register.

To start the test pattern generation, enable Test Mode using bit[1] of the Test and Scan Register (0x3D). Then load all parameters for the desired test pattern into the registers, and set Pattern Enable bit of the Test Pattern Control Register (0x34). Changing pattern parameters after the Pattern Enable bit is set may result in undesired output. The pattern will start at the next leading edge of CLPIN.

Test Mode 0 - Fixed Pattern

This test mode provides an LVDS output with a fixed value output during the valid pixel region. The fixed value is set via the Test Pattern Value registers. The Test Pattern Value register is split into two registers the upper 6 bits of the test code in first register, and the lower 8 bits of the test code in the second.

Test Mode 1 - Horizontal Gradient

This mode provides LVDS data that progresses horizontally from dark to light output values. This mode is highly variable, allowing control over the starting value of the gradient, the width of the gradient, and the increment rate of the gradient. The starting value can be set in the Test Pattern Value register, the width (in number of pixels) of each gradient step is set via Test Pattern Pitch register, and increment rate (in LSBs) is set via the Test Pattern Step register. When the LVDS Horizontal Gradient test pattern is selected, the ramp begins immediately and counts to the maximum value, and then repeats throughout the entire Valid Pixel region.

Test Mode 2 - Vertical Gradient

This mode is similar to the Horizontal Gradient, only the gradient is in the vertical direction. See the Horizontal Gradient mode description for details.

Test Mode 3 - Lattice Pattern

This mode provides LVDS data that creates a lattice grid. The lattice is made of dark lines on a light background. The line output value is set by Test Pattern Step register, and background value is set by Test Pattern Value register. The number of pixels & lines in the lattice is set via Test Pattern Pitch register.

Test Mode 4 - Stripe Pattern

This mode provides LVDS data that creates a vertical stripe pattern. The stripe pattern is made of dark and light lines. The output value of the dark portion is set via Test Pattern Step register, and the light portion is set via Test Pattern Value register. The stripe width in pixels is set via Test Pattern Pitch register.

Test Mode 5 - LVDS Test Pattern (Synchronous)

This mode provides an LVDS output with a fixed value repeated continuously. The pattern starts at the leading edge of CLPIN. The fixed value is set via the Test Pattern Value registers. The Test Pattern Value register is split into two registers the upper 8 bits of the test code in first register, and the lower 8 bits of the test code in the second. This is useful for system debugging of the LVDS link and receiver circuitry.

Test Mode 6 - LVDS Test Pattern (Asynchronous)

This mode provides an LVDS output with a fixed value repeated continuously. The pattern starts asynchronously without CLPIN. The fixed value is set via the Test Pattern Value registers. The Test Pattern Value register is split into two registers the upper 8 bits of the test code in first register, and the lower 8 bits of the test code in the second. This is useful for system debugging of the LVDS link and receiver circuitry.

Psuedo Random Number Mode

This mode provides LVDS data produced from the following polynomial:

$$P(x) = X^{14} + X^{13} + X^{11} + X^{9} + 1 \quad (1)$$

To start the Psuedo Random Number mode, set the Test Mode bit of the Test and Scan Register. Then load the seed value in the Test Pattern Value register, and set the Psuedo Random Enable bit of the Test Pattern Control register. The pattern will start outputting after the next leading edge of CLPIN.

Clock Receiver

A differential clock receiver is used to generate all clock signals on the LM98640. The clock input should be externally terminated with 100 Ohms between the input clock pins. The clock may be DC or AC coupled to the AFE.

Power Trimming

The LM98640 provides an adaptive power scaling feature that allows the user to optimize power consumption based on the maximum operating frequency and the maximum amount of gain required. The power scaling mode is selectable through the PGA Power Trimming and ADC Power Trimming registers (0x02,0x03). The settings in these registers are common for both channels PGA and ADC. Using these registers the user can control the current of the two stages of the PGA, and the current for the two levels of the ADC. The following table provides a set of baseline configurations for various operating frequencies and gain ranges.

These configurations should be treated as baseline values and can be tuned to your specific application.

Operating Frequency	1-4x Max PGA Gain	1-8x Max PGA Gain
5 - 15 MSPS	PGA Power Trimming = 0x00 ADC Power Trimming = 0x00	PGA Power Trimming = 0x01 ADC Power Trimming = 0x00
15 - 25 MSPS	PGA Power Trimming = 0x01 ADC Power Trimming = 0x00	PGA Power Trimming = 0x09 ADC Power Trimming = 0x00
25 - 40 MSPS	PGA Power Trimming = 0x01 ADC Power Trimming = 0x08	PGA Power Trimming = 0x09 ADC Power Trimming = 0x08

Powerdown Modes

The LM98640 provides several ways to save power when the device is not in normal usage mode. Using the Powerdown Control Register (0x01) the part can be placed into Powerdown Mode, or Single Channel Mode. In Powerdown Mode (Powerdown Control, bit[7]) the following blocks are placed in a Powerdown mode: VCLP, Channel 1 & 2 Reference Buffers, Channel 1 & 2 PGA OpAmps, and Channel 1 & 2 Amplifiers. Powerdown Mode will override all other Powerdown Control Register bits. To place the part in Single Channel Mode each block of the unused channel can be powered down using their respective control bits (Powerdown Control, bits[5:0]). If an external reference clamp is used the VCLP block can be powered down during any Power mode. For applications operating at a low enough frequency additional power can be saved by powering down one channel reference buffer, then externally tie both channel's reference pins together.

Serial Interface

A serial interface is used to write and read the configuration registers. The interface is a four wire interface using SCLK, $\overline{\text{SEN}}$, SDI, and SDO connections. The serial interface clock (SCLK) must be less than the main input clock (INCLK) for INCLK speeds of less than 20 MHz, for INCLK speeds greater than 20 MHz SCLK must remain below 20 MHz. The main input clock (INCLK) to the LM98640 must be active during all Serial Interface commands. The Serial Interface pins are high impedance while $\overline{\text{SEN}}$ is high, this allows multiple slave devices to be used with a single master device.

After power-up, the configuration registers must be written with the baseline values, using the serial interface, to place the part in a valid state.

Writing to the Serial Registers

To write to the serial registers using the four wire interface, the timing diagram shown in Figure 28 must be met. First, SEN is toggled low. At the rising edge of the first clock, the master should assume control of the SDI pin and begin issuing the write command. The write command is built of a "write" bit (0), device address bit (0), six bit register address, and eight bit register value to be written. SDI is clocked into the LM98640 at the rising edge of SCLK. The LM98640 assumes control of the SDO pin during the first eight clocks of the cycle. During this period, data is clocked out of the device at the rising edge of SCLK. The eight bit value clocked out is the contents of the previously addressed register, regardless if the previous command was a read or a write. When SEN toggles high, the register is written to, and the LM98640 now functions with this new data.

Reading the Serial Registers

To read to the serial registers using the four wire interface, the timing diagram shown in Figure 29 must be met. Reading the registers takes two cycles. To start the first cycle, $\overline{\text{SEN}}$ is toggled low. At the rising edge of the first clock, the master should assume control of the SDI pin and begin issuing the read command. The read command is built of a "read" bit (1), device address bit (0), six bit register address, and eight "don't care" bits. SDI is clocked into the LM98640 at the rising edge of SCLK. $\overline{\text{SEN}}$ is toggled high for a delay of at least t_{SENW} (see Figure 30). The second cycle begins when $\overline{\text{SEN}}$ is toggled low. The LM98640 assumes control of the SDO pin during the first eight clocks of the cycle. During this period, data is clocked out of the device at the rising edge of SCLK. The eight bit value clocked out is the contents of the previously addressed register. The next command can be sent on the SDI pin simultaneously during this second cycle. When $\overline{\text{SEN}}$ toggles high, the register is not written to, but its contents are staged to be outputted at the beginning of the next command.

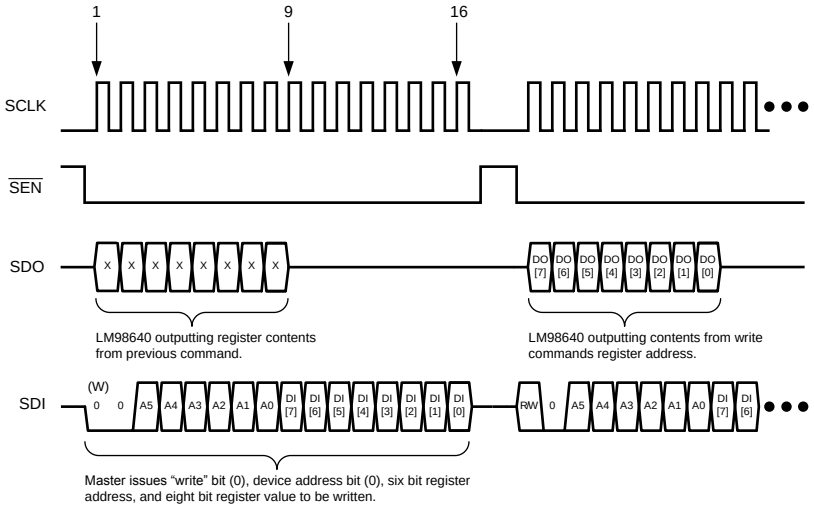


Figure 28. Four-Wire Serial Write

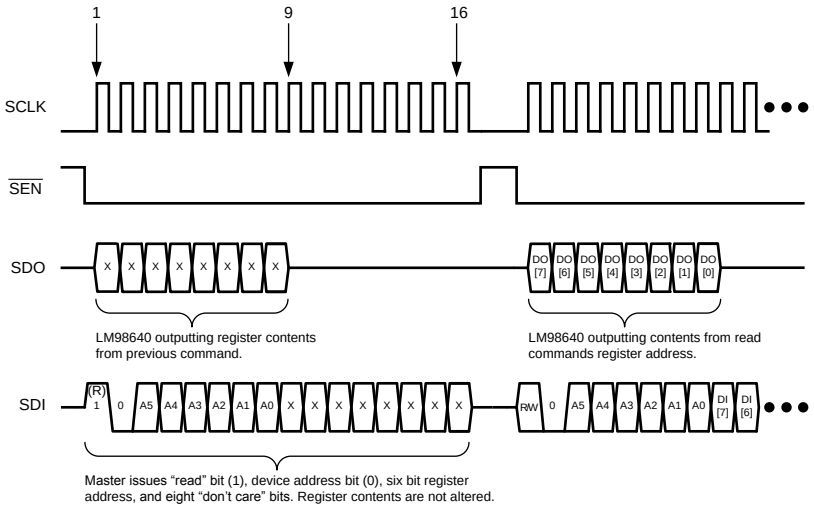


Figure 29. Four-Wire Serial Read

Serial Interface Timing Details

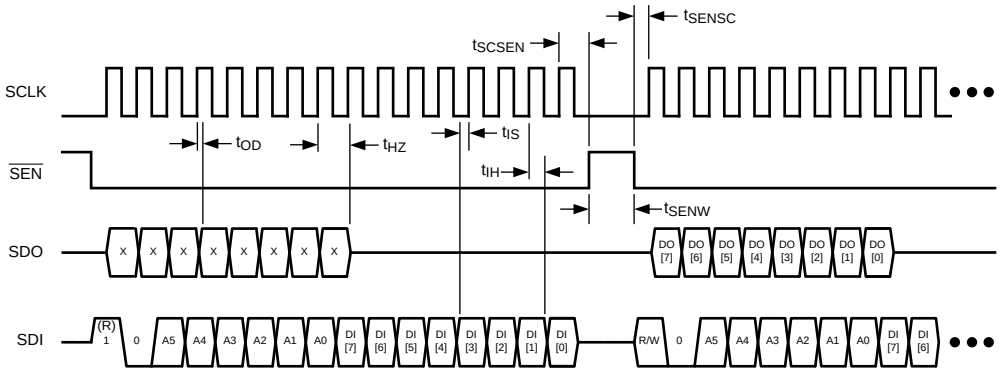


Figure 30. Serial Interface Specification Diagram

Supply/Grounding, Layout and Thermal Recommendations

Power Planes

Power for the LM98640 should be provided through a broad plane which is located on one layer adjacent to the ground plane(s). Placing the power and ground planes on adjacent layers will provide low impedance decoupling of the AFE supplies, especially at higher frequencies. The output of a linear regulator should feed into the power plane through a low impedance multi-via connection. The power plane should be split into individual power peninsulas near the AFE. Each peninsula should feed a particular power bus on the AFE, with decoupling for that power bus connecting the peninsula to the ground plane near each power/ground pin pair. Using this technique can be difficult on many printed circuit CAD tools. To work around this, zero ohm resistors can be used to connect the power source net to the individual nets for the different AFE power buses. As a final step, the zero ohm resistors can be removed and the plane and peninsulas can be connected manually after all other error checking is completed.

Bypass Capacitors

The general recommendation is to have one 100 nF capacitor for each power/ground pin pair. The capacitors should be surface mount multi-layer ceramic chip capacitors.

Ground Plane

Grounding should be done using continuous full ground planes to minimize the impedance for all ground return paths, and provide the shortest possible image/return path for all signal traces.

Thermal Management

The exposed pad on bottom of the package is attached to the back of the die to act as a heat sink. Connecting this pad to the PCB ground planes with a low thermal resistance path is the best way to remove heat from the AFE. This pad should also be connected to the ground planes through low impedance path for electrical purposes.

Table 5. Configuration Registers

Registers need to be written with baseline values after power-up to place part in a valid state.										
Address (Binary)	**Register Title (Mnemonic)**	**Baseline (Binary)**	**Register/Bit Description**							
			Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Analog Configuration										
00 0000	Main Configuration	0000 0100	Not Used	Coarse DAC Enable	Fine DAC Enable	Reserved	CLPIN Gating Enable	CDS Gain Enable	Reserved	CDS Enable
00 0001	Powerdown Control	0000 0000	Master Powerdown	VCLP Powerdown	Ch2 Ref Buf Powerdown	Ch1 Ref Buf Powerdown	Ch2 PGA Powerdown	Ch1 PGA Powerdown	Ch2 ADC Powerdown	Ch1 ADC Powerdown
00 0010	PGA Power Trimming	0010 0100	Reserved		PGA Stage 2 Bias Current Trimming			PGA Stage 1 Bias Current Trimming		
00 0011	ADC Power Trimming	0101 1011	Reserved		ADC Current Trimming 2			ADC Current Trimming 1		
00 0100	VCLP Control	0111 0100	Not Used	Buffer Enable	VCLP Enable	VCLP Voltage Level				
00 0101	LVDS Output Modes	0000 1110	Clear	Reserved	Reserved	Reserved	Quad Lane Enable	LVDS Enable	LVDS Control	
00 0110	Sample & Hold	1000 0001	S/H Enable	Not Used				Ref Buf Power Level		Reserved
00 0111	Status	0000 0000	Not Used							False Lock
00 1000	Reserved	0000 0000	Reserved							
00 1001	Clock Monitor	0000 0000	Not Used			Enable/Select		Not Used		
00 1010	Reserved	0000 0000	Not Used							

Table 5. Configuration Registers (continued)

Registers need to be written with baseline values after power-up to place part in a valid state.									
Address (Binary)	**Register Title (Mnemonic)**	**Baseline (Binary)**	**Register/Bit Description**						
			Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
00 1011	Reserved	0000 0000	Not Used							
00 1100	Reserved	0000 0000	Not Used							
00 1101	Reserved	0000 0000	Not Used							
00 1110	Reserved	0000 0000	Not Used							
00 1111	Reserved	0000 0000	Not Used							
Gain & Offset DAC Configuration										
01 0000	CDAC1	0000 0000	Not Used							Offset bit 8
01 0001	CDAC1	1111 1111	Offset Value bits 7:0							
01 0010	FDAC1	0000 0000	Not Used							Offset bit 8
01 0011	FDAC1	1111 1111	Offset Value bits 7:0							
01 0100	Reserved	0000 0000	Not Used							
01 0101	PGA1	0110 0001	PGA Gain Value							
01 0110	Reserved	0000 0000	Not Used							
01 0111	Reserved	0000 0000	Not Used							
01 1000	CDAC2	0000 0000	Not Used							Offset Bit 8
01 1001	CDAC2	1111 1111	Offset Value bits 7:0							
01 1010	FDAC2	0000 0000	Not Used							Offset Bit 8
01 1011	FDAC2	1111 1111	Offset Value bits 7:0							
01 1100	PGA2	0110 0001	PGA Gain Value							
01 1101	Reserved	0000 0000	Not Used							
01 1110	Reserved	0000 0000	Not Used							
01 1111	Reserved	0000 0000	Not Used							
Timing Configuration										
10 0000	Clamp Start	0000 1000	Not Used			Clamp Start Index				
10 0001	Clamp End	0001 1100	Not Used			Clamp End Index				
10 0010	Sample Start	0010 1000	Not Used			Sample Start Index				
10 0011	Sample End	0011 1100	Not Used			Sample End Index				
10 0100	Reserved	0011 0100	Reserved							
10 0101	INCLK Range	0000 0010	Not Used	INCLK Range			Not Used		Reserved	
10 0110	Reserved	0000 0000	Not Used							
10 0111	Reserved	0000 0000	Not Used							
10 1000	DLL Configuration	0000 1111	Reserved							DLL Reset
10 1001	Reserved	0000 0000	Not Used							
10 1010	Reserved	0000 0000	Not Used							
10 1011	Reserved	0000 0000	Not Used							
10 1100	Reserved	0000 0000	Not Used							
10 1101	Reserved	0000 0000	Not Used							
10 1110	Reserved	0000 0000	Not Used							
10 1111	Reserved	0000 0000	Not Used							
Digital Configuration Registers										
11 0000	Test Pattern Start	0000 0000	Start Upper Bits							
11 0001	Test Pattern Start	0000 0000	Start Lower Bits							

Table 5. Configuration Registers (continued)

Registers need to be written with baseline values after power-up to place part in a valid state.										
Address (Binary)	**Register Title (Mnemonic)**	**Baseline (Binary)**	**Register/Bit Description**							
			Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
11 0010	Test Pattern Width	0000 0000	Width Upper Bits							
11 0011	Test Pattern Width	0000 0000	Width Lower Bits							
11 0100	Test Pattern Control	0000 0000	Pattern Enable	Pattern Mode			Pseudo Random Enable	Seed Enable	Pattern Output Channel	
11 0101	Test Pattern Pitch	0000 0000	Test Pattern Pitch							
11 0110	Test Pattern Step	0000 0000	Test Pattern Step Code							
11 0111	Test Pattern Channel Offset	0000 0000	Not Used				Test Pattern Channel Offset			
11 1000	Test Pattern Value	0000 0000	Pattern Upper Bits							
11 1001	Test Pattern Value	0000 0000	Pattern Lower Bits							
11 1010	Reserved	0000 0000	Not Used							
11 1011	Reserved	0000 0000	Not Used							
11 1100	Digital Configuration	0000 0000	Not Used							Auto Read
11 1101	Test & Scan Control	0000 0000	Not Used		Pattern Voting Enable	U-Wire Voting Enable	Not Used	Test Reset	Test Mode	Not Used
11 1110	Device ID	0000 0001	Device Revision ID							
11 1111	Reserved	0000 0000	Not Used							

Register Definitions

Table 6. Register Definitions - Analog Configuration

Registers need to be written with baseline values after power-up to place part in a valid state.				
Address (Binary)	**Register Title**	**Baseline (Binary)**	**Bit(s)**	**Description**
00 0000	Main Configuration	0000 0100	[7:0]	Main Configuration
			[7]	Not Used
			[6]	Coarse DAC Enable
				0 Disable
				1 Enable
			[5]	Fine DAC Enable
				0 Disable
				1 Enable
			[4]	Reserved
			[3]	CLPIN Gating Enable
				0 CLPIN not gated by CLAMP
				1 CLPIN gated by CLAMP (=logical "and" of CLPIN and CLAMP)
			[2]	Gain Mode Select. Selects either a 1x or 2x gain mode in the CDS/Sample/Hold Block
				0 1x Gain in the CDS/Sample/Hold Block
				1 2x Gain in the CDS/Sample/Hold Block
			[1]	Reserved. Set to 0.
			[0]	CDS / Sample/Hold Mode select.
				0 Disabled. Correlated Double Sample Mode disabled.
				1 Enabled. Correlated Double Sample Mode enabled.

Table 6. Register Definitions - Analog Configuration (continued)

Registers need to be written with baseline values after power-up to place part in a valid state.				
Address (Binary)	**Register Title**	**Baseline (Binary)**	**Bit(s)**	**Description**
00 0001	Powerdown Control	0000 0000	[7:0]	Powerdown Control Register
			[7]	Master Powerdown
				0 Fully Powered.
				1 Powerdown Mode. Over rides bits [6:0].
			[6]	VCLP Powerdown
				0 VCLP Fully Powered.
				1 VCLP Powerdown Mode.
			[5]	Channel 2 Reference Buffer Powerdown
				0 Reference Buffer Fully Powered.
				1 Reference Buffer Powerdown Mode.
			[4]	Channel 1 Reference Buffer Powerdown
				0 Reference Buffer Fully Powered.
				1 Reference Buffer Powerdown Mode.
			[3]	Channel 2 PGA Powerdown
				0 OpAmp Fully Powered.
				1 OpAmp Powerdown Mode.
			[2]	Channel 1 PGA Powerdown
				0 OpAmp Fully Powered.
				1 OpAmp Powerdown Mode.
			[1]	Channel 2 ADC Powerdown
				0 Amplifier Fully Powered.
				1 Amplifier Powerdown Mode.
			[0]	Channel 1 ADC Powerdown
				0 ADC Fully Powered.
				1 ADC Powerdown Mode.
00 0010	PGA Power Trimming	0010 0100	[7:0]	PGA Power Trimming Register.
			[7:6]	Not Used
			[5:3]	PGA Stage 1 Current Trimming
				Tunable between **000**-Weak to **111**-Strong (Default **100**)
			[2:0]	PGA Stage 2 Current Trimming
				Tunable between **000**-Weak to **111**-Strong (Default **100**)
00 0011	ADC Power Trimming	0101 1011	[7:0]	ADC Power Trimming Register.
			[7:6]	Reserved. Set to 2'b01.
			[5:3]	ADC Current Trimming 2(Not Binary Weighted)
				000 25% Power
				001 50% Power
				011 75% Power (Default)
				111 100% Power
			[2:0]	ADC Current Trimming 1 (Not Binary Weighted)
				000 25% Power
				001 50% Power
				011 75% Power (Default)
				111 100% Power

Table 6. Register Definitions - Analog Configuration (continued)

Registers need to be written with baseline values after power-up to place part in a valid state.				
Address (Binary)	**Register Title**	**Baseline (Binary)**	**Bit(s)**	**Description**
00 0100	VCLP Control	0111 0100	[7:0]	Voltage Clamp Buffer Control Register.
			[7]	Not Used
			[6]	Buffer Enable
				0 Disabled. Resistor Ladder is driving VCLP pin.
				1 Enabled. Resistor Ladder is buffered to VCLP pin.
			[5]	VCLP Enable
				0 Disabled. VCLP pin can be externally driven.
				1 Enabled. VCLP pin is in output mode.
			[4:0]	Voltage Level of VCLP pin.
				VCLP range is 200 mV to 3.1V in 100 mV steps for (binary) settings 00000 to 11101. Settings 11110 and 11111 are not used.
00 0101	LVDS Output Modes	0000 1110	[7:0]	LVDS Output Configuration Register.
			[7]	Serializer Data Reset. (Not self-clearing)
			[6:4]	Not Used.
			[3]	LVDS Output Mode
				0 Dual Lane Mode (see Output Mode 1 - Dual Lane)
				1 Quad Lane Mode (see Output Mode 2 - Quad Lane)
			[2]	LVDS Driver Enable.
				0 LVDS Drivers Disabled
				1 LVDS Drivers Enabled
				(Note: In Dual Lane Mode TX0 and TX3 are disabled regardless of driver enable)
			[1:0]	LVDS Amplitude and Common Mode Voltage.
				00 250mV (1.2V DC Offset)
				01 300mV (1.2V DC Offset)
				10 350 mV (1.1V DC Offset)
				11 400 mV (1.1V DC Offset)
00 0110	Sample & Hold	1000 0001	[7:0]	Sample & Hold Mode Register
			[7]	Sample & Hold Mode Enable
				0 Disabled.
				1 Enabled.
			[6:3]	Not Used.
			[2:1]	Reference Buffer Power Level
				11 100% Power. Used for F_{INCLK} = 20-40 MHz.
				10 60% Power. Used for F_{INCLK} = 10-20 MHz.
				01 60% Power. Used for F_{INCLK} = 10-20 MHz.
				00 30% Power. Used for F_{INCLK} = 5-10 MHz.
			[0]	Reserved.
00 0111	Status	0000 0000	[7:0]	Status Register. (Read Only)
			[7:1]	Not Used.
			[0]	False Lock Detect.
				Indicates if DLL is locked into a half frequency state.

Table 6. Register Definitions - Analog Configuration (continued)

Registers need to be written with baseline values after power-up to place part in a valid state.				
Address (Binary)	**Register Title**	**Baseline (Binary)**	**Bit(s)**	**Description**
00 1001	Clock Monitor	0000 0000	[7:0]	Internal Clock Signal Monitor Register
			[7:5]	Not Used.
			[4:3]	Enable and select clocks to be monitored on the Digital Timing Monitor. (DTM)
				00 Disable Digital Timing Monitor Pins (DTM0, DTM1)
				01 Send $CLAMP_{EVEN}$ to DTM0 pin, and $SAMPLE_{EVEN}$ to DTM1
				10 Send $CLAMP_{ODD}$ to DTM0 pin, and $SAMPLE_{ODD}$ to DTM1
				11 Send ODD tag and ADC Clock to the DTM.
			[2:0]	Reserved. Set to 000.

Table 7. Register Definitions - GAIN & Offset DAC Configuration

Registers need to be written with baseline values after power-up to place part in a valid state.				
Address (Binary)	**Register Title**	**Baseline (Binary)**	**Bit(s)**	**Description**
01 0000	CDAC1	0000 0000	[7:0]	Channel 1 Coarse DAC Register.
			[7:1]	Not Used.
			[0]	Bit 8 of Channel 1 Coarse DAC Offset Value.
01 0001	CDAC1	1111 1111	[7:0]	Channel 1 Coarse DAC Offset Value bits 7:0.
01 0010	FDAC1	0000 0000	[7:0]	Channel 1 Fine DAC Register.
			[7:1]	Not Used.
			[0]	Bit 8 of Channel 1 Fine DAC Offset Value.
01 0011	FDAC1	1111 1111	[7:0]	Channel 1 Fine DAC Offset Value bits 7:0.
01 0101	PGA1	0110 0001	[7:0]	Channel 1 Programmable Gain Amplifier Value.
01 1000	CDAC2	0000 0000	[7:0]	Channel 2 Coarse DAC Register.
			[7:1]	Not Used.
			[0]	Bit 8 of Channel 2 Coarse DAC Offset Value.
01 1001	CDAC2	1111 1111	[7:0]	Channel 2 Coarse DAC Offset Value bits 7:0.
01 1010	FDAC2	0000 0000	[7:0]	Channel 2 Fine DAC Register.
			[7:1]	Not Used.
			[0]	Bit 8 of Channel 2 Fine DAC Offset Value.
01 1011	FDAC2	1111 1111	[7:0]	Channel 2 Fine DAC Offset Value bits 7:0.
01 1100	PGA2	0110 0001	[7:0]	Channel 2 Programmable Gain Amplifier Value.

Table 8. Register Definitions - Timing Configuration

Registers need to be written with baseline values after power-up to place part in a valid state.				
Address (Binary)	**Register Title**	**Baseline (Binary)**	**Bit(s)**	**Description**
10 0000	Clamp Start	0000 1000	[7:0]	Clamp Start Register.
			[7:6]	Not Used.
			[5:0]	CLAMP Starting Index. 0-63d position for rising edge of CLAMP signal. Valid only in CDS Mode.
10 0001	Clamp End	0001 1100	[7:0]	Clamp End Register.
			[7:6]	Not Used.
			[5:0]	CLAMP End Index. 0-63d position for falling edge of CLAMP signal. Valid only in CDS Mode.

Table 8. Register Definitions - Timing Configuration (continued)

Registers need to be written with baseline values after power-up to place part in a valid state.				
Address (Binary)	**Register Title**	**Baseline (Binary)**	**Bit(s)**	**Description**
10 0010	Sample Start	0010 1000	[7:0]	Sample Start Register.
			[7:6]	Not Used.
			[5:0]	SAMPLE starting Index. 0-63d position for rising edge of SAMPLE signal.
10 0011	Sample End	0011 1100	[7:0]	Sample End Register.
			[7:6]	Not Used.
			[5:0]	SAMPLE End Index. 0-63d position for falling edge of SAMPLE signal.
10 0101	INCLK Range	0000 0010	[7:0]	INCLK Range Register.
			[7]	Not Used.
			[6:4]	INCLK Range.
				000 25-40 MHz Operation
				001 14-25 MHz Operation
				010 10-14 MHz Operation
				011 7.5-10 MHz Operation
				100 6-7.5 MHz Operation
				101 5-6 MHz Operation
				110 Not Used
				111 Not Used
			[3:2]	Not Used.
			[1:0]	DLL Range
				11 Reserved
				10 14-40 MHz Operation
				01 7.5-14 MHz Operation
				00 5 -7.5 MHz Operation
10 1000	DLL Configuration	0000 1111	[7:0]	DLL Configuration Register
			[7:1]	Reserved
			[0]	DLL Reset. (Self Clearing)

Table 9. Register Definitions - Digital Configuration

Registers need to be written with baseline values after power-up to place part in a valid state.				
Address (Binary)	**Register Title**	**Baseline (Binary)**	**Bit(s)**	**Description**
11 0000	Test Pattern Start	0000 0000	[15:8]	Upper 8 bits of the Test Pattern start value. Specifies the number of pixels after the leading edge of CLPIN to the Valid Pixel region.
11 0001	Test Pattern Start	0000 0000	[7:0]	Lower 8 bits of the Test Pattern start value. Specifies the number of pixels after the leading edge of CLPIN to the Valid Pixel region.
11 0010	Test Pattern Width	0000 0000	[15:8]	Upper 8 bits of the Test Pattern Width value. Specifies, in number of pixels, the width of the Valid Pixel region.
11 0011	Test Pattern Width	0000 0000	[7:0]	Lower 8 bits of the Test Pattern Width value. Specifies, in number of pixels, the width of the Valid Pixel region.

Table 9. Register Definitions - Digital Configuration (continued)

Registers need to be written with baseline values after power-up to place part in a valid state.				
Address (Binary)	**Register Title**	**Baseline (Binary)**	**Bit(s)**	**Description**
11 0100	Test Pattern Control	0000 0000	[7:0]	Test Pattern Control Register.
			[7]	Programmable Pattern Switch
				0 Disabled. Normal LVDS output operation.
				1 Enabled. AFE outputs LVDS test patterns.
			[6:4]	Test Pattern Mode
				000 Fixed Code
				001 Horizontal Gradient Scan (Main Scan)
				010 Vertical Gradient Scan (Sub Scan)
				011 Grid Scan (Lattice Pattern)
				100 Strip Pattern
				101 LVDS Test Pattern. (Synchronous to CLPIN)
				110 LVDS Test Pattern. (Asynchronous)
				111 Not Used.
			[3]	Pseudo Random Pattern Enable.
				Overrides Programmable Patter Switch setting (bit 7).
				Normally only one should be on.
			[2]	Load Seed Enable.
				When set, the seed value in the Test Pattern Value Register is loaded in the LFSR at the leading edge of CLPIN.
			[1:0]	Test Pattern Output Channel Select.
				00 Both Channels
				01 Channel 1
				10 Channel 2
				11 Not Used
11 0101	Test Pattern Pitch	0000 0000	[7:0]	Test Pattern pitch, specifies number of pixels for H Gradient pattern and Stripe pattern, or number of lines in the V Gradient pattern, or specifies pixels & lines in the Lattice pattern.
11 0110	Test Pattern Step	0000 0000	[7:0]	Test Pattern Step Code. Specifies step size in LSB codes the pattern is incremented in H Gradient and V Gradient pattern. In Lattice and Stripe pattern it specifies the code during the lower step.
11 0111	Test Pattern Channel Offset	0000 0000	[7:0]	Test Pattern Channel Offset Register.
			[7:4]	Not Used.
			[3:0]	Test Pattern Channel Offset. This specifies the number of lines the pattern on Channel 2 is delayed from Channel 1. This offset is maintained throughout the pattern.
11 1000	Test Pattern Value	0000 0000	[15:8]	Upper 8 bits of Test Pattern Value Register. Specifies the upper 8 bits of the test value code during Fixed Pattern and LVDS test, initial value during H Gradient & V Gradient pattern, and higher value in the Lattice and Stripe Pattern.
11 1001	Test Pattern Value	0000 0000	[7:0]	Lower 6 bits of Test Pattern Value Register. Specifies the lower 6 bits of the test code value during Fixed Pattern and LVDS test, initial value during H Gradient & V Gradient pattern, and higher value in the Lattice and Stripe Pattern.

Table 9. Register Definitions - Digital Configuration (continued)

Registers need to be written with baseline values after power-up to place part in a valid state.				
Address (Binary)	**Register Title**	**Baseline (Binary)**	**Bit(s)**	**Description**
11 1100	Digital Configuration	0000 0000	[7:0]	Serial Communication Configuration Register.
			[7:1]	Not Used.
			[0]	Micro-Wire Automatic Read Disable.
				0 Read data is always sent out on SDO during the first 8 SCLK cycles.
				The register is selected by the register address in the previous cycle. (read or write)
				1 Automatic read is disabled.
				To read from a register two cycles need to be initiated by the master, first cycle should be a read with the correct register address and second can be a dummy read or read from another address or a write cycle, and the data is sent first 8 SCLK of the second cycle. After a write command SDO remains in Tri-State during first 8 SCLK.
11 1101	Test & Scan Control	0000 0000	[7:0]	Test & Scan Control Register
			[7:6]	Not Used.
			[5]	Test Pattern Voting Switch.
				0 Enable. Circuit Redundancy Voting is active.
				1 Disable. First redundancy block output is used.
			[4]	Micro-wire Voting Switch.
				0 Enable. Circuit Redundancy Voting is active.
				1 Disable. First Micro-wire block output is used.
			[3]	Not Used.
			[2]	Test Reset. Resets the test block when High, normal test block function when Low. This bit is not self-clearing.
			[1]	Test Mode Enable.
				0 Disable.
				1 Enable. Needed to run Test Pattern functions.
			[0]	Not Used.
11 1110	Device ID	0000 0001	[7:0]	Device Revision ID.

REVISION HISTORY

Changes from Original (May 2013) to Revision A	Page
• Changed layout of National Data Sheet to TI format	37

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM98640CILQ/NOPB	ACTIVE	VQFN	NKE	68	168	TBD	Call TI	Call TI			Samples

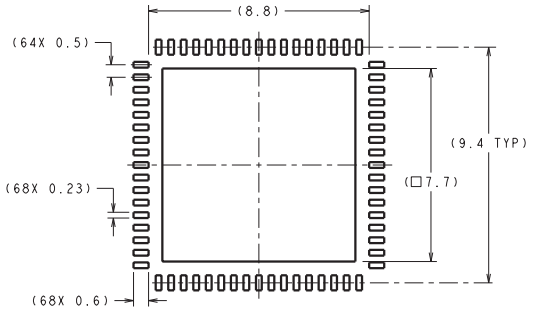
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

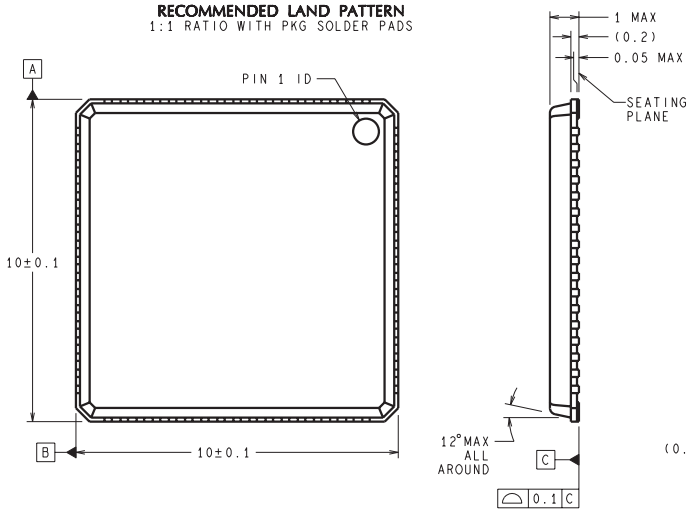
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

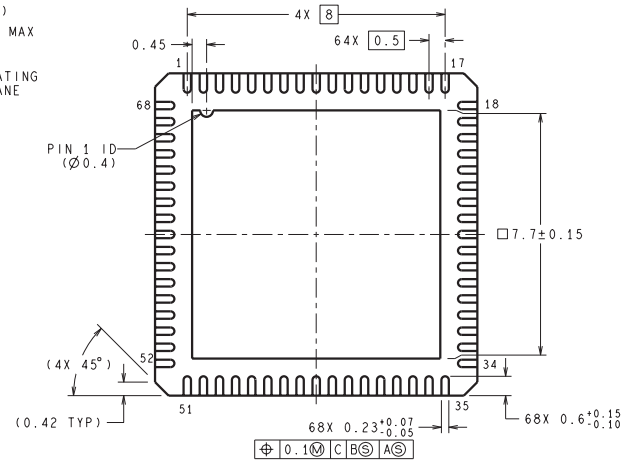
NKE0068A



RECOMMENDED LAND PATTERN
1:1 RATIO WITH PKG SOLDER PADS

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY





LQA68A (Rev B)

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265