LMH6570 2:1 High Speed Video Multiplexer

Check for Samples: LMH6570

FEATURES

- **500 MHz, 500 mV_{PP}, −3 dB Bandwidth, A_V=2**
- **400 MHz, 2V_{PP}, −3 dB Bandwidth, A_V=2**
- **8 ns Channel Switching Time**
- **70 dB Channel to Channel Isolation @ 10 MHz**
- **0.02%, 0.05° Diff. Gain, Diff. Phase**
- **0.1 dB Gain Flatness to 150 MHz**
- **2200 V/µs Slew Rate**
- **Wide Supply Voltage Range: 6V (±3V) to 12V (±6V)**
- **−68 dB HD2 @ 5 MHz**
- **−84 dB HD3 @ 5 MHz**

APPLICATIONS

- **Video Router**
- **Multi Input Video Monitor**
- **Instrumentation / Test Equipment**
- **Receiver IF Diversity Switch**
- **Multi Channel A/D Driver**
- **Picture in Picture Video Switch**

DESCRIPTION

The LMH™6570 is a high performance analog multiplexer optimized for professional grade video and other high fidelity, high bandwidth analog applications. The output amplifier selects one of two buffered input signals based on the state of the SEL pin. The LMH6570 provides a 400 MHz bandwidth at 2 V_{PP} output signal levels. Multimedia and high definition television (HDTV) applications can benefit from the LMH6570's 0.1 dB bandwidth of 150 MHz and its 2200 V/µs slew rate.

The LMH6570 supports composite video applications with its 0.02% and 0.05° differential gain and phase errors for NTSC and PAL video signals while driving a single, back terminated 75Ω load. An 80 mA linear output current is available for driving multiple video load applications.

The LMH6570 gain is set by external feedback and gain set resistors for maximum flexibility.

The LMH6570 is available in the 8-pin SOIC package.

Connection Diagram

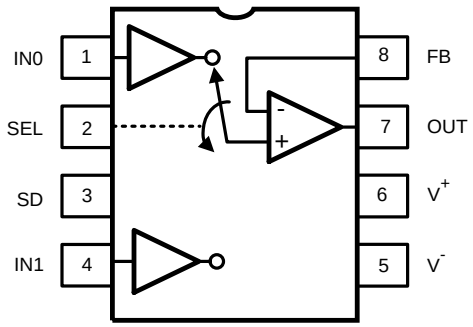


Figure 1. 8-Pin SOIC - Top View
See D Package

Truth Table

SEL	SD	OUTPUT
1	0	IN1 * (1+RF/RG)
0	0	IN0 * (1+RF/RG)
X	1	Shutdown

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

ESD Tolerance(3)	Human Body Model	2000V
	Machine Model	200V
Supply Voltage ($V^+ - V^-$)		13.2V
I_{OUT}(4)		130 mA
Signal & Logic Input Pin Voltage		±(V_S+0.6V)
Signal & Logic Input Pin Current		±20 mA
Maximum Junction Temperature		+150°C
Storage Temperature Range		−65°C to +150°C
Soldering Information: See SNOA549		

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For specifications, see the Electrical Characteristics tables.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Human Body model, 1.5kΩ in series with 100 pF. Machine model, 0Ω In series with 200 pF
(4) The maximum output current (I_{OUT}) is determined by the device power dissipation limitations (The junction temperature cannot be allowed to exceed 150°C). See POWER DISSIPATION of the Application Notes for more details. A short circuit condition should be limited to 5 seconds or less.

Operating Ratings(1)

Operating Temperature			−40 °C to 85 °C
Supply Voltage Range			6V to 12V
Thermal Resistance	Package	(θ_{JA})	150°C/W
	8-Pin SOIC	(θ_{JC})	50°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For specifications, see the Electrical Characteristics tables.

±5V Electrical Characteristics

V_S = ±5V, R_L = 100Ω, R_F=576Ω, A_V=2 V/V, T_J=25 °C, Unless otherwise specified. **Bold** numbers specify limits at temperature extremes.

Symbol	Parameter	Conditions(1)	Min(2)	Typ(3)	Max(2)	Units
Frequency Domain Performance						
SSBW	−3 dB Bandwidth	V_{OUT} = 0.5 V_{PP}		500		MHz
LSBW	–3 dB Bandwidth	V_{OUT} = 2 V_{PP}(4)		400		MHz
.1 dBBW	0.1 dB Bandwidth	V_{OUT} = 0.25 V_{PP}		150		MHz
DG	Differential Gain	R_L = 150Ω, f=4.43 MHz		0.02		%
DP	Differential Phase	R_L = 150Ω, f=4.43 MHz		0.05		deg
XTLK	Channel to Channel Crosstalk	All Hostile, f = 5 MHz		−70		dBc
Time Domain Response						
TRS	Channel to Channel Switching Time	Logic transition to 90% output		8		ns
	Enable and Disable Times	Logic transition to 90% or 10% output.		10		ns
TRL	Rise and Fall Time	4V Step		2.4		ns

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No specification of parametric performance is indicated in the electrical tables under conditions of internal self heating where $T_J > T_A$. See Application Notes for information on temperature de-rating of this device. Min/Max ratings are based on product testing, characterization and simulation. Individual parameters are tested as noted.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods.
(3) Typical numbers are the most likely parametric norm.
(4) Parameter ensured by design.

±5V Electrical Characteristics (continued)

V_S = ±5V, R_L = 100Ω, R_F=576Ω, A_V=2 V/V, T_J=25 °C, Unless otherwise specified. **Bold** numbers specify limits at temperature extremes.

Symbol	Parameter	Conditions[1]	Min[2]	Typ[3]	Max[2]	Units
TSS	Settling Time to 0.05%	2V Step		17		ns
OS	Overshoot	2V Step		5		%
SR	Slew Rate	4V Step[4][5]		2200		V/µs
Distortion						
HD2	2nd Harmonic Distortion	2 V_{PP} , 5 MHz		−68		dBc
HD3	3rd Harmonic Distortion	2 V_{PP} , 5 MHz		−84		dBc
IMD	3rd Order Intermodulation Products	10 MHz, Two tones 2 Vpp at output		−80		dBc
Equivalent Input Noise						
VN	Voltage	>1 MHz, Input Referred		5		nV/√HZ
ICN	Current	>1 MHz, Input Referred		5		pA/√Hz
Static, DC Performance						
CHGM	Channel to Channel Gain Difference	DC, Difference in gain between channels		±0.005	±0.034 **±0.036**	%
VIO	Input Offset Voltage	V_{IN} = 0V		1	±15 **±21**	mV
DVIO	Offset Voltage Drift[6]			30		µV/°C
IBN	Input Bias Current[7]	V_{IN} = 0V		−3	±8 **±10**	µA
DIBN	Bias Current Drift[6]			11		nA/°C
IBI	Inverting Input Bias Current[8]	Pin 8, Feedback point, V_{IN} = 0V		−3	±18 **±22**	uA
PSRR	Power Supply Rejection Ratio	DC, Input referred	48 **46**	50		dB
ICC	Supply Current	No Load, Shutdown Pin (SD) > 0.8V		13.8	15 **16**	mA
	Supply Current Shutdown	Shutdown Pin (SD) > 2V		1.1	1.3 **1.4**	mA
VIH	Logic High Threshold	Select Pin & Shutdown pin (SEL, SD)	2.0			V
VIL	Logic Low Threshold	Select Pin & Shutdown pin (SEL, SD)			0.8	V
IiL	Logic Pin Input Current Low[8]	Logic Input = 0V Select Pin & Shutdown pin (SEL, SD)	−8 **-10**	−1		µA
IiH	Logic Pin Input Current High[8]	Logic Input = 5.0V, Select Pin & Shutdown pin (SEL, SD)		57	68 **75**	µA
Miscellaneous Performance						
RIN+	Input Resistance			5		kΩ
CIN	Input Capacitance			0.8		pF
ROUT	Output Resistance	Output Active, (SD < 0.8V)		0.04		Ω
ROUT	Output Resistance	Output Disabled, (SD > 2V)		3000		Ω
COUT	Output Capacitance	Output Disabled, (SD > 2V)		3.1		pF
VO	Output Voltage Range	No Load	±3.51 **±3.50**	±3.7		V
VOL		R_L = 100Ω	±3.16 **±3.15**	±3.5		V
CMIR	Input Voltage Range		±2.5	±2.6		V
IO	Linear Output Current[8]	V_{IN} = 0V,	+60 -70 **±55**	±80		mA

(5) Slew Rate is the average of the rising and falling edges.
(6) Drift determined by dividing the change in parameter at temperature extremes by the total temperature change.
(7) Positive Value is current into device.
(8) Positive Value is current into device.

±5V Electrical Characteristics (continued)

V_S = ±5V, R_L = 100Ω, R_F=576Ω, A_V=2 V/V, T_J=25 °C, Unless otherwise specified. **Bold** numbers specify limits at temperature extremes.

Symbol	Parameter	Conditions[1]	Min[2]	Typ[3]	Max[2]	Units
ISC	Short Circuit Current[9]	V_{IN} = ±2V, Output shorted to ground		±230		mA

(9) The maximum output current (I_{OUT}) is determined by the device power dissipation limitations (The junction temperature cannot be allowed to exceed 150°C). See POWER DISSIPATION of the Application Notes for more details. A short circuit condition should be limited to 5 seconds or less.

±3.3V Electrical Characteristics

V_S = ±3.3V, R_L = 100Ω, R_F=576Ω, A_V=2 V/V; Unless otherwise specified.

Symbol	Parameter	Conditions[1]	Min[2]	Typ[3]	Max[2]	Units
Frequency Domain Performance						
SSBW	−3 dB Bandwidth	V_{OUT} = 0.5 V_{PP}		475		MHz
LSBW	−3 dB Bandwidth	V_{OUT} = 2.0 V_{PP}		375		MHz
0.1 dBBW	0.1 dB Bandwidth	V_{OUT} = 0.5 V_{PP}		100		MHz
GFP	Peaking	DC to 200 MHz		0.4		dB
XTLK	Channel to Channel Crosstalk	All Hostile, f = 5 MHz		−70		dBc
Time Domain Response						
TRL	Rise and Fall Time	2V Step		2		ns
TSS	Settling Time to 0.05%	2V Step		20		ns
OS	Overshoot	2V Step		5		%
SR	Slew Rate	2V Step		1400		V/µs
Distortion						
HD2	2nd Harmonic Distortion	2 V_{PP}, 10 MHz		−67		dBc
HD3	3rd Harmonic Distortion	2 V_{PP}, 10 MHz		−87		dBc
Static, DC Performance						
VIO	Input Offset Voltage	V_{IN} = 0V		1		mV
IBN	Input Bias Current[4]	V_{IN} = 0V		-3		µA
PSRR	Power Supply Rejection Ratio	DC, Input Referred		49		dB
ICC	Supply Current	No Load		12.5		mA
VIH	Logic High Threshold	Select Pin & Shutdown pin (SEL, SD), VIH ≅V^+ * 0.4		1.3		V
VIL	Logic Low Threshold	Select Pin & Shutdown pin (SEL, SD), VIL ≅V^+ * 0.12		0.4		V
Miscellaneous Performance						
RIN+	Input Resistance			5		kΩ
CIN	Input Capacitance			0.8		pF
ROUT	Output Resistance			0.06		Ω
VO	Output Voltage Range	No Load		±2		V
VOL		R_L = 100Ω		±1.8		V
CMIR	Input Voltage Range			±1.2		V
IO	Linear Output Current[5]	V_{IN} = 0V		±60		mA

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No specification of parametric performance is indicated in the electrical tables under conditions of internal self heating where $T_J > T_A$. See Application Notes for information on temperature de-rating of this device. Min/Max ratings are based on product testing, characterization and simulation. Individual parameters are tested as noted.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods.
(3) Typical numbers are the most likely parametric norm.
(4) Positive Value is current into device.
(5) The maximum output current (I_{OUT}) is determined by the device power dissipation limitations (The junction temperature cannot be allowed to exceed 150°C). See POWER DISSIPATION of the Application Notes for more details. A short circuit condition should be limited to 5 seconds or less.

±3.3V Electrical Characteristics (continued)

V_S = ±3.3V, R_L = 100Ω, R_F=576Ω, A_V=2 V/V; Unless otherwise specified.

Symbol	Parameter	Conditions[1]	Min[2]	Typ[3]	Max[2]	Units
ISC	Short Circuit Current[5]	V_{IN} = ±1V, Output shorted to ground		±150		mA

Typical Performance Characteristics

V_s = ±5V, R_L = 100Ω, A_V=2, R_F=R_G=576Ω; unless otherwise specified.

Frequency Response vs. V_{OUT}

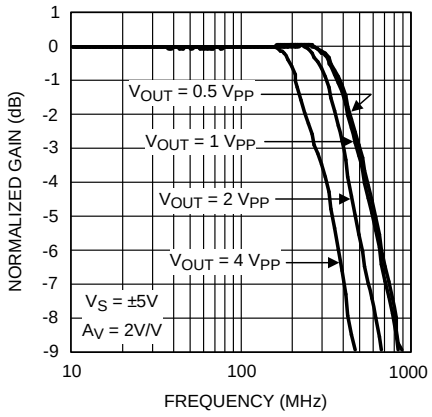


Figure 2.

Frequency Response vs. Gain

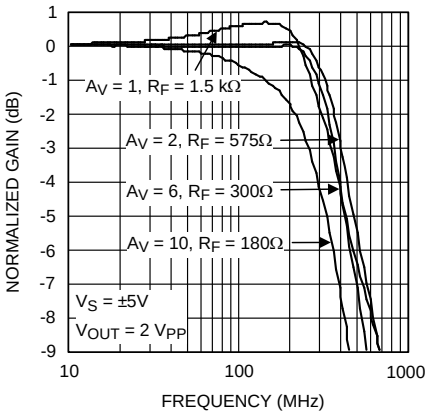


Figure 3.

Frequency Response vs. Capacitive Load

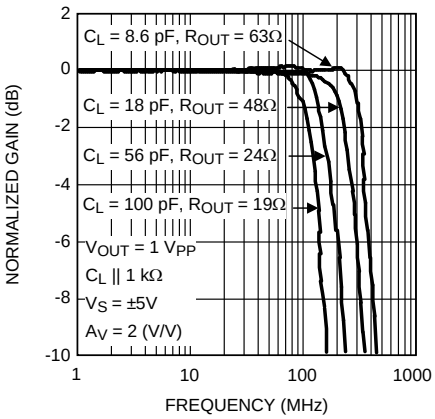


Figure 4.

Suggested R_{OUT} vs. Capacitive Load

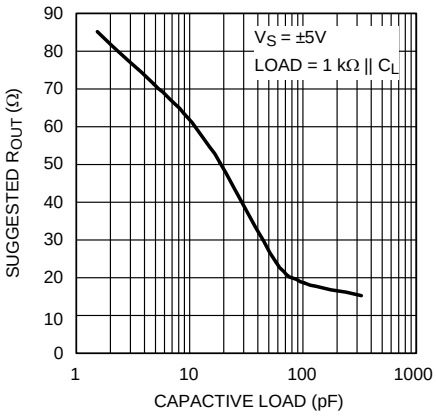


Figure 5.

Suggested Value of R_F vs. Gain

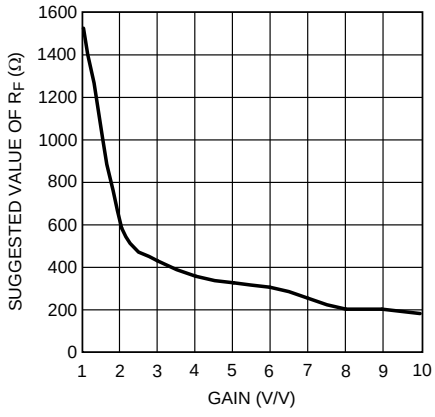


Figure 6.

Pulse Response 4V_{PP}

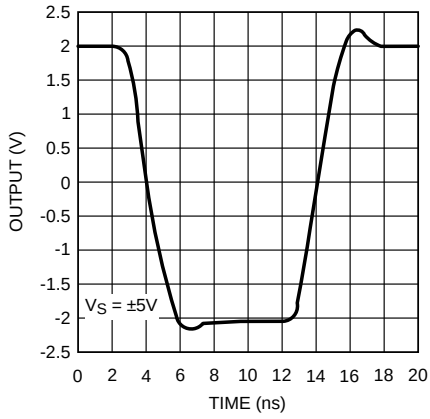


Figure 7.

Typical Performance Characteristics (continued)

V_s = ±5V, R_L = 100Ω, A_V=2, R_F=R_G=576Ω; unless otherwise specified.

Pulse Response $2V_{PP}$

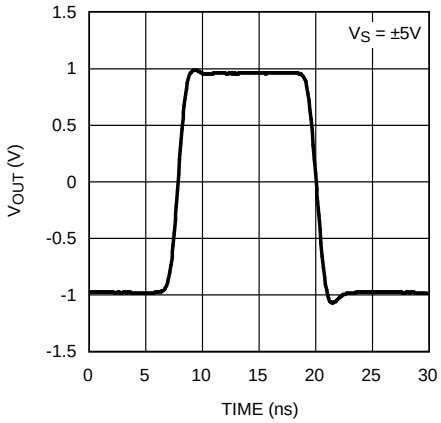


Figure 8.

Pulse Response $2V_{PP}$

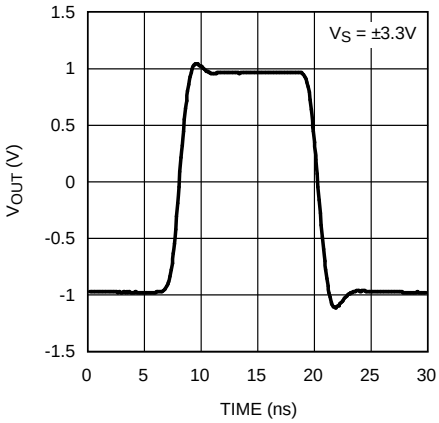


Figure 9.

Closed Loop Output Impedance

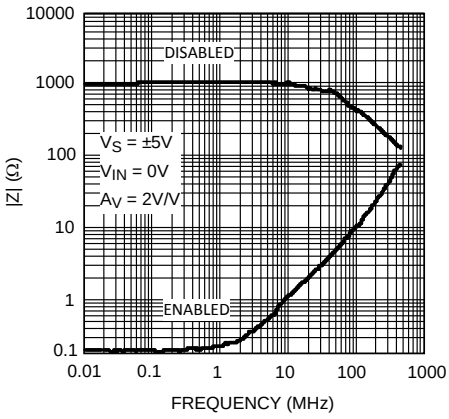


Figure 10.

Closed Loop Output Impedance

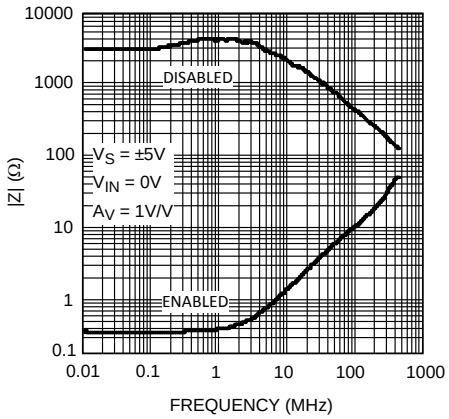


Figure 11.

PSRR vs. Frequency

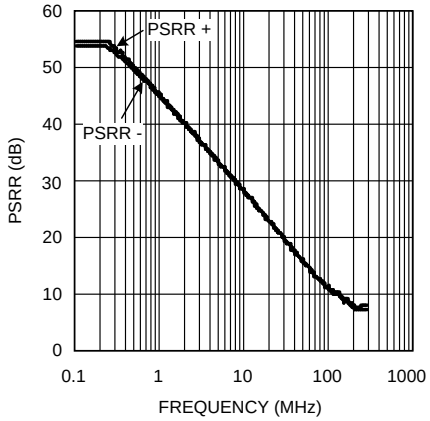


Figure 12.

Channel Switching

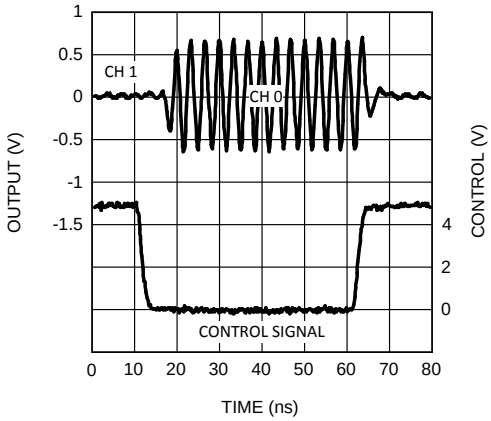


Figure 13.

Typical Performance Characteristics (continued)

V_s = ±5V, R_L = 100Ω, A_V=2, R_F=R_G=576Ω; unless otherwise specified.

SHUTDOWN Switching

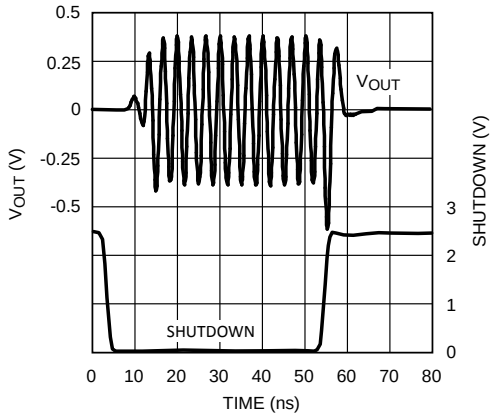


Figure 14.

Shutdown Glitch

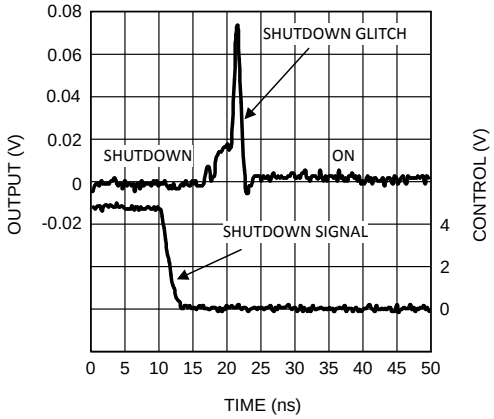


Figure 15.

HD2 vs. Frequency

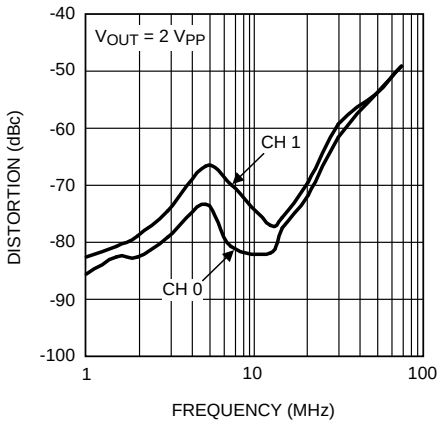


Figure 16.

HD3 vs. Frequency

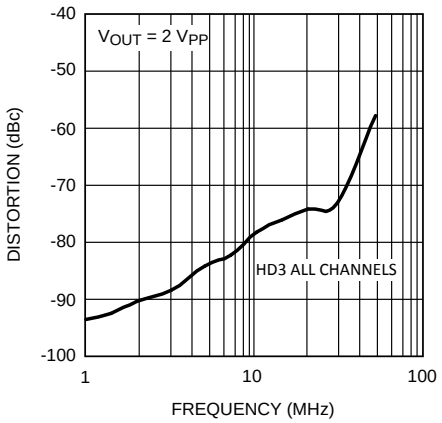


Figure 17.

HD2 vs. V_S

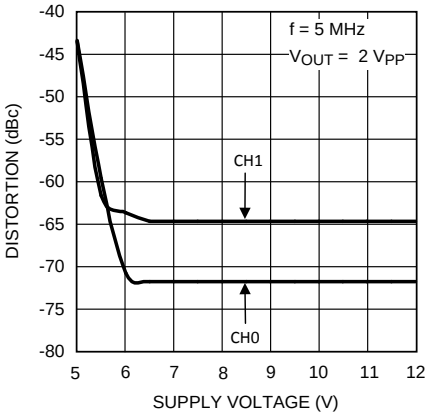


Figure 18.

HD3 vs. V_S

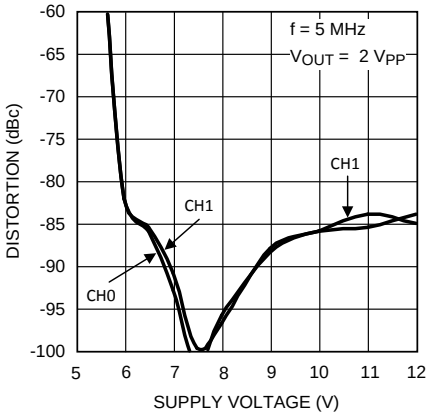


Figure 19.

Typical Performance Characteristics (continued)

V_s = ±5V, R_L = 100Ω, A_V=2, R_F=R_G=576Ω; unless otherwise specified.

HD2 vs. V_{OUT}

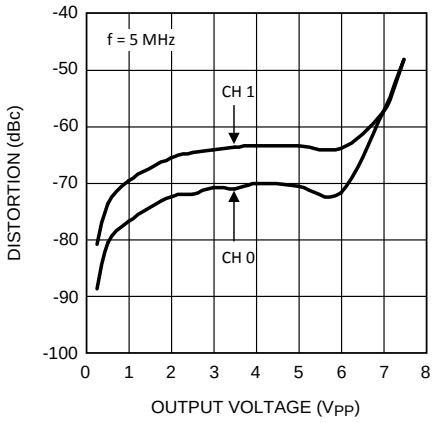


Figure 20.

HD3 vs. V_{OUT}

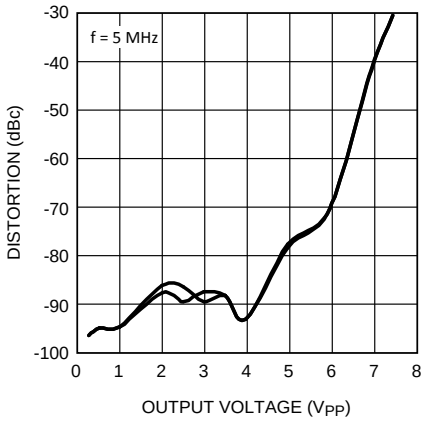


Figure 21.

Minimum V_{OUT} vs. I_{OUT}(1)

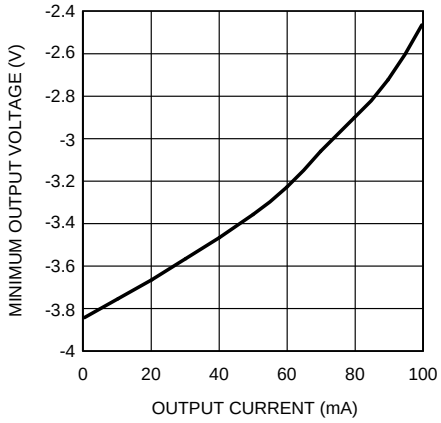


Figure 22.

Maximum V_{OUT} vs. I_{OUT}(1)

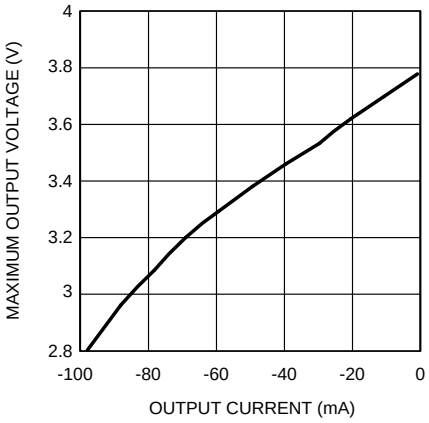


Figure 23.

Crosstalk vs. Frequency

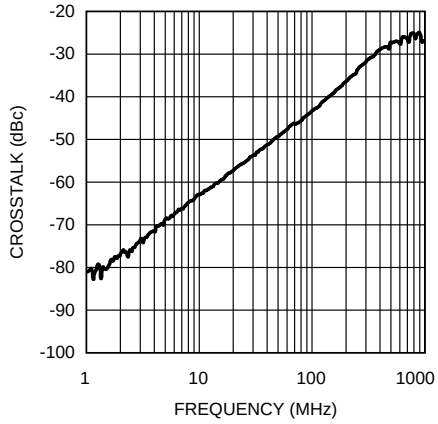


Figure 24.

Off Isolation

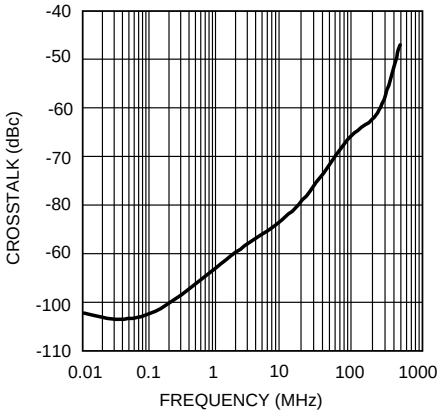


Figure 25.

(1) Positive Value is current into device.

APPLICATION NOTES

GENERAL INFORMATION

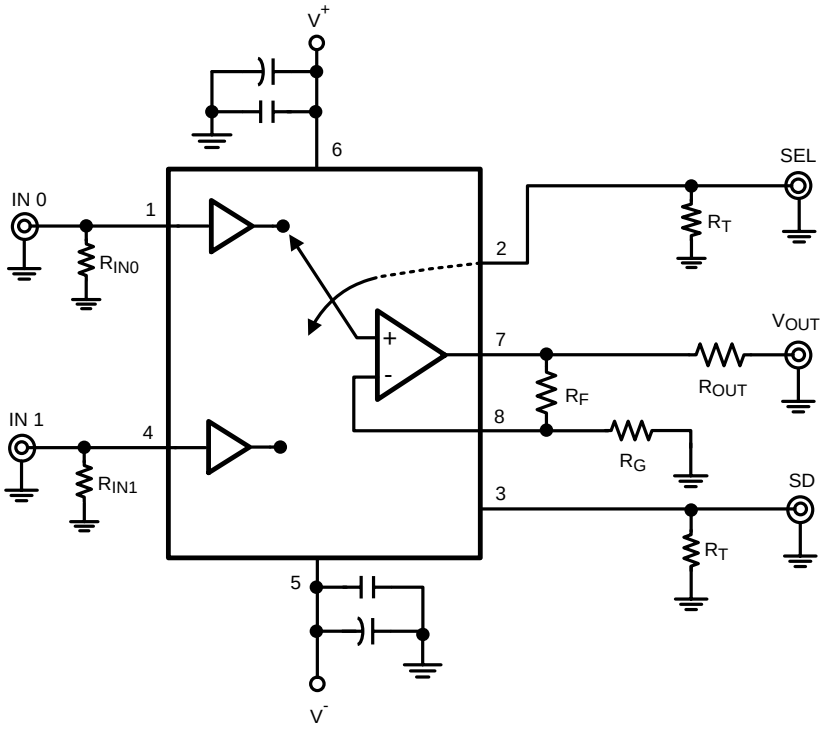


Figure 26. Typical Application

The LMH6570 is a high-speed 2:1 analog multiplexer, optimized for very high speed and low distortion. With selectable gain and excellent AC performance, the LMH6570 is ideally suited for switching high resolution, presentation grade video signals. The LMH6570 has no internal ground reference. Single or split supply configurations are both possible, however, all logic functions are referenced to the mid supply point. The LMH6570 features very high speed channel switching and disable times. When disabled the LMH6570 output is high impedance making MUX expansion possible by combining multiple devices. See MULTIPLEXER EXPANSION. The LMH6570 SEL defaults to logic low (IN0 active). The default state for the SD pin is also logic low (device enabled). Both pins can be left floating if the default state is desired.

VIDEO PERFORMANCE

The LMH6570 has been designed to provide excellent performance with production quality video signals in a wide variety of formats such as HDTV and High Resolution VGA. Best performance will be obtained with back-terminated loads. The back termination reduces reflections from the transmission line and effectively masks transmission line and other parasitic capacitances from the amplifier output stage. Figure 26 shows a typical configuration for driving a 75Ω cable. The output buffer is configured for a gain of 2, so using back terminated loads will give a net gain of 1.

FEEDBACK RESISTOR SELECTION

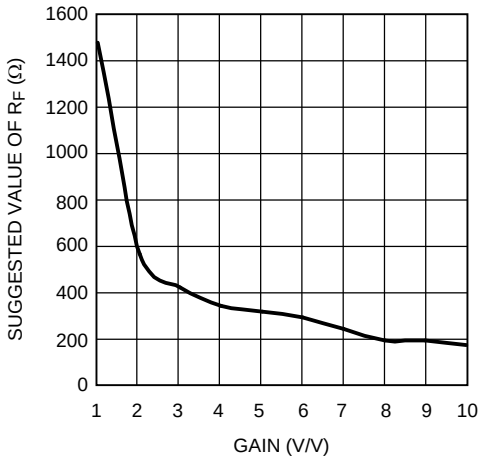


Figure 27. Suggested R_F vs. Gain

The LMH6570 has a current feedback output buffer with gain determined by external feedback (R_F) and gain set (R_G) resistors. With current feedback amplifiers, the closed loop frequency response is a function of R_F. For a gain of 2 V/V, the recommended value of R_F is 576Ω. For other gains see Figure 6. Generally, lowering R_F from the recommended value will peak the frequency response and extend the bandwidth while increasing the value of R_F will cause the frequency response to roll off faster. Reducing the value of R_F too far below the recommended value will cause overshoot, ringing and, eventually, oscillation.

Since all applications are slightly different it is worth some experimentation to find the optimal R_F for a given circuit. For more information see Application Note OA-13 which describes the relationship between R_F and closed-loop frequency response for current feedback operational amplifiers. The impedance looking into pin 8 is approximately 20Ω. This allows for good bandwidth at gains up to 10 V/V. When used with gains over 10 V/V, the LMH6570 will exhibit a “gain bandwidth product” similar to a typical voltage feedback amplifier. For gains of over 10 V/V consider selecting a high performance video amplifier like the LMH6720 to provide additional gain.

MULTIPLEXER EXPANSION

With the SHUTDOWN pin putting the output stage into a high impedance state, several LMH6570’s can be tied together to form a larger input MUX. However, there is a loading effect on the active output caused by the unselected devices. The circuit in Figure 28 shows how to compensate for this effect. For the 8:1 MUX function shown in Figure 28 below the gain error would be about 0.7% or −0.06dB. In the circuit in Figure 28, resistor ratios have been adjusted to compensate for this gain error. By adjusting the gain of each multiplexer circuit the error can be reduced to the tolerance of the resistors used (1% in this example).

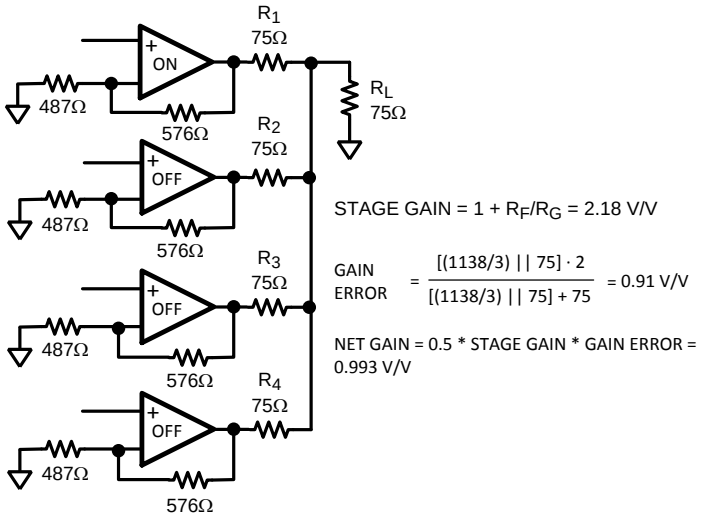


Figure 28. Multiplexer Gain Compensation

BUILDING A 4:1 MULITPLEXER

Figure 29 shows an 4:1 MUX using two LMH6570's.

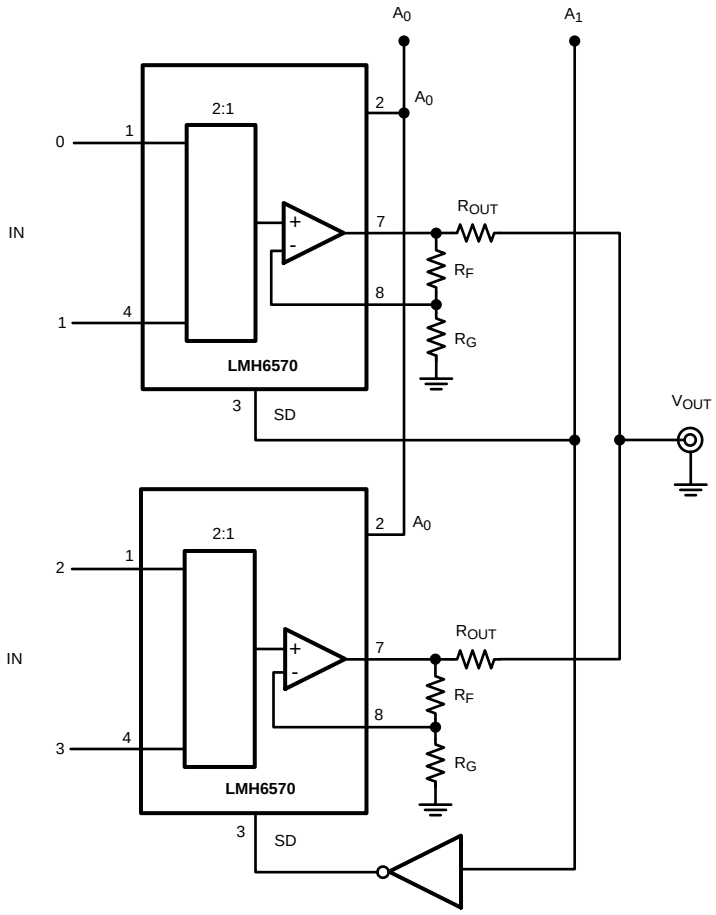


Figure 29. 4:1 MUX USING TWO LMH6570's

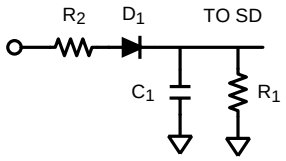


Figure 30. Delay Circuit Implementation

If it is important in the end application to make sure that no two inputs are presented to the output at the same time, an optional delay block can be added, to drive the SHUTDOWN pin of each device, as shown. Figure 30 shows one possible approach to this delay circuit. The delay circuit shown will delay SHUTDOWN's H to L transitions (R_1 and C_1 decay) but won't delay its L to H transition. R_2 should be kept small compared to R_1 in order to not reduce the SHUTDOWN voltage and to produce little or no delay to SHUTDOWN.

Other Applications

The LMH6570 could support a dual antenna receiver with two physically separate antennas. Monitoring the signal strength of the active antenna and switching to the other antenna when a fade is detected is a simple way to achieve spacial diversity. This method gives about a 3dB boost in average signal strength and is the least expensive method for combining signals.

DRIVING CAPACITIVE LOADS

Capacitive output loading applications will benefit from the use of a series output resistor R_{OUT}. Figure 31 shows the use of a series output resistor, R_{OUT}, to stabilize the amplifier output under capacitive loading. Capacitive loads of 5 to 120 pF are the most critical, causing ringing, frequency response peaking and possible oscillation. Figure 32 gives a recommended value for selecting a series output resistor for mitigating capacitive loads. The values suggested in the charts are selected for 0.5 dB or less of peaking in the frequency response. This gives a good compromise between settling time and bandwidth. For applications where maximum frequency response is needed and some peaking is tolerable, the value of R_{OUT} can be reduced slightly from the recommended values.

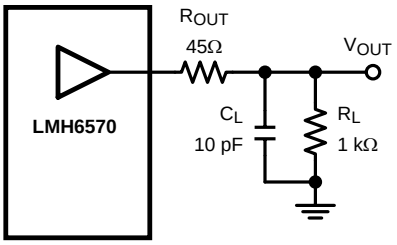


Figure 31. Decoupling Capacitive Loads

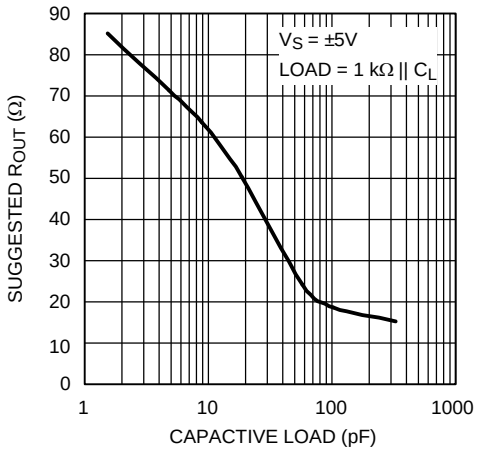


Figure 32. Suggested R_{OUT} vs. Capacitive Load

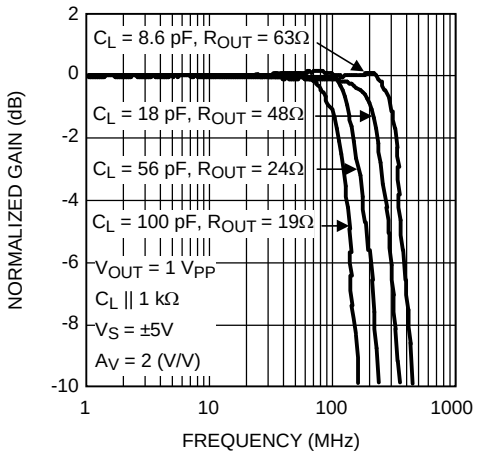


Figure 33. Frequency Response vs. Capacitive Load

LAYOUT CONSIDERATIONS

To reduce parasitic capacitances, ground and power planes should be removed near the input and output pins. For long signal paths controlled impedance lines should be used, along with impedance matching elements at both ends. Bypass capacitors should be placed as close to the device as possible. Bypass capacitors from each rail to ground are applied in pairs. The larger electrolytic bypass capacitors can be located farther from the device, the smaller ceramic capacitors should be placed as close to the device as possible. In Figure 26, the capacitor between V^+ and V^- is optional, but is recommended for best second harmonic distortion. Another way to enhance performance is to use pairs of 0.01µF and 0.1µF ceramic capacitors for each supply bypass.

POWER DISSIPATION

The LMH6570 is optimized for maximum speed and performance in the small form factor of the standard SOIC package. To ensure maximum output drive and highest performance, thermal shutdown is not provided. Therefore, it is of utmost importance to make sure that the T_{JMAX} is never exceeded due to the overall power dissipation.

Follow these steps to determine the maximum power dissipation for the LMH6570:

1. Calculate the quiescent (no-load) power:

$P_{AMP} = I_{CC}* (V_S)$,

where

- $V_S = V^+ - V^-$ (1)

2. Calculate the RMS power dissipated in the output stage:

P_D (rms) = rms $((V_S - V_{OUT}) * I_{OUT})$

where

- V_{OUT} and I_{OUT} are the voltage across
- The current through the external load and V_S is the total supply voltage (2)

3. Calculate the total RMS power:

$P_T = P_{AMP} + P_D$ (3)

The maximum power that t-he LMH6570 package can dissipate at a given temperature can be derived with the following equation:

$P_{MAX} = (150° – T_{AMB})/ \theta_{JA}$

where

- T_{AMB} = Ambient temperature (°C)
- θ_{JA} = Thermal resistance, from junction to ambient, for a given package (°C/W)
- For the SOIC package θ_{JA} is 150 °C/W (4)

ESD PROTECTION

The LMH6570 is protected against electrostatic discharge (ESD) on all pins. The LMH6570 will survive 2000V Human Body model and 200V Machine model events. Under normal operation the ESD diodes have no effect on circuit performance. There are occasions, however, when the ESD diodes will be evident. If the LMH6570 is driven by a large signal while the device is powered down the ESD diodes will conduct . The current that flows through the ESD diodes will either exit the chip through the supply pins or will flow through the device, hence it is possible to power up a chip with a large signal applied to the input pins. Using the shutdown mode is one way to conserve power and still prevent unexpected operation.

REVISION HISTORY

Changes from Revision B (April 2013) to Revision C **Page**

- Changed layout of National Data Sheet to TI format 15

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LMH6570MA	ACTIVE	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 85	LMH65 70MA	Samples
LMH6570MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMH65 70MA	Samples
LMH6570MAX	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 85	LMH65 70MA	Samples
LMH6570MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMH65 70MA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

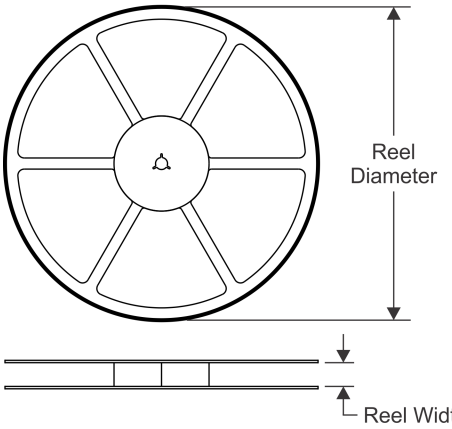
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

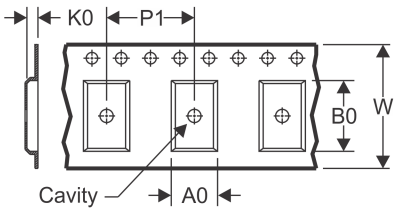
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

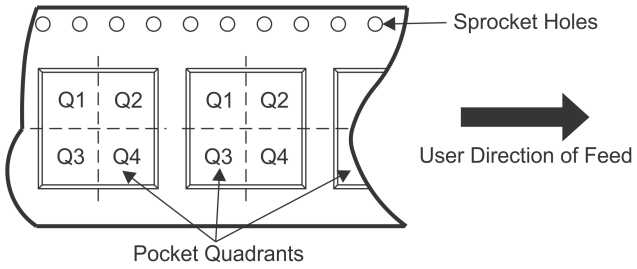


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

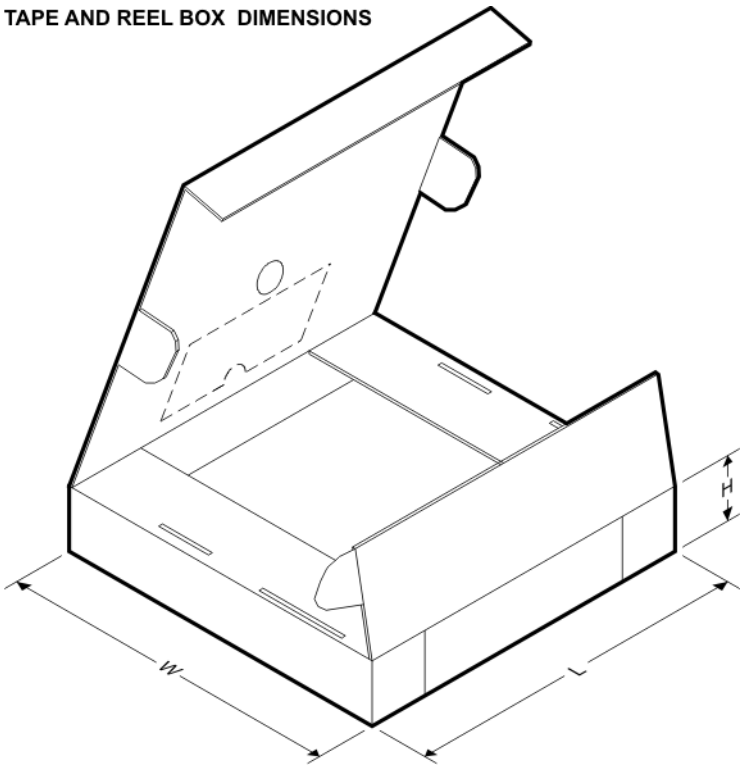
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6570MAX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMH6570MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

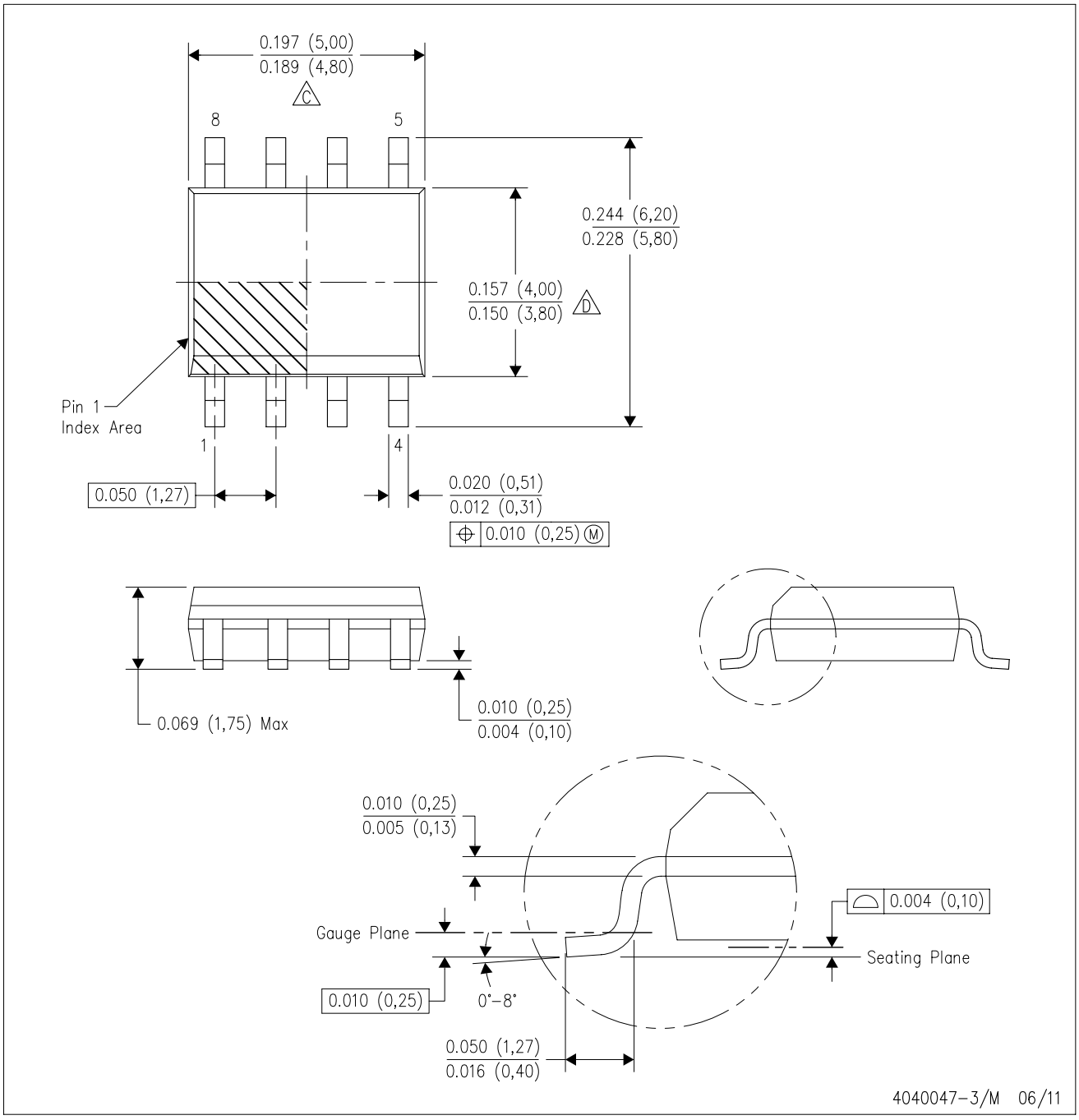
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6570MAX	SOIC	D	8	2500	367.0	367.0	35.0
LMH6570MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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