DS90LV027A LVDS Dual High Speed Differential Driver

Check for Samples: DS90LV027A

FEATURES

- **>600 Mbps (300MHz) Switching Rates**
- **0.3 ns Typical Differential Skew**
- **0.7 ns Maximum Differential Skew**
- **1.5 ns Maximum Propagation Delay**
- **3.3V Power Supply Design**
- **±360 mV Differential Signaling**
- **Low Power Dissipation (46 mW @ 3.3V Static)**
- **Flow-Through Design Simplifies PCB Layout**
- **Interoperable with Existing 5V LVDS Devices**
- **Power Off Protection (Outputs in High Impedance)**
- **Conforms to TIA/EIA-644 Standard**
- **8-Lead SOIC Package Saves Space**
- **Industrial Temperature Operating Range**
  - **(−40°C to +85°C)**

DESCRIPTION

The DS90LV027A is a dual LVDS driver device optimized for high data rate and low power applications. The device is designed to support data rates in excess of 600Mbps (300MHz) utilizing Low Voltage Differential Signaling (LVDS) technology. The DS90LV027A is a current mode driver allowing power dissipation to remain low even at high frequency. In addition, the short circuit fault current is also minimized.

The device is in a 8-lead SOIC package. The DS90LV027A has a flow-through design for easy PCB layout. The differential driver outputs provides low EMI with its typical low output swing of 360 mV. It is perfect for high speed transfer of clock and data. The DS90LV027A can be paired with its companion dual line receiver, the DS90LV028A, or with any of TI's LVDS receivers, to provide a high-speed point-to-point LVDS interface.

Connection Diagram

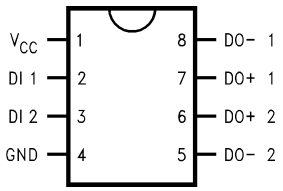
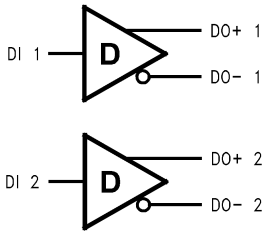


Figure 1. Dual-In-Line
See Package Number D (R-PDSO-G8)

Functional Diagram



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)

Supply Voltage (V_{CC})		−0.3V to +4V
Input Voltage (DI)		−0.3V to +3.6V
Output Voltage (DO±)		−0.3V to +3.9V
Maximum Package Power Dissipation @ +25°C	D Package	1190 mW
	Derate D Package	9.5 mW/°C above +25°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature Range Soldering (4 sec.)		+260°C
ESD Ratings	HBM 1.5 kΩ, 100 pF	≥ 8kV
	EIAJ 0 Ω, 200 pF	≥ 1000V
	CDM	≥ 1000V
	IEC direct 330 Ω, 150 pF	≥ 4kV

(1) "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the devices should be operated at these limits. Electrical Characteristics specifies conditions of device operation.

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	3.0	3.3	3.6	V
Temperature (T_A)	−40	25	+85	°C

Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified(1)(2)(3)

Symbol	Parameter	Conditions		Pin	Min	Typ	Max	Units
DIFFERENTIAL DRIVER CHARACTERISTICS								
V_{OD}	Output Differential Voltage	R_L = 100Ω (Figure 2)		DO+, DO−	250	360	450	mV
ΔV_{OD}	V_{OD} Magnitude Change					1	35	mV
V_{OH}	Output High Voltage					1.4	1.6	V
V_{OL}	Output Low Voltage				0.9	1.1		V
V_{OS}	Offset Voltage				1.125	1.2	1.375	V
ΔV_{OS}	Offset Magnitude Change				0	3	25	mV
I_{OXD}	Power-off Leakage	V_{OUT} = V_{CC} or GND, V_{CC} = 0V				±1	±10	µA
I_{OSD}	Output Short Circuit Current					−5.7	−8	mA
V_{IH}	Input High Voltage			DI	2.0		V_{CC}	V
V_{IL}	Input Low Voltage				GND		0.8	V
I_{IH}	Input High Current	V_{IN} = 3.3V or 2.4V				±2	±10	µA
I_{IL}	Input Low Current	V_{IN} = GND or 0.5V				±1	±10	µA
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA			−1.5	−0.6		V
I_{CC}	Power Supply Current	No Load	V_{IN} = V_{CC} or GND	V_{CC}		8	14	mA
		R_L = 100Ω				14	20	mA

(1) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except V_{OD}.
(2) All typicals are given for: V_{CC} = +3.3V and T_A = +25°C.
(3) The DS90LV027A is a current mode device and only function with datasheet specification when a resistive load is applied to the drivers outputs.

Switching Characteristics

Over Supply Voltage and Operating Temperature Ranges, unless otherwise specified(1)(2)(3)(4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DIFFERENTIAL DRIVER CHARACTERISTICS						
t_{PHLD}	Differential Propagation Delay High to Low	R_L = 100Ω, C_L = 15 pF	0.3	0.8	1.5	ns
t_{PLHD}	Differential Propagation Delay Low to High	(Figure 3 and Figure 4)	0.3	1.1	1.5	ns
t_{SKD1}	Differential Pulse Skew $\|t_{PHLD} - t_{PLHD}\|$(5)		0	0.3	0.7	ns
t_{SKD2}	Channel to Channel Skew(6)		0	0.4	0.8	ns
t_{SKD3}	Differential Part to Part Skew(7)		0		1.0	ns
t_{SKD4}	Differential Part to Part Skew(8)		0		1.2	ns
t_{TLH}	Transition Low to High Time		0.2	0.5	1.0	ns
t_{THL}	Transition High to Low Time		0.2	0.5	1.0	ns
f_{MAX}	Maximum Operating Frequency(9)			350		MHz

(1) All typicals are given for: V_{CC} = +3.3V and T_A = +25°C.
(2) These parameters are ensured by design. The limits are based on statistical analysis of the device over PVT (process, voltage, temperature) ranges.
(3) C_L includes probe and fixture capacitance.
(4) Generator waveform for all tests unless otherwise specified: f = 1 MHz, Z_O = 50Ω, t_r ≤ 1 ns, t_f ≤ 1 ns (10%-90%).
(5) t_{SKD1}, $|t_{PHLD} - t_{PLHD}|$, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.
(6) t_{SKD2} is the Differential Channel to Channel Skew of any event on the same device.
(7) t_{SKD3}, Differential Part to Part Skew, is defined as the difference between the minimum and maximum specified differential propagation delays. This specification applies to devices at the same V_{CC} and within 5°C of each other within the operating temperature range.
(8) t_{SKD4}, part to part skew, is the differential channel to channel skew of any event between devices. This specification applies to devices over recommended operating temperature and voltage ranges, and across process distribution. t_{SKD4} is defined as |Max − Min| differential propagation delay.
(9) f_{MAX} generator input conditions: $t_r = t_f$ < 1 ns (0% to 100%), 50% duty cycle, 0V to 3V. Output criteria: duty cycle = 45%/55%, V_{OD} > 250mV, all channels switching.

Parameter Measurement Information

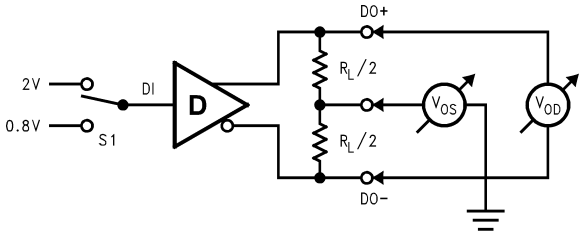


Figure 2. Differential Driver DC Test Circuit

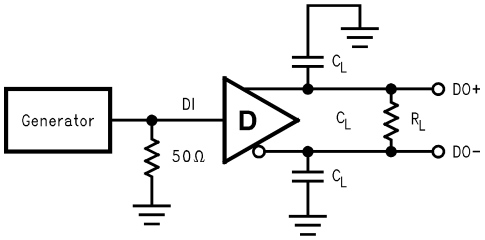


Figure 3. Differential Driver Propagation Delay and Transition Time Test Circuit

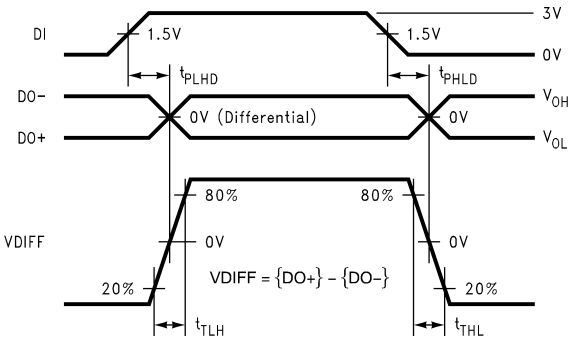


Figure 4. Differential Driver Propagation Delay and Transition Time Waveforms

APPLICATION INFORMATION

Table 1. Device Pin Descriptions

Pin #	Name	Description
2, 3	DI	TTL/CMOS driver input pins
6, 7	DO+	Non-inverting driver output pin
5, 8	DO−	Inverting driver output pin
4	GND	Ground pin
1	V_{CC}	Positive power supply pin, +3.3V ± 0.3V

Typical Performance Curves

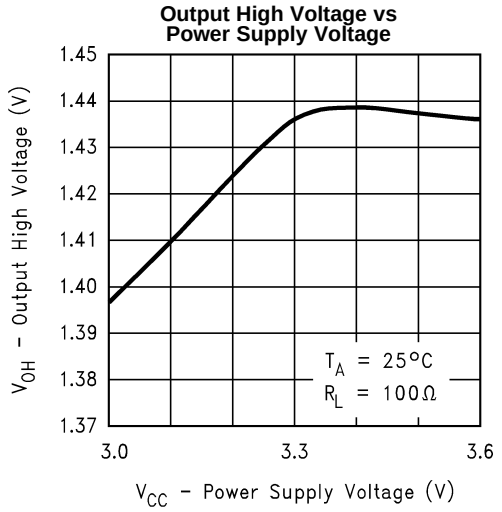


Figure 5.

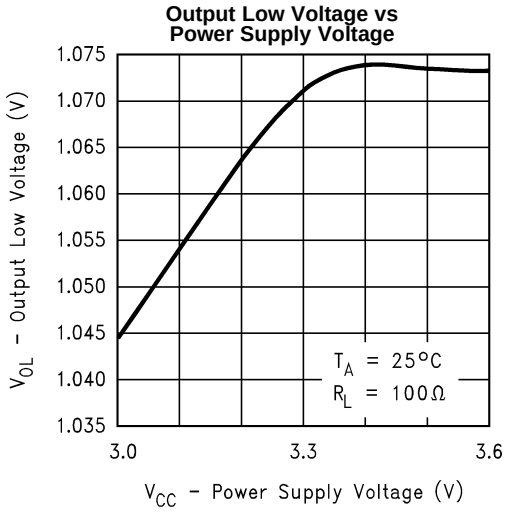


Figure 6.

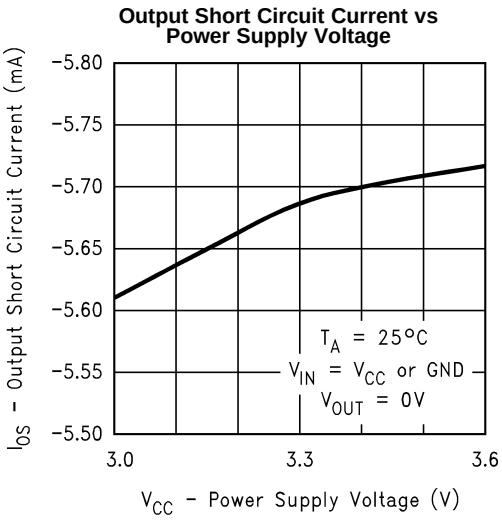


Figure 7.

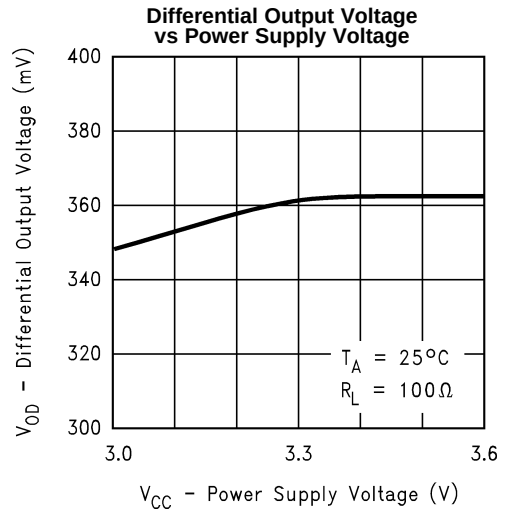


Figure 8.

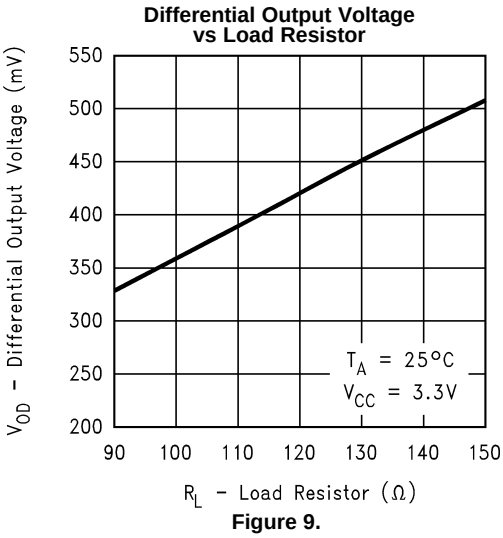


Figure 9.

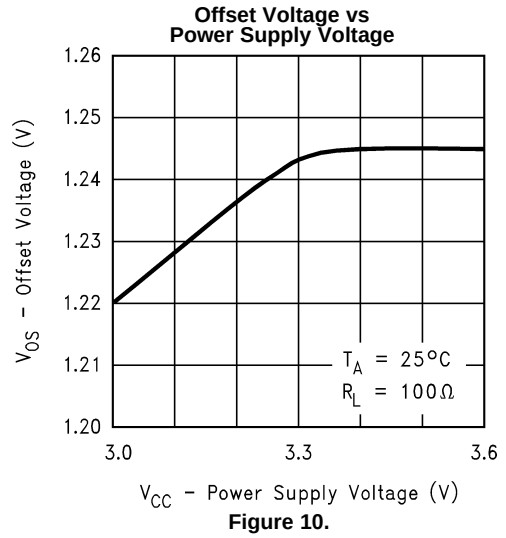


Figure 10.

Typical Performance Curves (continued)

Power Supply Current vs Frequency

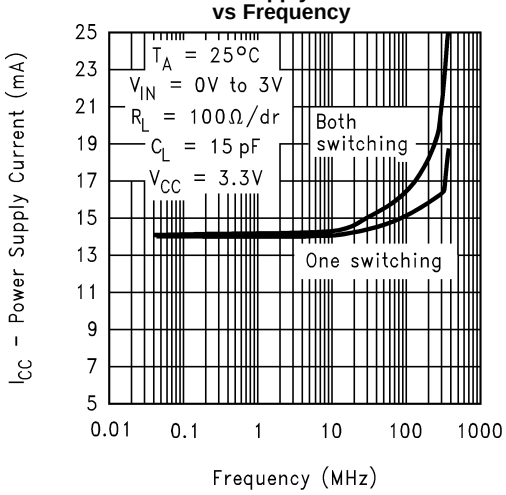


Figure 11.

Power Supply Current vs Power Supply Voltage

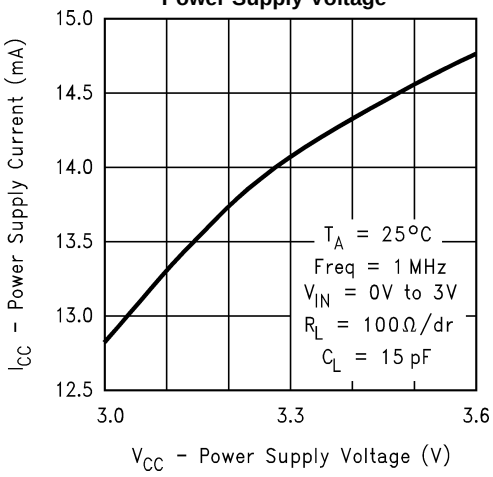


Figure 12.

Power Supply Current vs Ambient Temperature

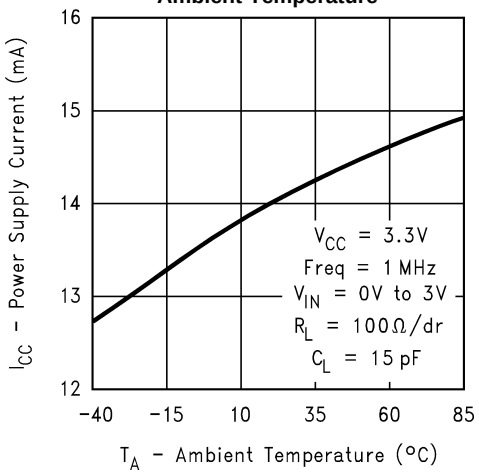


Figure 13.

Differential Propagation Delay vs Power Supply Voltage

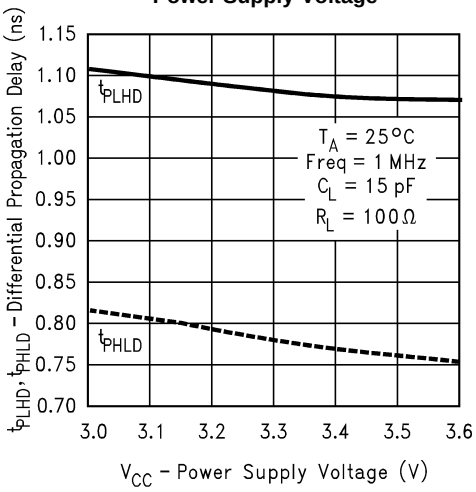


Figure 14.

Differential Propagation Delay vs Ambient Temperature

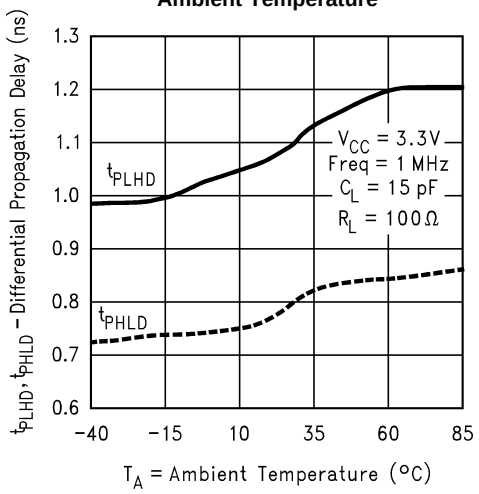


Figure 15.

Differential Skew vs Power Supply Voltage

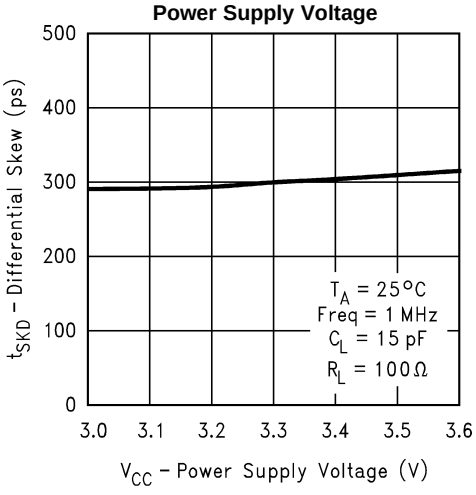


Figure 16.

Typical Performance Curves (continued)

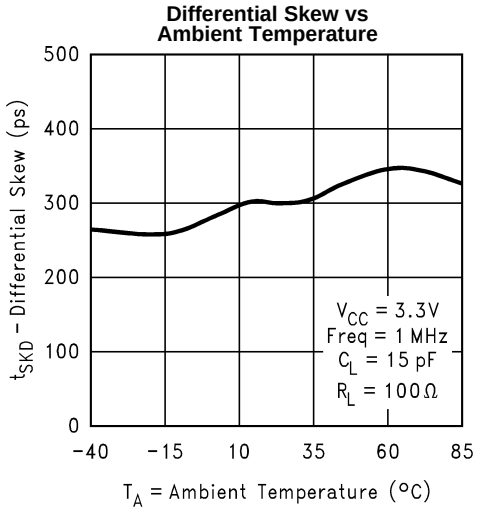


Figure 17.

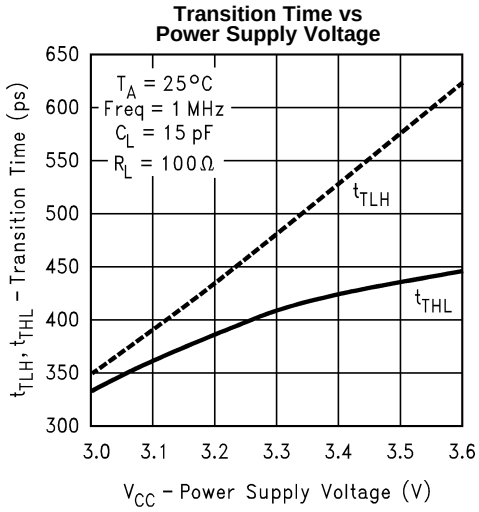


Figure 18.

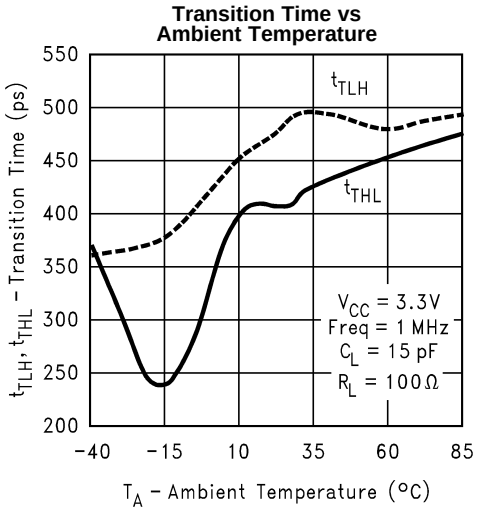


Figure 19.

REVISION HISTORY

Changes from Revision B (April 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	7

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
DS90LV027ATM	ACTIVE	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 85	LV27A TM	Samples
DS90LV027ATM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LV27A TM	Samples
DS90LV027ATMX	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 85	LV27A TM	Samples
DS90LV027ATMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LV27A TM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

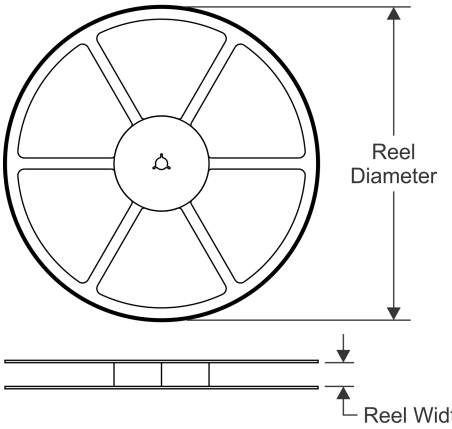
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

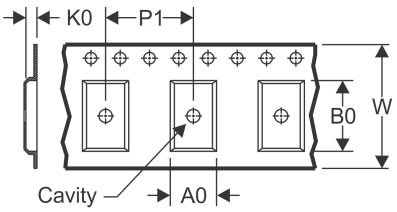
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

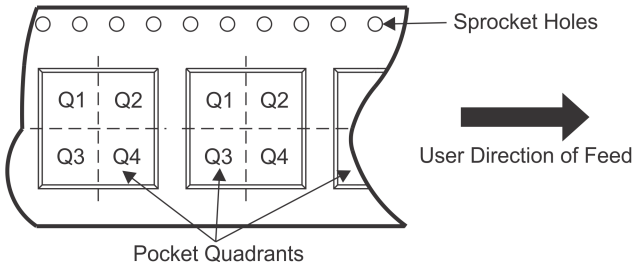


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

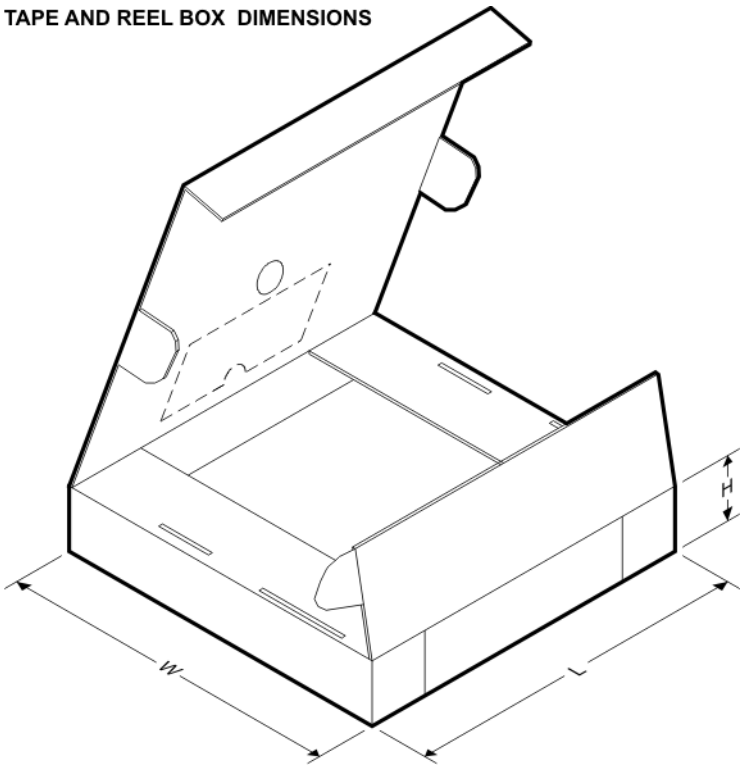
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90LV027ATMX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
DS90LV027ATMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

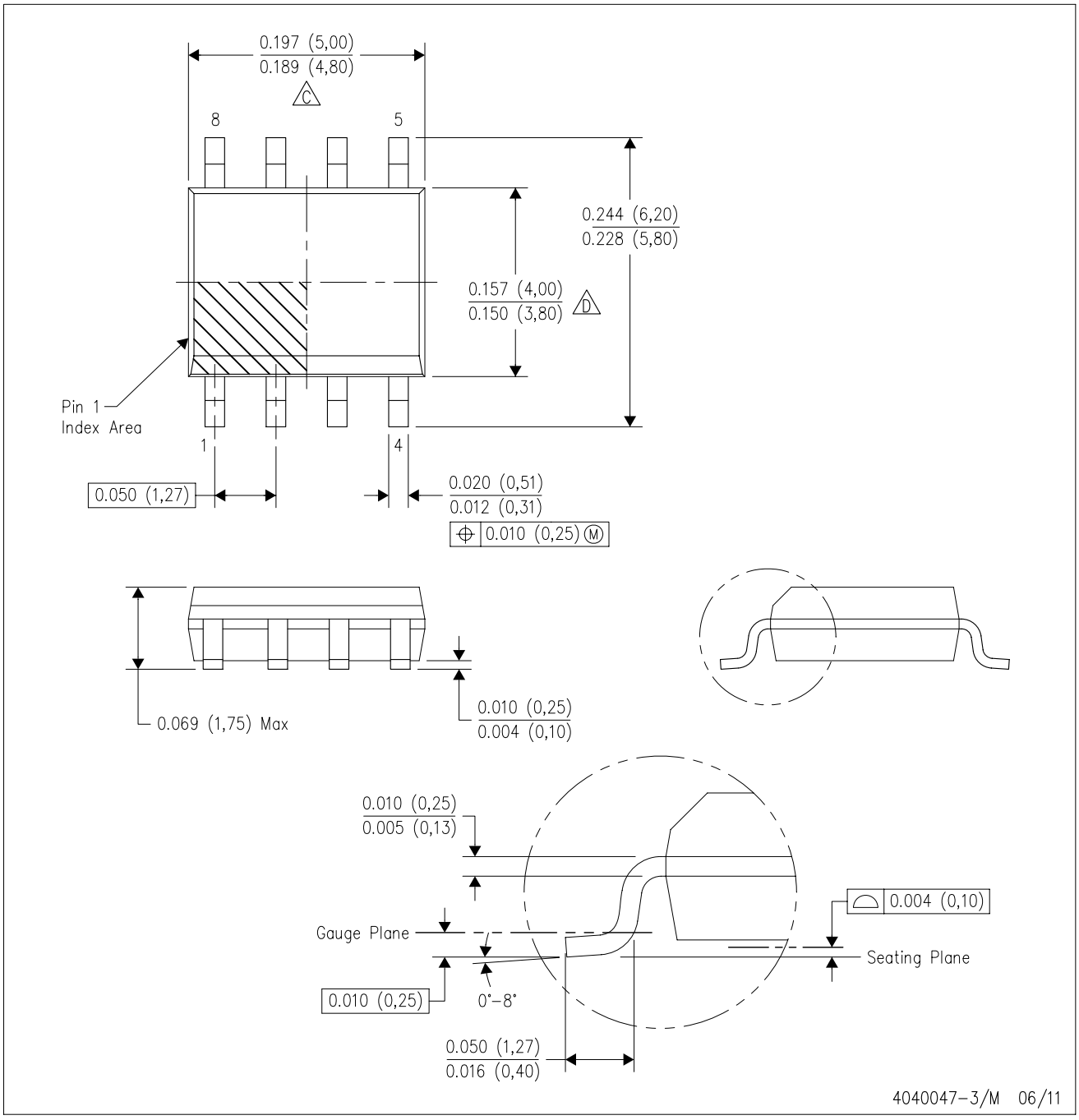
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90LV027ATMX	SOIC	D	8	2500	349.0	337.0	45.0
DS90LV027ATMX/NOPB	SOIC	D	8	2500	349.0	337.0	45.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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