SCAN18245T Non-Inverting Transceiver with Tri-State Outputs

Check for Samples: SCAN18245T

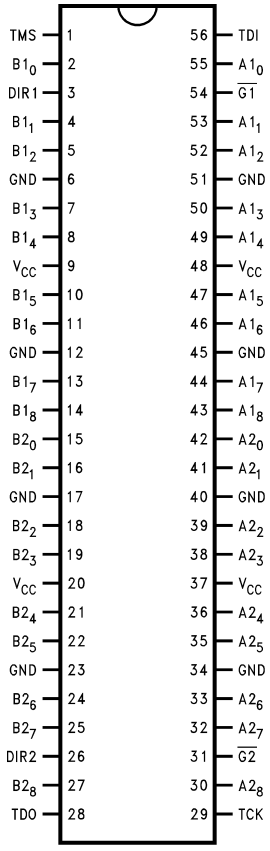
FEATURES

- **IEEE 1149.1 (JTAG) Compliant**
- **Dual Output Enable Control Signals**
- **Tri-State Outputs for Bus-Oriented Applications**
- **9-bit Data Busses for Parity Applications**
- **Reduced-Swing Outputs Source 24 mA/sink 48 mA**
- **Ensured to Drive 50Ω Transmission Line to TTL Input Levels of 0.8V and 2.0V**
- **TTL Compatible Inputs**
- **25 mil Pitch Cerpack Package**
- **Includes CLAMP and HIGHZ Instructions**
- **Available as Known Good Die**
- **Standard Microcircuit Drawing (SMD) 5962-9311501**

DESCRIPTION

The SCAN18245T is a high speed, low-power bidirectional line driver featuring separate data inputs organized into dual 9-bit bytes with byte-oriented output enable and direction control signals. This device is compliant with IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture with the incorporation of the defined boundary-scan test logic and test access port consisting of Test Data Input (TDI), Test Data Out (TDO), Test Mode Select (TMS), and Test Clock (TCK).

Connection Diagram



Pin Names	Description
$A1_{(0–8)}$	Side A1 Inputs or TRI-STATE Outputs
$B1_{(0–8)}$	Side B1 Inputs or TRI-STATE Outputs
$A2_{(0–8)}$	Side A2 Inputs or TRI-STATE Outputs
$B2_{(0–8)}$	Side B2 Inputs or TRI-STATE Outputs
$\overline{G1}$, $\overline{G2}$	Output Enable Pins
DIR1, DIR2	Direction of Data Flow Pins

TRUTH TABLES

Inputs(1)		A1 (0–8)		B1 (0–8)
$\overline{G1}$	DIR1			
L	L	H	←	H
L	L	L	←	L
L	H	H	→	H
L	H	L	→	L
H	X	Z		Z

(1) H= HIGH Voltage Level
L= LOW Voltage Level
X= Immaterial
Z= High Impedance

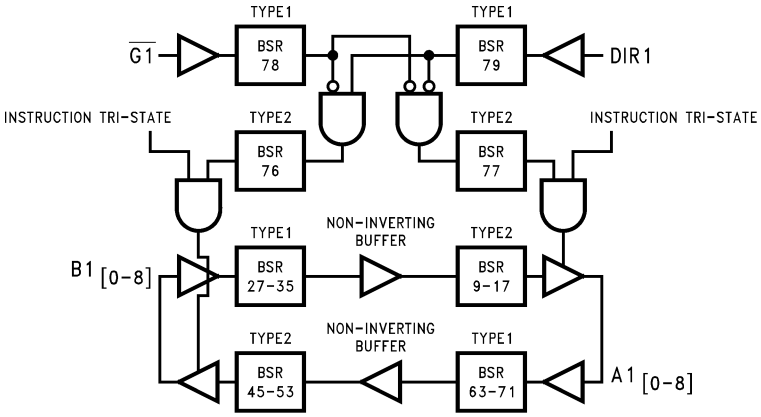
Inputs(1)		A2 (0–8)		B2 (0–8)
$\overline{G2}$	DIR2			
L	L	H	←	H
L	L	L	←	L
L	H	H	→	H
L	H	L	→	L
H	X	Z		Z

(1) H= HIGH Voltage Level
L= LOW Voltage Level
X= Immaterial
Z= High Impedance

FUNCTIONAL DESCRIPTION

The SCAN18245 consists of two sets of nine non-inverting bidirectional buffers with TRI-STATE outputs and is intended for bus-oriented applications. Direction pins (DIR1 and DIR2) LOW enables data from B ports to A ports, when HIGH enables data from A ports to B ports. The Output Enable pins ($\overline{G1}$ and $\overline{G2}$) when HIGH disables both A and B ports by placing them in a high impedance condition.

Block Diagrams



Note: BSR stands for Boundary Scan Register.

Figure 1. A1, B1, $\overline{G1}$ and DIR1

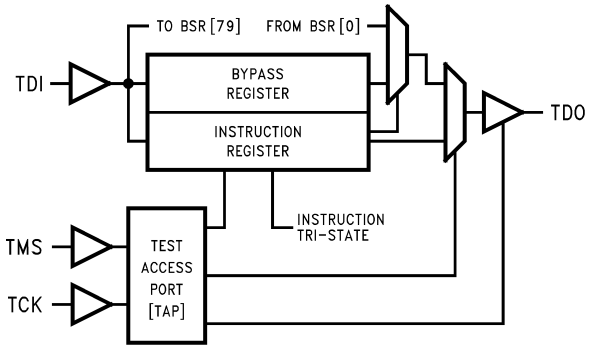
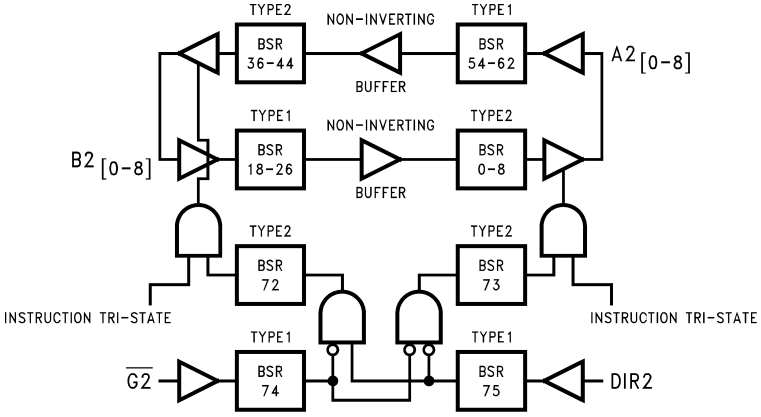


Figure 2. Tap Controller



Note: BSR stands for Boundary Scan Register.

Figure 3. A2, B2, $\overline{G2}$ and DIR2

Description of Boundary-Scan Circuitry

The scan cells used in the BOUNDARY-SCAN register are one of the following two types depending upon their location. Scan cell TYPE1 is intended to solely observe system data, while TYPE2 has the additional ability to control system data. (See IEEE Standard 1149.1 *Figure 10–11* for a further description of scan cell TYPE1 and *Figure 10–12* for a further description of scan cell TYPE2.)

Scan cell TYPE1 is located on each system input pin while scan cell TYPE2 is located at each system output pin as well as at each of the two internal active-high output enable signals. AOE controls the activity of the A-outputs while BOE controls the activity of the B-outputs. Each will activate their respective outputs by loading a logic high.

The BYPASS register is a single bit shift register stage identical to scan cell TYPE1. It captures a fixed logic low.

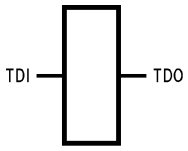


Figure 4. Bypass Register Scan Chain Definition Logic 0

The INSTRUCTION register is an eight-bit register which captures the value 00111101.

The two least significant bits of this captured value (01) are required by IEEE Std 1149.1. The upper six bits are unique to the SCAN18245T device. SCAN CMOS Test Access Logic devices do not include the IEEE 1149.1 optional identification register. Therefore, this unique captured value can be used as a “pseudo ID” code to confirm that the correct device is placed in the appropriate location in the boundary scan chain.

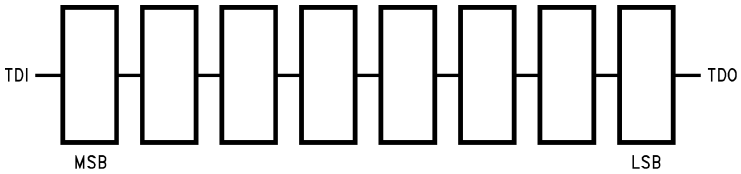


Figure 5. Instruction Register Scan Chain Definition

MSB → LSB

Instruction Code	Instruction
00000000	EXTEST
10000001	SAMPLE/PRELOAD
10000010	CLAMP
00000011	HIGHZ
All Others	BYPASS

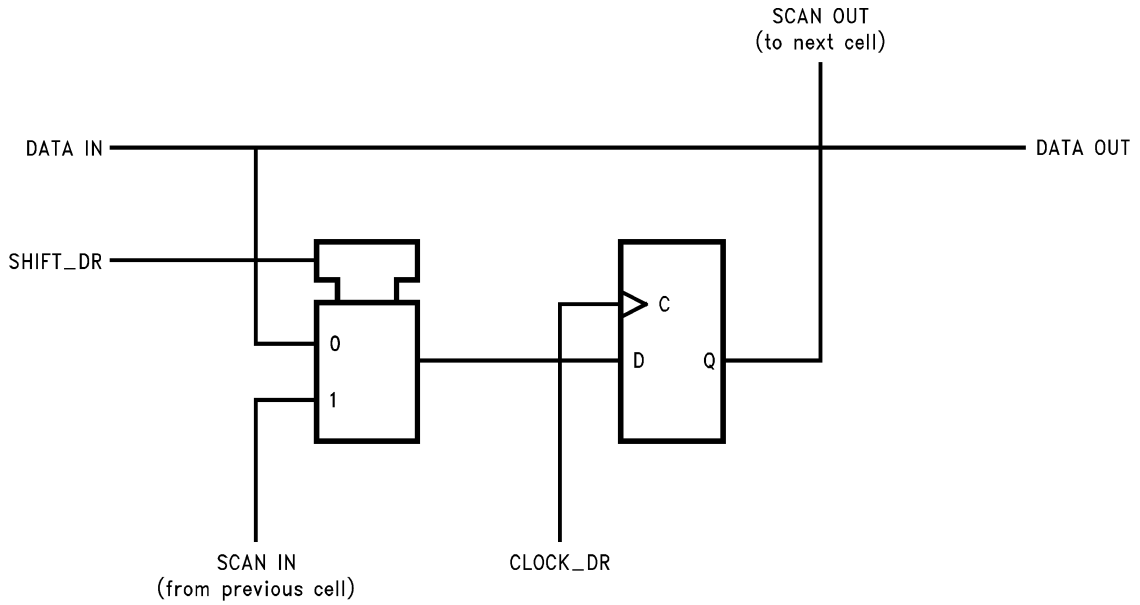


Figure 6. Scan Cell TYPE1

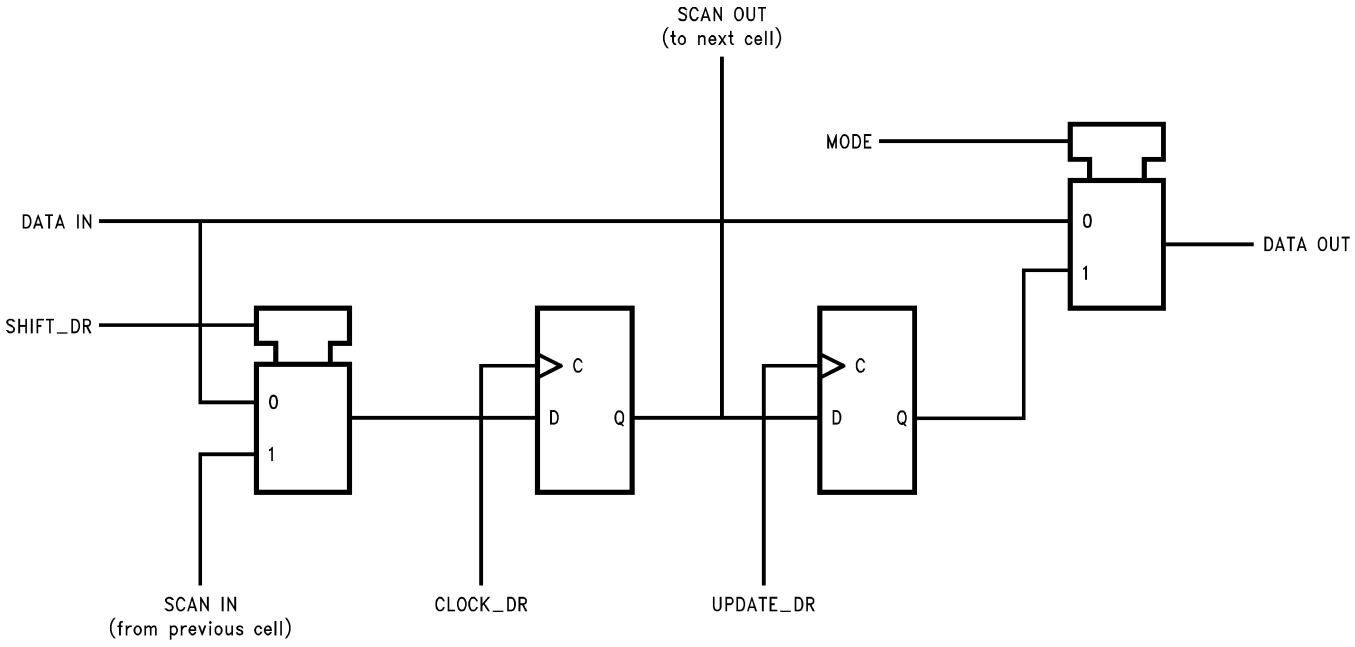


Figure 7. Scan Cell TYPE2

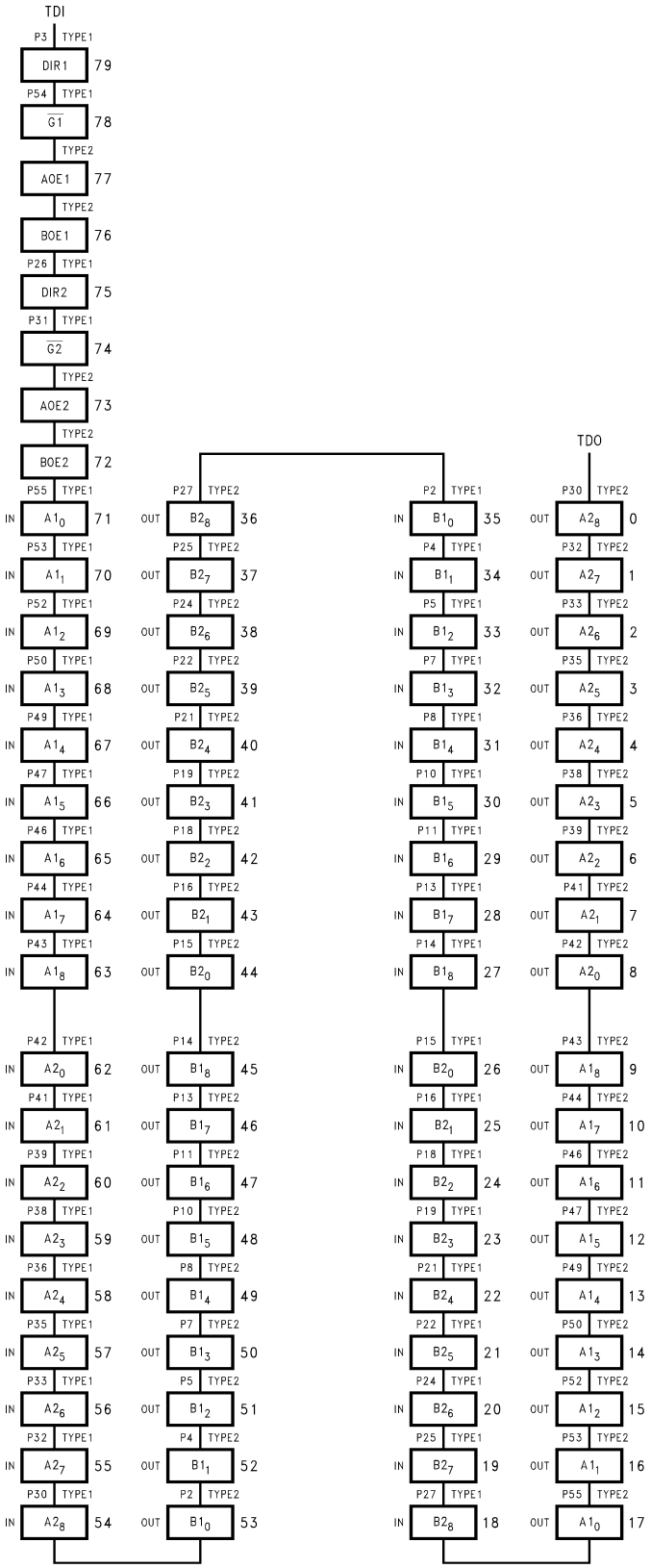


Figure 8. Boundary-Scan Register Scan Chain Definition (80 Bits in Length)

Boundary-Scan Register Definition Index

Bit No.	Pin Name	Pin No.	Pin Type	Scan Cell Type	
79	DIR1	3	Input	TYPE1	Control Signals
78	$\overline{G1}$	54	Input	TYPE1	
77	AOE_1		Internal	TYPE2	
76	BOE_1		Internal	TYPE2	
75	DIR2	26	Input	TYPE1	
74	$\overline{G2}$	31	Input	TYPE1	
73	AOE_2		Internal	TYPE2	
72	BOE_2		Internal	TYPE2	
71	$A1_0$	55	Input	TYPE1	A1–in
70	$A1_1$	53	Input	TYPE1	
69	$A1_2$	52	Input	TYPE1	
68	$A1_3$	50	Input	TYPE1	
67	$A1_4$	49	Input	TYPE1	
66	$A1_5$	47	Input	TYPE1	
65	$A1_6$	46	Input	TYPE1	
64	$A1_7$	44	Input	TYPE1	
63	$A1_8$	43	Input	TYPE1	
62	$A2_0$	42	Input	TYPE1	A2–in
61	$A2_1$	41	Input	TYPE1	
60	$A2_2$	39	Input	TYPE1	
59	$A2_3$	38	Input	TYPE1	
58	$A2_4$	36	Input	TYPE1	
57	$A2_5$	35	Input	TYPE1	
56	$A2_6$	33	Input	TYPE1	
55	$A2_7$	32	Input	TYPE1	
54	$A2_8$	30	Input	TYPE1	
53	$B1_0$	2	Output	TYPE2	B1–out
52	$B1_1$	4	Output	TYPE2	
51	$B1_2$	5	Output	TYPE2	
50	$B1_3$	7	Output	TYPE2	
49	$B1_4$	8	Output	TYPE2	
48	$B1_5$	10	Output	TYPE2	
47	$B1_6$	11	Output	TYPE2	
46	$B1_7$	13	Output	TYPE2	
45	$B1_8$	14	Output	TYPE2	
44	$B2_0$	15	Output	TYPE2	B2–out
43	$B2_1$	16	Output	TYPE2	
42	$B2_2$	18	Output	TYPE2	
41	$B2_3$	19	Output	TYPE2	
40	$B2_4$	21	Output	TYPE2	
39	$B2_5$	22	Output	TYPE2	
38	$B2_6$	24	Output	TYPE2	
37	$B2_7$	25	Output	TYPE2	
36	$B2_8$	27	Output	TYPE2	

Boundary-Scan Register Definition Index (continued)

Bit No.	Pin Name	Pin No.	Pin Type	Scan Cell Type	
35	$B1_0$	2	Input	TYPE1	
34	$B1_1$	4	Input	TYPE1	
33	$B1_2$	5	Input	TYPE1	
32	$B1_3$	7	Input	TYPE1	
31	$B1_4$	8	Input	TYPE1	B1–in
30	$B1_5$	10	Input	TYPE1	
29	$B1_6$	11	Input	TYPE1	
28	$B1_7$	13	Input	TYPE1	
27	$B1_8$	14	Input	TYPE1	
26	$B2_0$	15	Input	TYPE1	
25	$B2_1$	16	Input	TYPE1	
24	$B2_2$	18	Input	TYPE1	
23	$B2_3$	19	Input	TYPE1	
22	$B2_4$	21	Input	TYPE1	B2–in
21	$B2_5$	22	Input	TYPE1	
20	$B2_6$	24	Input	TYPE1	
19	$B2_7$	25	Input	TYPE1	
18	$B2_8$	27	Input	TYPE1	
17	$A1_0$	55	Output	TYPE2	
16	$A1_1$	53	Output	TYPE2	
15	$A1_2$	52	Output	TYPE2	
14	$A1_3$	50	Output	TYPE2	
13	$A1_4$	49	Output	TYPE2	A1–out
12	$A1_5$	47	Output	TYPE2	
11	$A1_6$	46	Output	TYPE2	
10	$A1_7$	44	Output	TYPE2	
9	$A1_8$	43	Output	TYPE2	
8	$A2_0$	42	Output	TYPE2	
7	$A2_1$	41	Output	TYPE2	
6	$A2_2$	39	Output	TYPE2	
5	$A2_3$	38	Output	TYPE2	
4	$A2_4$	36	Output	TYPE2	A2–out
3	$A2_5$	35	Output	TYPE2	
2	$A2_6$	33	Output	TYPE2	
1	$A2_7$	32	Output	TYPE2	
0	$A2_8$	30	Output	TYPE2	

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS (1)(2)

Supply Voltage (V_{CC})		−0.5V to +7.0V
DC Input Diode Current (I_{IK})	V_I = −0.5V	−20 mA
	V_I = V_{CC} +0.5V	+20 mA
DC Output Diode Current (I_{OK})	V_O = −0.5V	−20 mA
	V_O = V_{CC} +0.5V	+20 mA
DC Output Voltage (V_O)		−0.5V to V_{CC} +0.5V
DC Output Source/Sink Current (I_O)		±70 mA
DC V_{CC} or Ground Current	Per Output Pin	±70 mA
Junction Temperature	Cerpack	+175°C
Storage Temperature		−65°C to +150°C
ESD (Min)		2000V

(1) Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Texas Instruments does not recommend operation of SCAN circuits outside databook specifications.

(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage (V_{CC})	SCAN Products	4.5V to 5.5V
Input Voltage (V_I)		0V to V_{CC}
Output Voltage (V_O)		0V to V_{CC}
Operating Temperature (T_A)	Military	−55°C to +125°C
Minimum Input Edge Rate dV/dt	V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC ELECTRICAL CHARACTERISTICS

All outputs loaded; thresholds associated with output under test.

Symbol	Parameter	V_{CC} (V)	Military T_A = −55°C to +125°C Specified Limits	Units	Conditions
V_{IH}	Minimum High Input Voltage	4.5 5.5	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} −0.1V
V_{IL}	Maximum Low Input Voltage	4.5 5.5	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} −0.1V
V_{OH}	Minimum High Output Voltage	4.5 5.5	3.15 4.15	V	I_{OUT} = −50 µA
		4.5 5.5	2.4 2.4	V	V_{IN} = V_{IL} or V_{IH} I_{OH} = −24 mA
V_{OL}	Maximum Low Output Voltage	4.5 5.5	0.1 0.1	V	I_{OUT} = 50 µA
		4.5 5.5	0.55 0.55	V	V_{IN} = V_{IL} or V_{IH} I_{OL} = 48 mA
I_{IN}	Maximum Input Leakage Current	5.5	±1.0	µA	V_I = V_{CC}, GND
I_{IN} TDI, TMS	Maximum Input Leakage	5.5	3.7	µA	V_I = V_{CC}
			−385	µA	V_I = GND
	Minimum Input Leakage	5.5	−160	µA	V_I = GND
I_{OLD}	Minimum Dynamic Output Current(1)	5.5	63	mA	V_{OLD} = 0.8V Max
I_{OHD}			−27	mA	V_{OHD} = 2.0V Min

(1) Maximum test duration 2.0 ms, one output loaded at a time.

DC ELECTRICAL CHARACTERISTICS (continued)

All outputs loaded; thresholds associated with output under test.

Symbol	Parameter	V_{CC} (V)	Military T_A = −55°C to +125°C Specified Limits	Units	Conditions
I_{OZT}	Maximum I/O Leakage Current	5.5	±11.0	µA	V_I (OE) = V_{IL}, V_{IH}
					V_I = V_{CC}, GND
					V_O = V_{CC}, GND
I_{OS}	Output Short Circuit Current	5.5	−100	mA (min)	V_O = 0V
I_{CC}	Maximum Quiescent Supply Current	5.5	168	µA	V_O = High TDI, TMS = V_{CC}
		5.5	930	µA	V_O = High TDI, TMS = GND
I_{CCt}	Maximum I_{CC} Per Input	5.5	2.0	mA	V_I = V_{CC}–2.1V
					V_I = V_{CC}–2.1V
		5.5	2.15	mA	TDI/TMS Pin, test one with the other floating

NOISE SPECIFICATIONS

Symbol	Parameter	V_{CC} (V)	Military T_A = −55°C to +125°C Specified Limits	Units	Fig. No.
V_{OLP}	Maximum High Output Noise(1)(2)	5.0	0.8	V	
V_{OLV}	Minimum Low Output Noise(1)(2)	5.0	-0.8	V	

(1) Maximum number of outputs that can switch simultaneously is n. (n-1) outputs are switched LOW and one output held LOW.
(2) Maximum number of outputs that can switch simultaneously is n. (n-1) outputs are switched HIGH and one output held HIGH.

AC ELECTRICAL CHARACTERISTICS

Normal Operation

Symbol	Parameter	V_{CC} (V)(1)	Military T_A=−55°C to +125°C C_L = 50 pF		Units	Fig. No.
			Min	Max		
t_{PLH}, t_{PHL}	Propagation Delay A to B, B to A	5.0	1.6 1.6	10.0 11.0	ns	
t_{PLZ}, t_{PHZ}	Disable Time	5.0	1.2 1.2	10.0 9.5	ns	
t_{PZL}, t_{PZH}	Enable Time	5.0	1.6 1.6	13.0 11.0	ns	

(1) Voltage Range 5.0 is 5.0V ±0.5V. All Input Timing Delays involving TCK are measured from the rising edge of TCK.

AC ELECTRICAL CHARACTERISTICS

Scan Test Operation

All Propagation Delays involving TCK are measured from the falling edge of TCK.

Symbol	Parameter	V_{CC} (V)(1)	Military		Units	Fig. No.
			T_A=−55°C to +125°C C_L = 50 pF			
			Min	Max		
t_{PLH}, t_{PHL}	Propagation Delay TCK to TDO	5.0	2.8 2.8	15.8 15.8	ns	
t_{PLZ}, t_{PHZ}	Disable Time TCK to TDO	5.0	2.0 2.0	12.8 12.8	ns	
t_{PZL}, t_{PZH}	Enable Time TCK to TDO	5.0	2.4 2.4	16.7 16.7	ns	
t_{PLH}, t_{PHL}	Propagation Delay TCK to Data Out During Update-DR State	5.0	4.0 4.0	21.7 21.7	ns	
t_{PLH}, t_{PHL}	Propagation Delay TCK to Data Out During Update-IR State	5.0	4.0 4.0	21.2 21.2	ns	
t_{PLH}, t_{PHL}	Propagation Delay TCK to Data Out During Test Logic Reset State	5.0	4.4 4.4	23.0 23.0	ns	
t_{PLZ}, t_{PHZ}	Propagation Delay TCK to Data Out During Update-DR State	5.0	3.2 3.2	19.6 19.6	ns	
t_{PLZ}, t_{PHZ}	Propagation Delay TCK to Data Out During Update-IR State	5.0	2.8 2.8	20.9 20.9	ns	
t_{PLZ}, t_{PHZ}	Propagation Delay TCK to Data Out During Test Logic Reset State	5.0	2.8 2.8	21.8 21.8	ns	
t_{PZL}, t_{PZH}	Propagation Delay TCK to Data Out During Update-DR State	5.0	4.0 4.0	22.6 22.6	ns	
t_{PZL}, t_{PZH}	Propagation Delay TCK to Data Out During Update-IR State	5.0	3.2 3.2	23.7 23.7	ns	
t_{PZL}, t_{PZH}	Propagation Delay TCK to Data Out During Test Logic Reset State	5.0	3.6 3.6	24.9 24.9	ns	

(1) Voltage Range 5.0 is 5.0V ±0.5V. All Input Timing Delays involving TCK are measured from the rising edge of TCK.

AC OPERATING REQUIREMENTS

Scan Test Operation

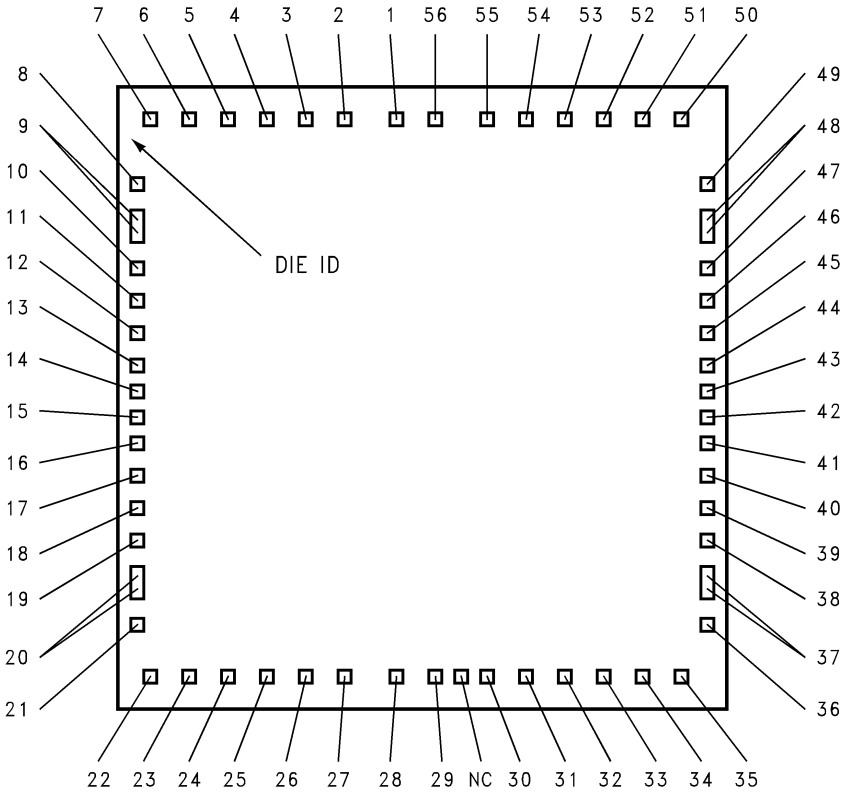
Symbol	Parameter		V_{CC} (V)(1)	Military T_A = −55°C to +125°C C_L = 50 pF Specified Minimum	Units	Fig. No.
t_S	Setup Time, H or L Data to TCK(2)		5.0	0.0	ns	
t_H	Hold Time, H or L TCK to Data(2)		5.0	6.5	ns	
t_S	Setup Time, H or L $\overline{G1}$, $\overline{G2}$ to TCK(3)		5.0	0.0	ns	
t_H	Hold Time, H or L TCK to $\overline{G1}$, $\overline{G2}$(3)		5.0	4.0	ns	
t_S	Setup Time, H or L DIR1, DIR2 to TCK(4)		5.0	0.0	ns	
t_H	Hold Time, H or L TCK to DIR1, DIR2(4)		5.0	4.0	ns	
t_S	Setup Time, H or L Internal AOE_n, BOE_n to TCK(5)		5.0	1.0	ns	
t_H	Hold Time, H or L TCK to Internal AOE_n, BOE(5)		5.0	4.0	ns	
t_S	Setup Time, H or L TMS to TCK		5.0	7.0	ns	
t_H	Hold Time, H or L TCK to TMS		5.0	2.0	ns	
t_S	Setup Time, H or L TDI to TCK		5.0	1.0	ns	
t_H	Hold Time, H or L TCK to TDI		5.0	3.5	ns	
t_W	Pulse Width	H	5.0	12.0	ns	
		L		5.0		
f_{max}	Maximum TCK Clock Frequency		5.0	25	MHz	
T_{PU}	Wait Time, Power Up to TCK		5.0	100	ns	
T_{DN}	Power Down Delay		0.0	100	ms	

(1) Voltage Range 5.0 is 5.0V ±0.5V. All Input Timing Delays involving TCK are measured from the rising edge of TCK.
(2) Timing pertains to the TYPE1 BSR and TYPE2 BSR after the buffer (BSR 0–8, 9–17, 18–26, 27–35, 36–44, 45–53, 54–62, 63–71).
(3) Timing pertains to BSR 74 and 78 only.
(4) Timing pertains to BSR 75 and 79 only.
(5) Timing pertains to BSR 72, 73, 76 and 77 only.

CAPACITANCE

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Pin Capacitance	4	pF	V_{CC} = 5.0V
$C_{I/O}$	Input/Output Capacitance	20	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	41	pF	V_{CC} = 5.0V

PAD DIAGRAM



PAD LOCATIONS

Signal Number	Signal Name	Pad Location(1)
1	TMS	−8.58, 77.81
2	$B1_0$	−19.94, 77.81
3	DIR1	−30.50, 77.81
4	$B1_1$	−40.98, 77.81
5	$B1_2$	−53.59, 77.81
6	GND	−63.73, 77.81
7	$B1_3$	−74.47, 77.81
8	$B1_4$	−79.73, 62.30
9	V_{CC}	−79.73, 51.55
		−79.73, 46.28
10	$B1_5$	−79.73, 36.05
11	$B1_6$	−79.73, 27.48
12	GND	−79.72, 19.46
13	$B1_7$	−79.73, 10.09
14	$B1_8$	−79.73, 3.46
15	$B2_0$	−79.73, −3.43
16	$B2_1$	−79.73, −10.06
17	GND	−79.72, −19.43
18	$B2_2$	−79.73, −27.45
19	$B2_3$	−79.73, −36.02

(1) X, Y coordinates measured in mils from center of die.

PAD LOCATIONS (continued)

Signal Number	Signal Name	Pad Location(1)
20	V_{CC}	−79.73, −46.24
		−79.73, −51.52
21	$B2_4$	−79.73, −62.27
22	$B2_5$	−74.47, −77.81
23	GND	−63.73, −77.81
24	$B2_6$	−53.59, −77.81
25	$B2_7$	−40.98, −77.81
26	DIR2	−30.50, −77.81
27	$B2_8$	−19.94, −77.81
28	TDO	−8.58, −77.81
29	TCK	5.54, −77.81
30	$A2_8$	19.94, −77.81
31	$\overline{G2}$	30.50, −77.81
32	$A2_7$	40.98, −77.81
33	$A2_6$	53.59, −77.81
34	GND	63.73, −77.81
35	$A2_5$	74.47, −77.81
36	$A2_4$	79.73, −62.27
37	V_{CC}	79.73, −51.50
		79.73, −46.23
38	$A2_3$	79.73, −36.02
39	$A2_2$	79.73, −27.40
40	GND	79.73, −19.43
41	$A2_1$	79.73, −10.06
42	$A2_0$	79.73, −3.43
43	$A1_8$	79.73, 3.46
44	$A1_7$	79.73, 10.09
45	GND	79.72, 19.46
46	$A1_6$	79.73, 27.43
47	$A1_5$	79.73, 36.05
48	V_{CC}	79.73, 46.26
		79.73, 51.54
49	$A1_4$	79.73, 62.30
50	$A1_3$	74.47, 77.81
51	GND	63.73, 77.81
52	$A1_2$	53.59, 77.81
53	$A1_1$	40.98, 77.81
54	$\overline{G1}$	30.50, 77.81
55	$A1_0$	19.94, 77.81
56	TDI	5.54, 77.81

REVISION HISTORY

Changes from Original (April 2013) to Revision A	Page
• Changed layout of National Data Sheet to TI format	13

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265